(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
24 November 2022 (24.11.2022)

WIPO | PCT

(10) International Publication Number
WO 2022/245576 A1

(51) International Patent Classification:
H05K 3/42 (2006.01) *C25D 5/18* (2006.01)
C25D 3/38 (2006.01) *H05K 1/02* (2006.01)
C25D 5/00 (2006.01) *H05K 1/18* (2006.01)

(21) International Application Number:
PCT/US2022/028462

(22) International Filing Date:
10 May 2022 (10.05.2022)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
63/189,640 17 May 2021 (17.05.2021) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

(54) Title: SINGLE STEP ELECTROLYTIC METHOD OF FILLING THROUGH HOLES IN PRINTED CIRCUIT BOARDS AND OTHER SUBSTRATES

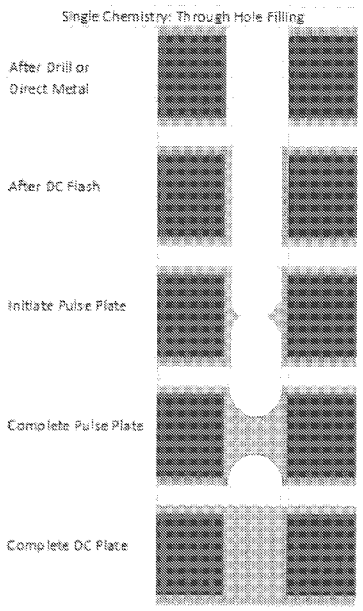


Figure 1

(57) Abstract: A method of copper electroplating in the manufacture of printed circuit boards. The method is used for filling through-holes and micro-vias with copper. The method includes the steps of: (1) preparing an electronic substrate to receive copper electroplating thereon; (2) forming at least one of one or more through-holes and/or one or more micro-vias in the electronic substrate; and (3) electroplating copper in the at least one or more through-holes and/or one or more blind micro-vias by contacting the electronic substrate with an acid copper electrolyte. The acid copper electrolyte is used to plate the one or more through-holes and/or the one or more blind micro-vias. A first pulse reverse plating waveform sequence is used to create a copper bridge in the center of the through-holes followed by direct plating until metallization is complete.

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Declarations under Rule 4.17:

— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

SINGLE STEP ELECTROLYTIC METHOD OF FILLING THROUGH HOLES IN PRINTED CIRCUIT BOARDS AND OTHER SUBSTRATES

FIELD OF THE INVENTION

[0001] The present invention relates generally to an electrolytic deposition method for metallizing electronic substrates.

BACKGROUND OF THE INVENTION

[0002] Electrolytic metal plating solutions are used in many industrial applications, including anticorrosion and decorative coatings, and in the electronics industry for metallizing substrates used in electronic devices, including substrates that include one or more vias, through-holes, and trenches. For example, printed circuit boards, printed wiring boards and other similar substrates may be metallized with electrolytic copper. Copper has a better electrical conductivity than many other metals and allows for smaller features application. Aqueous copper baths, including baths based on sulfuric acid and methane sulfonic acid, are used for the fabrication of printed circuit boards (PCB) and semiconductors.

[0003] Interconnect features are features such as blind micro-vias (BMV), trenches and through-holes that are formed in a dielectric substrate. These features are metallized, preferably with copper, to render the interconnect electrically conductive. During circuit fabrication, copper is electroplated over select portions of the surface of the printed circuit board, into blind vias and trenches and onto the wall of through-holes passing between the surfaces of the circuit board base material. The walls of the through-holes are metallized to provide conductivity between the circuit layers of the printed circuit boards.

[0004] As electronic devices shrink and get packed closer together on circuit boards, heat management of electronics becomes an issue. Many electronic devices are sensitive to heat, which can make them less efficient and shorten their life. Thus, it is necessary to manage heat dissipation and provide a way to draw heat away from heat-generating components and direct it to other areas of a panel or other substrate for dissipation.

[0005] In circuit board modules and electronic devices, electronic components mounted on the circuit board include surface mounting-type electronic components and insertion mounting-type electronic components. Surface mounting-type electronic component are typically mounted on a board by soldering a terminal to a copper foil provided on a front surface of the circuit board.

Insertion mounting-type electronic components are typically mounted on the board by inserting a lead terminal into a penetrating hole provided in the circuit board and soldering the lead terminal.

[0006] Electronic components mounted on the circuit board emit heat when current flows through them. In addition, large amounts of heat can be generated in electronic components in which large current flows. When the temperature of the electronic component or the circuit board rises excessively due to heat emitted by the electronic component, there is a concern that an electronic component or an electric circuit formed on the circuit board can malfunction.

[0007] Various methods have been developed to manage heat dissipation in electronic devices including, for example, filling through holes with conductive metal-filled epoxy plugging material, inserting copper coins under devices, inserting heat pumps into the circuit boards, the use of conductive adhesives, attachment of heat sinks to the heat generating devices, and electroplating of copper.

[0008] Resin or paste plugging of through-holes has been part of the build-up technology in high density interconnect constructions and IC substrates for many years. However, increasing circuit density and stacked via constructions coupled with higher power devices have added an extra dimension of thermal management. It has been found that solid copper filling of through-holes offers many advantages over resin or paste plugging including, for example, reducing the CTE mismatch, providing a stable platform for stacking microvias, and offering thermal management properties for high power devices.

[0009] However, the miniaturization of electronic devices involves a combination of thinner core materials, reduced line widths and smaller diameter through-holes. Filling the through-holes by copper plating has become more and more difficult with higher aspect ratios, often resulting in larger voids and deeper dimples. Another problem with through-hole filling is the manner of filling. Unlike vias which are closed at one end and fill from bottom to top, through-holes pass through a substrate and are open at two ends. When through-holes are being filled with copper, plating parameters and bath additives are chosen so that the copper begins to deposit on the walls at the center of the through-hole where it bridges at the center to form two blind vias as shown in Figure 1.

[0010] Plating bath additives enable the right type of fill. If the right combination of additives is not chosen, the copper plating can result in undesired conformal copper deposition on the sides of the through-holes rather than filling of the through-holes.

[0011] One problem with through-hole plating is that the copper fails to completely fill the through-hole and both ends remain unfilled. An incomplete through-hole fill in which the middle of the hole does not fully close can result in large cavities in the center of the hole as the tops and bottoms of the hole close off due to the deposit preferentially thickening from what is referred to as "dog-boning". The result is a pinching off of the top and bottom and cavities in the center. Another issue is the incomplete filling of the holes after a bridge is formed across the center of the hole leaving deep depressions or open spaces at the tops and bottoms of the hole. The open spaces at the top and bottom of the holes are referred to as "dimples". Thus, it is desirable that the through-hole filling process be optimized to completely fill the hole and eliminate the presence of dimples. An ideal process completely fills through-holes with a high degree of planarity, i.e., build up consistency, without voids, to provide optimum reliability and electrical properties and at as low as possible a surface thickness for optimum line width and impedance control in an electrical device.

[0012] In order to address these problems, it is common to use two different copper electrolytes. A first copper bath is used to fill the through-holes until a bridge is formed, creating two blind vias and then a second bath having a substantially different formulation specifically directed to filling blind vias replaces the first bath to complete the filling process, which is both time consuming and inefficient. The through-hole filling process must be closely monitored to gauge the time when the first bath where the bridge is formed must be replaced with a via filling bath for the final filling of the via and failure to change baths at the correct time can result in dimple and void formation. Moreover, using two distinct plating baths for a single process increases the cost to both the manufacture and the customer.

[0013] U.S. Pat. Pub. No. 2021/0130970 to Desalvo et al., the subject matter of which is herein incorporated by reference describes a method of filling through-holes and vias with copper in the fabrication of printed circuit board, printed wiring boards, and other electronic substrates.

SUMMARY OF THE INVENTION

[0014] It is an object of the present invention to provide a reliable method of metallizing through-holes and vias (including microvias) with high aspect ratios and without any voids or defects.

[0015] It is another object of the present invention to provide a reliable method of metallizing through-holes and vias in a plating process arranged in a vertical configuration.

[0016] It is another object of the present invention to provide a reliable method of metallizing through-holes and vias in a plating process arranged in a horizontal configuration.

[0017] It is still another object of the present invention to provide an improved method of dissipating heat in a circuit board by metallizing through holes with copper and in which the resulting solid copper structures, when locating beneath heat generating devices, are capable of providing an effective means of transporting heat or thermal energy from these devices to areas of the circuit board, panel, or other electronic substrate, where it can be harmlessly dissipated

[0018] It is still another object of the present invention to provide a one-step process for filling copper through holes in a copper electrolyte, which shortens the number of tanks in a line, reducing equipment costs, reducing the number of tanks to analyze and maintain, and reduces the number of rectifiers required for plating.

[0019] It is still another object of the present invention to eliminate potential separation issues between the via fill plating and bridge plating realized by other processes.

[0020] The present invention provides a method for electrolytically filling through holes in electronic substrates, such as printed circuit boards or printed wiring boards, with copper in a single-step, single solution plating process. The method described herein provides circuit designers with a method for heat management of electronic systems where higher packing of higher power heat generating devices is needed. The resulting solid copper structures, when located beneath heat generating devices, provide an effective means of transporting heat energy from these devices to other areas of the panel where it can be harmlessly dissipated. The result is devices that operate more efficiently and that exhibit a longer life.

[0021] In one embodiment, the present invention comprises a method of plating a metal on an electronic substrate, wherein the electronic substrate comprises one or more features, wherein the one or more features comprise one of one or more through-holes and/or one or more micro-vias in the electronic substrate, the method comprising the steps of:

a) preparing the electronic substrate to receive metal plating thereon;

b) bringing the electronic substrate and at least one counter electrode into contact with an acid copper electroplating bath comprising a source of copper ions to be plated;

c) electrically polarizing first and second sides of the electronic substrate to initiate metal plating thereon, wherein the acid copper electroplating bath plates the one or more through-holes and/or the one or more micro-vias using a plating cycle until metallization is complete;

wherein the plating cycle comprising the steps of, in order:

1) pulse plating for a first time period on a first side and a second side of the electronic substrate to cause copper to preferentially plate in the center of the one or more through-holes, wherein the copper merges together in the center of the hole to form two opposing blind vias; and
2) direct plating for a second time period to fill the two opposing blind vias formed by pulse plating;

wherein the pulse plating step comprises applying an electrical current to electrodeposit metal from the acid copper electroplating bath to the first side and second side of the electronic substrate, wherein the electrical current is applied as a pulse plating cycle comprising a repeatable sequence, the repeatable sequence comprising a set of pulse plating periods, the set of pulse plating periods including, in any order:

(i) at least a first forward pulse period;
(ii) at least a first reverse pulse period;
(iii) at least a second forward pulse period; and
(iv) at least a rest period.

[0022] The pulse plating step forms the proper bridge across the center of the hole. The additives are chosen to give good bottom up via filling of the resulting blind microvias. Without proper additives, the blind microvias will either not fill, leaving large dimples or will pinch off at the tops due to dog boning leaving cavities within the blind microvia along with unacceptable dimples.

BRIEF DESCRIPTION OF THE FIGURES

[0023] Figure 1 depicts the steps of the single chemistry through-hole plating of copper.

[0024] Figure 2 depicts the steps of through-hole plating of copper in accordance with one aspect of the present invention in which an optional shaping step is included.

[0025] Figure 3 depicts an apparatus in one embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0026] As used herein, "a," "an," and "the" refer to both singular and plural referents unless the context clearly dictates otherwise.

[0027] As used herein, the term "about" refers to a measurable value such as a parameter, an amount, a temporal duration, and the like and is meant to include variations of +/-15% or less, preferably variations of +/-10% or less, more preferably variations of +/-5% or less, even more preferably variations of +/-1% or less, and still more preferably variations of +/-0.1% or less of and from the particularly recited value, in so far as such variations are appropriate to perform herein. Furthermore, it is also to be understood that the value to which the modifier "about" refers is itself specifically disclosed herein.

[0028] As used herein, spatially relative terms, such as "beneath", "below", "lower", "above", "upper" and the like, are used for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. It is further understood that the terms "front" and "back" are not intended to be limiting and are intended to be interchangeable where appropriate.

[0029] As used herein, the terms "comprises" and/or "comprising," specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0030] As used herein the term "substantially-free" or "essentially-free" if not otherwise defined herein for a particular element or compound means that a given element or compound is not detectable by ordinary analytical means that are well known to those skilled in the art of metal plating for bath analysis. Such methods typically include atomic absorption spectrometry, titration, UV-Vis analysis, secondary ion mass spectrometry, and other commonly available analytically methods.

[0031] The terms "printed circuit board" and "printed wiring board" are used interchangeably throughout this specification.

[0032] The terms "plating" and "electroplating" are used interchangeably throughout this specification.

[0033] As used herein, the term "immediately" means that there are no intervening steps.

[0034] As used herein, the term "dimple" refers to a depression in the bridge or conformal copper plating layer over the filled through-holes and/or blind micro-vias.

[0035] As used herein, the term "asynchronous wave" refers to a waveform that during plating, when periodic pulse reverse rectification is supplied separately to a first side and a second side of a substrate, the waveforms supplied to each side are either phase shifted or completely different from each other.

[0036] As used herein the term "synchronous wave" refers to a waveform that during plating, when periodic pulse reverse rectification is supplied separately to a first side and a second side of a substrate, the waveforms supplied to each side are identical and in phase and are synchronous.

[0037] One of the benefits of the present invention is that plating, especially copper plating, is already a part of the PCB manufacturing process, so being able to use copper plating to fill a through-hole eliminates the need for other processes such as plugging and sanding, copper coining, etc.

[0038] Furthermore, the use of pure copper provides a much higher thermal conductivity than conductive plugs and adhesives. Thus, there is an added benefit of thermal conductivity if it is needed.

[0039] Finally, in one embodiment, the process allows for the complete filling of through-holes in a single-step in a single copper electrolyte. The benefits of using a single electrolyte include shortening the number of tanks in a line and thus equipment costs, and reducing the number of tanks to maintain, and the number of rectifiers needed for plating. In addition, potential separation issues between via fill plating and bridge plating are also reduced or eliminated.

[0040] The general steps of the process to manufacture a printed circuit board that provides improved heat dissipation include the following:

[0041] The initial step is to provide the PCB with various drilled through-hole arrays. Thus, the printed circuit board comprises a metallized panel with an array or arrangement of drilled through-holes. Through-holes, blind micro vias, and such can be formed by various methods,

including, for example, mechanical drilling, laser drilling, plasma etching, or single or double shot.

[0042] Next, the through-holes are made conductive using a metallization technique as is generally known in the art. Various metallization techniques may be used including, for example, sputter coating, electroless copper, carbon-based direct metallization, graphite-based direct metallization, conductive polymers, palladium-based direct metallization, among others. Other metallization techniques would be known to those skilled in the art and would be usable in the process described herein. The primary metallization layer may be electroless copper, electrolytic copper flashing, or a direct metallization layer formed by carbon, graphite, or conductive polymer-based direct metallization.

[0043] In one embodiment, a conductive seed layer is formed on the non-conductive surface to initiate the electroplating of copper. The seed layer is electrically conductive, provides adhesion and permits the exposed portions of its upper surface to be electroplated. Examples of the conductive seed layer include, but are not limited to, metal layers such as copper or palladium that may be formed by electroless deposition, graphite, carbon, and conductive polymers.

[0044] The panel to be plated is preferably copper or a copper-coated substrate.

[0045] Next, the metallized panels are cleaned and activated using conventional pretreatment techniques such as acid or alkaline cleaning and acid dip or microetching with rinsing in between steps.

[0046] Thereafter, the panels are contacted with the acid copper electrolyte comprising a source of copper ions, sulfuric acid, halide ions, and specialized organic additives comprising suppressors, accelerators, and secondary suppressors. The acid copper electrolyte, in combination with a specialized rectification procedure as described herein, is capable of filling through-holes in the panel in a highly effective process. The aqueous acidic copper electrolyte can be used in conventional vertical or horizontal plating equipment. In contrast, as discussed above, prior art copper electroplating processes for plating through-holes can require a two-step process, including a first copper plating solution and plating conditions to close a hole and a second copper plating solution and plating conditions to fill the two blind vias thus formed.

[0047] In one embodiment, the plating cycle comprises (a) pulse plating for a first time period, wherein the pulse plating uses pulse reverse plating with a multiple-step pulse waveform on

opposite sides of the electronic substrate, followed by (b) direct current plating using forward current for a second time period.

[0048] The source of copper ions in the acid copper electrolyte may be copper sulfate. The resistivity of the copper plating solution is greater when the concentration is increased. The solubility of copper sulfate decreases when the sulfuric acid concentration is increased. The concentration of copper sulfate in the acid copper electrolyte is typically maintained within the range of about 100 to about 300 g/L, more preferably about 180 to about 280 g/L, most preferably in the range of about 200 to about 250 g/L.

[0049] The principal function of sulfuric acid is to provide for maximum solution conductivity. Due to the high conductivity of the solution, the anode and cathode polarizations are small as is the voltage required for depositing copper. In addition, when very high cathode current densities are used, a higher concentration of copper sulfate is required within the recommended limits. Changes in sulfuric acid concentration have more influence than changes in copper sulfate concentration on anode and cathode polarization and on solution conductivity. The concentration of sulfuric acid in the acid copper electrolyte is typically maintained within the range of about 10 to about 150 g/L, more preferably about 60 to about 100 g/L.

[0050] The acid copper electrolyte also contains halide ions, most preferably chloride ions. Chloride ions enhance the adsorption and inhibition of the wetter. In addition, a small amount of chloride ions acts as binding sites for the polyglycols to the electrode surface. Chloride made be added in the form of sodium chloride or as diluted hydrochloric acid. Chloride ions in the acid copper electrolyte act to eliminate striated deposits in high current density areas. Chloride ions also affect the surface appearance, structure, micro-hardness, crystallographic orientation and internal stress of the deposits. Chloride ions are consumed by electrochemical/chemical changes during electrolysis, partial inclusion into the deposit, dragout loss, bath dilution, and anode maintenance. The concentration of chloride ions in the acid copper electrolyte is typically maintained within the range of about 20 to about 200 ppm, more preferably about 60 to about 150 ppm, most preferably within the range of about 70 to about 100 ppm.

[0051] The characteristics of copper deposits are influenced by various factors, including concentration of copper sulfate, free acid, additives, temperature, cathode current density and the nature and degree of agitation.

[0052] In one embodiment, the acid copper electrolyte works well in the absence of any iron ions, including ferric ions and ferrous ions. Thus, the acid copper electrolyte is preferably at least essentially free of both ferric ions and ferrous ions, and more preferably is free of both ferric ions and ferrous ions.

[0053] Fill-in behavior in the through-hole is influenced at least in part by controlling the deposition kinetics within the through-holes and on the horizontal portions and edges. This may be achieved by introducing certain organic additives into the acid copper electrolyte to influence the rate of copper ions that deposit on the respective locations. As discussed above, the organic additives include a combination of one or more accelerators, one or more suppressors, and/or one or more secondary suppressors.

[0054] Suitable accelerators incorporate organic compounds that contain sulfur and other functional groups and is responsible for the formation of small grain refined deposit. The accelerator also acts as a leveling agent. The accelerator is consumed by incorporation into the electrolytic deposit at the cathode or by oxidation onto the surface of the anode, especially if insoluble anodes are used. The accelerator can also be consumed by de-coupling in the presence of metallic copper, generating by-products, or by air oxidation, anode maintenance or by dragout loss/bath dilution.

[0055] Examples of suitable accelerators include one or more of 3-(benzothiazolyl-2-thio)-propyl sulfonic acid, sodium salt; 3-mercaptopropane-1-sulfonic acid, sodium salt; ethylene dithiodipropyl sulfonic acid, sodium salt; bis-(p-sulfophenyl)-disulfide, disodium salt; bis-(ω-sulfobutyl)-disulfide, disodium salt; bis-(ω-sulfohydroxypropyl)-disulfide, disodium salt; bis-(ω-sulfopropyl)-disulfide, disodium salt; bis-(ω-sulfopropyl)-sulfide, disodium salt; methyl-(ω-sulfopropyl)-disulfide, disodium salt; methyl-(ω-sulfopropyl)-trisulfide, disodium salt; O-ethyldithio-carbonic acid-S-(ω-sulfopropyl)-ester, potassium salt; thioglycolic acid; thiophosphoric acid-O-ethyl-bis-(ω-sulfopropyl)-ester, disodium salt; and thiophosphoric acid-(ω-sulfopropyl)-ester, trisodium salt. Other suitable sulfur-containing compounds and salts thereof would also be known to those skilled in the art and would be usable in the acid copper electrolyte described herein. In a preferred embodiment, the accelerator comprises bis-(ω-sulfopropyl)-sulfide or 3-mercaptopropane-1-sulfonic acid or a salt thereof.

[0056] The concentration of the one or more accelerators in the acid copper electrolyte is typically maintained in the range of about 0.1 to about 30 ppm, more preferably about 0.5 to about 20 ppm, most preferably within the range of about 4-10 ppm.

[0057] The suppressor comprises a high molecular weight organic compound, such as a polyglycol, having low solubility in the solution and a low coefficient of diffusion. The suppressor is adsorbed on the cathode surface, uniformly forming a diffusion layer that limits the transfer of accelerator and secondary suppressor. In the presence of chloride ions, the degree of adsorption and inhibition is further enhanced. In one embodiment, the molecular weight of the suppressor is at least about 300. More preferably, the molecular weight of the suppressor is between about 500 and about 5,000.

[0058] The suppressor may be consumed during electrolysis, in which reduction of molecular weight occurs, or may be consumed by partial inclusion into the deposit. As with the accelerator, the suppressor may be consumed by anode maintenance or by dragout loss/bath dilution.

[0059] Examples of suitable suppressors include one or more of carboxymethylcellulose, nonylphenolpolyglycolether, octandiol-bis-(polyalkylene glycol ether), octanol polyalkylene glycol ether, oleic acid polyglycol ester, polyethylene glycol polypropylene glycol copolymerisate, polyethylene glycol, polyethylene glycol dimethylether, polypropylene glycol, polyvinylalcohol, β-naphthyl polyglycol ether, stearic acid polyglycol ester, stearic acid alcohol polyglycolether, and copolymers of propylene glycol and ethylene glycol. Other suitable polyglycols and similar compounds would also be known to those skilled in the art and would be usable as the suppressor in the acid copper electrolyte. In one preferred embodiment, the wetter comprises copolymers of propylene glycol and ethylene glycol.

[0060] The concentration of the suppressor in the acid copper electrolyte is typically maintained in the range of about 0.1 to about 50 g/L, more preferably about 1 to about 10 g/L.

[0061] The secondary suppressor is typically a medium molecular weight organic compound containing key functional groups. In one embodiment, the secondary suppressor has a molecular weight of between about 300 and about 10,000, more preferably between about 500 and about 5,000. The secondary suppressor has low solubility in the solution and a low coefficient of diffusion and acts through selective adsorption on a readily accessible surface (i.e., flat surface and protruding high points). The secondary suppressor is consumed by

electrochemical/chemical changes during the electrolysis, by partial inclusion in the deposit, by anode maintenance, and by dragout loss/bath dilution.

[0062] Examples of suitable secondary suppressors include polyamines, ethoxylated polyamines, polypyridine, polyimidazole, polyvinyl pyridine, polyvinyl imidazole, ethoxylated polyvinyl pyridine, and ethoxylated polyvinyl imidazole. In one preferred embodiment, the secondary suppressor comprises ethoxylated polyamines and/or polyvinyl pyridine.

[0063] The concentration of the secondary suppressor in the acid copper electrolyte is typically maintained in the range of about 0.001 to about 200 ppm, more preferably about 0.001 to about 100 ppm, most preferably about 0.001 to about 50 ppm.

[0064] Table 1 summarizes the ingredients of a typical copper electrolyte for use in the process described herein:

Table 1. Typical Ingredients and Concentrations of Copper Electrolyte

Ingredient	Concentration Range
Copper sulfate	100-300 g/L
Sulfuric acid	10-150 g/L
Chloride ions	40-200 ppm
Accelerator	4-10 ppm
Suppressor	1-10 g/L
Secondary suppressor	0.001-50 ppm

[0065] The substrate may be contacted with the aqueous acid copper electrolyte by various means known in the art including, for example, immersion of the substrate into the bath, spraying, or use of other plating equipment. By using specialized pulse rectification, pulse wave forms are initially used that result in accelerated filling of the middle of the through-holes to create a "bridge" while minimizing the amount of surface copper plated, which can be accomplished in both horizontal and vertical systems. The optimized cycle described herein ensures that formation of the bridge occurs quickly and efficiently. By minimizing the amount of time to form the bridge, the amount of surface copper plated can also be minimized. This important in the IC substrate industry because less copper that is deposited and finally etched to

define the circuitry results in better the line resolution capabilities. Since the trend is always to finer and finer circuitry, the ability to maximize trace resolution is an advantage of the process described herein. This is directly related to the amount of copper that needs to be finally etched at the end. In other words, better resolution means capabilities for finer lines and tighter spacing.

[0066] As the center of the through-hole closes, the wave form is transitioned to straight DC current in the same acid copper electrolyte. The result is a continuous plating of the through-hole until it is completely filled.

[0067] The use of a multi-step waveform as described herein can produce good results as compared with waveforms of the prior art. While various waveforms have been developed that utilize forward (cathodic) pulses of certain duration and intensity interspersed with reverse (anodic) pulses of certain duration and intensity, the waveform described herein is a multi-step waveform that in one embodiment includes pulses of higher intensity during the pulse duration of the forward pulse.

[0068] In one embodiment, the waveform includes a repeatable sequence, the repeatable sequence comprising a set of pulse plating periods, the set of pulse plating periods including, in any order:

[0069] (i) first forward pulse period(s);

[0070] (ii) first reverse pulse period(s);

[0071] (iii) second forward pulse period(s); and

[0072] (iv) rest period.

[0073] In one embodiment, the set of forward pulses and reverse pulses has a duration of about one second, more preferably the set of forward pulses and reverse pulses has a duration of exactly one second. In another embodiment, the set of forward pulses and reverse pulses may have a duration of between about 0.5 and about 5 seconds, so long as the proportion of the duration of the pulses remains substantially the same. The duration of the set of forward and reverse pulses could be further defined and calculated as would be known to those skilled in the art.

[0074] In one embodiment, the duration of the first forward pulse period is substantially the same as the duration of the second forward pulse period. More preferably, the duration of the first forward pulse period is the same as the duration of the second forward pulse period. In addition, the intensity of the pulse of the forward pulse period is preferably at least substantially

the same as the intensity of the pulse of the second forward pulse period, except for a time period of a high intensity pulse within at least one, and preferably each of the first forward pulse period and the second forward pulse period as further explained below.

[0075] In addition, at least one of the first forward pulse period and second forward pulse period (more preferably each of the first forward pulse period and the second forward pulse period) comprise a higher intensity pulse of a shorter duration within the first forward pulse period and/or the second forward pulse period. If the each of the first forward pulse and the second forward pulse comprise a high intensity pulse of a shorter duration, the higher intensity pulse of the shorter duration within each of the first forward pulse period and the second forward pulse period of the sequence may have the same intensity or may each have a different intensity. The intensity of the high intensity pulse within the first forward pulse period (otherwise known as the first high intensity pulse) and the intensity of the high intensity pulse within the second forward pulse period (otherwise known as the second high intensity pulse) also each have an intensity that is higher than the intensity of the first forward pulse period and the second forward pulse period. For example, the intensity of the first higher intensity pulse and the second high intensity pulse may be in the range of 100% to 500% of the intensity of the first forward pulse or the second forward pulse. In one embodiment the first high intensity pulse has an intensity that is 100-300% higher than the intensity of the first forward pulse and the second high intensity pulse has an intensity that is 100% to 300% higher than the intensity of the second forward pulse. In another preferred embodiment, the intensity of the second high intensity pulse is higher than the intensity of the first high intensity pulse.

[0076] It is further contemplated that the higher intensity pulse of a shorter duration may occur at the beginning, middle or end of the first forward pulse and/or second forward pulse. If the higher intensity pulse occurs at the beginning of the first forward pulse and/or the second forward pulse, the effect is that the pulse "steps down" from the higher intensity pulse. On the other hand, if the higher intensity pulse occurs at the end of the first forward pulse and/or the second forward pulse, the effect is that the pulse "steps up" to the higher intensity pulse.

[0077] The higher intensity pulse has a duration that is shorter than the duration of the first forward pulse and the second forward pulse. In one embodiment, the duration of the first high intensity pulse and the second high intensity pulse is each approximately 30-40% of the duration of the first forward pulse or the second forward pulse. For example, each of the first forward

pulse period and the second forward pulse period may have a duration of about 50 to about 300 ms, more preferably about 100 to about 200 ms, most preferably about 100 to about 170 ms. For example, within the first forward pulse and/or the second forward pulse, the higher intensity pulse may have a duration of between about 20 ms to about 200 ms. More particularly, for a forward pulse having a duration of about 100 to about 170 ms, the higher intensity pulse may have a duration of about 30 to about 60 ms, depending on the particular application.

[0078] In addition, the duration of the reverse pulse period is preferably within the range of about 50 to about 150 ms, more preferably about 90 to about 140 ms, more preferably about 100 to about 130 ms, most preferably within the range of about 110 to about 120 ms.

[0079] The duration of the rest period is preferably within the range of about 50 to about 150 ms, more preferably about 80 to about 130 ms, most preferably within the range of about 110 to about 120 ms.

[0080] Figure 1 depicts the steps of through-hole plating of copper in accordance with the present invention.

[0081] As set forth in Figure 1, through-holes are drilled or otherwise formed in the circuit board. A primary metallization step such as electroless copper or direct metallization is performed after drilling to render the laminate surface within the through-hole and/or blind micro-via conductive. Optionally, the primary metallization layer may be flash plated with a thin layer of copper to increase conductivity and increase robustness. Next, pulse plating is initiated to accelerate filling of the middle of the through-holes while minimizing the amount of surface copper plating. Next, as pulse plating is completed, the center of the through-hole closes, and the waveform is thereafter transitioned to DC current in the same acid copper plating solution to plate the through-hole until it is completely metallized.

[0082] The process described herein can be used for metallizing a substrate having a thickness of between 0.005 and about 3 mm, more preferably between about 0.01 and about 1.0 mm, most preferably between about 0.05 to about 0.5 mm. Through-hole diameters generally range from about 0.005 and about 1 mm, preferably about 0.01 to about 0.8 mm, most preferably about 0.075 to about 0.25 mm. Thus, the process described herein is suitable for metallizing through-holes having an aspect ratio of between about 0.5:1 and about 6:1, more preferably between about 0.5:1 and about 4:1, most preferably between about 0.5:1 and about 3:1.

[0083] The electrolytic plating of through-holes described herein combines pulse plating and direct current plating in a prescribed manner to achieve complete filling of the through-holes in a single-step, single bath plating process.

[0084] Table 2 depicts an example of the process parameters for direct current and pulse plating current.

Table 2. Process Parameters for Direct Current and Pulse Plating

Type of current	Parameter	Ranges
Direct Current	Forward current	0.5 to 7.0 ASD
Pulse Plating	Forward current	0.5 to 9.0 ASD
	Single or multi-step	50% to 300% forward current
	Reverse current	Up to 4x forward current density
	Frequency	0.5 to 5.0 Hz
	Forward pulse period	200-400 ms
	Reverse pulse period	50-250 ms
	Dead time	Up to 160 milliseconds

[0085] Table 3 describes an example of the steps in the process, including current density and cycle times that have been determined to produce a good result. It is noted that Step 1 is an optional step in the process and the process can be performed with only Steps 2 and 3. In another embodiment, Step 2A is included as an optional step to be performed between Steps 2 and 3 as further explained below.

Table 3. Steps in plating process

Step Number	Current Mode	Current Density (ASD)	Cycle time (min)
1	Direct Current	2.5	1-10
2	Pulse Current	1.5-3.5 (base)	5-180
2A	Synchronous Pulse Current	1.5-3.5 (base)	30-80
3	Direct Current	0.5-3.5	5-180

[0086] As described herein, the process uses a special type of metallization by means of a pulse reverse current. In one embodiment, the repeatable sequence comprising the set of pulse plating periods applied to a first side of the substrate is the same as the repeatable sequence applied to the second side of the substrate. In another embodiment, the repeatable sequence applied to the first side of the substrate is the same as the repeatable sequence applied to the second side of the substrate, except done in reverse order. In another embodiment, the repeatable sequence applied to the second side of the substrate is different from the repeatable sequence applied to the first side of the board. Thus, while the set of pulse plating periods on the second side of the substrate may be aligned, for example, so that the first high intensity pulse on a first side of the substrate coincides with the rest period on the second side of the substrate, the first high intensity pulse and the second high intensity pulse on the second side of the substrate may be of different intensities than the intensities of the first high intensity pulse and the second high intensity pulse on the first side of the substrate even if the pulses themselves are of the substantially the same or exactly the same duration.

[0087] By means of the two rectifiers, the two sides of a printed circuit board can be individually metallized. Furthermore, each of the rectifiers can be separately programmed by means of one or more microcontrollers to input the repeatable sequences for the first side and the second side of the substrate.

[0088] In still another embodiment, the repeatable sequence may comprise a plurality of two or more or even three or more repeatable sequences arranged in a repeating series. What is important is that each repeatable sequence has the same frequency period, which may be within a range of about 0.5 to 5 seconds, more preferably about 1 second, and most preferably exactly one second, while the duration of the first forward pulse(s), second forward pulse(s), reverse pulse(s) and rest period within the set of pulse plating periods that comprise the sequence(s) may be varied.

[0089] In another embodiment, the durations of the first forward pulse period(s), reverse pulse period(s), second forward pulse period(s), and rest period are varied as the plating cycle proceeds. In addition, the amplitude and/or peak current densities of the first forward pulse period(s), reverse pulse period(s), second forward pulse period(s) and rest period along with the first high intensity pulse and the second high intensity pulse can be varied as the plating cycle proceeds.

[0090] It is further contemplated that these changes in the set of pulse plating periods may be made independently on the first and second sides of the substrate. That is, if undesirable plating properties are observed (i.e., bridging is not at the center of the through-hole, voids are observed, etc.), the set of pulse plating periods may be modified to correct the deficiencies and the corrections may be made on the first side of the substrate and/or the second side of the substrates and the modifications may be the same or different on opposite sides of the substrate to achieve the results.

[0091] That is, depending on a thickness of the substrate and/or the diameter of the through-holes, it may be desirable to start the plating cycle at a higher current density and as the plating cycle proceeds, sequentially reduce or increase the current density to achieve more efficient through-hole plating.

[0092] In still another embodiment, a first pulse plating cycle is performed as outlined above, which pulse plating cycle may be an asynchroncous plating cycle in which the repeatable sequence on the first side of the substrate is the same as the repeatable sequence on the second side of the substrate, except in reverse order. Thereafter a second pulse plating cycle may be performed to shape the copper bridge formed in the first plating cycle as illustrated in Figure 2. This second pulse plating cycle may be a regular pulse plating cycle with synchronous waveforms on the first and second side of the substrate.

[0093] If this second pulse plating cycle is used, the regular pulse plating cycle uses a forward/reverse current ratio of 1:1 to 1:4, more preferably about 1:2. The forward plating pulse is in a range of 10-200 ms and the reverse plating pulse is in the range of about 0.5 to about 10 ms. Plating is performed for about 20 minutes to about 3 hours, more preferably about 30 minutes to about 90 minutes, more preferably about 30 to 45 minutes to shape the copper bridge. This pulse plating cycle can be used, for example, when plating through-holes having a small diameter (which, for example, may be 0.2 mm or less) where there is a tendency to form V-shaped blind vias. In this instance, the bridging creates a V-shape that is very deep, which is difficult to plate using direct plating without any dimples or voids as illustrated in Figure 2.

[0094] Thus, the second pulse plating cycle is used to shape the bridge from the deep-V shape to a U shape. The transition from the first pulse plating cycle utilizing an asynchronous waveform to the second plating cycle utilizing a synchronous waveform helps to shape the copper bridge to allow for more uniform plating of the through-holes without any dimples or voids. Monitoring

may be performed by observing and adjusting the cycle during the initial design/set up phase. In one embodiment, the second plating cycle is built into the cycle as an element of time and depending on the diameter of the through-holes being plated.

[0095] In one embodiment, the process includes a step of monitoring certain parameters of the through-hole filling and modifying the time periods of one or more of the steps in the plating sequence or modifying the amplitude/peak current density if inadequate through-hole plating is observed and/or if the certain parameters are outside of acceptable values.

[0096] The peak current density of the at least one forward current pulse at the work- piece is preferably adjusted to 15 A/dm^2 at most. Particularly preferable is a peak current density of the at least one forward current pulse at the workpiece of about 5 A/dm^2.

[0097] The peak current density of the at least one reverse current pulse at the work piece will preferably be adjusted to a value of no more than 60 A/dm^2. Particularly preferred is a peak current density of the at least one reverse current pulse at the workpiece of about 20 A/dm^2.

[0098] In the further progress of the metallization process at least one parameter of the pulse reverse current can be varied, wherein this parameter is chosen from a group comprising the ratio of the duration of the forward current pulse to the duration of the reverse current pulse and the ratio of the peak current density of the forward current pulse to the peak current density of the reverse current pulse. It has been proven to be particularly advantageous to increase the ratio of the peak current density of the forward current pulse to the peak current density of the reverse current pulse when metallizing the workpiece and/or to decrease the ratio of the duration of the forward current pulse to the duration of the reverse current pulse as further explained above.

[0099] As described herein, the aqueous acidic copper electrolyte can be used in conventional vertical or horizontal plating equipment. The plating system can be designed as a vertical hoist, VCP, or horizontal system with inert or soluble anodes. In a preferred embodiment, the system is a vertical system with inert anodes.

[0100] Examples of suitable anode materials include iridium oxide coating on titanium mesh or mixed metal oxide coated anodes. Other suitable anode materials would also be known to those skilled in the art. The anode is also optionally, but preferably, shielded to optimize macrodistribution.

[0101] In one embodiment, the anode material is iridium oxide/tantalum oxide coated titanium. One suitable anode is available from De Nora S.p.A under the tradename De Nora DT. Other suitable anode materials would be known to those skilled in the art and are also usable.

[0102] The substrate or at least a portion of its surface may be contacted with the aqueous acid coper plating solution by various methods, including spraying, wiping, dipping, immersing, or by other suitable means.

[0103] The process described herein also preferably includes cleaning, etching, reducing, rinsing and/or drying steps as is generally known in the art.

[0104] The acid copper electrolyte described herein is equipped with a solution manifold system comprising an array of nozzles for providing direct solution impingement against the panel. Nozzles on either side of the panel are directly aligned with each other and, with the pumps, are capable of solution flows of 0 to 5.0 L/min/nozzle.

[0105] Plating can be done in panel, pattern, or button plating mode as is generally known to those skilled in the art.

[0106] After plating, the panels can be used as is or the panels can be run through typical processes such as planarization or copper reduction or further layers can be built up where additional blind micro-vias may be stacked on the copper filled through-holes.

[0107] In one embodiment, and as shown in Figure 3, the apparatus includes:

A) a plating tank 5 in which the acid copper electrolyte is maintained;

B) a solution delivery system (not shown) comprising a dual box manifold or a vertical pipe manifold;

C) an array of eductor nozzles 2 or cone nozzles arranged to simultaneously impinge both sides of a circuit board immersed in the plating tank 5;

D) a plating rack 4 for securing the PCBs; and

E) an electroplating power supply rectifier 3 or plurality of rectifiers, each capable of direct current and pulse reverse plating connected to suitable control means, which may include one or more microcontrollers.

[0108] In one embodiment, the apparatus may comprise standard vertical hoist or automatic plating equipment. In another embodiment, the apparatus may comprise horizontal plating equipment. However, vertical plating equipment is preferred.

[0109] The plating tank preferably comprises a temperature controller to regulate heating and cooling, which is connected to a heating and cooling system that is capable of maintaining the acid copper electrolyte at the desirable bath temperature +/-1.5°C. In a preferred embodiment, the electrolyte is maintained at a temperature of between about 10 and about 50°C, more preferably between about 15 and about 45°C, more preferably between about 20 and about 30°C, most preferably at a temperature of between about 22 and about 25°C.

[0110] The acid copper electrolyte is optionally, but preferably, agitated. In one embodiment, a clean air agitation sparge dual pipe may be aligned underneath the cathode. Agitation may also be accomplished by mechanical movement of the bath such as by shaking, stirring, or continuous pumping of the electrolyte solution, or by ultrasonic treatment, elevated temperature, or gas feeds, such as purging with air or an inert gas (i.e., argon or nitrogen). Other means of agitation would also be known to those skilled in the art.

[0111] The anode to cathode ratio is preferably targeted at greater than 1:0.75, and may be up to 1:2, preferably about 1:1. What is important is to have enough surface area to even the current distribution across the entire PCB.

[0112] The plating tank is also preferably equipped with an automatic copper oxide replenishment system to maintain the concentration of copper sulfate to within a desired level. In addition, the apparatus also preferably includes a copper oxide mixing tank and a copper oxide feeder for introducing copper oxide into the replenishment system. The plating tank also includes means for replenishing other ingredients of the acid copper electrolyte and for monitoring the concentration of the ingredients.

[0113] The electroplating racks may be coated stainless steel or may be partially or non-coated plating racks. Optionally, the electroplating racks may comprise a coated copper core.

[0114] The copper electroplating tank is also preferably outfitted with a continuous solution filtration system that is capable of filtering particle of about 1 micron or more and that is designed to handle at least 3 solution turnovers per hour, preferably at least 4 solution turnovers per hour and more preferably at least 5 solution turnovers per hour.

[0115] The apparatus also preferably includes a controller capable of managing heating, cooling, and chemical additions with the plating tank.

[0116] Finally, it is also highly desirable that the copper electroplating apparatus be outfitted with a ventilation system as would generally be known to those skilled in the art.

[0117] The electroplating power supply rectifier 3 is configured to handle both direct current and pulse reverse current. The rectifier may be water or air cooled. The rectifier may comprise a single rectifier or may comprise a first rectifier for a first side of the substrate and a second rectifier for the second side of the substrate, each of which is programmable with a multistep capability.

[0118] In one embodiment, the rectifier(s) is/are programmable with multiple steps, including at least 4 steps or least 6 steps or even up to 12 steps. In one preferred embodiment, the rectifier(s) is/are programmable with 8 steps which define a single set of pulse plating periods as further explained herein, which 8 steps may include, for example:

[0119] 1) a first pulse of a first forward duration and first forward intensity;

[0120] 2) a second pulse of a second forward duration and second forward intensity;

[0121] 3) a third pulse of the first forward duration and first forward intensity;

[0122] 4) a fourth pulse of a reverse duration and reverse intensity;

[0123] 5) a fifth pulse of the first forward duration and first forward intensity;

[0124] 6) a sixth pulse of a third forward duration and third forward intensity;

[0125] 7) a seventh pulse of the first forward duration and first forward intensity; and

[0126] 8) a rest period.

[0127] Table 4 sets forth an example of a pulse plating cycle having 8 steps in accordance with the present invention.

Table 4. Pulse plating cycle.

(4 ASD)	Step 1	Step 2	Step 3	Step 4	Step 5	Step 6	Step 7	Step 8
Side 1 (%*)	100-130	230-300	100-130	(-290) – (-370)	100-130	130-180	100-130	0
Side 1 (ms)	80-250	80-250	80-250	80-250	80-250	80-250	80-250	80-250
Side 2 (%*)	100-130	0	100-130	130-180	100-130	(-290) – (-370)	100-130	230-300
Side 2 (ms)	80-250	80-250	80-250	80-250	80-250	80-250	80-250	80-250

* % describes the value as a percent of base current density

[0128] As discussed above, as the center of the through-hole bridges or closes, the wave form is transitioned to straight DC current in the same acid copper electrolyte. The result is a continuous plating of the through-hole until it is completely filled. Thus, the rectifier(s) is/are programmed to transition the pulse reverse waveform used for bridging to direct current and to continue plating until the through-holes are completely filled.

[0129] The box manifold/vertical pipes are designed to include the array of eductor nozzles or cone nozzles. Opposing nozzles are designed front to back side. The nozzles are preferably arranged in a staggered pattern and may be arranged about 2 to about 8 cm apart, more preferably about 3 to about 6 cm apart, most preferably about 4 to about 5 cm apart in both horizontal and vertical direction.

[0130] The process further explained by means of the following examples:

Examples 1:

An acid copper electrolyte was made up according to the following parameters:

Ingredient	Make Up
Copper sulfate	240 g/L
Sulfuric acid	90 g/L
Chloride ions	80 ppm
Accelerator	0.85 mL/L
Suppressor	10 mL/L
Secondary suppressor	2 mL/L
Bath Temperature	23°C

The concentration of copper sulfate was maintained with the addition of copper oxide, on either a manual or automatic basis, based on Amp hours of operation and/or with chemical titration analysis.

The concentration of sulfuric acid and chloride ions was replenished based on chemical titration analysis.

Replenishment of the accelerator, suppressor, and secondary suppressor was accomplished with an automatic dosing system, based on Amp hours of operation and/or cyclic voltametric stripping (CVS) analysis.

A flash plating layer was deposited by DC plating at a current density of 2 ASD for a period of 10 minutes. Thereafter, pulse reverse plating was performed at a current density of 2.4 ASD for a period of 60 minutes to create a copper bridge in the through-holes, followed by DC plating at a current density of 2.5 ASD for a period of 60 minutes until the through-holes were filled in a vertical plating process.

The pulse plating waveform on a first side and a second side of the substrate followed a sequence of:

Side A			Side B		
Step	Duration (ms)	Amplitude (%)	Step	Duration (ms)	Amplitude (%)
Step 1	120	110	Step 1	120	110
Step 2	120	260	Step 2	120	0
Step 3	140	110	Step 3	140	110
Step 4	120	-330	Step 4	120	150
Step 5	120	110	Step 5	120	110
Step 6	120	150	Step 6	120	-330
Step 7	140	110	Step 7	140	110
Step 8	120	0	Step 8	120	260

An observation of a cross-section of the plated circuit board showed good plating with no dimple.

Example 2:

An acid copper electrolyte was made up as in Example 1.

A flash plating layer was deposited by DC plating at a current density of 2 ASD for a period of 10 minutes. Thereafter, pulse reverse plating was performed at a current density of 3.0 ASD for a period of 45 minutes to create a copper bridge in the through-holes, followed by DC plating at a current density of 2.0 ASD for 90 minutes until the through-holes were filled in a vertical plating process.

The pulse plating waveform on a first side and a second side of the substrate followed a sequence of:

Side A			Side B		
Step	Duration (ms)	Amplitude (%)	Step	Duration (ms)	Amplitude (%)
Step 1	125	120	Step 1	125	120
Step 2	125	260	Step 2	125	0
Step 3	125	120	Step 3	125	120
Step 4	125	-330	Step 4	125	150
Step 5	125	120	Step 5	125	120
Step 6	125	150	Step 6	125	-330
Step 7	125	120	Step 7	125	120
Step 8	125	0	Step 8	125	260

An observation of a cross-section of the plated circuit board showed good plating with no dimple.

Example 3:

An acid copper electrolyte was made up according to the following parameters:

Ingredient	Make Up
Copper sulfate	240 g/L
Sulfuric acid	90 g/L
Chloride ions	80 ppm
Accelerator	0.85 mL/L
Suppressor	10 mL/L
Secondary suppressor	2 mL/L
Bath Temperature	23°C

A flash plating layer was deposited by DC plating at a current density of 2 ASD for a period of 10 minutes. Thereafter, pulse reverse plating was performed at a current density of 2.4 ASD for a period of 40 minutes to create a copper bridge in the through-holes. Thereafter

synchronous pulse plating was performed at a current density of 2.7 ASD for a period of 40 minutes to shape the bridge, followed by DC plating at a current density of 2.5 ASD for a period of 60 minutes until the through-holes were filled in a vertical plating process.

The pulse plating waveform on a first side and a second side of the substrate in the bridging step followed a sequence of:

Side A			Side B		
Step	Duration (ms)	Amplitude (%)	Step	Duration (ms)	Amplitude (%)
Step 1	120	110	Step 1	120	110
Step 2	120	260	Step 2	120	0
Step 3	140	110	Step 3	140	110
Step 4	120	-330	Step 4	120	150
Step 5	120	110	Step 5	120	110
Step 6	120	150	Step 6	120	-330
Step 7	140	110	Step 7	140	110
Step 8	120	0	Step 8	120	260

The synchronous pulse plating in the shaping step had the following parameters:

Parameter	**Value**
Reverse/Forward Ratio	2:1
Forward Time	100 ms
Reverse Time	5 ms

An observation of a cross-section of the plated circuit board showed good plating with no dimple when plating high aspect ratio through-holes.

Example 4:

An acid copper electrolyte was made up as in Example 3.

A flash plating layer was deposited by DC plating at a current density of 2 ASD for a period of 10 minutes. Thereafter, pulse reverse plating was performed at a current density of 2.4

ASD for a period of 40 minutes to create a copper bridge in the through-holes. Thereafter synchronous pulse plating was performed at a current density of 2.7 ASD for a period of 40 minutes to shape the bridge, followed by DC plating at a current density of 2.5 ASD for a period of 60 minutes until the through-holes were filled in a vertical plating process.

The pulse plating waveform on a first side and a second side of the substrate followed a sequence of:

Side A			Side B		
Step	Duration (ms)	Amplitude (%)	Step	Duration (ms)	Amplitude (%)
Step 1	110	110	Step 1	110	110
Step 2	110	260	Step 2	110	0
Step 3	110	110	Step 3	110	110
Step 4	170	-330	Step 4	170	150
Step 5	110	110	Step 5	110	110
Step 6	170	150	Step 6	170	-330
Step 7	110	110	Step 7	110	110
Step 8	110	0	Step 8	110	260

The synchronous pulse plating in the shaping step had the following parameters:

Parameter	**Value**
Reverse/Forward Ratio	2:1
Forward Time	100 ms
Reverse Time	5 ms

An observation of a cross-section of the plated circuit board showed good plating with no dimple when plating high aspect ratio through-holes.

[0131] Thus, it can be seen that the process described herein allows for the metallization of through-holes and/or blind micro-vias that do not exhibit any defects, such as unacceptable voids, cavities, or excessive dimples.

WHAT IS CLAIMED IS:

1. A method of plating a metal on an electronic substrate, wherein the electronic substrate comprises one or more features, wherein the one or more features comprise one of one or more through-holes and/or one or more micro-vias in the electronic substrate, the method comprising the steps of:

a) preparing the electronic substrate to receive metal plating thereon;

b) bringing the electronic substrate and at least one counter electrode into contact with a copper electroplating bath comprising a source of copper ions to be plated;

c) electrically polarizing first and second sides of the electronic substrate to initiate metal plating thereon, wherein the copper electroplating bath plates the one or more through-holes and/or the one or more micro-vias using a plating cycle until metallization is complete;

wherein the plating cycle comprising the steps of, in order:

1) pulse plating for a first time period on a first side and a second side of the electronic substrate to cause copper to preferentially plate in the center of the one or more through-holes, wherein the copper merges together in the center of the hole to form two opposing blind vias; and

2) direct plating for a second time period to fill the two opposing blind vias formed by pulse plating;

wherein the pulse plating step comprises applying an electrical current to electrodeposit metal from the copper electroplating bath to the first side and second side of the electronic substrate, wherein the electrical current is applied as a pulse plating cycle comprising a repeatable sequence, wherein the repeatable sequence comprises a set of pulse plating periods, each set of pulse plating periods including, in any order:

(i) at least a first forward pulse period;

(ii) at least a first reverse pulse period;

(iii) at least a second forward pulse period; and

(iv) at least a rest period.

2. The method according to claim 1, wherein the step of preparing the printed circuit board to accept electroplating thereon comprises the step of cleaning the printed circuit board prior to metallizing the one or more through-holes and/or one or more micro-vias.

3. The method according to claim 2, further comprising the step of microetching the cleaned printed circuit board.

4. The method according to any of claims 1 to 3, wherein the one or more metallized through-holes and/or one or more micro-vias do not exhibit any defects.

5. The method according to any of claims 1 to 4, wherein the metallized electroplated copper deposit completely fills the one or more through-holes and/or the one or more blind micro-vias and deposits a conformal copper deposit on the electronic substrate.

6. The method according to any of claims 1 to 3, wherein the acid copper electroplating bath is maintained at a temperature of between about 10 and about 50°C.

7. The method according to any of claims 1 to 3, further comprising the step of direct current plating using forward current for a time period prior to step 1).

8. The method according to claim 7, wherein direct current plating for the first time period deposits a flash copper layer on the surfaces of the one or through-holes and/or one or more blind micro-vias.

9. The method according to any of claims 1 to 3, wherein the electronic substrate is contacted with the acid copper electroplating solution by a method selected from the group consisting of spraying, wiping, dipping, and immersing.

10. The method according to claim 9, wherein the electronic substrate is contacted with the acid copper electroplating bath by immersing the electronic substrate in the acid copper electrolyte.

11. The method according to any of claims 1 to 3, wherein the pulse plating cycle comprising the repeatable sequence applied to the first side of the electronic substrate is the same as the

pulse plating cycle comprising the repeatable sequence applied to the second side of the electronic substrate.

12. The method according to any of claims 1 to 3, wherein the pulse plating cycle comprising the repeatable sequence applied to the first side of the electronic substrate is different from the pulse plating cycle comprising the repeatable sequence applied to the second side of the electronic substrate.

13. The method according to claim 1, wherein the set of pulse plating periods includes 8 steps, the 8 steps consisting of, in any order:

a) a first pulse of a first forward duration and first forward intensity;
b) a second pulse of a second forward duration and second forward intensity;
c) a third pulse of the first forward duration and first forward intensity;
d) a fourth pulse of a reverse duration and reverse intensity;
e) a fifth pulse of the first forward duration and first forward intensity;
f) a sixth pulse of a third forward duration and third forward intensity;
g) a seventh pulse of the first forward duration and first forward intensity; and
h) a rest period.

14. The method according to any of claims 1 to 3 or 11 to 13, wherein each set of pulse plating periods has a duration of between about 0.5 and about 5 seconds.

15. The method according to claim 14, wherein each set of pulse plating periods has a duration of 1 second.

16. The method according to any of claims 1 to 3 or 11 to 15, wherein the sequence comprises a plurality of two or more repeatable sequences arranged in a repeating series.

17. The method according to claim 12, wherein the pulse plating cycle is an asynchronous plating cycle, wherein the repeatable sequence applied to the first side of the substrate is the same as the repeatable sequence applied to the second side of the substrate, except in reverse order.

18. The method according to claim 17, wherein after the asynchronous plating cycle is performed for a period of time, a second pulse plating cycle with synchronous waveforms on the first side and the second side of the substrate is applied.

wherein the asynchronous plating cycle preferentially plates the copper in the center of the one or more through-holes such that the copper merges together in the center of the whole to form two opposing blind vias and the second pulse plating cycle shapes the thus formed two opposing blind vias.

19. The method according to claim 18, wherein the second pulse plating cycle uses a forward/reverse current ratio of between about 1:1 to 1:4 and wherein the duration of forward pulses is in the range of about 10 to 200 ms and the duration of the reverse pulses is in the range of about 0.5 to 10 ms.

20. The method according to claim 1, wherein the duration of each first forward pulse period and second forward pulse period is independently in the range of about 80 to 250 ms, the duration of each reverse pulse period is in the range of about 50 to about 150 ms, and the duration of each rest period is in the range of about 50 to about 150 ms.

21. The method according to any of claims 11 to 17, wherein at least one of the pulses of the first forward duration and the first forward intensity or the pulse of the second forward duration and second forward intensity comprises a higher intensity pulse of a shorter duration within the first forward duration or the second forward duration, wherein the higher intensity pulse has an intensity that is about 100% to about 500% of the intensity of the first forward intensity or the second forward intensity.

22. An apparatus for electroplating a metal on an electronic substrate, wherein the electronic substrate comprises one or more features, wherein the one or more features comprise one or more through-holes and/or one or more blind microvias in the electronic substrate, the apparatus comprising:

(a) means for securing the electronic substrate;

(b) at least one counter electrode;

(c) a plating tank for holding a copper electroplating bath;

(d) an array of nozzles arranged to simultaneously impinge a first side and a second side of the electronic substrate arranged in the plating tank;

(e) means for electrically polarizing first and second sides of the electronic substrate to initiate metal plating thereon;

wherein the means for electrically polarizing the first and second sides of the electronic substrates comprises one or more rectifiers, wherein the one or more rectifiers are each capable of direct and pulse reverse plating, wherein the one or more rectifiers are each connected to a microcontroller capable of being programmed with a plating cycle comprising a pulse plating cycle and a second direct current cycle;

wherein the plating cycle comprising the steps of, in order:

1) pulse plating for a first time period on a first side and a second side of the electronic substrate to cause copper to preferentially plate in the center of the one or more through-holes, wherein the copper merges together in the center of the hole to form two opposing blind vias; and
2) direct plating for a second time period to fill the two opposing blind vias formed by pulse plating;

wherein the one or more rectifiers are programmed with a first repeatable sequence comprising a set of pulse plating periods each set of pulse plating periods being composed of, in any order, (i) at least a first forward pulse period; (ii) at least a first reverse pulse period; (iii) at least a second forward pulse period; and (iv) at least a rest period, that is applied to the first side of the electronic substrate and a second repeatable sequence, the repeatable sequence comprising a set of pulse plating periods each set of pulse plating periods being composed of, in any order, (i) at least a first forward pulse period; (ii) at least a first reverse pulse period; (iii) at least a second forward pulse period; and (iv) at least a rest period, that is applied to the second side of the electronic substrate,

wherein once the pulse plating is completed, the one or more rectifiers are programmed to transition to direct current.

23. The apparatus according to claim 22, wherein the one or more rectifiers are programmed to transition to a regular pulse plating cycle comprising forward plating pulses and reverse

plating pulses between steps 1) and 2) for a period of time to shape the two opposing blind vias formed in the center of the though-holes.

24. An electronic substrate comprising one or more features metallized by the process of claim 1.

25. An electronic substrate comprising one or more features metallized by the process of claim 18.

26. A method of metallizing an electronic substrate comprising one or more high aspect ratio through holes, the method comprising the steps of:

a) preparing the electronic substrate to receive metal plating thereon;

b) bringing the electronic substrate and at least one counter electrode into contact with an acid copper electroplating bath comprising a source of copper ions to be plated;

c) electrically polarizing first and second sides of the electronic substrate to initiate metal plating thereon, wherein the acid copper electroplating bath plates the one or more through-holes using a plating cycle until metallization is complete;

wherein the plating cycle comprising the steps of, in order:

1) asynchronous pulse plating for a first time period on a first side and a second side of the electronic substrate to cause copper to preferentially plate in the center of the one or more through-holes, wherein the copper merges together in the center of the hole to form two opposing blind vias;
2) synchronous pulse plating to shape the two opposing blind vias formed in the center of the through-holes; and
3) direct plating for a second time period to fill the two opposing blind vias formed by pulse plating;

wherein the asynchronous pulse plating step comprises applying an electrical current to electrodeposit metal from the acid copper electroplating bath to the first side and second side of the electronic substrate, wherein the electrical current is applied as a pulse plating cycle comprising a repeatable sequence,

the repeatable sequence comprising a set of pulse plating periods, each set of pulse plating periods including, in any order:

(i) at least a first forward pulse period;

(ii) at least a first reverse pulse period;

(iii) at least a second forward pulse period; and

(iv) at least a rest period.

27. A printed circuit board, wherein the printed circuit board comprises:

a metallized panel in which one or more through-holes are formed;

wherein the printed circuit board comprises a conductive seed layer thereon to initiate electroplating of copper;

wherein the through-hole comprises:

a) a first copper plating layer in the center of the one or more through-holes, wherein the copper mergers together in the center of the through-hole to form two opposing blind vias;

b) optionally, a second copper plating layer deposited over the first copper plating layer, wherein the optional second copper plating layer shapes the blind vias formed by the first copper plating layer; and

c) a copper filling layer, wherein the copper filling layer is deposited over the first copper plating layer and the optional second copper plating layer to fill the one or more through-holes;

wherein the one or more through-holes are completely filled with copper, without any voids, dimples or other defects.

28. The printed circuit board according to claim 27, wherein all of layers a) to c) are present.

29. The printed circuit board according to claim 27 or claim 28, wherein the first copper layer, optional second copper layer, and copper filling layer are applied using the same acid copper plating electrolyte.

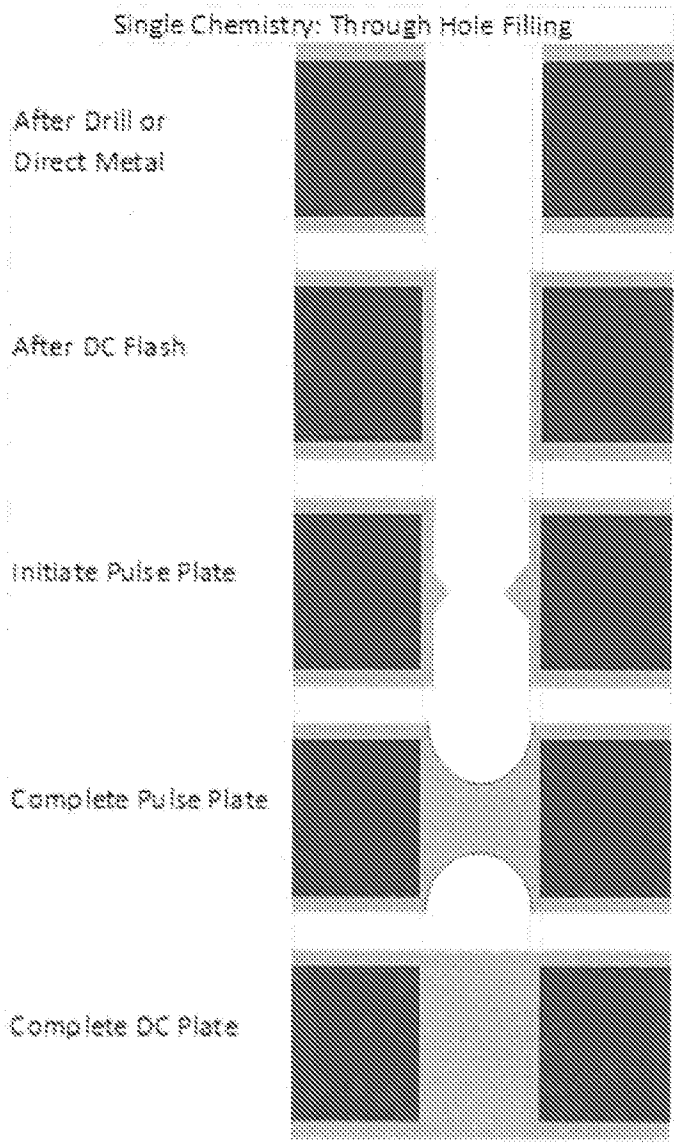

Single Chemistry: Through Hole Filling
After Drill or Direct Metal
After DC Flash
Initiate Pulse Plate
Complete Pulse Plate
Complete DC Plate

Figure 1

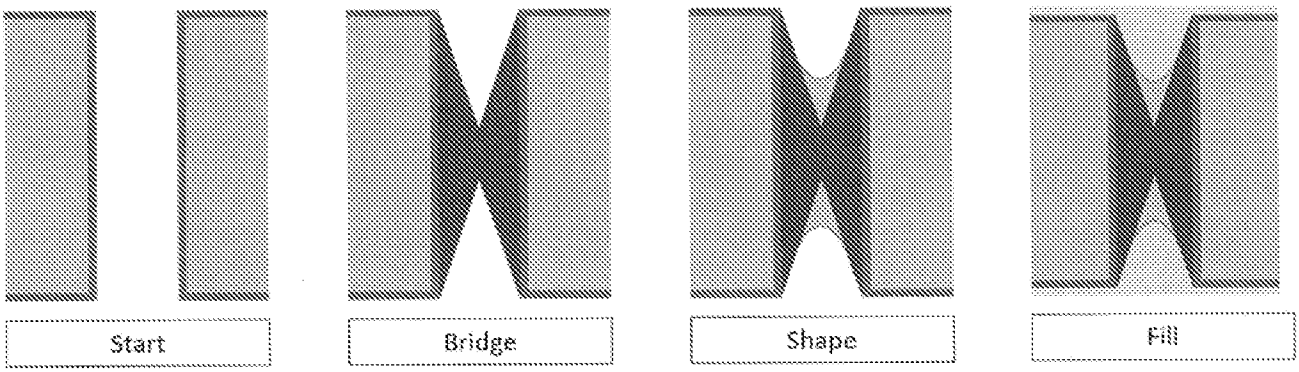


Figure 2

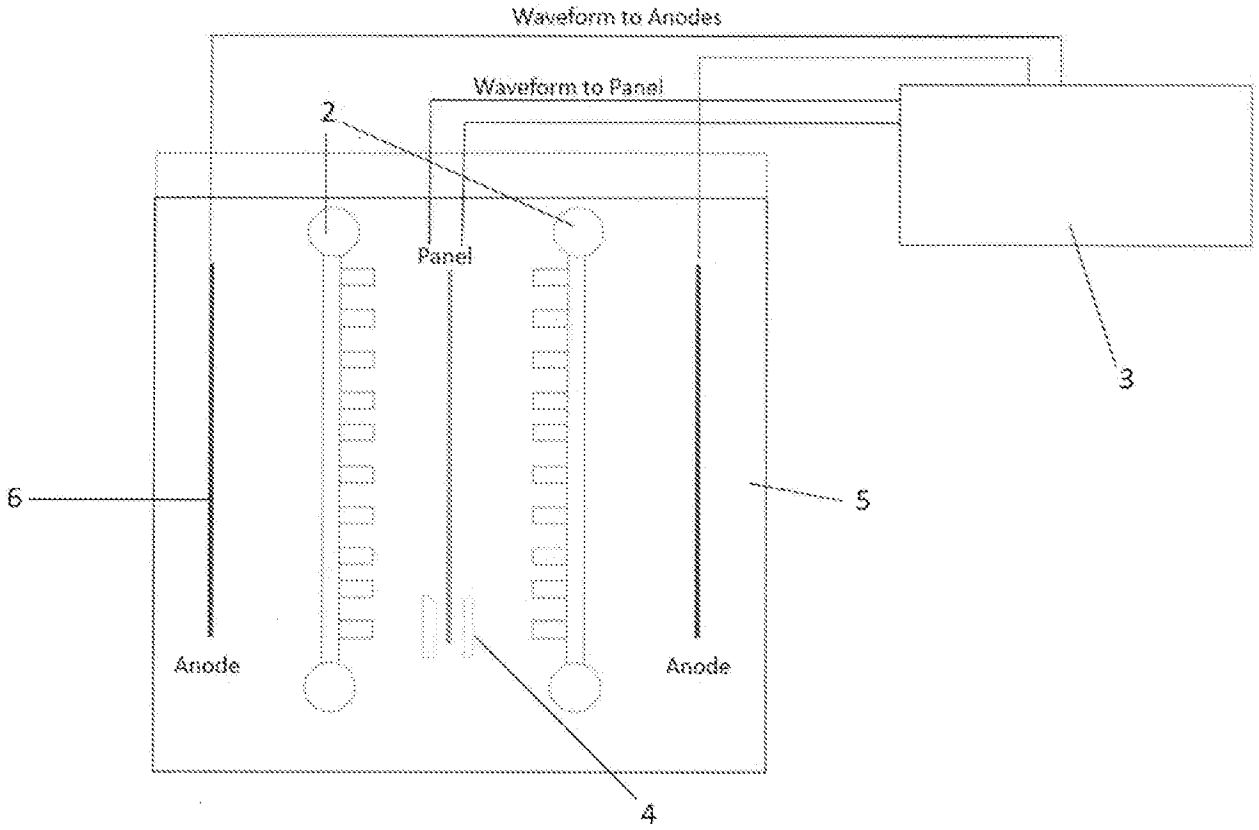

Waveform to Anodes
Waveform to Panel
2
Panel
3
6
5
Anode
Anode
4

Figure 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2022/028462

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H05K 3/42; C25D 3/38; C25D 5/00; C25D 5/18; H05K 1/02; H05K 1/18 (2022.01)
CPC - H05K 3/423; C25D 3/38; C25D 5/18; H05K 1/0206; H05K 1/181 (2022.08)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
see Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
see Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
see Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2021/0130970 A1 (MACDERMID ENTHONE INC.) 06 May 2021 (06.05.2021) entire document	1-4, 6-13, 17-20, 22-26
A	US 2010/0219081 A1 (ISONO et al) 02 September 2010 (02.09.2010) entire document	1-4, 6-13, 17-20, 22-26
A	US 2015/0289387 A1 (ATOTECH DEUTSCHLAND GMBH) 08 October 2015 (08.10.2015) entire document	1-4, 6-13, 17-20, 22-26
A	US 7,887,693 B2 (NIKOLOVA et al) 15 February 2011 (15.02.2011) entire document	1-4, 6-13, 17-20, 22-26

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 August 2022	SEP 21 2022
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450 Facsimile No. 571-273-8300	Authorized officer Taina Matos Telephone No. PCT Helpdesk: 571-272-4300

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2022/028462

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☒ Claims Nos.: 5, 14-16, 21
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

See extra sheet(s).

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-4, 6-13, 17-20, 22-26

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

Continued from Box No. III Observations where unity of invention is lacking

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fees must be paid.

Group I, claims 1-4, 6-13, 17-20, 22-26, is drawn to a method of plating a metal on an electronic substrate, the method comprising the steps of: preparing the electronic substrate to receive metal plating thereon; bringing the electronic substrate and at least one counter electrode into contact with a copper electroplating bath.

Group II, claims 27-29, is drawn to a printed circuit board, wherein the printed circuit board comprises; a metallized panel in which one or more through-holes are formed.

The inventions listed as Groups I-II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: the special technical feature of the Group I invention: pulse plating for a first time period on a first side and a second side of the electronic substrate to cause copper to preferentially plate in the center of the one or more through-holes, wherein the copper merges together in the center of the hole to form two opposing blind vias; and direct plating for a second time period to fill the two opposing blind vias formed by pulse plating; wherein the pulse plating step comprises applying an electrical current to electrodeposit metal from the copper electroplating bath to the first side and second side of the electronic substrate, wherein the electrical current is applied as a pulse plating cycle comprising a repeatable sequence, wherein the repeatable sequence comprises a set of pulse plating periods, each set of pulse plating periods including, in any order: (i) at least a first forward pulse period; (ii) at least a first reverse pulse period; (iii) at least a second forward pulse period; and (iv) at least a rest period as claimed therein is not present in the invention of Group II. The special technical feature of the Group II invention: the printed circuit board comprises; a metallized panel in which one or more through-holes are formed; wherein the printed circuit board comprises a conductive seed layer thereon to initiate electroplating of copper; optionally, a second copper plating layer deposited over the first copper plating layer, wherein the optional second copper plating layer shapes the blind vias formed by the first copper plating layer; and a copper filling layer, wherein the. copper filling layer is deposited over the first copper plating layer and the optional second copper• plating layer to till the one or more through-holes; wherein the one or more through-holes are completely filled with copper, without any voids, dimples or other defects as claimed therein is not present in the invention of Group I.

Groups I and II lack unity of invention because even though the inventions of these groups require the technical feature of the electronic substrate comprise one or more through-holes and/or one or more blind vias, wherein a first copper plating layer in the center of the one or more through-holes, wherein the copper mergers together in the center of the through-hole to form two opposing vias, this technical feature is not a special technical feature as it does not make a contribution over the prior art.

Specifically, US 2021/0130970 to MacDermid Enthone Inc. teaches the electronic substrate comprise one or more through-holes and/or one or more blind vias, wherein a first copper plating layer in the center of the one or more through-holes, wherein the copper mergers together in the center of the through-hole to form two opposing vias (Paras. [0060-0069]).

Since none of the special technical features of the Group I or II inventions are found in more than one of the inventions, unity of invention is lacking.