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(54) **Title**: METHOD OF FORMING FINNED SEMICONDUCTOR DEVICES WITH TRENCH ISOLATION

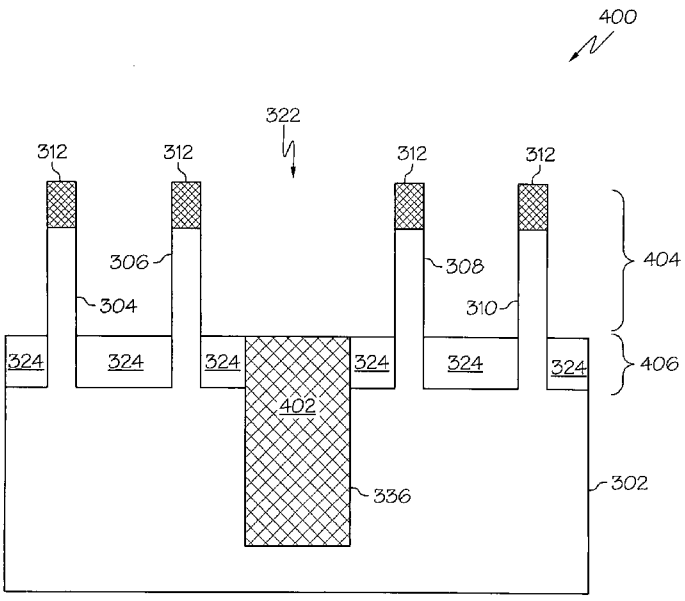

FIG. 12

(57) **Abstract**: A method of manufacturing a semiconductor device structure (300), such as a FinFET device structure, is provided. The method begins by providing a substrate comprising a bulk semiconductor material (302), a first conductive fin structure (306) formed from the bulk semiconductor material (302), and a second conductive fin structure (308) formed from the bulk semiconductor material (302). The first conductive fin structure (306) and the second conductive fin structure (308) are separated by a gap (322). Next, spacers (332, 334) are formed in the gap (322) and adjacent to the first conductive fin structure (306) and the second conductive fin structure (308). Thereafter, an etching step etches the bulk semiconductor material (302), using the spacers (332, 334) as an etch mask, to form an isolation trench (336) in the bulk semiconductor material (302). A dielectric material (340) is formed in the isolation trench (336), over the spacers (332, 334), over the first conductive fin structure (306), and over the second conductive fin structure (308). Thereafter, at least a portion of the dielectric material (340) and at least a portion of the spacers (332, 334) are etched away to expose an upper section (342) of the first conductive fin structure (306) and an upper section (342) of the second conductive fin structure (308), while preserving the dielectric material (340) in the isolation trench (336). Following these steps, the fabrication of the devices is completed in a conventional manner.

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METHOD OF FORMING FINNED SEMICONDUCTOR DEVICES WITH TRENCH ISOLATION

TECHNICAL FIELD

[0001] Embodiments of the subject matter described herein relate generally to semiconductor devices and related manufacturing processes. More particularly, embodiments of the subject matter relate to methods of forming semiconductor devices, such as FinFET devices, having trench isolation.

BACKGROUND

[0002] Transistors, such as metal oxide semiconductor field-effect transistors (MOSFETs), are the core building block of the vast majority of semiconductor devices. Some semiconductor devices, such as high performance processor devices, can include millions of transistors. For such devices, decreasing transistors size, and thus increasing transistor density, has traditionally been a high priority in the semiconductor manufacturing industry.

[0003] A FinFET is a type of transistor that can be fabricated using very small scale processes. FIG. 1 is a simplified perspective view of a FinFET 100, which is formed on a semiconductor wafer substrate 102. A FinFET is named for its use of one or more conductive fins (FinFET 100 includes only one fin 104). As shown in FIG. 1, fin 104 extends between a source region 106 and a drain region 108 of FinFET 100. FinFET 100 includes a gate structure 110 that is wrapped around fin 104. The dimensions of fin 104 wrapped by gate structure 110 determine the effective channel of FinFET 100. FIG. 2 is a simplified perspective view of another FinFET 200; this particular version includes three fins 202 extending between a source region 204 and a drain region 206. As with FinFET 100, a gate structure 208 is formed across the three fins 202. When multiple fins are employed in this manner, it can be extremely important to maintain uniform fin thickness and uniform fin pitch (the distance between two adjacent fins, plus fin thickness).

[0004] FinFET devices have historically been formed using silicon-on-insulator (SOI) substrates. Using an SOI substrate, the conductive fins are formed from the silicon material, while the insulator layer provides isolation between adjacent FinFET devices. Bulk silicon substrates are less expensive than SOI substrates, and FinFET devices can also be fabricated using bulk silicon if appropriate isolation methodologies are utilized. One known isolation methodology for FinFETs formed from a bulk silicon substrate requires multiple

photolithography and etching steps to create the trenches between n-channel and p-channel transistor devices. The cost and complexity of such multiple photolithography and etching steps can overshadow the benefits of using a bulk silicon substrate rather than SOI.

BRIEF SUMMARY

[0005] A FinFET fabrication technique as described herein can be utilized with a bulk semiconductor substrate, and can be used in conjunction with different process technologies. The fabrication technique creates isolation trenches between adjacent FinFET devices without requiring additional photolithography and etching steps. The resulting isolation trenches are self-aligned relative to the edges of the adjacent FinFET devices (e.g., adjacent PMOS and NMOS transistor devices).

[0006] The above and other aspects may be carried out by an embodiment of a trench isolation method for finned semiconductor devices. The method involves forming, from a bulk semiconductor substrate, a first conductive fin set and a second conductive fin set, the first conductive fin set and the second conductive fin set being separated by a gap. The method then deposits an oxide material over the first conductive fin set, the second conductive fin set, and the bulk semiconductor substrate. The oxide material forms a recess that corresponds to the gap, where the recess is defined by opposing sidewalls of the oxide material. The recess is deepened into the bulk semiconductor substrate to form a trench that is self-aligned with the opposing sidewalls, and the trench is filled with a dielectric material.

[0007] A method of manufacturing a semiconductor device structure is also provided. The method involves providing a substrate comprising a bulk semiconductor material, a first conductive fin structure formed from the bulk semiconductor material, and a second conductive fin structure formed from the bulk semiconductor material, where the first conductive fin structure and the second conductive fin structure are separated by a gap. The method forms spacers in the gap and adjacent the first conductive fin structure and the second conductive fin structure, and then etches the bulk semiconductor material, using the spacers as an etch mask, to form an isolation trench in the bulk semiconductor material. A dielectric material is placed in the isolation trench, over the spacers, over the first conductive fin structure, and over the second conductive fin structure, and the dielectric material is subsequently etched, along with the spacers, to expose an upper section of the first conductive fin structure and an upper section of the second conductive fin structure, while preserving the dielectric material in the isolation trench. An alternate embodiment of this

method removes the spacers before forming the dielectric material in the isolation trench, over the first conductive fin structure, and over the second conductive fin structure.

[0008] This summary is provided to introduce a selection of concepts in a simplified form that are further described below in the detailed description. This summary is not intended to identify key features or essential features of the claimed subject matter, nor is it intended to be used as an aid in determining the scope of the claimed subject matter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] A more complete understanding of the subject matter may be derived by referring to the detailed description and claims when considered in conjunction with the following figures, wherein like reference numbers refer to similar elements throughout the figures.

[0010] FIG. 1 is a simplified perspective view of a conventional FinFET;

[0011] FIG. 2 is a simplified perspective view of a conventional FinFET having a plurality of fins;

[0012] FIGS. 3-10 are cross sectional views that illustrate an embodiment of a semiconductor device structure and a related fabrication method; and

[0013] FIGS. 11 and 12 are cross sectional views that illustrate an alternate embodiment of a semiconductor device structure and steps of a related fabrication method.

DETAILED DESCRIPTION

[0014] The following detailed description is merely illustrative in nature and is not intended to limit the embodiments of the subject matter or the application and uses of such embodiments. As used herein, the word "exemplary" means "serving as an example, instance, or illustration." Any implementation described herein as exemplary is not necessarily to be construed as preferred or advantageous over other implementations. Furthermore, there is no intention to be bound by any expressed or implied theory presented in the preceding technical field, background, brief summary or the following detailed description.

[0015] For the sake of brevity, conventional techniques related to semiconductor device fabrication may not be described in detail herein. Moreover, the various tasks and process steps described herein may be incorporated into a more comprehensive procedure or process having additional steps or functionality not described in detail herein. In particular, various steps in the manufacture of semiconductor transistor devices are well known and so, in the

interest of brevity, many conventional steps will only be mentioned briefly herein or will be omitted entirely without providing the well known process details.

[0016] The techniques and technologies described herein may be utilized to fabricate MOS transistor devices, including NMOS transistor devices, PMOS transistor devices, and CMOS transistor devices. Although the term "MOS device" properly refers to a device having a metal gate electrode and an oxide gate insulator, that term will be used throughout to refer to any semiconductor device that includes a conductive gate electrode (whether metal or other conductive material) that is positioned over a gate insulator (whether oxide or other insulator) which, in turn, is positioned over a semiconductor substrate.

[0017] A variety of FinFET devices and related fabrication processes are known. For example, United States Patent numbers 6,872,647 and 6,921,963 – both assigned to Advanced Micro Devices, Inc. – are related to FinFETs and processes for manufacturing FinFETs (the relevant content of these two patents is incorporated by reference herein). In accordance with the traditional manufacturing techniques described in these two patents, conductive fins in a FinFET device are formed using photolithography, etching, and other conventional process steps. FinFET performance is dependent on the thickness and pitch of fins, and the thickness and pitch should be uniform and closely controlled during manufacturing. In this regard, fabricating FinFETs using modern semiconductor manufacturing processes (e.g., 32 nm and smaller technologies) can be challenging due to the importance of controlling the dimensions of the fins.

[0018] The techniques and technologies described herein can be utilized to form isolation regions between adjacent FinFET devices formed on a bulk semiconductor substrate. FIGS. 3-10 are cross sectional views that illustrate an embodiment of a semiconductor device structure 300 and an exemplary method of fabricating it. This fabrication process represents one implementation of a trench isolation method that is suitable for use with finned semiconductor devices, such as FinFETs. FIG. 3 depicts the semiconductor device structure 300 at an intermediate stage of the fabrication process, namely, after providing a suitable substrate, formation of conductive fins on the substrate, and formation of nitride caps on the conductive fins. For this particular embodiment, semiconductor device structure 300 utilizes a bulk semiconductor substrate, such as a bulk silicon substrate 302. The term "silicon substrate" is used herein to encompass the generally monocrystalline and relatively pure silicon materials typically used in the semiconductor industry. Bulk silicon substrate 302 can originally be either N-type or P-type silicon, but is typically P-type, and bulk silicon substrate

302 is subsequently doped in an appropriate manner to form active regions. Here, the conductive fins are formed from bulk silicon substrate 302 in a conventional manner.

[0019] Again, FIG. 3 illustrates semiconductor device structure 300 in a state after the formation of a plurality of conductive fins 304, 306, 308, and 310 from bulk silicon substrate 302, and after formation of silicon nitride caps 312 on the top of the fins. The combination of a conductive fin and its overlying nitride cap may be referred to herein as a "conductive fin structure." The fins and caps are formed using well known techniques and process steps (e.g., techniques and steps related to photolithography and patterning, sidewall image transfer, etching, material growth, material deposition, surface planarization, and the like). Conductive fins 304 and 306 together form a first conductive fin set 314, and conductive fins 308 and 310 form a second conductive fin set 316. Although semiconductor device structure 300 includes two fins per set, alternate embodiments need not be so configured. Indeed, a conductive fin set may include any number of fins, including one. Moreover, the number of fins in first conductive fin set 314 need not be equal to the number of fins in second conductive fin set 316 (due to mobility differences, there are usually more p-type device fins than n-type device fins). After fabrication of semiconductor device structure 300 is complete, the first set 314 will be utilized for a first device (e.g., an NMOS transistor device), and the second set 316 will be utilized for a second device (e.g., a PMOS transistor device), where the two devices are isolated from one another.

[0020] The conductive fins in each set are formed such that they have a uniform pitch and a uniform fin thickness. In practice, the fin pitch and thickness will typically be the same for both conductive fin sets 314 and 316. In FIG. 3, the arrow 318 represents the fin thickness of conductive fin 304, and the arrow 320 represents the pitch between the two adjacent and neighboring fins 308 and 310. In some embodiments, the fin thickness can be within the range of about 10-60 nm (preferably about 10-20 nm), and the fin pitch can be within the range of about 30-300 nm (preferably about 40-50 nm). For certain embodiments, the conductive fins are about 40-70 nm high, and silicon nitride caps 312 are about 20-40 nm high. It should be appreciated that these exemplary dimensions are provided to establish a convenient and realistic frame of reference, and that the actual dimensions of a practical embodiment of semiconductor device structure 300 might vary.

[0021] First conductive fin set 314 and second conductive fin set 316 are separated by a gap 322, which is generally defined between conductive fin 306 and conductive fin 308. Notably, the gap 322 separates first conductive fin set 314 from second conductive fin set 316 by a distance that is greater than the designated fin pitch 320 for semiconductor device

structure 300. The gap 322 may represent the space that would otherwise be occupied by at least one conductive fin formed in accordance with the designated fin pitch 320. For example, semiconductor device structure 300 represents an embodiment where the gap 322 would otherwise accommodate only one conductive fin. Other embodiments may utilize a wider gap that might correspond to more than one "missing" conductive fin.

[0022] Although other fabrication steps or sub-processes may be performed after the step in the process depicted in FIG. 3, this example continues by depositing an insulator material, such as an oxide (preferably, silicon oxide) over the first conductive fin set 314, over the second conductive fin set 316, and over the bulk silicon substrate 302 (FIG. 4). In other words, the oxide material 324 is deposited in a blanket manner to cover the exposed surfaces of semiconductor device structure 300. As depicted in FIG. 4, after deposition, the oxide material 324 fills in the spaces between adjacent fins in each conductive fin set, and lines the space defined by the gap 322. If this deposition step is controlled properly, then oxide material 324 will not completely fill the gap 322, and the oxide material 324 will generally follow the overall contour of the gap 322. For the illustrated embodiment, the oxide material 324 is deposited to a thickness of about 25-30 nm.

[0023] The deposition of the oxide material 324 results in the formation of a recess 326 that generally corresponds to the location and contour of the gap 322. This recess 326 is defined by certain features of oxide material 324. In particular, recess 326 is bounded by the opposing sidewalls 328 of oxide material 324, and by the lowermost exposed surface 330 of oxide material 324.

[0024] Although other fabrication steps or sub-processes may be performed after the formation of oxide material 324, this example continues with an etching step, which preferably employs an anisotropic etch technique (i.e., a directional etch). FIG. 5 depicts the result of anisotropically etching oxide material 324 to extend recess 326 to the bulk silicon substrate 302. In other words, recess 326 now terminates at bulk silicon substrate 302. The etchant chemistry used in this step selectively etches oxide material 324 while leaving silicon nitride caps 312 and bulk silicon substrate 302 substantially intact. The anisotropic nature of this etching step forms spacers 332 and 334 in gap 322. Spacer 332 is adjacent to conductive fin 306, and spacer 334 is adjacent to conductive fin 308. These spacers 332 and 334 are often referred to as sidewall spacers. Indeed, spacers 332 and 334 are generally aligned with, and correspond to, the opposing sidewalls 328 of the originally deposited oxide material 324.

[0025] Although other fabrication steps or sub-processes may be performed after the formation of spacers 332 and 334, this example continues with another etching step (FIG. 6).

The etchant chemistry used in this step selectively etches silicon while leaving oxide material 324 and silicon nitride caps 312 substantially intact. This etching step preferably utilizes an anisotropic etch technique to etch the bulk silicon substrate 302, using oxide material 324 as an etch mask. More specifically, spacers 332 and 334 serve as a hard etch mask to form an isolation trench 336 in the bulk silicon substrate 302. Notably, this etching step deepens recess 326 into bulk silicon substrate 302 to form isolation trench 336, which is self-aligned with opposing sidewalls 328 (and, therefore, self-aligned with spacers 332 and 334). In certain embodiments, isolation trench 336 is etched to a depth within the range of about 0.15-0.50 μm (with a preferred depth of about 0.15 μm).

[0026] FIG. 7 depicts the state of semiconductor device structure 300 after completion of an optional re-oxidation step. This optional step may be performed to repair the silicon material interface, which typically suffers some damage during etching. In accordance with conventional re-oxidation techniques, semiconductor device structure 300 will be exposed to oxygen while being maintained at a high temperature, which results in the oxidation of the exposed silicon material in isolation trench 336. FIG. 7 depicts this resulting oxide layer 338 using an exaggerated scale for ease of illustration. Notably, this re-oxidation step also oxidizes the conductive fins because in this embodiment the oxide material 324 does not serve as an adequate oxygen barrier. Thus, if this optional re-oxidation step is included in the fabrication process, then the original fin width and fin pitch may need to be controlled to accommodate the narrowing of the fins caused by the formation of the oxide layer 338.

[0027] For the sake of brevity and simplicity, the following description assumes that the optional re-oxidation step is not performed. Accordingly, although other fabrication steps or sub-processes may be performed after the formation of isolation trench 336, this example continues by removing the oxide material 324, including spacers 332 and 334, from semiconductor device structure 300. FIG. 8 depicts the state of semiconductor device structure 300 after removal of the oxide material 324. In practice, oxide material 324 is removed during a suitable etching step, which preferably employs an isotropic wet etch technique using, for example, a diluted HF chemistry. This wet oxide etch selectively etches oxide material 324 while leaving silicon nitride caps 312 and bulk silicon substrate 302 substantially intact. As shown in FIG. 8, this etching step exposes conductive fins 304, 306, 308, and 310, along with silicon nitride caps 312. Removal of oxide material 324 is preferred to improve the uniformity (device-to-device and wafer-to-wafer) and controllability of the subsequent process steps described below.

[0028] Although other fabrication steps or sub-processes may be performed after the removal of spacers 332 and 334, this example continues by filling isolation trench 336 with a suitable dielectric material (FIG. 9). In practice, a dielectric material 340 can be formed in isolation trench 336, over conductive fins 304, 306, 308, and 310, over silicon nitride caps 312, and over bulk silicon substrate 302 using, for example, an appropriate deposition technique such as chemical vapor deposition. In certain embodiments, the dielectric material 340 is silicon dioxide deposited using tetraethyl orthosilicate (TEOS) as a silicon source (commonly referred to as TEOS oxide).

[0029] FIG. 9 illustrates the condition of semiconductor device structure 300 after deposition of dielectric material 340, and after dielectric material 340 has been polished or planarized. For example, chemical mechanical polishing may be performed to polish the TEOS oxide to the height of the conductive fin structures. In this regard, FIG. 9 shows how silicon nitride caps 312 can be used to control the polishing such that the resulting height of the TEOS oxide corresponds to the height of silicon nitride caps 312.

[0030] Although other fabrication steps or sub-processes may be performed after the formation of dielectric material 340 as shown in FIG. 9, this example continues by reducing the height of dielectric material 340. FIG. 10 depicts the state of semiconductor device structure 300 after at least a portion of dielectric material 340 has been removed. In preferred embodiments, dielectric material 340 is removed during a timed endpoint etch that selectively etches the TEOS oxide material while leaving the conductive fins, the caps 312, and bulk silicon substrate 302 substantially intact. In this regard, the duration of the etching step is controlled to achieve the desired remaining height of the TEOS oxide material, and such that the layer of dielectric material 340 is uniformly recessed.

[0031] Referring to FIG. 10, the etching of dielectric material 340 exposes an upper section 342 of each conductive fin structure. In other words, silicon nitride caps 312 and the upper lengths of the conductive fins become exposed due to the etching of dielectric material 340 to a remaining height relative to the conductive fins. Notably, the dielectric material 340 that resides in isolation trench 336 is preserved. This serves to electrically isolate the two adjacent device structures from one another. Moreover, a layer 344 of the dielectric material 340 is retained at the base of the conductive fins. This layer 344 is utilized during subsequent process steps. For example, layer 344 of dielectric material 340 can be used to enable ion implantation into the underlying bulk silicon substrate 302.

[0032] Thereafter, any number of known process steps can be performed to complete the fabrication of the first device structure (which in this example includes conductive fins 304

and 306) and to complete the fabrication of the second device structure (which in this example includes conductive fins 308 and 310). In practice, the first device structure may be an NMOS transistor device structure, and the second device structure may be a PMOS transistor device structure, and the dielectric material 340 in isolation trench 336 serves to isolate the NMOS and PMOS transistor device structures.

[0033] Referring back to the state of semiconductor device structure 300 depicted in FIG. 6, an alternate fabrication process may proceed in a different manner than that described above. In this regard, FIGS. 11 and 12 are cross sectional views that illustrate an alternate embodiment of a semiconductor device structure 400 and steps of a related fabrication method. Referring to FIG. 11, this alternate embodiment does not remove oxide material 324 or spacers 332 and 334. Instead, a dielectric material 402 is formed in isolation trench 336, over oxide material 324 (which includes spacers 332 and 334), and over the conductive fin structures (which include the conductive fins 304, 306, 308 and 310, and the corresponding silicon nitride caps 312). In practice, the dielectric material 402 may be, for example, an oxide that is grown by heating the silicon in an oxidizing ambient (i.e., thermally grown oxide rather than a deposited oxide).

[0034] FIG. 11 illustrates the condition of semiconductor device structure 400 after deposition of dielectric material 402, and after dielectric material 402 has been polished or planarized. For example, chemical mechanical polishing may be performed to polish the dielectric material 402 to the height of the conductive fin structures. In this regard, FIG. 11 depicts some dielectric material 402 in the upper surface depressions of oxide material 324. Notably, silicon nitride caps 312 can be used to control the polishing such that the resulting height of the dielectric material 402 corresponds to the height of silicon nitride caps 312.

[0035] Although other fabrication steps or sub-processes may be performed after the formation of dielectric material 402 as shown in FIG. 11, this example continues by etching at least a portion of the dielectric material 402 and at least a portion of oxide material 324 (including spacers 332 and 334). FIG. 12 depicts the state of semiconductor device structure 400 after completion of this etching step. In practice, the fabrication process employs a timed endpoint etching technique and an appropriate etchant chemistry that selectively etches dielectric material 402 and oxide material 324, while leaving the conductive fins, the silicon nitride caps 312, and bulk silicon substrate 302 substantially intact.

[0036] Referring to FIG. 12, the etching of dielectric material 402 and oxide material 324 exposes an upper section 404 of each conductive fin structure, as explained above with reference to FIG. 10. Notably, the dielectric material 402 that resides in isolation trench 336

is preserved, and a layer 406 of the oxide material 324 is retained at the base of the conductive fins, as described above for the other embodiment. It should be appreciated that the state of semiconductor device structure 400 depicted in FIG. 12 is similar and functionally equivalent to the state of semiconductor device structure 300 depicted in FIG. 10.

[0037] Thereafter, any number of known process steps can be performed to complete the fabrication of the device structures in semiconductor device structure 400. Again, conductive fins 304 and 306 may form part of an NMOS transistor device structure, conductive fins 308 and 310 may form part of an adjacent PMOS transistor device structure, and the dielectric material 402 located in isolation trench 336 serves to isolate the NMOS and PMOS transistor device structures from each other.

[0038] While at least one exemplary embodiment has been presented in the foregoing detailed description, it should be appreciated that a vast number of variations exist. It should also be appreciated that the exemplary embodiment or embodiments described herein are not intended to limit the scope, applicability, or configuration of the claimed subject matter in any way. Rather, the foregoing detailed description will provide those skilled in the art with a convenient road map for implementing the described embodiment or embodiments. It should be understood that various changes can be made in the function and arrangement of elements without departing from the scope defined by the claims, which includes known equivalents and foreseeable equivalents at the time of filing this patent application.

CLAIMS

What is claimed is:

1. A trench isolation method for finned semiconductor devices, the method comprising:

forming, from a bulk semiconductor substrate (302), a first conductive fin set (314) and a second conductive fin set (316), the first conductive fin set (314) and the second conductive fin set (316) being separated by a gap (322);

depositing an oxide material (324) over the first conductive fin set (314), the second conductive fin set (316), and the bulk semiconductor substrate (302), the oxide material (324) forming a recess (326) that corresponds to the gap (322), the recess (326) being defined by opposing sidewalls (328) of the oxide material (324);

deepening the recess (326) into the bulk semiconductor substrate (302) to form a trench (336) that is self-aligned with the opposing sidewalls (328); and

filling the trench (336) with a dielectric material (340).

2. The method of claim 1, wherein the forming step forms a plurality of conductive fins (304, 306) in the first conductive fin set (314), and a plurality of conductive fins (308, 310) in the second conductive fin set (316).

3. The method of claim 2, wherein the forming step forms the plurality of conductive fins (304, 306) in the first conductive fin set (314) and the plurality of conductive fins (308, 310) in the second conductive fin set (316) in accordance with a designated fin pitch (320), and such that the gap (322) separates the first conductive fin set (314) from the second conductive fin set (316) by a distance greater than the designated fin pitch (320).

4. The method of claim 1, wherein deepening the recess (326) comprises:

etching the oxide material (324) to extend the recess (326) to the bulk semiconductor substrate (302); and

thereafter etching the bulk semiconductor substrate (302) using the oxide material (324) as an etch mask.

5. The method of claim 1, wherein filling the trench (336) comprises depositing an oxide (340) in the trench (336), over the bulk semiconductor substrate (302), over the first conductive fin set (314), and over the second conductive fin set (316).

6. The method of claim 5, further comprising polishing the oxide (340) to a height of the first conductive fin set (314) and the second conductive fin set (316).

7. The method of claim 6, further comprising etching the oxide (340) to expose only a portion of the first conductive fin set (314) and to expose only a portion of the second conductive fin set (316).

8. A method of manufacturing a semiconductor device structure (300), the method comprising:

providing a substrate comprising a bulk semiconductor material (302), a first conductive fin structure (306) formed from the bulk semiconductor material (302), and a second conductive fin structure (308) formed from the bulk semiconductor material (302), the first conductive fin structure (306) and the second conductive fin structure (308) being separated by a gap (322);

forming spacers (332, 334) in the gap (322) and adjacent the first conductive fin structure (306) and the second conductive fin structure (308);

etching the bulk semiconductor material (302), using the spacers (332, 334) as an etch mask, to form an isolation trench (336) in the bulk semiconductor material (302);

forming a dielectric material (340) in the isolation trench (336), over the spacers (332, 334), over the first conductive fin structure (306), and over the second conductive fin structure (308); and

etching at least a portion of the dielectric material (340) and at least a portion of the spacers (332, 334) to expose an upper section (342) of the first conductive fin structure and an upper section (342) of the second conductive fin structure (308), while preserving the dielectric material (340) in the isolation trench (336).

9. The method of claim 8, wherein forming spacers (332, 334) comprises:

depositing an oxide material (324) over the first conductive fin structure (306), the second conductive fin structure (308), and the bulk semiconductor material (302), the oxide material (324) forming a recess (326) that corresponds to the gap (322); and

anisotropically etching the oxide material (324) such that the recess (326) extends to the bulk semiconductor material (302).

10. The method of claim 8, wherein etching the bulk semiconductor material (302) forms the isolation trench (336) such that it is self-aligned with the spacers (332, 334).

11. The method of claim 8, further comprising polishing the dielectric material (340) to a height of the first conductive fin structure (306) and the second conductive fin structure (308), prior to etching at least a portion of the dielectric material (340) and at least a portion of the spacers (332, 334).

12. The method of claim 11, wherein the step of etching at least a portion of the dielectric material (340) and at least a portion of the spacers (332, 334) uses an endpoint etching technique.

13. The method of claim 8, further comprising:

completing fabrication of a first device structure that includes the first conductive fin structure (306); and

completing fabrication of a second device structure that includes the second conductive fin structure (308); wherein

the dielectric material (340) in the isolation trench (336) electrically isolates the first device structure from the second device structure.

14. A method of manufacturing a semiconductor device structure (300), the method comprising:

providing a substrate comprising a bulk semiconductor material (302), a first conductive fin structure (306) formed from the bulk semiconductor material (302), and a second conductive fin structure (308) formed from the bulk semiconductor material (302), the first conductive fin structure (306) and the second conductive fin structure (308) being separated by a gap (322);

forming spacers (332, 334) in the gap (322) and adjacent the first conductive fin structure (306) and the second conductive fin structure (308);

etching the bulk semiconductor material (302), using the spacers (332, 334) as an etch mask, to form an isolation trench (336) in the bulk semiconductor material (302);

removing the spacers (332, 334);

forming a dielectric material (340) in the isolation trench (336), over the first conductive fin structure (306), and over the second conductive fin structure (308); and

etching at least a portion of the dielectric material (340) to expose an upper section (342) of the first conductive fin structure (306) and an upper section (342) of the second conductive fin structure (308), while preserving the dielectric material (340) in the isolation trench (336).

15. The method of claim 14, wherein forming spacers (332, 334) comprises:

depositing an oxide material (324) over the first conductive fin structure (306), the second conductive fin structure (308), and the bulk semiconductor material (302), the oxide material (324) forming a recess (326) that corresponds to the gap (322); and

anisotropically etching the oxide material (324) such that the recess (326) extends to the bulk semiconductor material (302).

16. The method of claim 14, wherein etching the bulk semiconductor material (302) forms the isolation trench (336) such that it is self-aligned with the spacers (332, 334).

17. The method of claim 14, further comprising polishing the dielectric material (340) to a height of the first conductive fin structure (306) and the second conductive fin structure (308), prior to etching at least a portion of the dielectric material (340).

18. The method of claim 17, wherein the step of etching at least a portion of the dielectric material (340) uses an endpoint etching technique.

19. The method of claim 14, further comprising:

completing fabrication of an NMOS transistor device structure that includes the first conductive fin structure (306); and

completing fabrication of a PMOS transistor device structure that includes the second conductive fin structure (308); wherein

the dielectric material (340) in the isolation trench (336) electrically isolates the NMOS transistor device structure from the PMOS transistor device structure.

20. The method of claim 14, wherein removing the spacers (332, 334) comprises selectively etching away the spacers (332, 334).

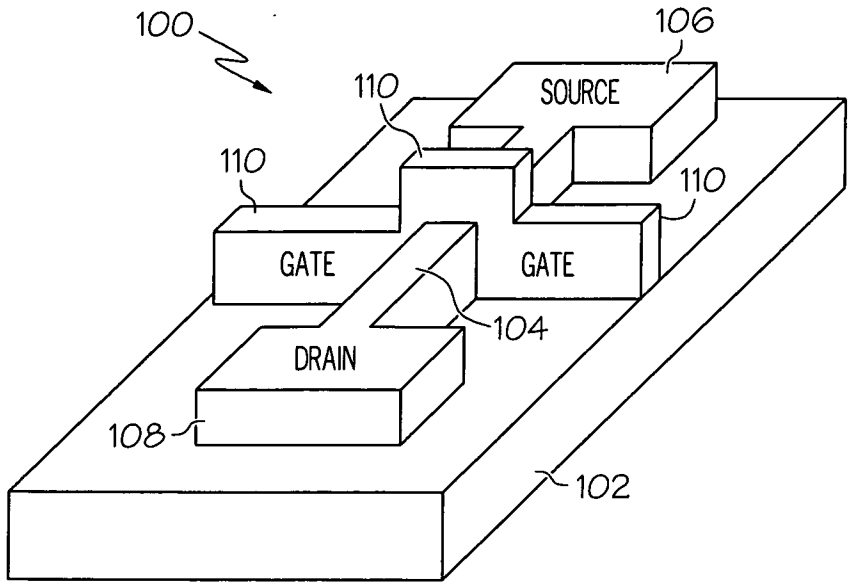


FIG. 1
(PRIOR ART)

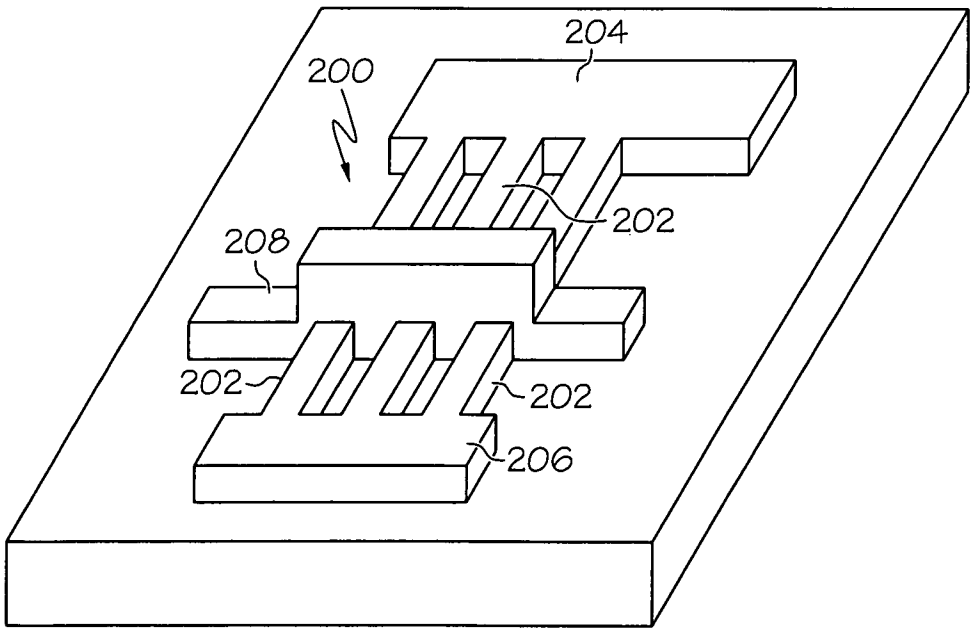


FIG. 2
(PRIOR ART)

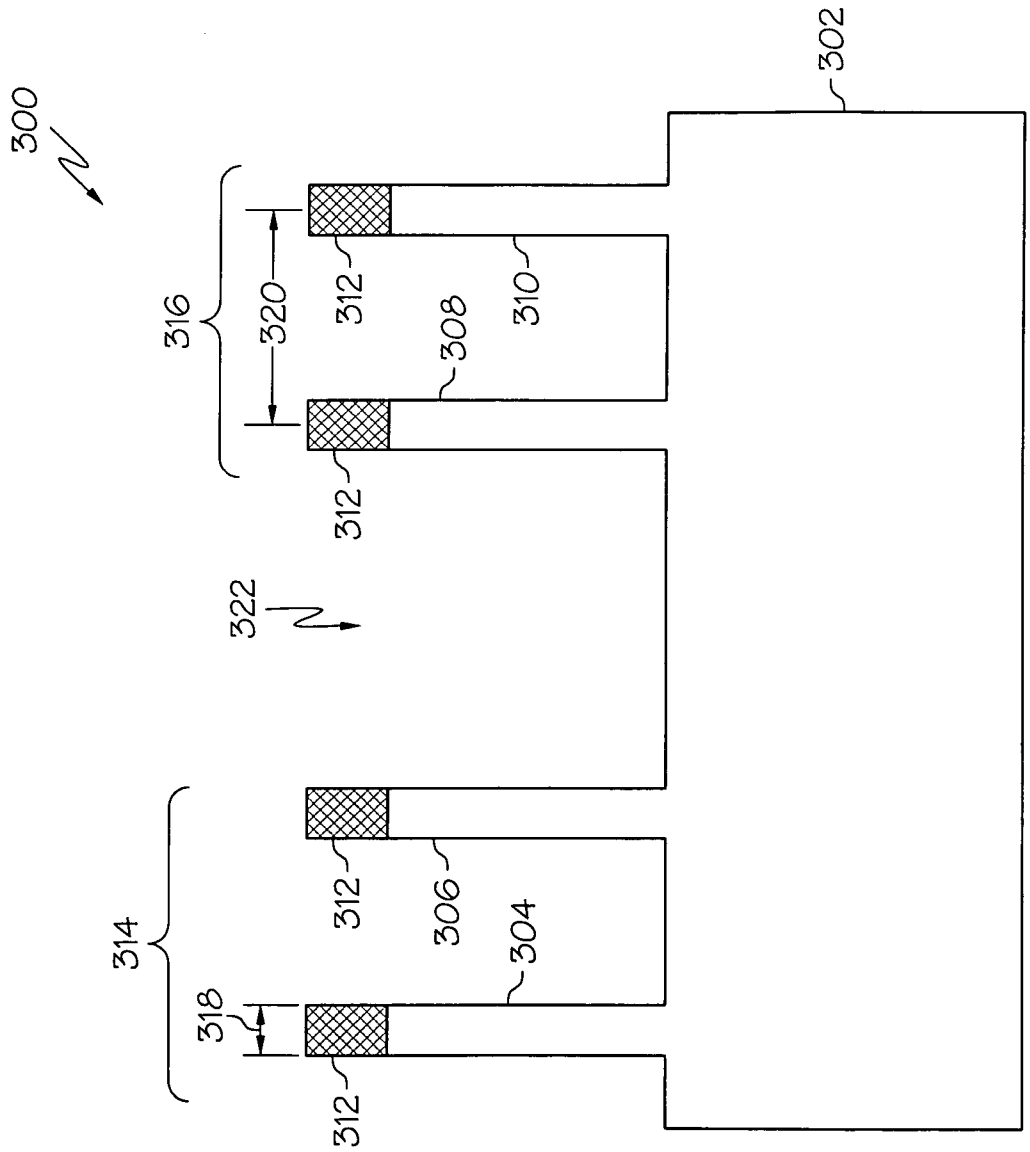
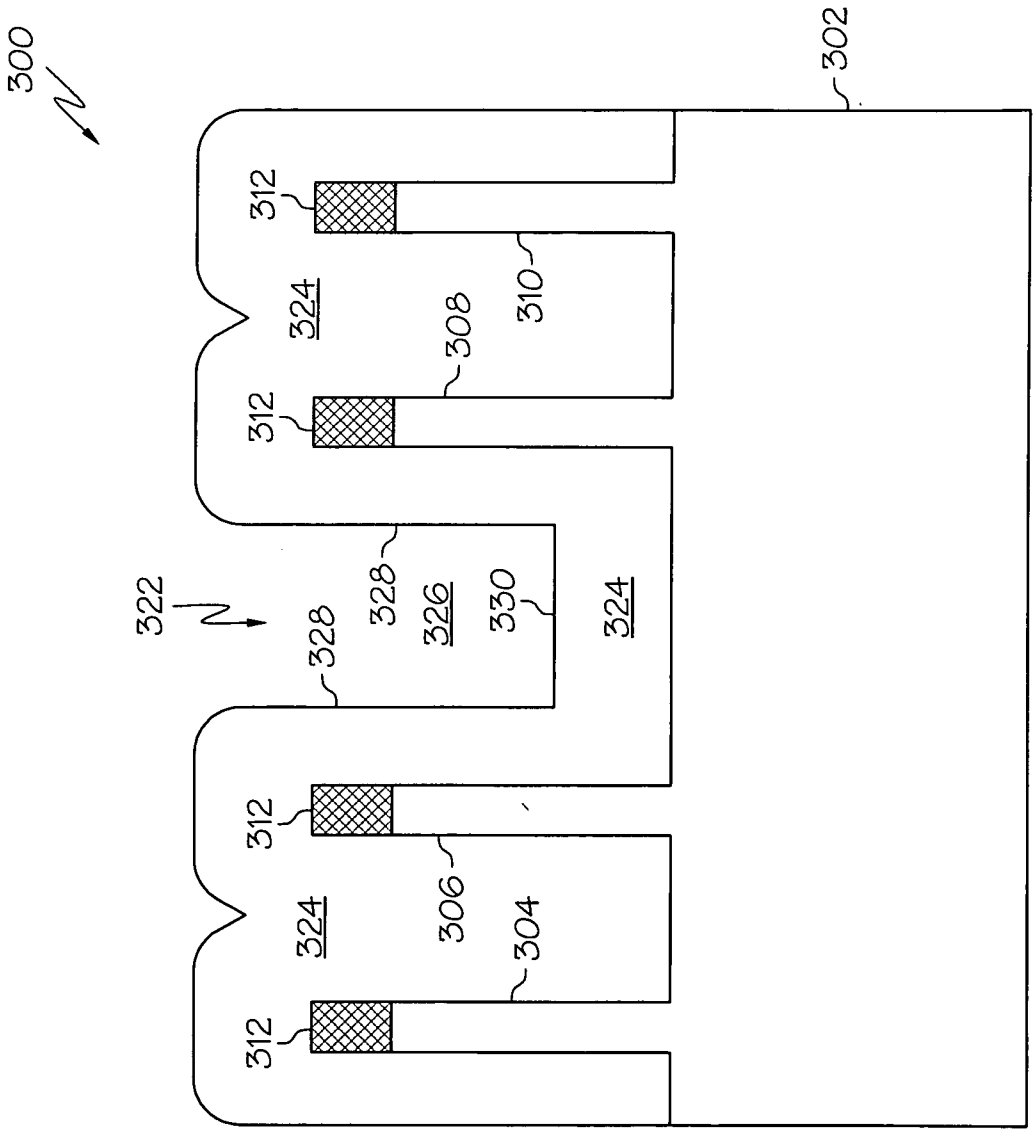


FIG. 3


300
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324
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306
324
304
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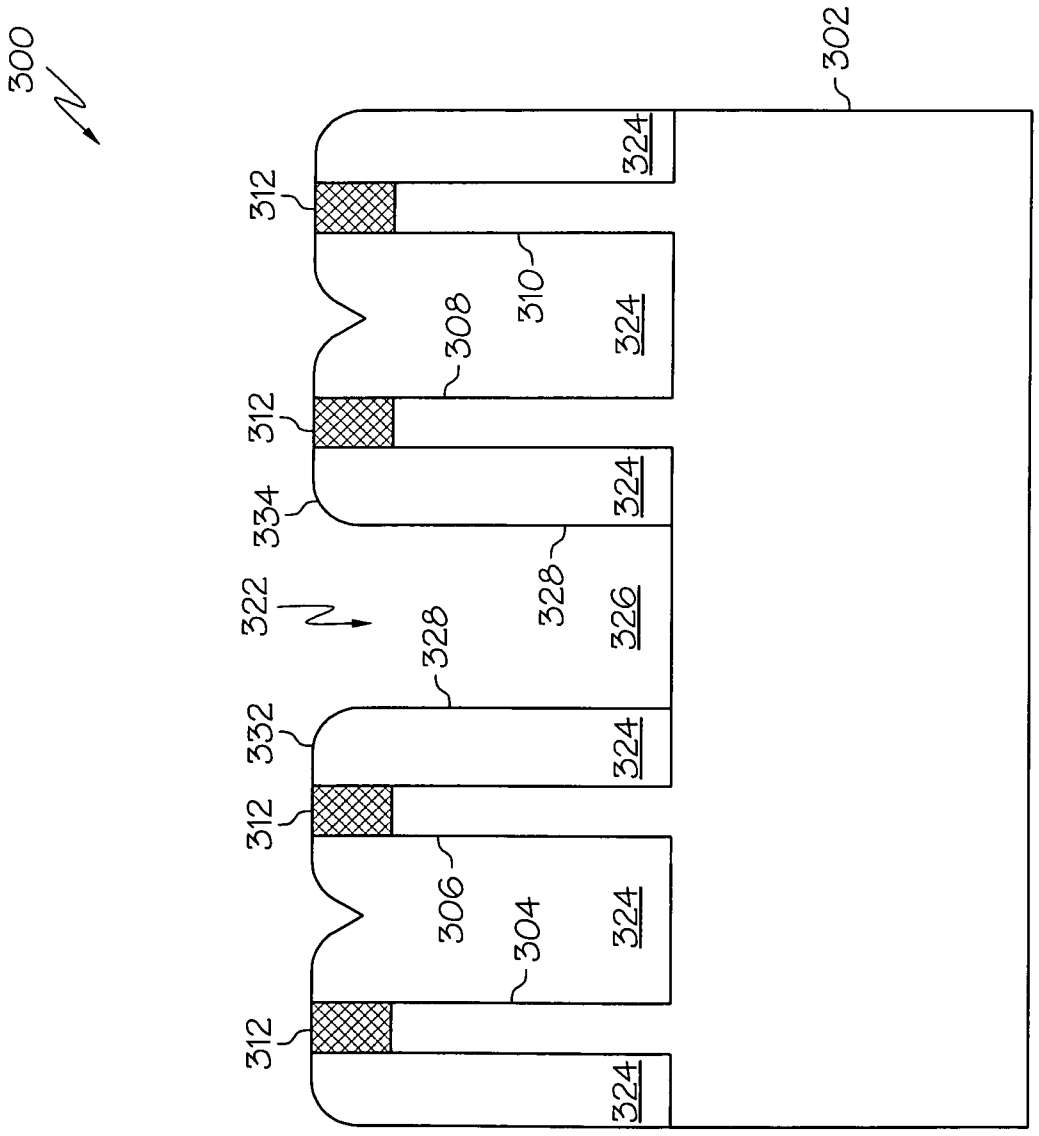
FIG. 4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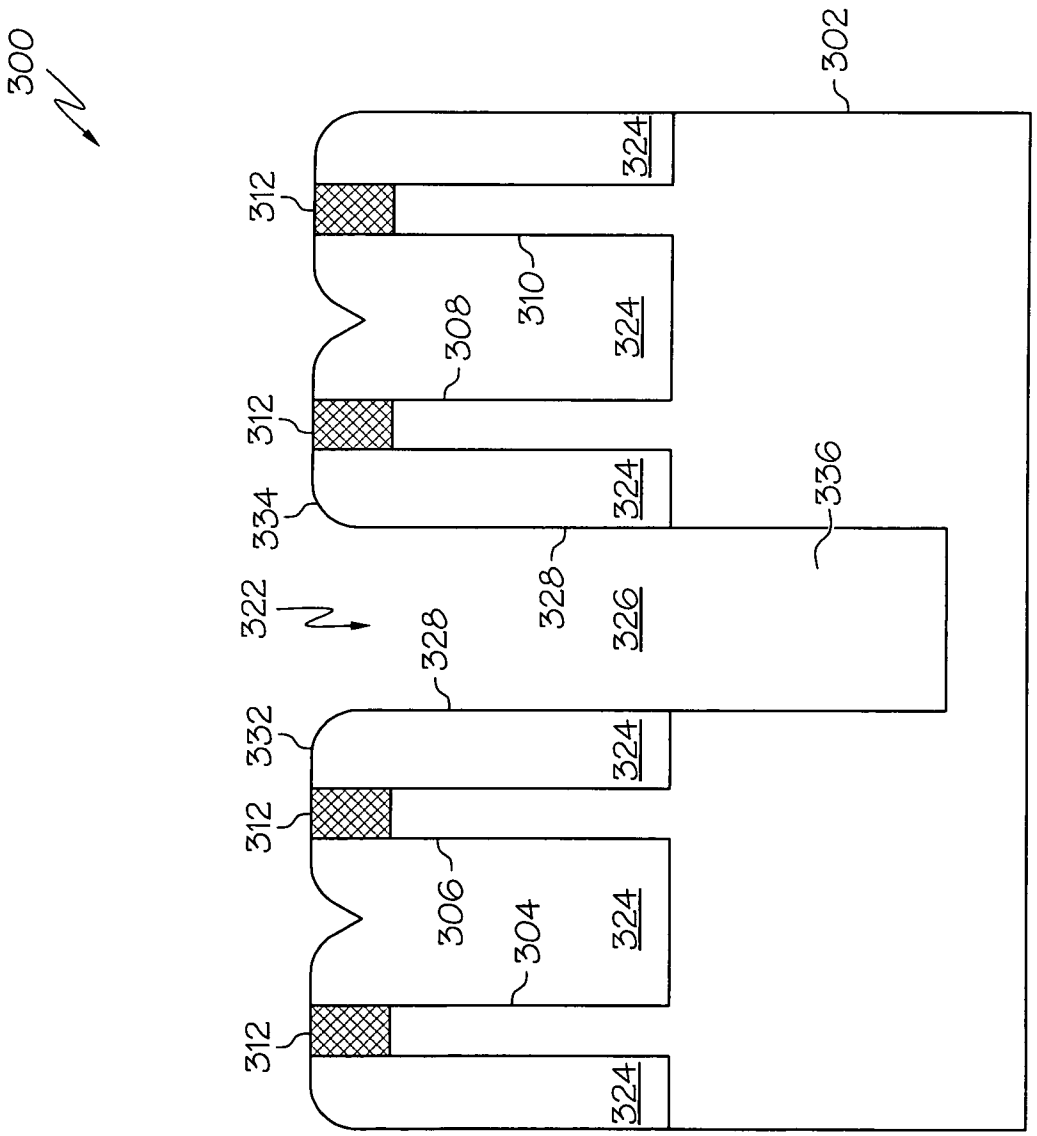
324

FIG. 5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324

FIG. 6

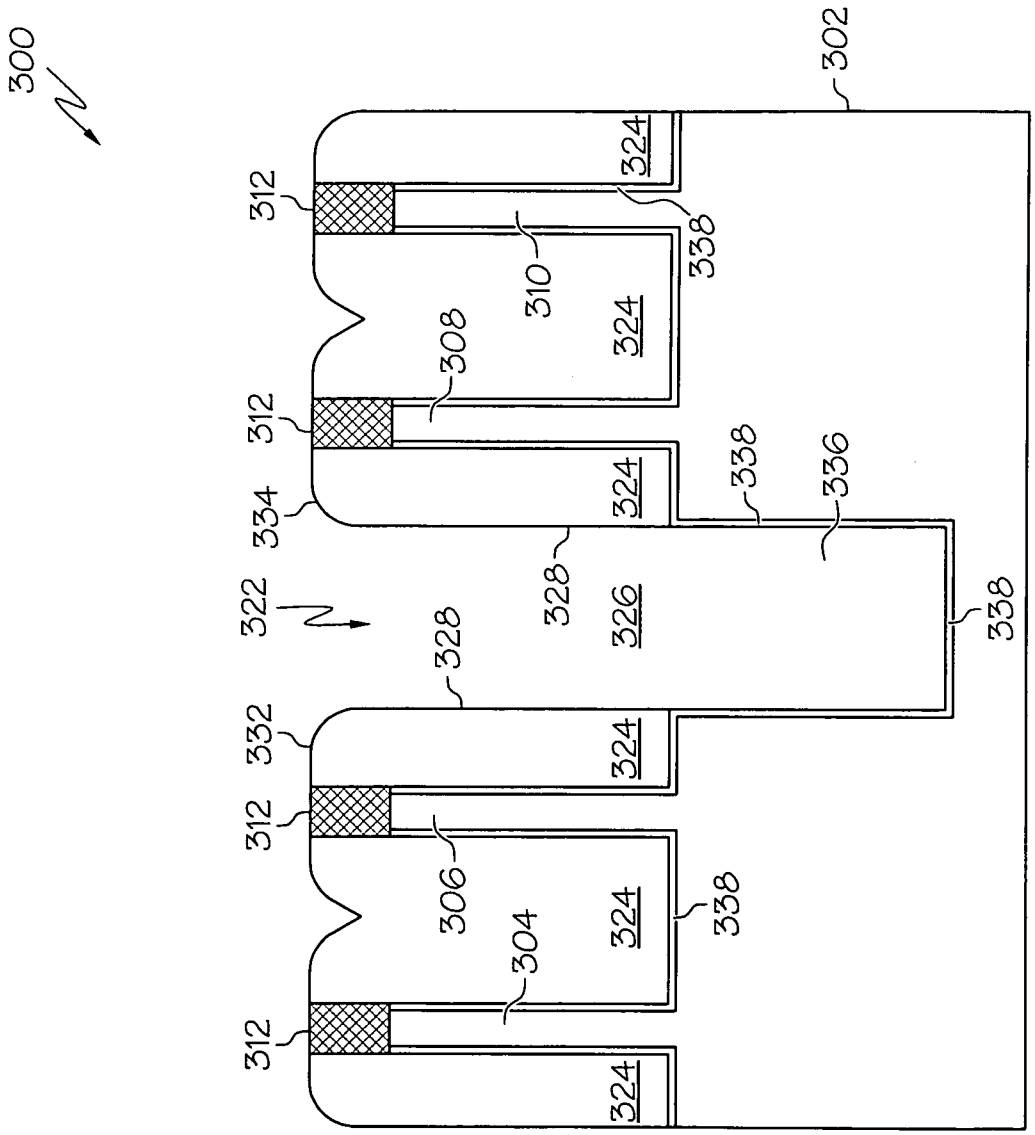


FIG. 7

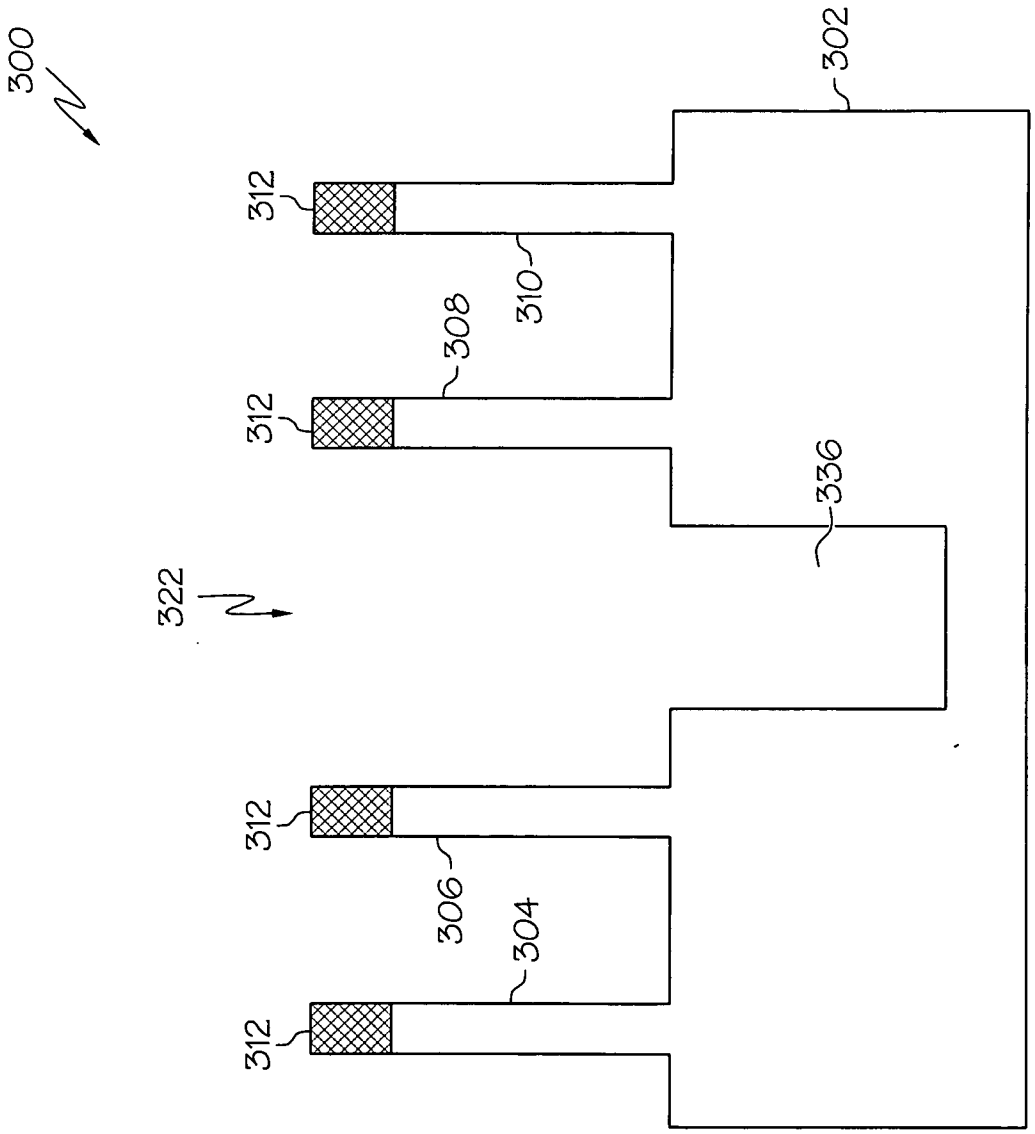


FIG. 8

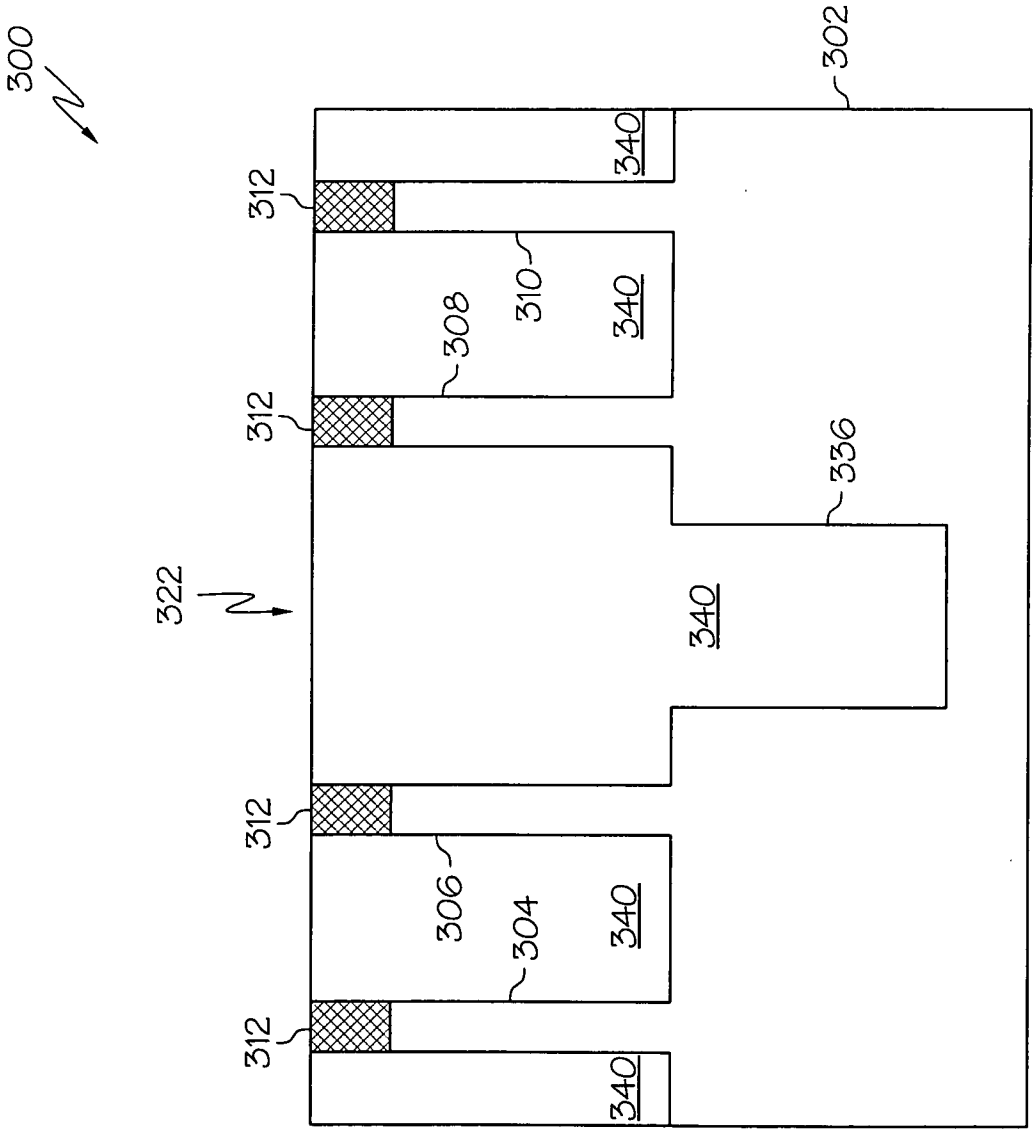
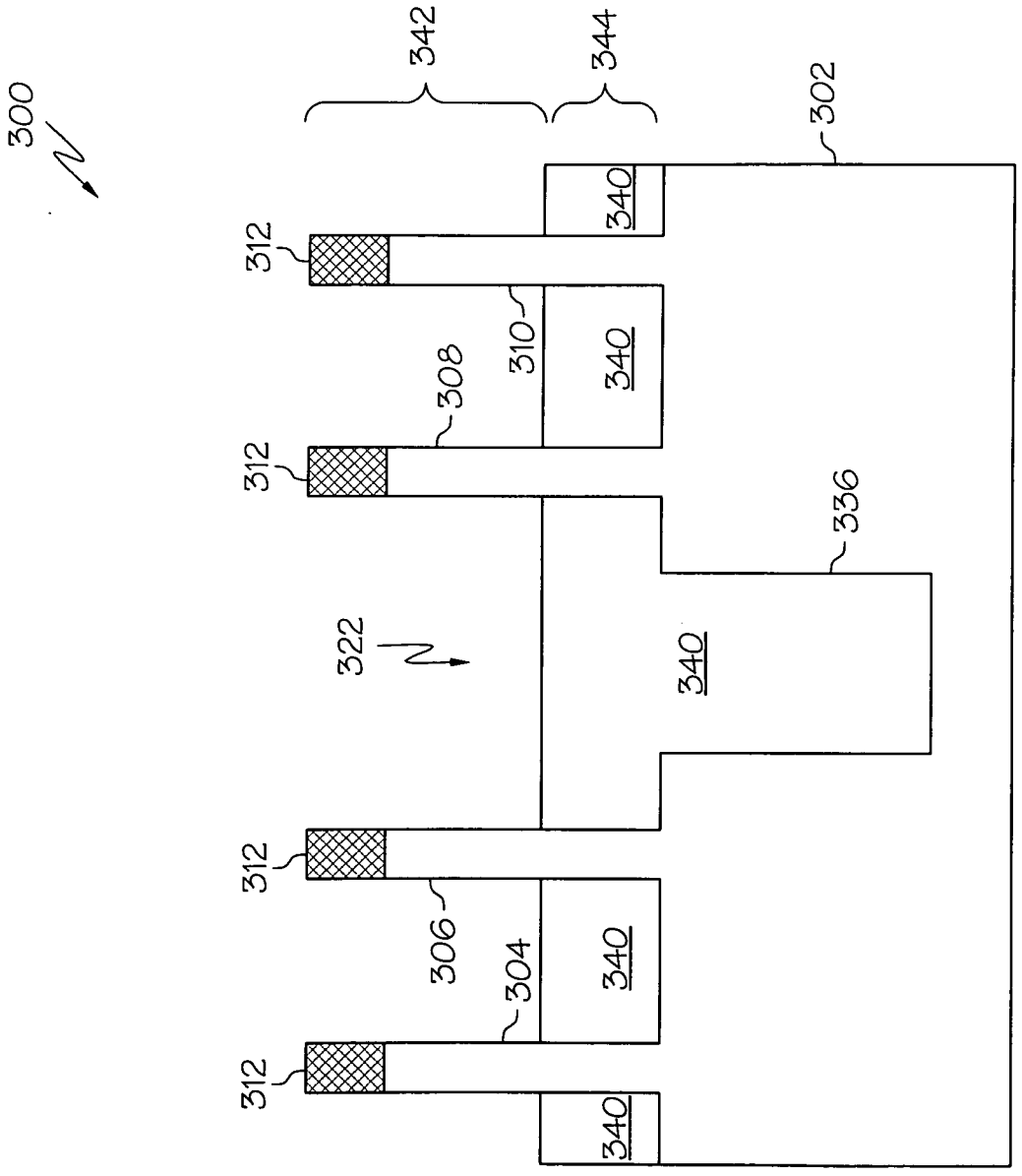


FIG. 9


300
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344
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340
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310
308
340
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336
322
340
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306
304
340
312
340

FIG. 10

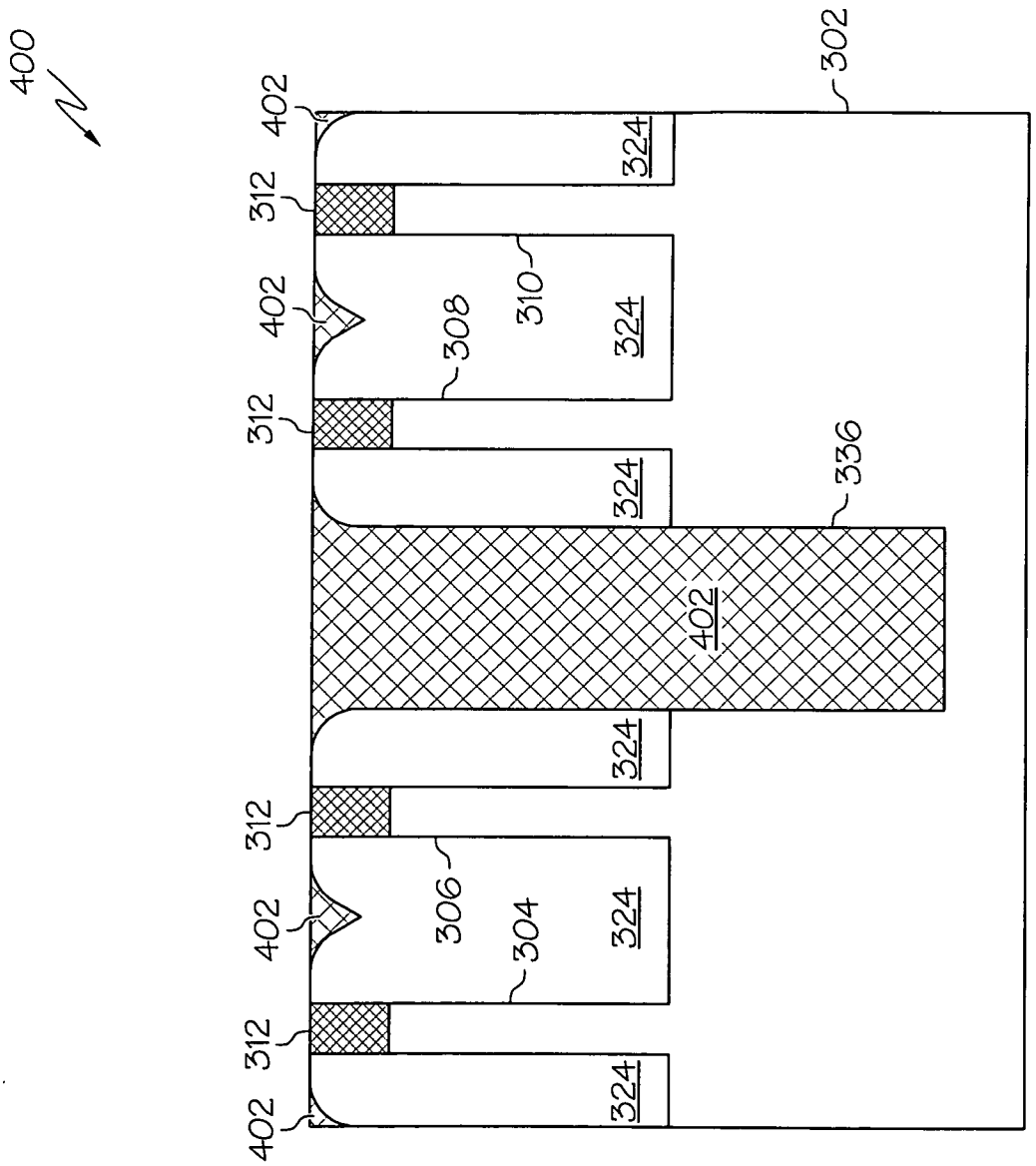

FIG. 11

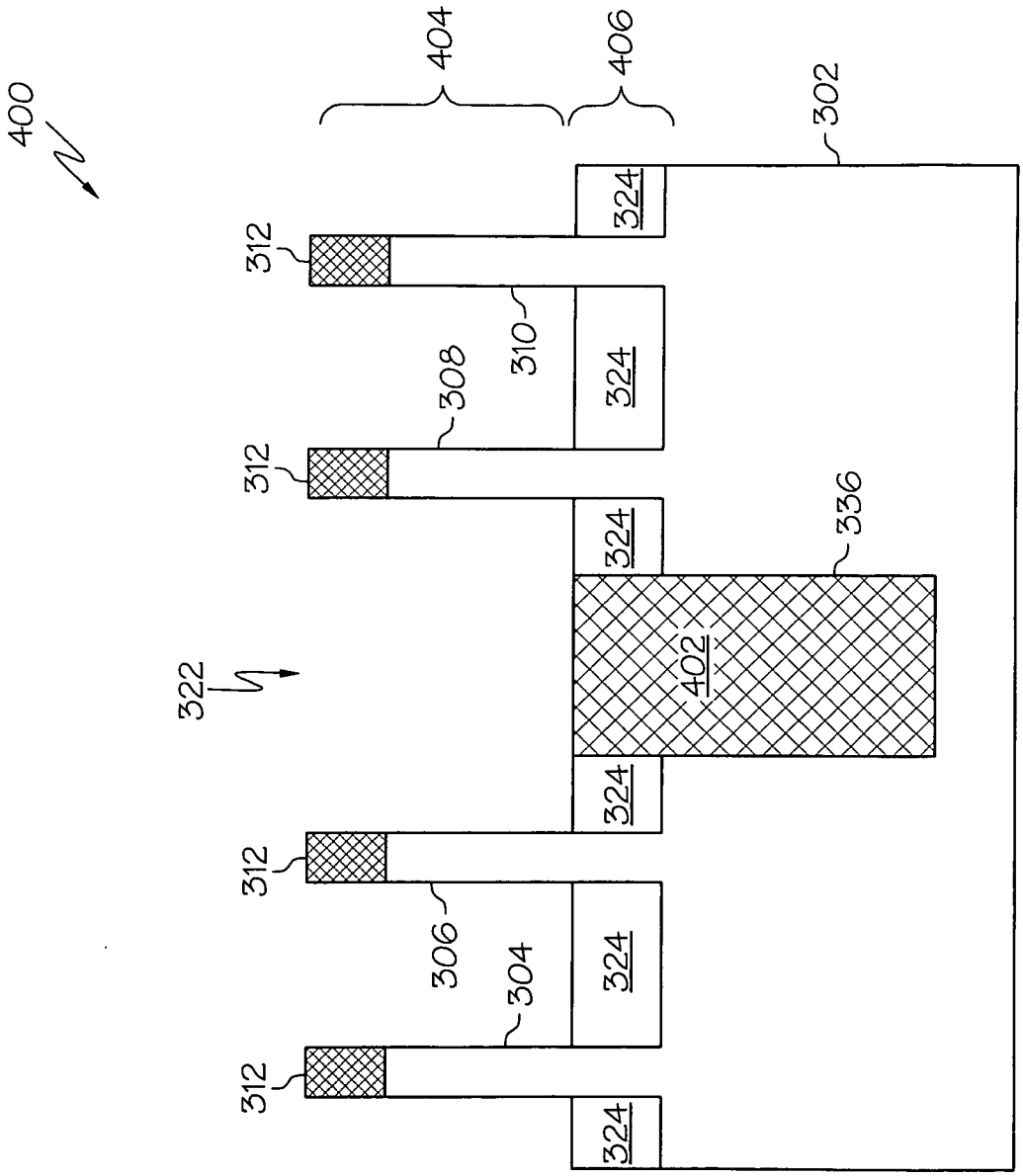

FIG. 12

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/004211

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/336 H01L29/78

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2006/134868 A1 (YOON JAE-MAN [KR] ET AL) 22 June 2006 (2006-06-22) paragraph [0035] - paragraph [0045]; figures 9-18	1-20
X	US 2008/121970 A1 (ARITOME SEIICHI [US]) 29 May 2008 (2008-05-29) paragraph [0033] - paragraph [0037]; figures 4A-E paragraph [0046] - paragraph [0047]; figures 6A,B	1-18
X	US 2006/141706 A1 (HONG SEUNG-WAN [KR]) 29 June 2006 (2006-06-29) paragraph [0106] - paragraph [0111]; figures 8A-8E	1-18

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
3 November 2009	09/11/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Hoffmann, Niels

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/004211

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2008/029821 A1 (YAMAGAMI SHIGEHARU [JP] ET AL) 7 February 2008 (2008-02-07) paragraph [0240] - paragraph [0255]; figures 32-42	1-18
A	WO 2006/090445 A (FUJITSU LTD [JP]; FUKUTOME HIDENOBU [JP]) 31 August 2006 (2006-08-31) abstract; figures 7G-80	1-18
A	US 6 872 647 B1 (YU BIN [US] ET AL) 29 March 2005 (2005-03-29) cited in the application the whole document	1-18
A	US 6 921 963 B2 (KRIVOKAPIC ZORAN [US] ET AL) 26 July 2005 (2005-07-26) cited in the application the whole document	1-18

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2009/004211

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