(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
17 July 2014 (17.07.2014)

WIPO | PCT

(10) International Publication Number
WO 2014/110178 A1

(51) International Patent Classification:
H01L 21/66 (2006.01) *H01L 21/20* (2006.01)

(21) International Application Number:
PCT/US2014/010743

(22) International Filing Date:
8 January 2014 (08.01.2014)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
13/737,677 9 January 2013 (09.01.2013) US

(71) Applicant: **KLA-TENCOR CORPORATION** (legal representative of the deceased inventor) [US/US]; Legal Department, One Technology Drive, Milpitas, California 95035 (US).

(72) Inventors: **CHU, Xing**; 2225 Valorie Street, Fremont, California 94539 (US). **LAUBER, Jan**; 208 Galewood Circle, San Francisco, California 94131 (US).

(72) Inventor: **RUNYON, Rex** *(deceased)*.

(74) Agent: **MCANDREWS, Kevin**; KLA-Tencor Corp., Legal Department, One Technology Drive, Milpitas, California 95035 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

(54) **Title**: DETECTING DEFECTS ON A WAFER USING TEMPLATE IMAGE MATCHING

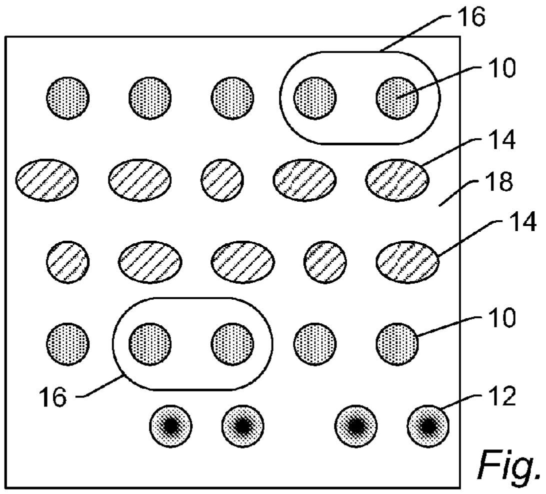

Fig. 1

(57) **Abstract**: Various embodiments for detecting defects on a wafer are provided. Some embodiments include matching a template image, in which at least some pixels are associated with regions in the device having different characteristics, to output of an electron beam inspection system and applying defect detection parameters to pixels in the output based on the regions that the pixels in the output are located within to thereby detect defects on the wafer.

WO 2014/110178 A1

TITLE: DETECTING DEFECTS ON A WAFER USING TEMPLATE IMAGE MATCHING

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to detecting defects on a wafer using template image matching.

2. Description of the Related Art

The following description and examples are not admitted to be prior art by virtue of their inclusion in this section.

Inspection processes are used at various steps during a semiconductor manufacturing process to detect defects on wafers to promote higher yield in the manufacturing process and thus higher profits. Inspection has always been an important part of fabricating semiconductor devices. However, as the dimensions of semiconductor devices decrease, inspection becomes even more important to the successful manufacture of acceptable semiconductor devices because smaller defects can cause the devices to fail.

Inspection generally involves applying some defect detection parameters to output generated by scanning and/or imaging a wafer. The defect detection parameters may include a threshold that is applied to the output or to a difference between the output and some reference output. Different detection thresholds can be set depending on varying characteristics of the output such as brightness and/or noise due to roughness of different regions of a device, but typically not depending on the locations of the regions within the inspected area. There is no easy way to treat different regions in the output separately according to the device context resolved in the output.

Information beyond simple defect detection is often generated during inspection processes. For example, the detected defects are often classified into different groups. In one such example, after finding defects, they may be classified into different groups based on the defect characteristics such as size, magnitude, and location. Defects can also be classified based on the information contained within a patch image, a relatively small subsection of the full image. Sometimes, the context in which a defect was found cannot be determined from a patch image alone, requiring a larger section of the image surrounding the defect.

Accordingly, it would be advantageous to develop methods and systems for detecting defects on a wafer that do not have one or more of the disadvantages described above.

SUMMARY OF THE INVENTION

The following description of various embodiments is not to be construed in any way as limiting the subject matter of the appended claims.

One embodiment relates to a computer-implemented method for detecting defects on a wafer. The method includes generating a template image using information about a device being formed on the wafer. At least some pixels in the template image are associated with regions in the device having different characteristics. The method also includes acquiring output of an electron beam inspection system for the wafer and matching the template image to the output based on patterns in the template image and the output. In addition, the method includes identifying the regions that pixels in the output are located within based on the regions that are associated with the pixels of the template image that match the pixels in the output. The method further includes applying defect detection parameters to the pixels in the output based on the regions that the pixels are located within to thereby detect defects on the wafer. The steps described above are performed by a computer system.

Each of the steps of the method described above may be further performed as described herein. In addition, the method described above may include any other step(s) of any other method(s) described herein. Furthermore, the method described above may be performed by any of the systems described herein.

Another embodiment relates to a non-transitory computer-readable medium containing program instructions stored therein for causing a computer system to perform a computer-implemented method for detecting defects on a wafer. The computer-implemented method includes the steps of the method described above. The computer-readable medium may be further configured as described herein. The steps of the method may be performed as described further herein. In addition, the method may include any other step(s) of any other method(s) described herein.

An additional embodiment relates to a system configured to detect defects on a wafer. The system includes an electron beam inspection subsystem configured to acquire output for a wafer. The system also includes a computer subsystem configured to generate a template image using information about a device being formed on the wafer. At least some pixels in the template image are associated with regions in the device having different characteristics. The computer subsystem is also configured to match the template image to the output based on patterns in the template image and the output and to identify the regions that pixels in the output are located within based on the regions that are associated with the pixels of the template image that match the pixels in the output. The computer subsystem is further configured to apply defect detection parameters to the pixels in the output based on the regions that the pixels are located within to thereby detect defects on the wafer. The system may be further configured according to any embodiment(s) described herein.

BRIEF DESCRIPTION OF THE DRAWINGS

Further advantages of the present invention will become apparent to those skilled in the art with the benefit of the following detailed description of the preferred embodiments and upon reference to the accompanying drawings in which:

Fig. 1 is a schematic diagram illustrating a plan view of one embodiment of a template image that may be generated according to embodiments described herein;

Fig. 2 is a schematic diagram illustrating one embodiment of matching a template image to output generated by an electron beam inspection system;

Fig. 3 is a block diagram illustrating one embodiment of a non-transitory computer-readable medium; and

Fig. 4 is a block diagram illustrating one embodiment of a system configured to detect defects on a wafer.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and are herein described in detail. The drawings may not be to scale. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Turning now to the drawings, it is noted that the figures are not drawn to scale. In particular, the scale of some of the elements of the figures is greatly exaggerated to emphasize characteristics of the elements. It is also noted that the figures are not drawn to the same scale. Elements shown in more than one figure that may be similarly configured have been indicated using the same reference numerals.

One embodiment relates to a computer-implemented method for detecting defects on a wafer. The method includes generating a template image using information about a device being formed on a wafer. At least some pixels in the template image are associated with regions in the device having different characteristics. The method, therefore, partitions a semiconductor device to be inspected into different regions of interest (ROIs) according to the device context. The device context (or a section of it) may then be rendered into a template image appropriate for inspection.

The different characteristics of the regions in the device may include different electrical characteristics that the regions will have in the final manufactured device. For example, as described further herein, different contacts within an array area of a device may have different electrical functions in the completed device and therefore may have different electrical characteristics. Each of the contacts having the same electrical functions may be grouped into one region while the electrical functions of contacts in different regions may be different. Other disparate device elements may be similarly grouped. For example, each contact, regardless of its region, may be in a region different than the dielectric material that electrically insulates the contacts from each other.

In one embodiment, the information includes design data for the device. For example, device context can be obtained in the form of a device layout design database (e.g., GDSII files) and may include any design information known in the art. In another embodiment, the information includes a high resolution image of the device being formed on the wafer. For example, device context information can be obtained in the form of relatively high resolution images of the device to be inspected. A “high resolution image,” as used herein, generally refers to any image in which the patterns on the wafer are resolved, and are preferably relatively well resolved, such that information about patterns in the device formed on the wafer can be determined from the image with relatively high accuracy. High resolution images of patterns of a device formed on a wafer can be acquired using, for example, an electron beam inspection system. In this manner, the context can be derived empirically from a relatively good quality image.

In one embodiment, the method includes determining the regions that the pixels in the template image are associated with prior to acquiring the output as described further herein. For example, the method may partition the semiconductor device into different ROIs prior to the inspection of the wafer. The template image with the information for the different regions may then be stored into some file or data structure that can be accessed by the inspection system that will be performing the inspection of the wafer. In addition, the template image and the associated information may be used for the inspection of more than one wafer.

In another embodiment, the method includes determining the regions that the pixels in the template image are associated with based on properties of the device, defects of interest (DOI), known nuisance defects, or some combination thereof. For example, segmentation schemes can be formed to partition the device context into multiple regions based on the device physics, DOI at the moment, and/or the presence of dominating nuisances. In many cases, the locations of DOI within a cell or a device are known as is the location of noise and/or nuisance. Such information can be used to separate the regions in the template image into those that correspond to DOI and those that do not. The device context-based segmentation scheme can be formulated with the assistance of design-based hot spot analysis software. In addition, from an abstracted unit cell context, the user can mark out the areas of interest, and these may be the only areas to be inspected for defects during the inspection. However, the determination of the regions may be completely automated.

In one embodiment, at least one of the regions corresponds to only a single contact within a repeating memory cell structure of the device. For example, regions can be as small as individual contacts within a repeating memory cell structure. In addition, one or more of the regions may be as small a contact or as any other feature or structure in the device while other regions may include more than one feature, a layer, etc.

In another embodiment, at least some of the regions correspond to different types of contacts within a repeating memory cell structure of the device. For example, Fig. 1 shows one embodiment of a template image that can be used for an inspection of a memory cell structure. As described further herein, the device context for a unit cell can be identified from a design database or from a high resolution image. The segmentation scheme shown in Fig. 1 may partition the structures in this portion of the device into the background dielectric, different groups of contacts, and particular locations within the context to be different regions. For example, as shown in Fig. 1, one group of contacts having one type may be identified as first regions 10 that are ROI or DOI areas. Another group of contacts having a second type different than the first group may be identified as second regions 12 that are also ROI or DOI areas. An additional group of contacts having a third type different than the first and second groups may be identified as third regions 14 that are not ROI. For example, this group of contacts may be contacts in or near which no DOIs are located. Fourth regions 16 may be identified as locations near some of the contacts that are of interest as perhaps containing DOI. The dielectric background may be identified as fifth region 18 that is not a region of interest. The device context may then be rendered into a template image appropriate for matching with images from the upcoming inspection, which can be performed as described further herein.

In some embodiments, at least one of the regions corresponds to an oxide area between contacts in a repeating memory cell structure of the device, and applying defect detection parameters as described further herein is not performed for the oxide area. For example, some regions can be excluded from the inspection such as the oxide area between contacts. In the example shown in Fig. 1, fifth region 18 that includes the dielectric background between contacts in a repeating memory cell structure may be indicated as a non-ROI and defect detection may not be performed for pixels located in that region.

As described herein, the regions may be defined based on electrical characteristics of features in the device, known DOI, and known nuisances. Therefore, regions that may produce output in the inspection system having similar characteristics (e.g., noise, signal, signal-to-noise ratio, brightness, contrast, and any other image, signal, or data characteristics) may be separated into different regions. In other words, unlike other methods that may separate pixels based on image characteristics, the embodiments described herein may separate at least some of the inspection area into regions without regard to how the regions affect the inspection system output.

In an additional embodiment, the method includes generating multiple template images using the information about the device, and each of the multiple template images is generated for one of multiple pixel sizes and optical conditions for the electron beam inspection system described further herein. For example, the template image (i.e., the abstracted unit cell context) may be rendered to the pixel size of the inspection system (i.e., the correct pixel size). In addition, a relatively high resolution template unit cell can be rendered to be used in multiple pixel sizes and/or optics conditions. In this manner, the template image may be rendered to simulate how the portion of the device corresponding to the template image will appear to the inspection system thereby increasing the ability of the method to correctly match the template image to the output of the inspection system. In addition, when there are more than one template image, each of which corresponds to different pixel sizes and/or other optical conditions of the inspection system, the correct template image may be selected at the beginning of the inspection based on the parameters of the inspection system in the inspection recipe that will be used for inspection of the wafer.

The method also includes acquiring output of an electron beam inspection system for the wafer. Acquiring the output may include actually performing an inspection of the wafer (e.g., by scanning the wafer using the electron beam inspection system). However, acquiring the output may not include performing an inspection on the wafer. For example, acquiring the output may include acquiring the output from a storage medium in which the output has been stored by another method or the electron beam inspection system. The inspection may include any suitable inspection including any of those described further herein. The output may include any and all output that may be generated by an inspection process or system.

The method further includes matching the template image to the output based on patterns in the template image and the output. For example, during the inspection process, the device context template image is matched to the acquired output (e.g., an inspection image or images) to determine the location of the context (e.g., each unit cell context) within the inspection image. In particular, pattern matching may be used to locate the unit cell or portion of the device corresponding to the template image within the array region or another region of the device. In one such embodiment, as shown in Fig. 2, template image 20 may be moved to various positions 22 and 24 within inspection image 26 until a match is found. For example, template image 20 may be overlaid with the inspection image at position 22 and since a match of the patterns in the template image and that portion of the inspection image is not found, the template image may be overlaid with the inspection image at the other position, position 24, where a match between the patterns is found.

As shown in Fig. 2, the template image may be smaller than the inspection image such that the inspection image contains enough pixels such that a match between the template image and the inspection image can be found. In addition, as shown in Fig. 2, multiple portions of the inspection image may match the template image. As such, multiple matches between different portions of the inspection image and the template image may be searched for and found or one instance of a match between the inspection image and the template image may be found and then the matching may be propagated through the inspection image as described further herein.

As further shown in Fig. 2, the template image may include information about the different regions within the template image (i.e., the different regions that various contacts are assigned to). However, the template image and the information about the different regions may be stored in different data structures (e.g., if the information about the different regions will make the matching step more difficult).

A match between the template image and the output of the electron beam inspection system may be declared in situations in which a “perfect” match cannot be found. For example, “matching” may include searching for “perfect matches” and also matches within some range of uncertainty or error. In this manner, the matching may be performed while taking into account the fact that the output of the electron beam inspection system may vary due to variations in the wafer itself, which may be caused by, for example, variations in the parameters of the process used to form the patterns on the wafer.

In one embodiment, the template image corresponds to a unit cell within an array region of the device, and matching the template image to the output includes matching the template image to the pixels in the output corresponding to one unit cell in the array region based on the patterns and propagating the matching throughout the array region based on information about the unit cell and the array region. For example, the unit cell may be propagated throughout the array region utilizing the array cell size and a small search range. In other words, if the template image corresponds to one unit cell, since the array region is made up of multiple unit cells, once a match between the template image and some portion of the output has been found, the template image will be matched to one unit cell in the output. Information about the dimensions and arrangement of the unit cells in the array region may then be used to identify other unit cells in the output without performing the matching. Propagating the matching in this manner may be advantageous because it may speed up the inspection process overall and, in instances in which the wafer properties vary across unit cells in the same array region, propagating the matching in this manner can increase the accuracy in which the locations of the unit cells in the output can be identified.

In another embodiment, the template image corresponds to a unit cell within an array region of the device, and matching the template image to the output is performed for an entire row and column of unit cells within a care area in the array region. For example, in “smart” array inspection, pattern matching of the template image to the inspection pixels may be performed for a complete row and column of cells within the array care area. The array care area may be determined in any suitable manner by the embodiments described herein or another method or system.

In some embodiments, the template image corresponds to a unit cell within an array region of the device, and the matching is performed for every unit cell within the array region. For example, for array real time alignment (RTA), pattern matching may be performed for every unit cell inside the array region. In addition, the alignment can be performed in both the x and y directions, similar to multi-segmented alignment (MS).

The method also includes identifying the regions that pixels in the output are located within based on the regions that are associated with the pixels in the template image that match the pixels in the output. In this manner, during the inspection, the locations of the different regions are identified according to the details of the device context resolved in the image. Each pixel in the image can then be allocated to one of the predetermined regions. In this manner, rendering and matching of the device context is performed for the purpose of identifying the location of the context within the inspection image. In addition, the device context-based segmentation of the inspection image can be performed prior to defect detection. As such, the embodiments described herein can be used to “bin” pixels in the inspection image before inspection is performed using those pixels.

In one embodiment, identifying the regions includes overlaying a region segmentation scheme onto the pixels in the output that match the template image. For example, once the location of the context within the inspection image is obtained, the region segmentation scheme may be overlaid on the inspection image to partition all pixels in the inspection image into different regions. In addition, once the location of each unit cell context is obtained, the region segmentation scheme may be applied in any other manner and all pixels in the inspection image may be partitioned into appropriate regions.

The method also includes applying defect detection parameters to the pixels in the output based on the regions that the pixels are located within to thereby detect defects on the wafer. In this manner, the embodiments described herein are configured for context sensitive electron beam wafer inspection. For example, pixels in the different regions can be processed separately using different defect detection methods that are appropriate for each individual region. In one such example, pixels in each region can be processed with different detection methods or ignored altogether if desired. For example, there could be multiple groups of areas of interest, and each group could have its own threshold, defect detection method, or defect detection parameters. In another example, during inspection of the context regions, since the exact location of each feature within a cell is known due to the matching described herein, each of the regions may be histogrammed and inspected separately with their individual threshold method and parameters. In addition, some areas can be marked as background and will not be inspected.

In this manner, context sensitive inspection (CSI) may utilize the design knowledge of a unit cell within an array region or of any other region within a device to perform targeted inspections of specific ROIs at sensitive locations where the DOI are expected to occur. In addition, the embodiments described herein can be used to determine the location of each unit cell within a swath image and the location of the ROIs within the cell such that only the part of the cell that is of potential interest needs to be inspected while leaving out uninteresting background areas. In this manner, only the pixels within the user-defined areas of interest can be inspected for defects. Therefore, nuisances outside these areas do not decrease the signal-to-noise ratio for DOI and do not need binning to filter out. As such, the embodiments described herein provide a sensible way for a user to perform targeted inspection based on the design knowledge of the device context. In addition, segmentation of the inspection image gives the user the flexibility to customize the inspection for each region thereby making possible new ways to suppress nuisance defects and improve inspection sensitivity for DOIs. Furthermore, optics selection could utilize the reduction in nuisance detection due to the methods described herein to increase the signal-to-noise ratio for DOI only, with no need to suppress irrelevant nuisances. In one such example, the embodiments described herein can be used with optics selector, which may be configured and/or performed as described in U.S. Patent No. 8,073,240 issued on December 6, 2011 to Fischer et al., which is incorporated by reference as if fully set forth herein, and even image optimization, where the gain of the inspection system is adjusted to maximize contrast of the ROI.

In one embodiment, the defect detection parameters include whether or not to perform defect detection in one or more of the regions and, for the regions in which the defect detection is to be performed, a threshold that depends on the regions in which the pixels are located, and the threshold is to be applied to a difference between the pixels in the output and reference pixels. For example, after the region segmentation scheme has been applied to pixels in the inspection image, defect detection can be performed on the predetermined DOI regions (each with its own detection threshold) only, while ignoring all information from the background dielectric and non-DOI regions. The detection threshold of each region can be set individually. In one such example, knowing the layout of a cell, each contact could be assigned its own region with its own threshold. Regions where a relatively small DOI is expected can be inspected with relatively high sensitivity while other regions that may contain lots of leakage nuisance defects can be detuned. In addition, regions that contain significant noise can be excluded before they overwhelm a defect detection algorithm. Therefore, thresholds can be significantly lowered in other regions, which could make possible or optimize the detection of DOI.

In one such example, a memory structure that is relatively well-resolved with electron beam inspection system optics can be partitioned into individual contact types such as PMOS/NMOS/Bitline or Wordline contacts, etc. The threshold for each of these contacts can be set individually. For example, if one contact type is prone to leakage-induced gray level variation that is considered a nuisance, its detection threshold can be detuned so as to not overwhelm the inspection result with nuisances. The segmentation of these leakage-proven contacts also prevents the leakage signal from impacting the detection sensitivity of defects from other regions, which can greatly improve the overall inspection sensitivity to the defect types that the customer is interested in.

In another embodiment, applying the defect detection parameters includes averaging multiple pixels in the output corresponding to multiple unit cells in an array region of the device to generate a reference image, subtracting the reference image from a test image in the output that corresponds to one of the multiple unit cells to generate a difference image, and applying the defect detection parameters to the difference image based on the regions that pixels in the difference image are located within. For example, for cell averaging, neighboring cells can be averaged for a relatively low noise reference image, without the restriction of alignment. Cells from above and below can be used in the averaging as well.

In one embodiment, the method includes automatically associating the detected defects with the regions in which they are located. In other words, defects that are detected as described herein can be automatically associated with the region in which they are detected. For example, all defects detected in inspections described herein can be associated with a particular region and relative location within the unit cell context.

The above-described information can then be used for further classification of the defects. For example, in another embodiment, the method includes classifying the detected defects based on the regions in which they are located. In this manner, any defect that is detected during an inspection can be automatically classified by the region it was found in. As such, the information about the region in which the defects are detected can be used for further classification of the defects. In addition, classifying the detected defects may include using the region and location-within-context information for each defect (automatically obtained from the device context-based segmentation) for the purpose of defect classification. In this manner, defects detected during the inspection may be classified according to the device context-based region and/or location thereby giving the user useful information relevant to the design faster.

In some embodiments, each contact type in the device is associated with a different one of the regions, and the method includes displaying density of the detected defects in each contact type. For example, detected defects can be automatically binned by region based on the region in the template image that they are located within. Therefore, wafer maps of each defect type would be trivial to generate. In addition, every contact type can be set as its own ROI. After the inspection, the defect density of each contact type can be displayed in any suitable manner. In one such example, defect density can be displayed for PMOS contact defects, Bitline contact mis-shaped defects, Bitline contact open defects, Wordline contact open defects, and/or NMOS S/D contact open defects.

Generating the template image, acquiring the output, matching the template image to the output, identifying the regions, and applying the defect detection parameters are performed using a computer system, which may be configured as described further herein.

Although some of the steps of the method are described herein with respect to memory cell portions of a device, similar operations can be performed for non-memory cell parts of the wafer if the relevant design database is available.

All of the methods described herein may include storing results of one or more steps of the method embodiments in a non-transitory, computer-readable storage medium. The results may include any of the results described herein and may be stored in any manner known in the art. The storage medium may include any storage medium described herein or any other suitable storage medium known in the art. After the results have been stored, the results can be accessed in the storage medium and used by any of the method or system embodiments described herein, formatted for display to a user, used by another software module, method, or system, etc.

Each of the embodiments of the method described above may include any other step(s) of any other method(s) described herein. In addition, each of the embodiments of the method described above may be performed by any of the systems described herein.

Another embodiment relates to a non-transitory computer-readable medium containing program instructions stored therein for causing a computer system to perform a computer-implemented method for detecting defects on a wafer. One embodiment of such a computer-readable medium is shown in Fig. 3. In particular, computer-readable medium 28 contains program instructions 30 stored therein for causing computer system 32 to perform a computer-implemented method for detecting defects on a wafer.

The computer-implemented method includes the steps of the method described herein. The computer-implemented method may also include any other step(s) of any other method(s) described herein. In addition, the computer-readable medium may be further configured as described herein.

Program instructions 30 implementing methods such as those described herein may be stored on computer-readable medium 28. The computer-readable medium may be a non-transitory computer-readable storage medium such as a magnetic or optical disk, a magnetic tape, or any other suitable non-transitory computer-readable medium known in the art.

The program instructions may be implemented in any of various ways, including procedure-based techniques, component-based techniques, and/or object-oriented techniques, among others. For example, the program instructions may be implemented using ActiveX controls, C++ objects, JavaBeans, Microsoft Foundation Classes (“MFC”), or other technologies or methodologies, as desired.

Computer system 32 may take various forms, including a personal computer system, mainframe computer system, workstation, image computer, parallel processor, or any other device known in the art. In general, the term “computer system” may be broadly defined to encompass any device having one or more processors, which executes instructions from a memory medium.

Fig. 4 illustrates one embodiment of a system configured to detect defects on a wafer. The system includes electron beam inspection subsystem 34 configured to acquire output for a wafer. The electron beam inspection subsystem may include an existing inspection subsystem (e.g., by adding functionality described herein to an existing inspection system) such as any of the inspection tools that are commercially available from KLA-Tencor. For some such systems, the methods described herein may be provided as optional functionality of the system (e.g., in addition to other functionality of the system). Alternatively, the system described herein may be designed “from scratch” to provide a completely new system.

The system also includes computer subsystem 36 configured to generate a template image using information about a device being formed on the wafer, according to any of the embodiments described herein. As described further herein, at least some pixels in the template image are associated with regions in the device having different characteristics. The computer subsystem is also configured to match the template image to the output based on patterns in the template image and the output, which may be performed according to any of the embodiments described further herein. In addition, the computer subsystem is configured to identify the regions that pixels in the output are located within based on the regions that are associated with the pixels of the template image that match the pixels in the output, which may be performed according to any of the embodiments described further herein. The computer subsystem is further configured to apply defect detection parameters to the pixels in the output based on the regions that the pixels are located within to thereby detect defects on the wafer, which may be performed according to any of the embodiments described further herein. The computer subsystem and the system may be further configured to perform any other step(s) of any method(s) described herein.

Further modifications and alternative embodiments of various aspects of the invention will be apparent to those skilled in the art in view of this description. For example, methods and systems for detecting defects on a wafer are provided. Accordingly, this description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the general manner of carrying out the invention. It is to be understood that the forms of the invention shown and described herein are to be taken as the presently preferred embodiments. Elements and materials may be substituted for those illustrated and described herein, parts and processes may be reversed, and certain features of the invention may be utilized independently, all as would be apparent to one skilled in the art after having the benefit of this description of the invention. Changes may be made in the elements described herein without departing from the spirit and scope of the invention as described in the following claims.

WHAT IS CLAIMED IS:

1. A computer-implemented method for detecting defects on a wafer, comprising:

generating a template image using information about a device being formed on a wafer, wherein at least some pixels in the template image are associated with regions in the device having different characteristics;

acquiring output of an electron beam inspection system for the wafer;

matching the template image to the output based on patterns in the template and the output;

identifying the regions that pixels in the output are located within based on the regions that are associated with the pixels of the template image that match the pixels in the output; and

applying defect detection parameters to the pixels in the output based on the regions that the pixels are located within to thereby detect defects on the wafer, wherein said generating, said acquiring, said matching, said identifying, and said applying are performed using a computer system.

2. The method of claim 1, wherein the information comprises design data for the device.

3. The method of claim 1, wherein the information comprises a high resolution image of the device being formed on the wafer.

4. The method of claim 1, further comprising determining the regions that the pixels in the template image are associated with prior to said acquiring.

5. The method of claim 1, further comprising determining the regions that the pixels in the template image are associated with based on properties of the device, defects of interest, known nuisance defects, or some combination thereof.

6. The method of claim 1, wherein at least one of the regions corresponds to only a single contact within a repeating memory cell structure of the device.

7. The method of claim 1, wherein at least some of the regions correspond to different types of contacts within a repeating memory cell structure of the device.

8. The method of claim 1, wherein at least one of the regions corresponds to an oxide area between contacts in a repeating memory cell structure of the device, and wherein said applying is not performed for the oxide area.

9. The method of claim 1, further comprising generating multiple template images using the information about the device, wherein each of the multiple template images is generated for one of multiple pixel sizes and optical conditions for the electron beam inspection system.

10. The method of claim 1, wherein the template image corresponds to a unit cell within an array region of the device, and wherein said matching comprises matching the template image to the pixels in the output corresponding to one unit cell in the array region based on the patterns and propagating the matching throughout the array region based on information about the unit cell and the array region.

11. The method of claim 1, wherein the template image corresponds to a unit cell within an array region of the device, and wherein said matching is performed for an entire row and column of unit cells within a care area in the array region.

12. The method of claim 1, wherein the template image corresponds to a unit cell within an array region of the device, and wherein said matching is performed for every unit cell within the array region.

13. The method of claim 1, wherein said identifying comprises overlaying a region segmentation scheme onto the pixels in the output that match the template image.

14. The method of claim 1, wherein the defect detection parameters comprise whether or not to perform defect detection in one or more of the regions and for the regions in which the defect detection is to be performed, a threshold that depends on the regions in which the pixels are located, and wherein the threshold is to be applied to a difference between the pixels in the output and reference pixels.

15. The method of claim 1, wherein said applying comprises averaging multiple pixels in the output corresponding to multiple unit cells in an array region of the device to generate a reference image, subtracting the reference image from a test image in the output that corresponds to one of the multiple unit cells to generate a difference image, and applying the defect detection parameters to the difference image based on the regions that pixels in the difference image are located within.

16. The method of claim 1, further comprising automatically associating the detected defects with the regions in which they are located.

17. The method of claim 1, further comprising classifying the detected defects based on the regions in which they are located.

18. The method of claim 1, wherein each contact type in the device is associated with a different one of the regions, the method further comprising displaying density of the detected defects in said each contact type.

19. A non-transitory computer-readable medium containing program instructions stored therein for causing a computer system to perform a computer-implemented method for detecting defects on a wafer, wherein the computer-implemented method comprises:

generating a template image using information about a device being formed on a wafer, wherein at least some pixels in the template image are associated with regions in the device having different characteristics;

acquiring output of an electron beam inspection system for the wafer;

matching the template image to the output based on patterns in the template and the output;

identifying the regions that pixels in the output are located within based on the regions that are associated with the pixels of the template image that match the pixels in the output; and

applying defect detection parameters to the pixels in the output based on the regions that the pixels are located within to thereby detect defects on the wafer.

20. A system configured to detect defects on a wafer, comprising:

an electron beam inspection subsystem configured to acquire output for a wafer; and

a computer subsystem configured to:

generate a template image using information about a device being formed on the wafer, wherein at least some pixels in the template image are associated with regions in the device having different characteristics;

match the template image to the output based on patterns in the template and the output;

identify the regions that pixels in the output are located within based on the regions that are associated with the pixels of the template image that match the pixels in the output; and

apply defect detection parameters to the pixels in the output based on the regions that the pixels are located within to thereby detect defects on the wafer.

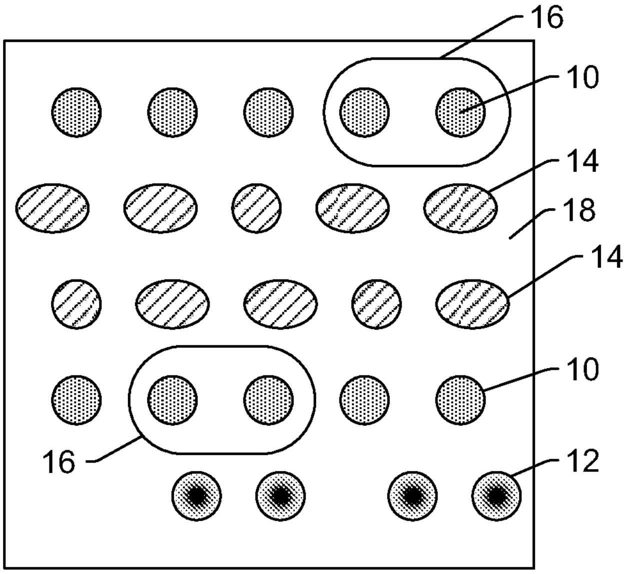

Fig. 1

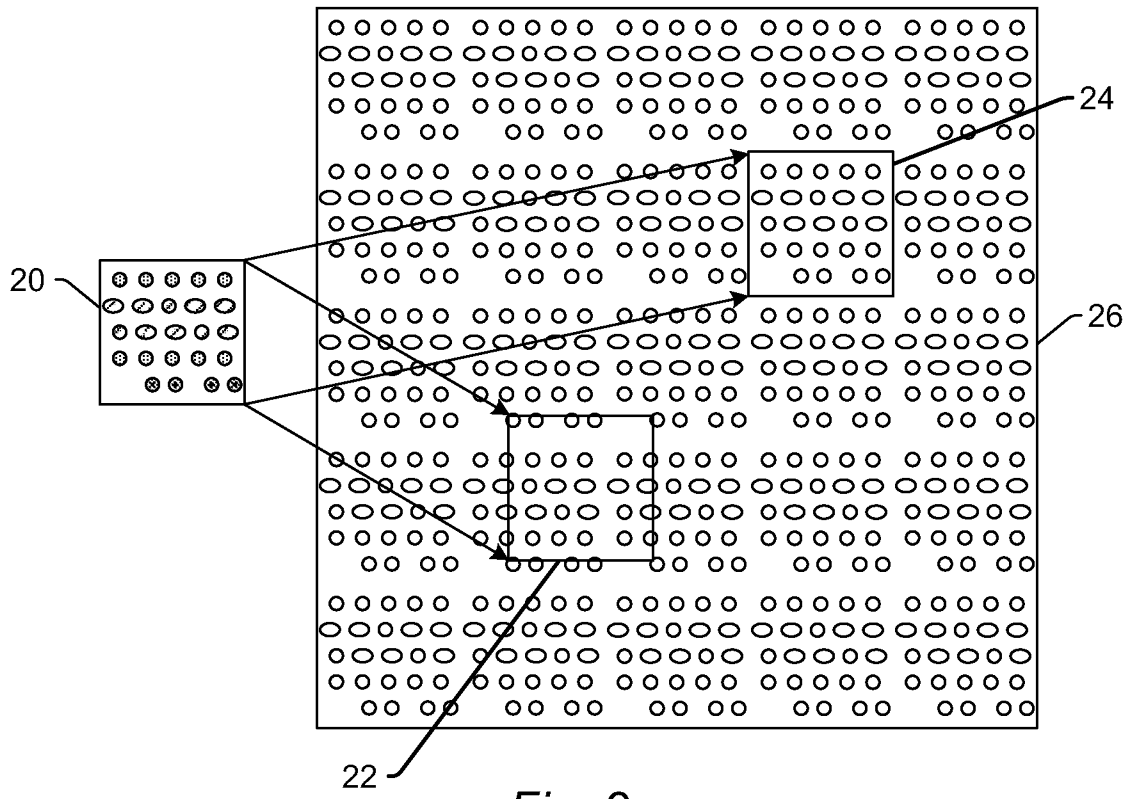

Fig. 2

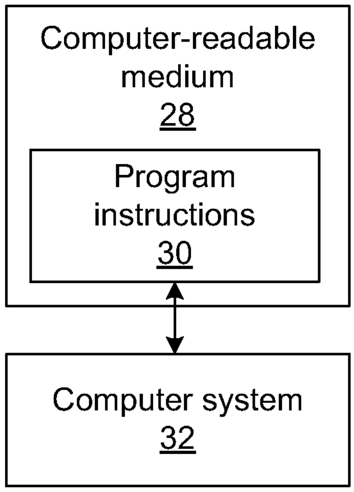
Computer-readable medium 28
Program instructions 30
Computer system 32

Fig. 3

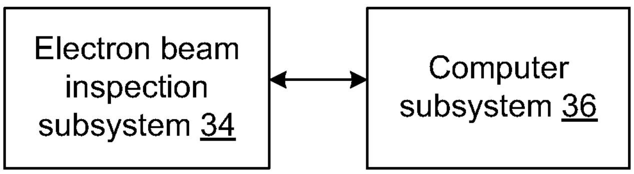
Electron beam inspection subsystem 34
Computer subsystem 36

Fig. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/010743

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/66(2006.01)i, H01L 21/20(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/66; G06F 17/50; G06K 9/68; G21K 7/00; G01N 21/00; G01N 21/95; G06K 9/00; G06F 9/45; H01L 21/20

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: template image, match, output, detecting defect, information, inspection

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 7752584 B2 (HYUN JO YANG) 06 July 2010 See column 2, line 32 - column 3, line 29, claim 1 and figure 1.	1-20
A	US 7170593 B2 (TOSHIFUMI HONDA et al.) 30 January 2007 See abstract, column 3, line 16 - column 6, line 60, claim 1 and figures 1-2D.	1-20
A	WO 2009-018337 A1 (KLA-TENCOR CORPORATION et al.) 05 February 2009 See abstract, pages 22-24 and claim 1.	1-20
A	US 6295374 B1 (DAVID A. ROBINSON et al.) 25 September 2001 See abstract, column 3, line 34 - column 7, line 13 and figures 4-8.	1-20
A	US 2002-0168099 A1 (AMIR NOY) 14 November 2002 See abstract, paragraphs [0021]-[0040] and figure 1.	1-20

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 June 2014 (19.06.2014)	**20 June 2014 (20.06.2014)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea
Facsimile No. +82-42-472-7140

Authorized officer
CHOI, Sang Won
Telephone No. +82-42-481-8291

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2014/010743

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 7752584 B2	06/07/2010	CN 101334802 A	31/12/2008
		CN 101334802 B	09/02/2011
		KR 10-0877105 B1	07/01/2009
		KR 10-2008-0114402 A	31/12/2008
		TW 200901277 A	01/01/2009
		US 2009-0007052 A1	01/01/2009
		US E044221 E1	14/05/2013
US 7170593 B2	30/01/2007	JP 2003-098114 A	03/04/2003
		JP 4035974 B2	23/01/2008
		US 2003-0058435 A1	27/03/2003
		US 2006-0038986 A1	23/02/2006
		US 6965429 B2	15/11/2005
WO 2009-018337 A1	05/02/2009	JP 2010-535430 A	18/11/2010
		KR 10-1381300 B1	04/04/2014
		KR 10-2010-0046240 A	06/05/2010
		US 2009-0037134 A1	05/02/2009
		US 8611639 B2	17/12/2013
US 6295374 B1	25/09/2001	EP 1076877 A1	21/02/2001
		JP 2002-510824 A	09/04/2002
		WO 99-52064 A1	14/10/1999
US 2002-0168099 A1	14/11/2002	IL 149588 A	24/07/2007
		IL 149588 D0	10/11/2002
		TW 577995 A	01/03/2004
		US 7127099 B2	24/10/2006