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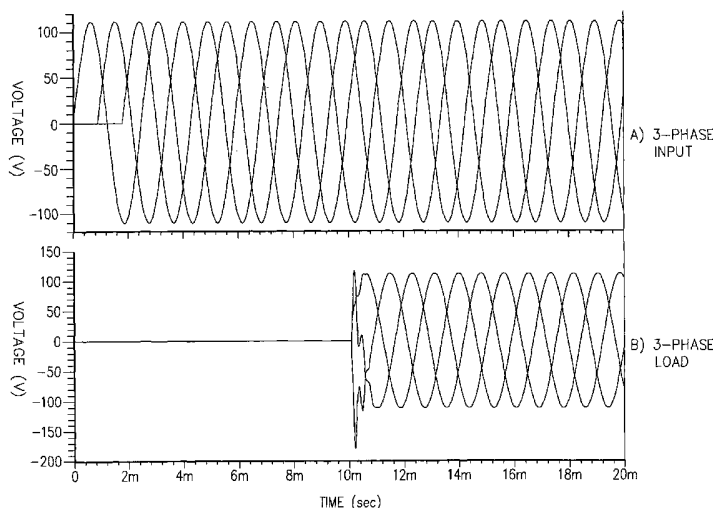
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(54) Title: SYSTEM AND METHOD UTILIZING A SOLID STATE POWER CONTROLLER (SSPC) FOR CONTROLLING AN ELECTRICAL LOAD OF A VARIABLE FREQUENCY THREE-PHASE POWER SOURCE



(57) Abstract: A solid state power controller (SSPC) (100) includes a power switching controller (30) and power switching devices (PSDs) (20A, 20B, 20C) for controlling each phase of a multiple-phase load to switch-on or -off at a zero-crossing point of a corresponding phase of a multiple-phase power source. The power switching controller (30) may include an ASIC (25A, 25B, 25C) for controlling each PSD (20A, 20B, 20C) to switch the corresponding load phase on or off. The ASIC (25A, 25B, 25C) may be configured to control the PSD (20A, 20B, 20C) to switch-on the load phase at a detected zero-crossing point of the voltage supplied by the corresponding phase of the power source, and to switch-off the load phase at a detected zero-crossing point of the load current supplied by the corresponding phase of the power source.



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**SYSTEM AND METHOD UTILIZING A SOLID STATE  
POWER CONTROLLER (SSPC) FOR CONTROLLING AN ELECTRICAL  
LOAD OF A VARIABLE FREQUENCY THREE-PHASE POWER SOURCE**

**Field of the Invention**

**[0001]** The present invention relates to power control for electrical loads of variable frequency three-phase power sources utilizing solid state power controllers (SSPCs).

**Background of the Invention**

5 **[0002]** Conventional mechanical and electro-mechanical power switches suffer from disadvantages including high levels of noise and spike voltages generated when an electrical load is switched on. To overcome these problems, a solid state power controller (SSPC) may be utilized, which includes a solid state switching device, e.g., a power  
10 MOSFET switch. Such SSPCs also have the advantages of occupying less space and being light-weight.

**[0003]** In an electrical system with a variable frequency AC power source, it is desirable to switch-on the loads (e.g., single-phase and three-phase loads) at zero-crossing points of the waveform of the voltage  
15 generated by the power source. This reduces the harmonics that are produced when the loads are turned on, and minimizes electromagnetic interference (EMI) effects. It is also advantageous to switch-off such loads at the zero-crossing points of the current supplied by the power source, in order to reduce the effects of EMI and thermal stress on the  
20 switching devices and load equipment.

**Summary of the Invention**

**[0004]** Exemplary embodiments of the present invention include a solid state power control (SSPC) device that controls a multiple-phase electrical load of a multiple-phase voltage source, which includes a power  
25 switching device (PSD) that switches each phase of the electrical load on or off at a zero-crossing point of a corresponding phase of the power source.

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[0005] According to an exemplary embodiment, the SSPC device includes zero-crossing detectors operably connected to the PSDs. Each zero-crossing detector may be configured to receive a waveform corresponding to a phase of the power source, and to convert the received waveform into a digital pulse waveform whose rising and falling edges occur at zero-crossing points for the phase. The rising edges of these digital pulse waveforms may act as triggering signals for a power switching controller in the SSPC device. Accordingly, when the power switching controller receives a command signal to turn the electrical load on or off, the power switching controller may be triggered by these triggering signals to control the PSDs to switch on or off the corresponding load phases.

[0006] According to an exemplary embodiment of the present invention, the SSPC device is configured to invert the digital pulse waveform of the third phase of the power source in order to ensure that the rising edges, i.e., triggering signals, for each of the three phases occur within one-half cycle of one another.

[0007] In another exemplary embodiment, the SSPC device may include a fail-safe device in the power switching controller that is configured to switch any of the phases on or off at an arbitrary time when the triggering signal of the corresponding phase is not received by the PSD. According to an exemplary embodiment, the fail-safe device may wait at least one-half ( $\frac{1}{2}$ ) of the phase cycle time before arbitrarily turning on or off the phase.

[0008] According to exemplary embodiments of the present invention, the SSPC device is configured to control each phase of a three-phase electrical load to switch on at a zero-crossing point of a corresponding phase of the voltage supplied by a three-phase power source. In other exemplary embodiments, the SSPC device may be configured to control each phase of the electrical load to switch off at a

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zero-crossing point of a corresponding phase of the current supplied to the load by the power source.

[0009] By utilizing the digital pause waveforms as zero-crossing detection signals for the phases of a multiple-phase power source (e.g., three-phase source), exemplary embodiments of the present invention provide power switching for the corresponding phases of an electrical load without dependence on the frequency or phase-shift among the phases of the power source. Thus, exemplary embodiments of the present invention may be used for controlling the electrical loads of multiple-phase power sources of various frequencies.

[0010] Further advantages and scope of applicability of the present invention will become apparent from the detailed description provided hereinafter. However, it should be understood that the detailed description and specific embodiments therein, while disclosing exemplary embodiments of the invention, are provided by way of illustration only.

#### Brief Description of the Drawings

[0011] A more complete understanding of the present invention will become apparent from the following description taken in conjunction with the accompanying drawings, wherein:

[0012] Fig. 1 illustrates the effects of switching on the phases of a three-phase electrical load at arbitrary points with respect to a three-phase power source;

[0013] Fig. 2 illustrates an instance where each phase of a three-phase load is switched on at a detected zero-crossing point of a corresponding phase of a three-phase power source in accordance with an exemplary embodiment of the present invention;

[0014] Fig. 3 illustrates a triggering signal for a particular phase of a three-phase load, which is generated based on the detected zero-crossing points of a corresponding phase in a three-phase power source, in accordance with an exemplary embodiment of the present invention;

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[0015] Fig. 4 illustrates the phases of a three-phase load being switched-on at zero-crossing points in an instance where a triggering signal for the third phase is inverted, in accordance with an exemplary embodiment of the present invention;

5 [0016] Fig. 5 illustrates the triggering signals for switching -on or -off each phase of a three-phase load, in which the third triggering signal is inverted to ensure that the three phases of the load are switched on or off within one-half cycle of one another, in accordance with an exemplary embodiment of the present invention;

10 [0017] Fig. 6 illustrates a block diagram of a solid state power controller (SSPC) in accordance with an exemplary embodiment of the present invention; and

[0018] Fig. 7 illustrates a schematic diagram of the SSPC illustrated in Fig. 6, in accordance with an exemplary embodiment of the present invention.

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#### Detailed Description of Exemplary Embodiments

[0019] Exemplary embodiments of the present invention are disclosed in the following description.

[0020] A solid state power controller (SSPC) is generally a circuit card assembly that contains one or more solid state power switching devices and a power switching controller. The power switching controller may, for instance, include multiple Application Specific Integrated Circuits (ASICs). In AC electrical systems, an SSPC may be used to distribute AC power to various electrical loads and to protect the wiring in the system from overcurrent conditions. The SSPC may be modular in design so that it can be applied to many applications.

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[0021] A power switching device (PSD) of an SSPC provides line power switching to thereby turn an electrical load on or off. The PSD is controlled by the power switching controller of the SSPC. According to an exemplary embodiment, the PSD may utilize power MOSFET technology to minimize power dissipation.

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[0022] The power switching controller of an SSPC incorporates load switching and protective functions. These functions are enabled by related "logic" which refers to any combination of hardware, software, and/or combinations of hardware and software to implement the associated function, as will be appreciated by those skilled in the art.

[0023] According to an exemplary embodiment, the protective functions of a power switching controller may include monitoring the heating conditions of a PSD and ensuring that the thermal limits of certain components and wiring in the system is not exceeded. For example, the power switching controller may include logic for monitoring the substrate temperature and/or load current for a corresponding PSD, and shut-down logic for opening the switching device when either the temperature or load current exceeds a predetermined threshold.

[0024] According to an exemplary embodiment, the load switching functions of the power switching controller includes controlling the timing at which a corresponding PSD switches its load on or off. For example, the power switching controller may control the PSD to turn a load on or off in response to a received command signal. Such command signals may be sent by a micro-controller, which controls the distribution of power in the electrical system.

[0025] According to an exemplary embodiment of the present invention, the load switching logic of the power switching controller is operable to control a particular PSD to switch-on or -off a connected load at zero-crossing points when the PSD is operating in AC mode. For instance, when an electrical load is to be turned on, the power switching controller may control the corresponding PSD to switch the load on at a detected zero-crossing point of the voltage waveform supplied by the power source. When the load is to be turned off, the power switching controller may control the PSD to switch the load off at a detected zero-crossing point of the waveform of the current supplied by the power source (i.e., the load current of the PSD).

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[0026] In an exemplary embodiment, the SSPC may include a power switching controller connected to multiple PSDs in order to control a multiple-phase power source. For example, such an SSPC may be configured to control a three-phase power source. In such a configuration, the SSPC may include three PSDs in order to control a three-phase load (each PSD controlling a corresponding phase), and the power switching controller of the SSPC may include three ASICs that are gang-operated such that each ASIC controls a corresponding one of the PSDs. Thus, each of the three phases of the load may be controlled in a coordinated manner.

[0027] In the situation where an SSPC is controlling a three-phase load, or other multiple-phase load, it would be advantageous for the PSDs to switch each of the load phases on/off at a zero-crossing point.

[0028] Fig. 1 illustrates the effects of switching the phases of the three-phase electrical load on without regard to the zero-crossing points of the voltage waveform A) supplied by a three-phase power source. Waveform B) illustrates the three load phases, which are all turned on at an arbitrary point. Particularly, waveform B) shows the voltage harmonics and noise that can be generated as each phase of the load is switched on.

[0029] Conversely, Fig. 2 illustrates an instance where each phase of a three-phase load, as illustrated by waveform A), is turned on at a zero-crossing point of the corresponding phase in the voltage supplied by the three-phase power source. In Fig. 2, waveform B) illustrates the voltage waveform of the power source. Specifically, waveform A) shows that the noise and harmonics of each phase of the load are significantly reduced when the phases are switched-on at a zero-crossing point.

[0030] In order to reduce the thermal stress on the components and the wiring of the PSDs and load circuitry, it is also advantageous to turn off each phase of a multiple-phase load at a zero-crossing point of the corresponding phase of the current supplied by the power source. For instance, the PSD associated with a particular phase may include a shunt



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resistor, from which the load current (supplied by the particular phase of the power source) can be measured. To reduce the risk of overcurrent, the PSD may be controlled to turn the connected phase of the electrical load off at a zero-crossing point of the measured current.

5    **[0031]**       According to an exemplary embodiment, each ASIC in the power switching controller may include logic for performing zero-crossing voltage detection and zero-crossing current detection. To ensure proper control of the multiple-phase load, the ASICs may also include fail-safe mechanisms for ensuring that each phase of the electrical load is  
10   switched -on/-off in case the zero-crossing detection signal corresponding to that phase is disabled. The fail-safe mechanism will be described in greater detail below.

**[0032]**       According to an exemplary embodiment, the zero-crossing detection logic utilized in the power switching controller may generate  
15   triggering signals comprised of digital pulse (square) waveforms.

**[0033]**       For example, the zero-crossing voltage detection in each ASIC may generate a triggering signal that represents a square waveform in-phase with the corresponding phase of the AC voltage generated by the power source. Such a triggering signal follows the period and phase of  
20   the corresponding voltage phase of the power source, regardless of whether this voltage has a constant or variable frequency.

**[0034]**       Fig. 3 illustrates the triggering signal generated by the zero-crossing voltage detection logic of an ASIC in response to a voltage phase supplied by the power source. Each pulse in the triggering signal of Fig. 3  
25   includes a rising edge. Any of these rising edges may be used for triggering logic within the ASIC, for instance, to activate a PSD to turn on a corresponding phase load.

**[0035]**       The zero-crossing current detection logic of the ASIC may similarly output a triggering signal, as illustrated by Fig. 3, by generating a  
30   digital pulse waveform based on a load current supplied by the power source.

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[0036] As discussed above, the power switching controller of an SSPC may include logic to protect the PSDs and load equipment from overheating and/or overcurrent conditions. For example, the power switching controller may include mechanisms for automatically switching  
5 off all of the phases of the electrical load when a measured temperature or current is too high. It is important that each load phase be turned off as quickly as possible during such situations.

[0037] However, if an overheating or overcurrent condition occurs after one while the phases of the load are turning on, these protective  
10 mechanisms must wait until all of the phases of the load have been switched-on before any of them can be switched-off. When this situation arises, the risk of damage is significant if the gap between turn-on times for the respective load phases is large. Specifically, damage may occur to the PSD(s) and load equipment of the phase(s) already switched-on, while  
15 the last phase is waiting to be turned on.

[0038] To reduce these risks, the load should be controlled so that each phase will be turned on within a certain time limit. Thus, according to an exemplary embodiment, the power switching controller is designed to cause each phase of a multiple-phase load to be turned on within a  
20 predetermined time of one another, for example within one-half cycle of one other. In other words, exemplary embodiments of the present invention should switch-on the last load phase within  $\frac{1}{2}$  cycle of the first.

[0039] However, for a three-phase power source in which the phases (0, 240°) are 120° apart, the rising edges of the above-  
25 described triggering signals (digital pulse waveforms) for the first and third phases do not occur within one-half cycle of each other. To remedy this, the triggering signal corresponding to the third phase according to an exemplary embodiment.

[0040] Fig. 4 illustrates the effects of inverting the triggering signal  
30 for the third phase on the corresponding load. As shown in Fig. 4, the third phase (240°) of the three -phase load is switched on at a point

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where the corresponding voltage phase of the three-phase power source crosses zero toward a negative amplitude, while the first two phases of the load ( $0^\circ$ ,  $120^\circ$ ) are switched on at the points at which the corresponding voltage phases of the power source cross zero to a positive amplitude. Accordingly, each phase of the load is turned on within one-half cycle of one another.

[0041] Fig. 5 illustrates the pulse-type triggering signals generated for each phase of a three-phase load, in which the triggering signal for the third phase is inverted. In Fig. 5, the digital pulse waveforms A) and B) illustrate the triggering signals of the first and second load phases, respectively. Digital pulse waveform C) represents a non-inverted triggering signal generated by zero-crossing detection logic for the third pulse of the electrical load, while digital pulse waveform D) represents the inverted triggering signal generated for the third phase.

[0042] Referring to Fig. 5, after a command signal is received to switch-on the three-phase load (indicated by the star), Fig. 5 shows that inverting the triggering signal for the third phase will ensure that the rising edges of the triggering signals for the three load phases will occur within one-half cycle of each other.

[0043] According to an exemplary embodiment, the ASICs corresponding to each phase may be configured to invert the triggering signals generated by both the voltage and current zero-crossing detection logic, to ensure that the load phases are switched-on and -off within  $\frac{1}{2}$  cycle of one another. In an alternative exemplary embodiment, only the triggering signal of the voltage zero-crossing detection is inverted.

[0044] As described above, each ASIC may also be configured to include fail-safe logic to ensure that each phase of the load is switched - on/-off, even in cases where the corresponding triggering signal, i.e., the digital pulse waveform of the voltage/current detection circuit, becomes disabled.

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[0045] The fail-safe mechanism of each ASIC may include logic that waits a predetermined time (e.g., at least  $\frac{1}{2}$  cycle of the phase) after receiving the command signal to see if a rising edge of the digital pulse waveform is generated. If no rising edge is generated within the  
5 predetermined time, the ASIC may be triggered by the fail-safe logic to control the PSD to switch the corresponding phase of the load on/off at an arbitrary point.

[0046] Fig. 6 illustrates a block diagram of an SSPC 100 configured to control a multiple-phase electrical load of a multiple-phase power  
10 source. In particular, Fig. 6 illustrates an exemplary embodiment of an SSPC 100 for use in an AC electrical system to control a three-phase load of a three-phase power source.

[0047] In Fig. 6, each of the first phase, second phase, and third phase of the power source is fed into a respective low VA transformer  
15 10A, 10B, 10C. Each low VA transformer 10A, 10B, 10C is operably connected to a PSD 20A, 20B, 20C and an ASIC 25A, 25B, 25C, respectively. Each ASIC 25A, 25B, 25C is operably connected to the respective PSD 20A, 20B, 20C to control the corresponding phase of the load.

20 [0048] In particular, each ASIC 25A, 25B, 25C includes logic for processing the line voltage output from the connected low VA transformer 10A, 10B, 10C, and outputting a sensed voltage waveform to a voltage zero-crossing detection circuit 40.

[0049] The ASIC 25A, 25B, 25C also includes logic for processing  
25 and sensing the load current supplied to the connected PSD 20A, 20B, 20C from the corresponding low VA transformer 10A, 10B, 10C. For example, the load current may be measured across a shunt resistor included in the PSD 20A, 20B, 20C. The AC load current waveform is then output to a current zero-crossing circuit 50.

30 [0050] Both the voltage zero-crossing circuit 40 and the current zero-crossing circuit 50 send their respective detection signals to a control

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circuit 60, which in turn is operably connected to control the PSD 20A, 20B, 20C. As shown in Fig. 6, the PSD 20A, 20B, 20C is operably connected to the corresponding load of the electrical phase.

[0051] An exemplary embodiment of the operation of the SSPC 100 is provided in the following description.

[0052] Each low VA transformer 10A, 10B, 10C is configured to isolate a phase voltage of the power source to a PSD 20A, 20B, 20C, which controls the corresponding phase of the load. The low VA transformer 10A, 10B, 10C is also operable to lower the voltage level of the phase to a suitable level for the digital circuitry in the ASIC 25A, 25B, 25C.

[0053] Each ASIC 25A, 25B, 25C includes a voltage zero-crossing detection circuit 40 that converts the AC line voltage waveform, which is output by the low VA transformer 10A, 10B, 10C, for the corresponding power phase. Specifically, the voltage zero-crossing detection circuit 40 converts the voltage waveform to a digital pulse waveform, e.g., as illustrated in Fig. 3. This digital pulse waveform is sent to the control device 60 to be used as a triggering signal to control the connected PSD 20A, 20B, 20C to switch-on the corresponding load phase.

[0054] Accordingly, when the power switching controller 30 receives a command signal (not shown) to switch the load on, the control device 60 is instructed to turn on its corresponding phase load. After receiving such an instruction, logic within the control device 60 waits for the next rising edge of the triggering signal to be received from voltage zero-crossing detection circuit 40. The control device 60 is triggered by this rising edge to control the connected PSD 20A, 20B, 20C to switch-on the phase of the load.

[0055] As discussed above, if the control device 60 fails to receive a rising edge in the digital pulse waveform within a predetermined time (e.g., one-half phase cycle) of the time at which the command signal is received, a fail-safe mechanism (not shown) in the ASIC 25A, 25B, 25C

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may automatically trigger the control device 60 to control the PSD 20A, 20B, 20C to turn on its respective load phase. Thus, a failure with respect to the voltage zero-crossing detection circuit(s) 40 will not disable the load equipment.

5 [0056] In a similar fashion, the control device 60 uses a digital pulse waveform received from the current zero-crossing detection circuit 50 to control the PSD 20A, 20B, 20C to turn off its respective phase load. Specifically, after a switch-off command signal (not shown) is received by the power switching controller 30, the control device 60 is instructed to  
10 switch-off a corresponding phase load. Thereafter, the control device is triggered by the next rising edge of the triggering signal from current zero-crossing circuit 50 to control the PSD 20A, 20B, 20C to switch the load off.

[0057] However, fail-safe logic (not shown) may be included within  
15 each ASIC 25A, 25B, and 25C to trigger the control device 60 to control the connected PSD 20A, 20B, 20C to switch the load phase off if the control device 60 does not receive a rising edge within a predetermined time (e.g., one-half cycle) after the switch-off command signal is received. Such a mechanism decreases the risk of overheating within a  
20 particular PSD 20A, 20B, 20C, whose light weight and small size make it susceptible to overcurrent conditions.

[0058] As shown in Fig. 6, the digital pulse waveforms of the voltage and current zero-crossing detection circuits 40 and 50, respectively, may be inverted before being sent to the control device 60.  
25 Thus, the control device 60 of ASIC 25C may be triggered to control the PSD 20C to switch-on or -off the third phase of the load at a zero-crossing point at which the third phase of the power source transitions from positive to negative, rather than from negative to positive. As illustrated in Fig. 5, this inverted zero-crossing detection signal allows  
30 each of the three phases of the electrical load to be turned on or off within one-half cycle of one another. Thus, each phase of the electrical

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load may be turned on and off at zero-crossing points when the above-described fail-safe logic is utilized.

[0059] According to the above-described operation, the ASICs 25A, 25B, and 25C of the power switching controller 30 are operable to turn each phase of a multiple-phase electrical load on at a zero-crossing point of supplied voltage, thus reducing noise and harmonics, as well as the effects of EMI, in the load. Further, the ASICs are operable to switch each phase of the load off at a zero-crossing point of the load current, thereby decreasing the adverse effects of thermal stress on the components and wiring of the electrical system.

[0060] Fig. 7 is a schematic diagram more specifically illustrating circuit components configured to implement line voltage isolation and voltage zero-crossing detection, according to an exemplary embodiment of the present invention. In particular, Fig. 7 illustrates circuits 210, 220, and 230 for generating the triggering signals corresponding to voltage zero-crossing detection for the first phase, second phase, and third phase, respectively.

[0061] In Fig. 7, each of the circuits (210, 220, and 230) includes a low VA transformer (10A, 10B, and 10C, respectively) for isolating the corresponding phase of the input voltage  $V_{\text{INPUT}}$  to voltage detection circuitry. The voltage detection circuitry of each circuit (210, 220, 230) is configured with a voltage comparator IC 70. Further, the circuit 230, which corresponds to the third phase, includes an inverting circuit 80 for providing an inverted zero-crossing detection signal. However, Fig. 7 illustrates an exemplary embodiment, and the present invention covers all circuit designs which are functionally equivalent or obvious variations.

[0062] According to an exemplary embodiment, the SSPC 100 may be implemented in an electrical power distribution system (EPDS), which includes one or more micro-controllers for issuing command signals to the SSPC 100 to turn the electrical load on or off. However, the power switching controller 30 of the SSPC 100 may also make its own

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determination to switch the load off based on monitoring and protective functions. Where the power switching controller 30 makes such a determination, it may generate its own command signal to instruct each ASIC 25A, 25B, 25C to switch its respective load phase on or off.

5     [0063]     As described above, exemplary embodiments of the present invention may be utilized in an electrical power distribution system, such as the Electrical Load Management Center (ELMC) described in U.S. Patent Application No. 10/017,125 entitled "Electric Load Management Center," filed on December 14, 2001, the entire contents of which are  
10    herein incorporated by reference. For example, the SSPC 100 of the present invention may be implemented in a Load Management Module (LMM) in the ELMC described in this application, as will be readily apparent to those of ordinary skill in the art.

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WHAT IS CLAIMED IS:

1. A method for operating a solid state power control (SSPC) device (100) to control a multiple-phase electrical load for a multiple-phase power source, comprising:  
switching at least one phase of the multiple-phase electrical load on  
5 or off at a zero-crossing point for a corresponding phase of the multiple-phase power source.
2. The method according to claim 1, further comprising:  
generating, for each voltage phase of the power source, a digital  
pulse waveform whose rising and falling edges occur at zero-crossing  
10 points for the voltage phase, wherein the switching step uses at least one of the edges of each digital pulse waveform to trigger a corresponding phase of the electrical load to be switched-on.
3. The method according to claim 2, wherein the switching step  
is performed in response to a switch-on command received by the SSPC  
15 device.
4. The method according to claim 3, wherein the switching step  
switches on each phase of the electrical load within a predetermined time  
after a first one of the phases of the electrical load is switched on.
5. The method according to claim 3, wherein  
20 the electrical load is a three-phase electrical load,  
the power source is a three-phase power source, and  
the generating step includes,  
generating a first, second and third digital pulse waveform  
for the first, second and third voltage phases of the power source,  
25 respectively;  
inverting the third digital pulse waveform, and  
the switching step includes;

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using the rising edge of the first and second digital pulse waveform to trigger a first and second phase of the electrical load, respectively, to be switched-on; and

5 using the rising edge of the inverted third digital pulse waveform to trigger a third phase of the electrical load to be switched-on.

6. The method according to claim 1, further comprising:  
generating, for each current phase of the power source, a digital pulse waveform whose rising and falling edges occur at zero-crossing points for the current phase, wherein the switching step uses at least one  
10 of the edges of the digital pulse waveform to trigger a corresponding phase of the electrical load to be switched-off.

7. The method according to claim 6, wherein the switching step is performed in response to a switch-off command received by the SSPC device.

15 8. The method according to claim 7, wherein the electrical load is a three-phase electrical load, the power source is a three-phase power source, and the generating step includes,  
generating a first, second and third digital pulse waveform  
20 for the first, second and third current phase of the power source, respectively;

inverting the third digital pulse waveform, and  
the switching step includes;  
using the rising edge of the first and second digital pulse  
25 waveform to trigger a first and second phase of the electrical load, respectively, to be switched-off; and  
using the rising edge of the inverted third digital pulse waveform to trigger a third phase of the electrical load to switched-off.

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9. A solid state power control (SSPC) device (100) for controlling a multiple-phase electrical load of a multiple-phase power source, comprising:

5 one or more power switching devices (PSDs) (20A, 20B, 20C), each of which is configured to switch a phase of the multiple-phase electrical load on or off at a zero-crossing point of a corresponding phase of the variable frequency multiple-phase power source.

10. The SSPC device according to claim 9, further comprising:  
10 one or more zero-crossing detection devices (40, 50), each of which is configured to receive a waveform corresponding to a phase of the power source, and to convert the received waveform into a digital pulse waveform whose rising and falling edges occur at zero-crossing points for the received waveform.

11. The SSPC device according to claim 10, further comprising:  
15 one or more control devices (60), each of which is configured to receive the digital pulse waveform from an operably connected zero-crossing detection device as the triggering signal for a corresponding PSD, wherein the control device is triggered by a rising edge of the received triggering signal to control the PSD to switch the respective phase of the  
20 electrical load on or off.

12. The SSPC device according to claim 11, wherein at least one of the control devices is configured to receive, and be triggered by, an inverted digital pulse waveform of the operably connected zero-crossing detection device

25 13. The SSPC device according to claim 11, wherein each control device is configured to:  
receive a command signal, and

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be triggered by the rising edge of the triggering signal, which is received after the command signal, to control the corresponding PSD to switch the respective phase of the electrical load on or off.

14. The SSPC device according to claim 11, wherein  
5 at least one of the zero-crossing detection devices is a voltage zero-crossing detector (40) configured to receive a waveform corresponding to a voltage phase of the power source, and to convert the received waveform into a digital pulse waveform, and

10 the control circuit, which is operably connected to the voltage zero-crossing detector, is triggered to control the corresponding PSD to switch-on the respective phase of the electrical load.

15 15. The SSPC device according to claim 11, wherein  
at least one of the zero-crossing detection devices is a current zero-crossing detector (50) configured to receive a waveform corresponding to a current phase of the power source, and to convert the received waveform into a digital pulse waveform, and

the control circuit, which is operably connected to the current zero-crossing detector, is triggered to control the corresponding PSD to switch-off the respective phase of the electrical load.

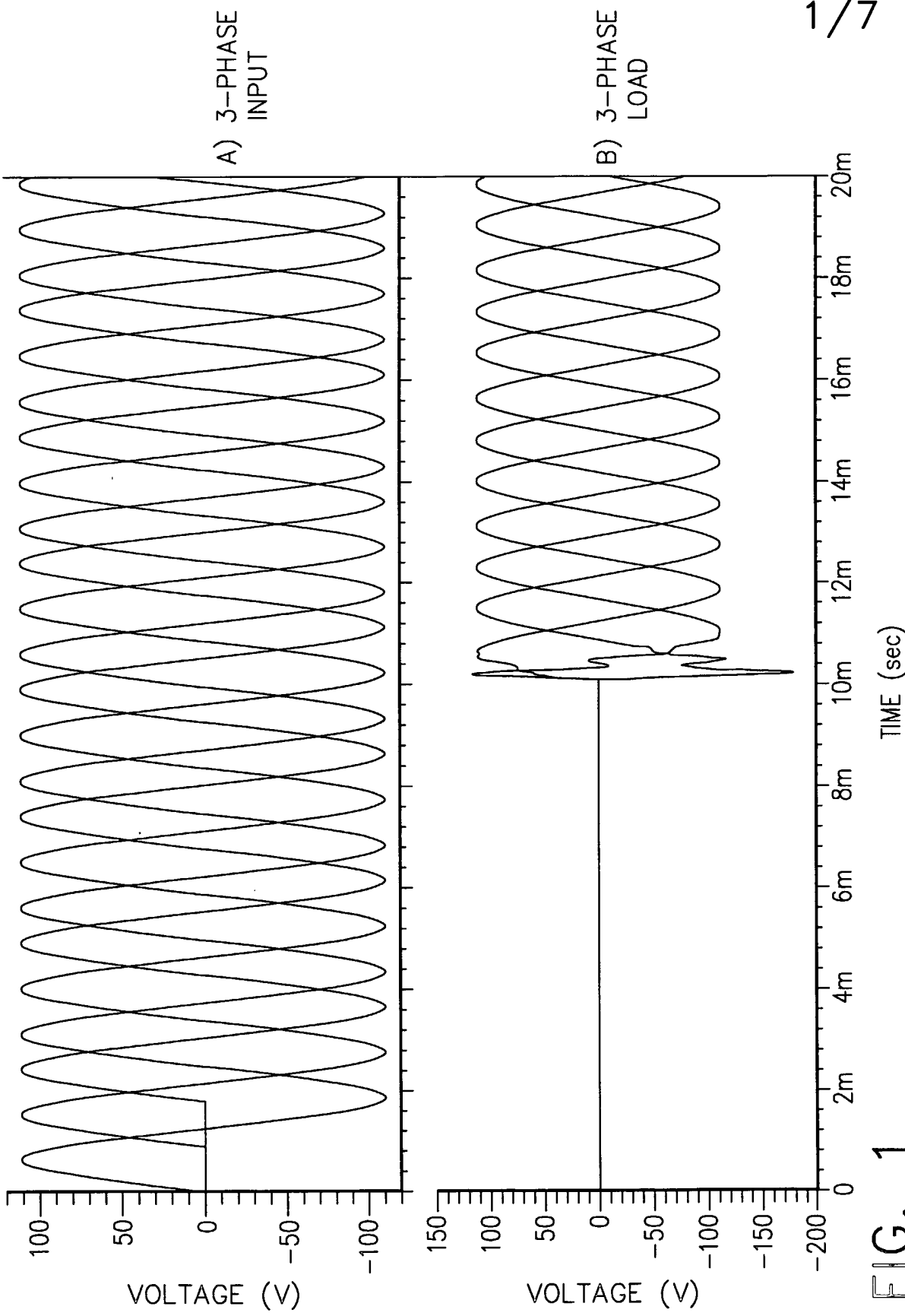
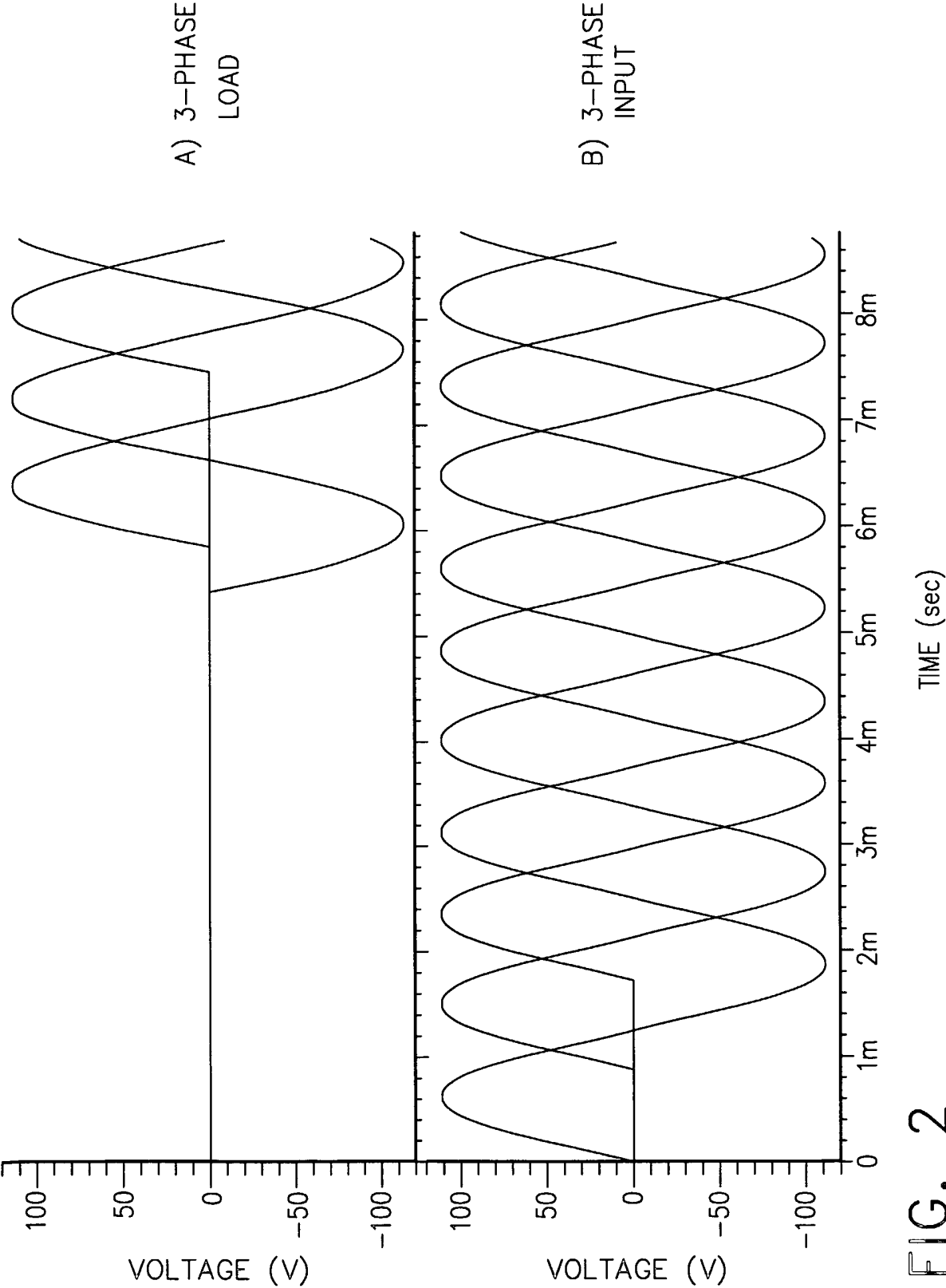


FIG. 1



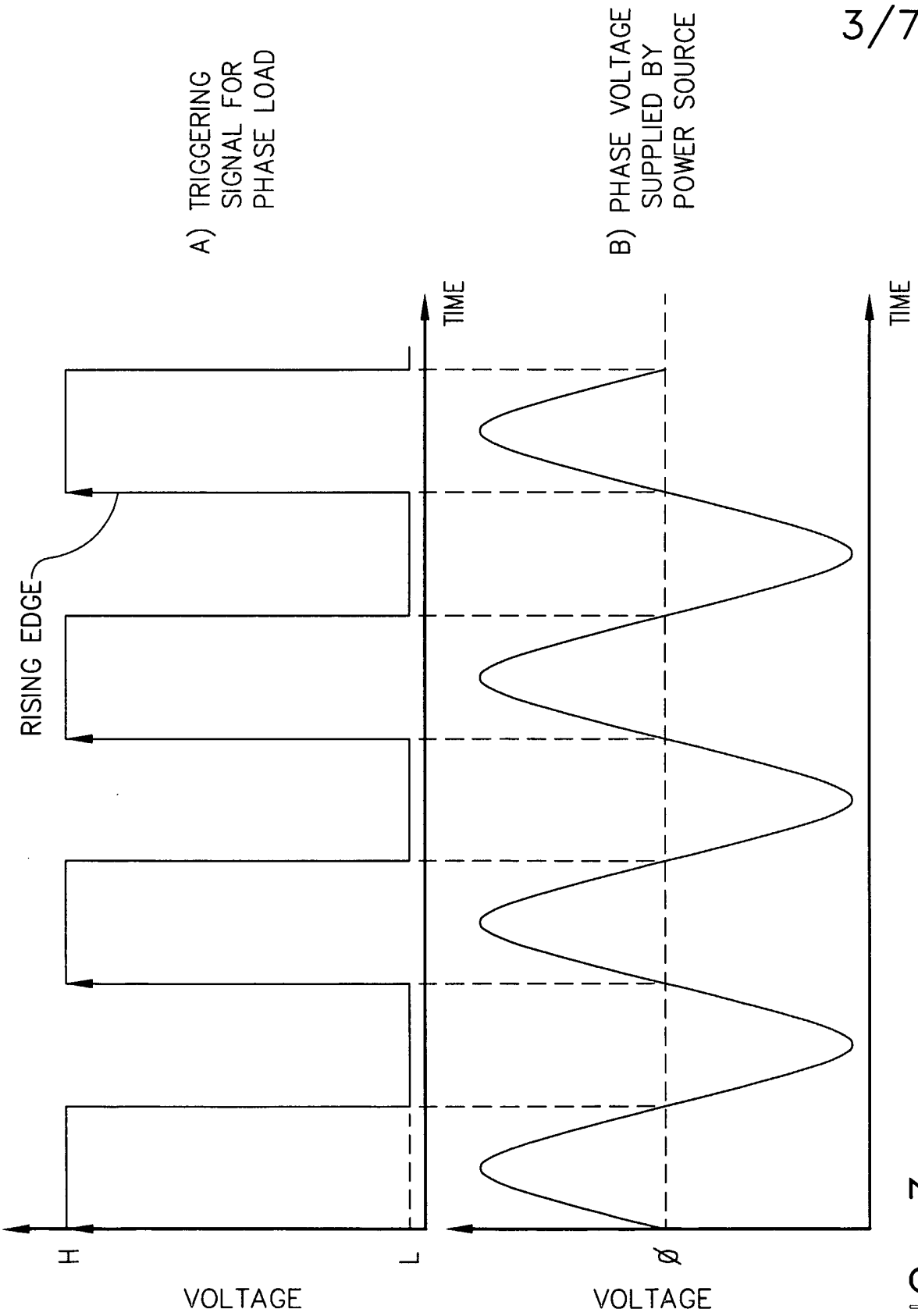
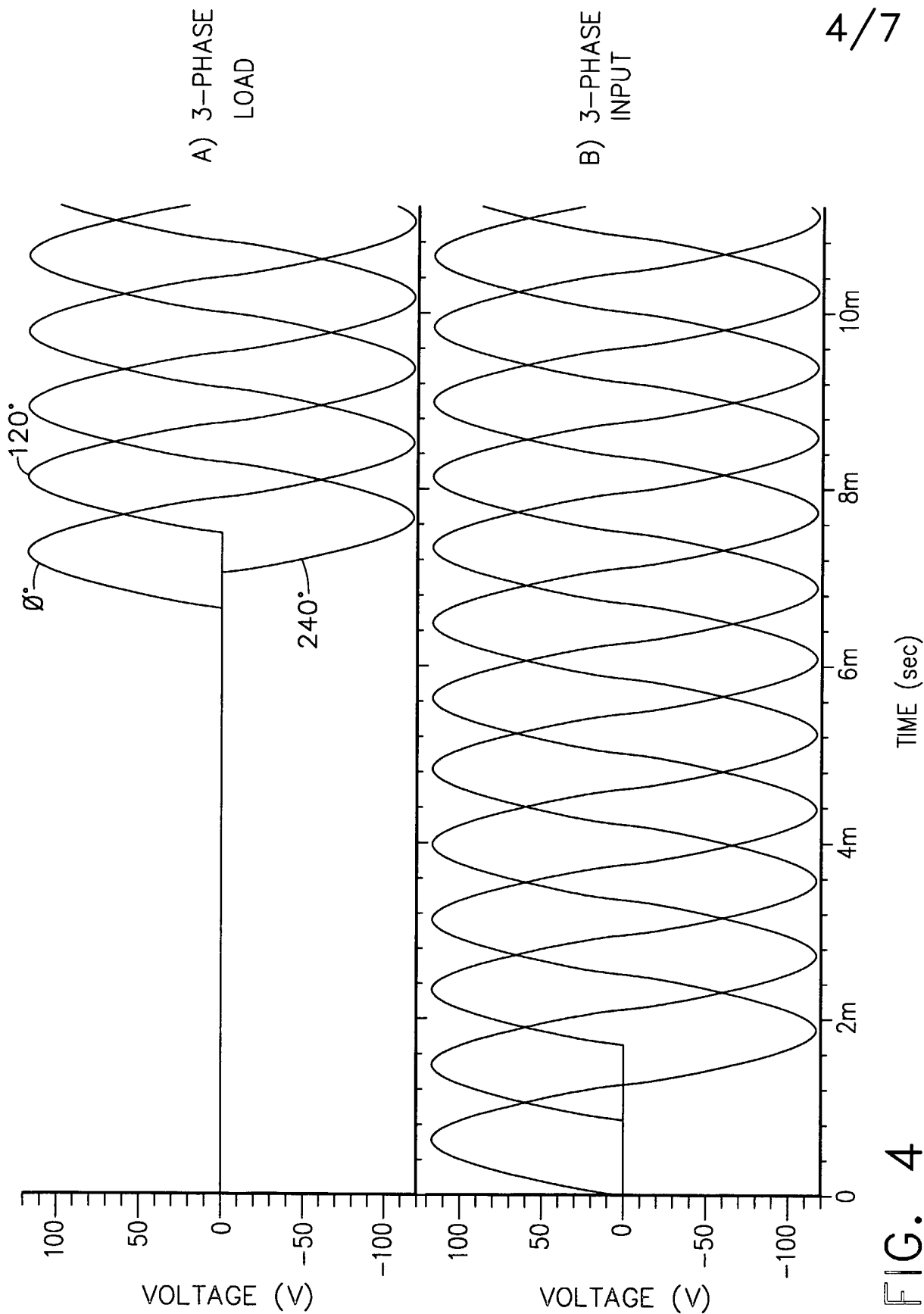


FIG. 3





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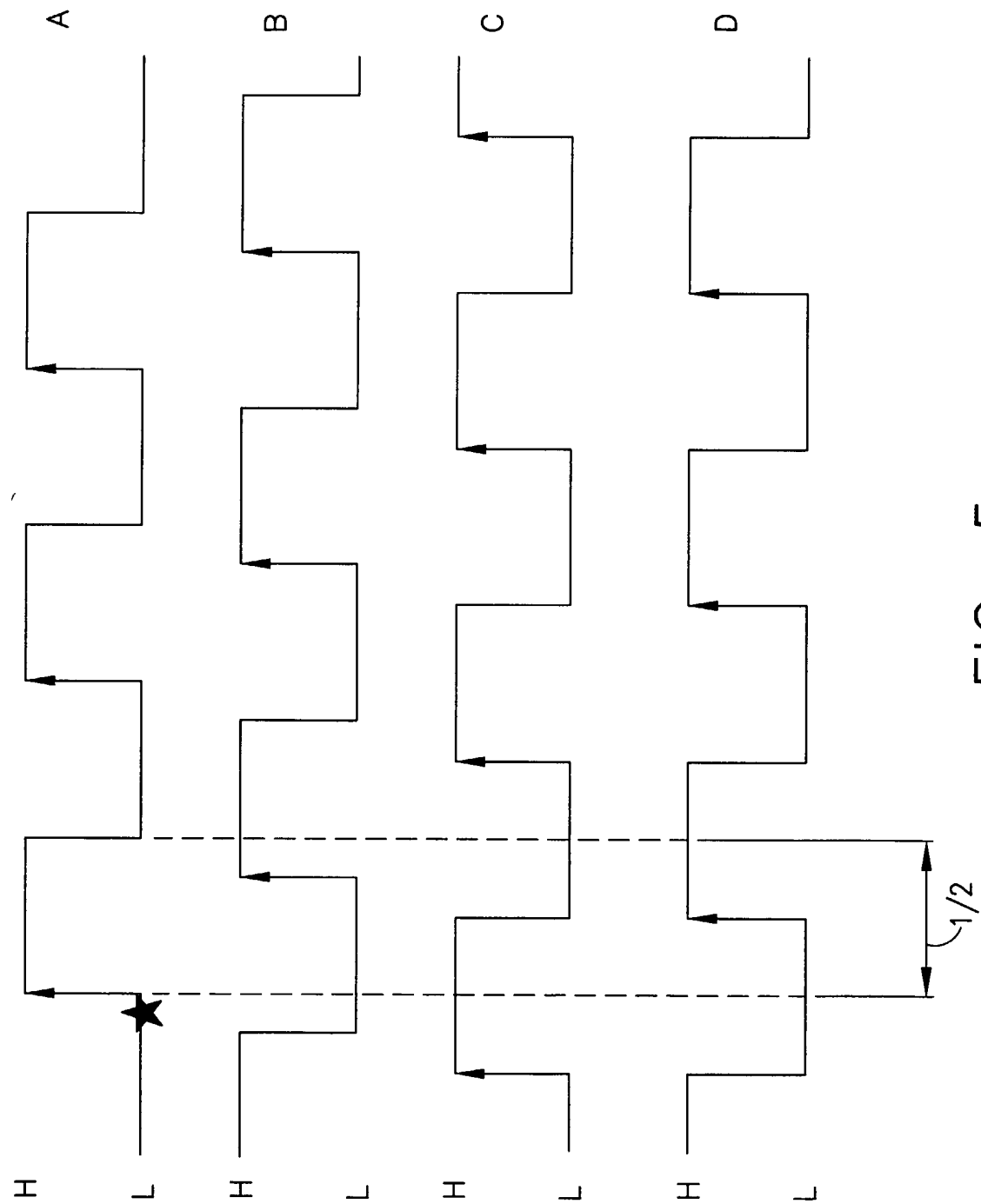


FIG. 5

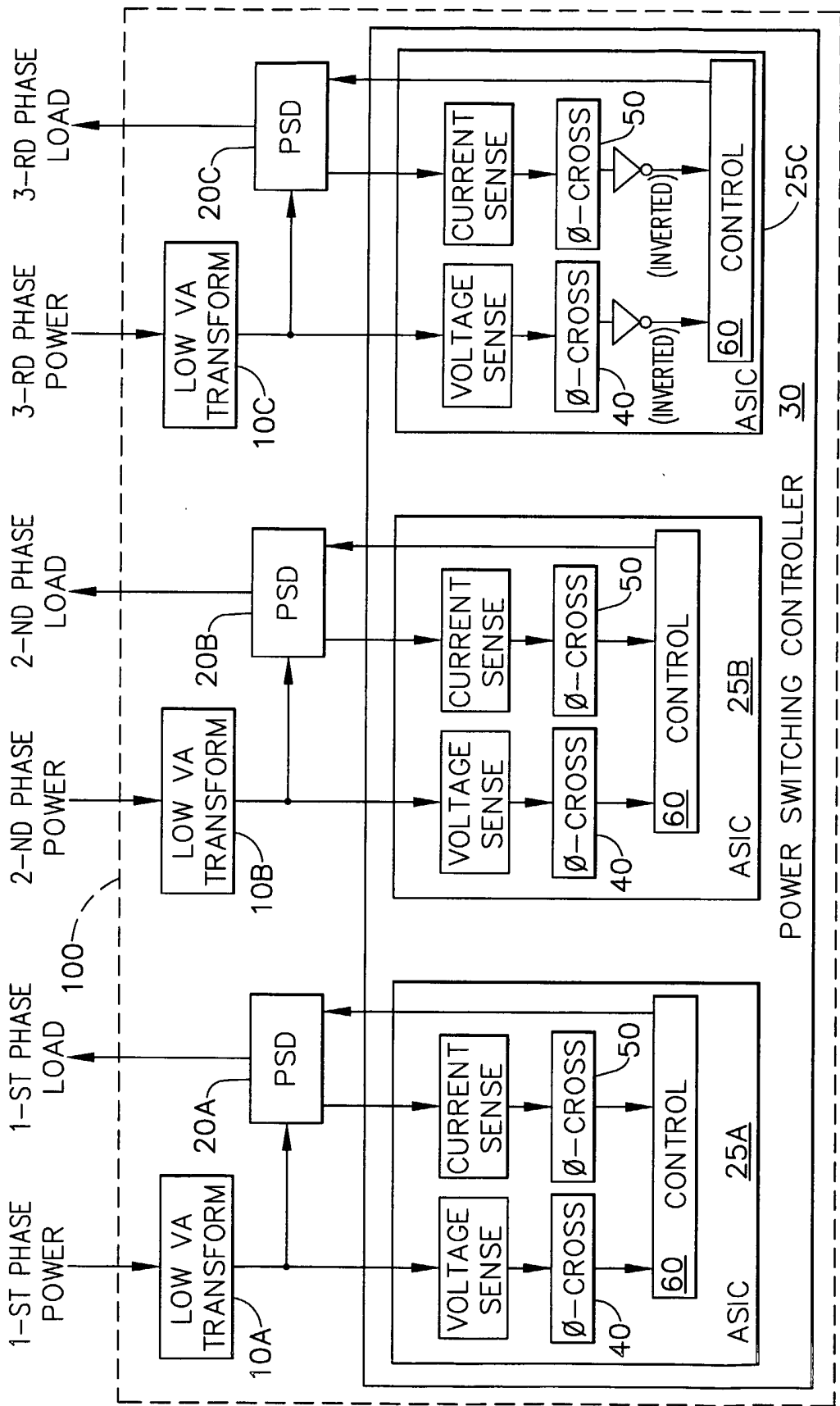


FIG. 6

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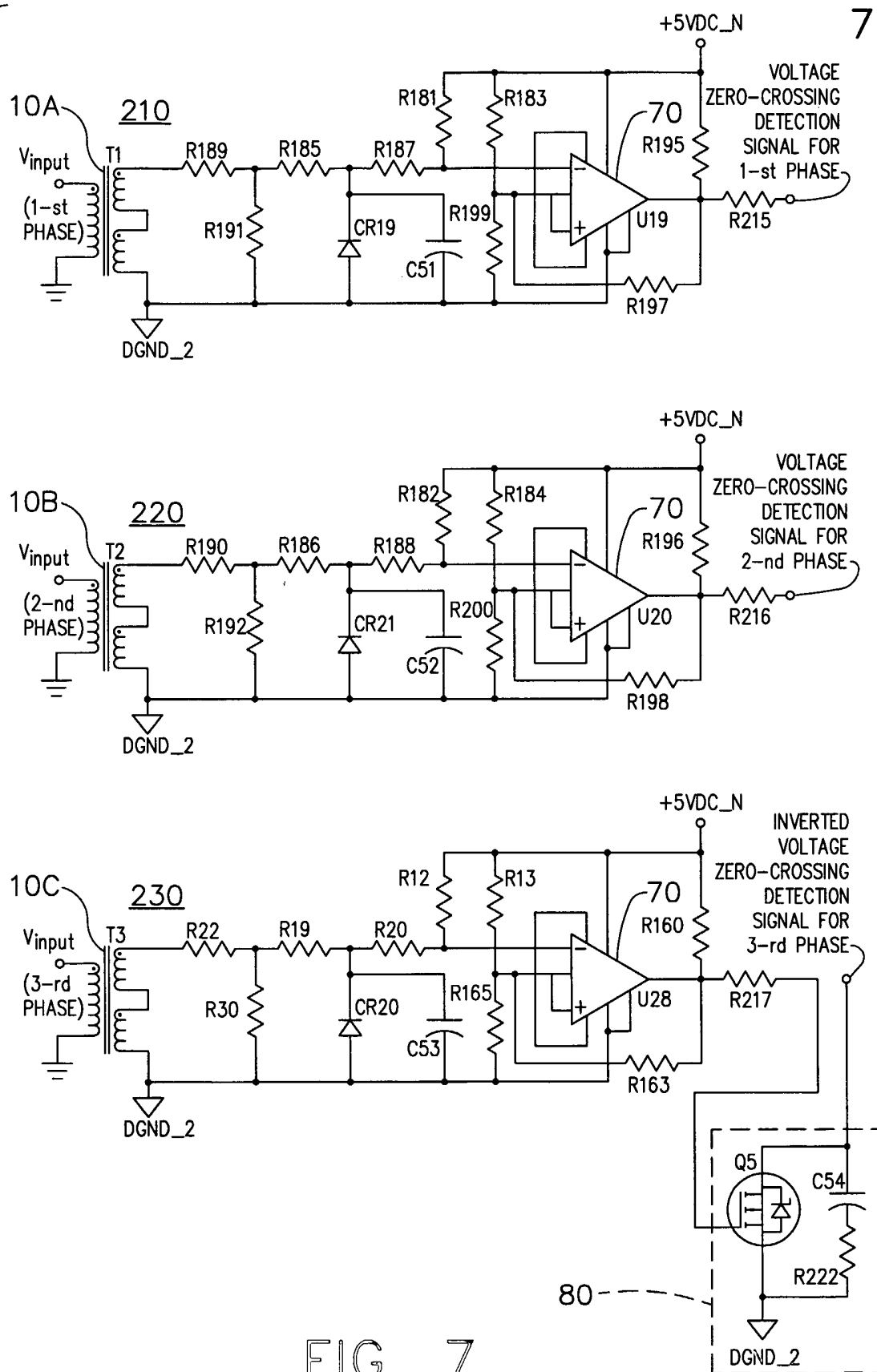


FIG. 7

## INTERNATIONAL SEARCH REPORT

International Application No

PCT/US2004/029414

**A. CLASSIFICATION OF SUBJECT MATTER**  
IPC 7 H02M5/257

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 713 744 A (COSTON ET AL) 15 December 1987 (1987-12-15) abstract column 2, line 52 - line 65 claim 11 figure 1	1-15
A	----- US 4 570 214 A (TANAKA ET AL) 11 February 1986 (1986-02-11) abstract column 10, line 37 - line 47 column 14, line 2 - line 11 ----- -/--	1-15

☒ Further documents are listed in the continuation of box C.☒ Patent family members are listed in annex

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Date of the actual completion of the international search

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## INTERNATIONAL SEARCH REPORT

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## C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Information on patent family members

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US 4570214	A	11-02-1986	NONE	
JP 59096869	A	04-06-1984	NONE	
JP 56115170	A	10-09-1981	NONE	