Office de la Propriété Intellectuelle du Canada
Un organisme d'Industrie Canada

Canadian Intellectual Property Office
An agency of Industry Canada

CA 2583654 A1 2006/04/27

(21) 2 583 654

(12) DEMANDE DE BREVET CANADIEN
CANADIAN PATENT APPLICATION

(13) A1

(86) Date de dépôt PCT/PCT Filing Date: 2005/10/12
(87) Date publication PCT/PCT Publication Date: 2006/04/27
(85) Entrée phase nationale/National Entry: 2007/04/02
(86) N° demande PCT/PCT Application No.: US 2005/036513
(87) N° publication PCT/PCT Publication No.: 2006/044372
(30) Priorité/Priority: 2004/10/12 (US60/618,240)

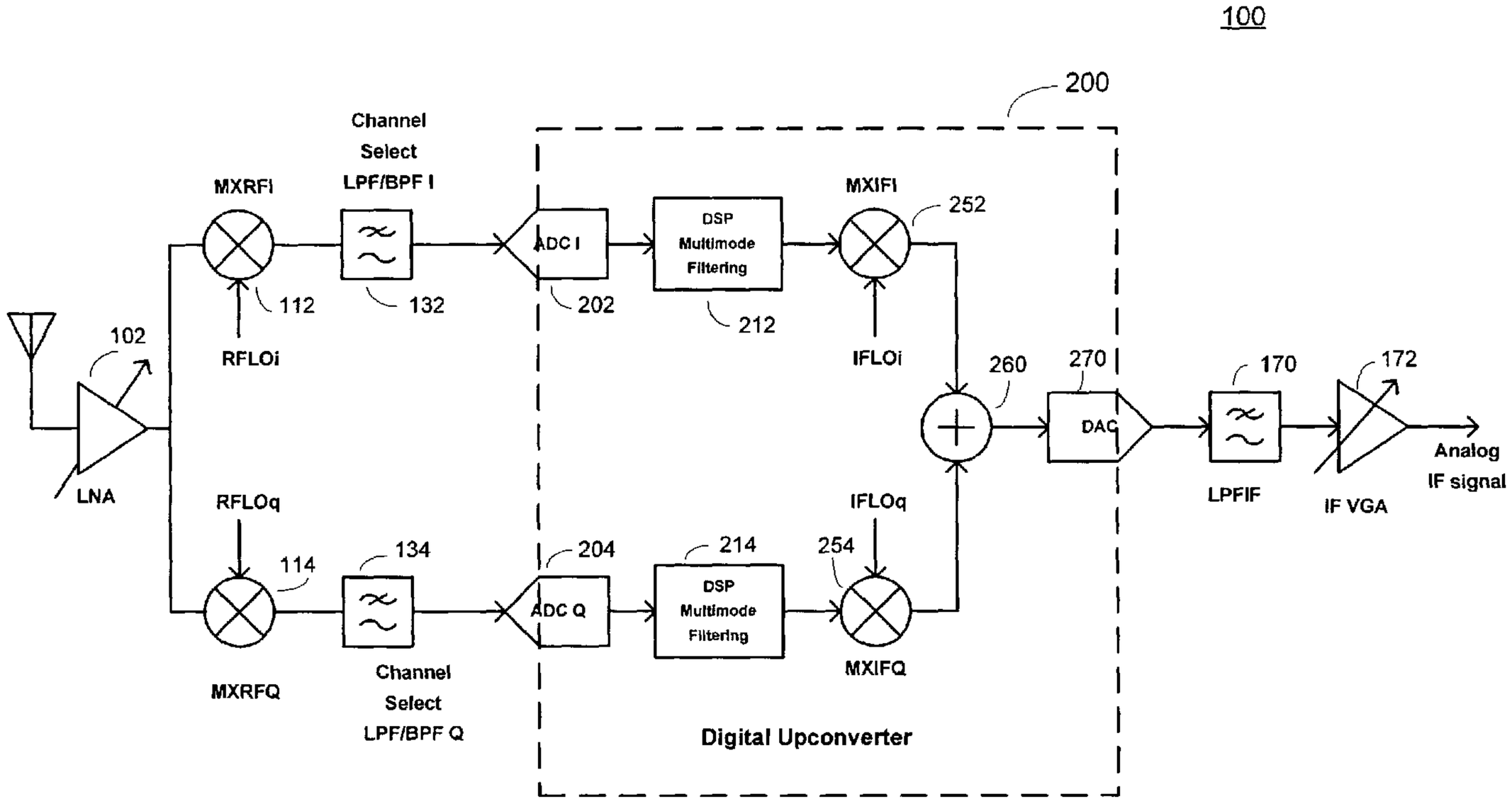
(51) Cl.Int./Int.Cl. *H04B 1/30* (2006.01)

(71) Demandeur/Applicant:
MAXLINEAR, INC., US

(72) Inventeurs/Inventors:
SEENDRIPU, KISHORE, US;
MONTEMAYOR, RAYMOND, US;
YE, SHENG, US;
CHANG, GLENN, US;
LING, CURTIS, US

(74) Agent: SMART & BIGGAR

(54) Titre : ARCHITECTURE DE RECEPTEUR A FREQUENCE INTERMEDIAIRE GENEREE NUMERIQUEMENT
(54) Title: A RECEIVER ARCHITECTURE WITH DIGITALLY GENERATED INTERMEDIATE FREQUENCY



(57) Abrégé/Abstract:
A receiver can be configured to include an RF front end that is configured to downconvert a received signal to a baseband signal or a low Intermediate Frequency (IF) signal. The receiver can downconvert the desired signal from an RF frequency in the presence of numerous interference sources to a baseband or low IF signal for filtering and channel selection. The filtered baseband or low IF signal can be converted to a digital representation. The digital representation of the signal can be upconverted in the digital domain to a programmable IF frequency. The digital IF signal can be converted to an analog IF signal that can be processed by legacy hardware.

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
27 April 2006 (27.04.2006)

PCT

(10) International Publication Number
WO 2006/044372 A3

(51) **International Patent Classification:**
H04B 1/30 (2006.01)

(21) **International Application Number:**
PCT/US2005/036513

(22) **International Filing Date:** 12 October 2005 (12.10.2005)

(25) **Filing Language:** English

(26) **Publication Language:** English

(30) **Priority Data:**
60/618,240 12 October 2004 (12.10.2004) US

(71) **Applicant** *(for all designated States except US)*: **MAXLINEAR, INC.** [US/US]; 2036 Corte Del Nogal, #200, Carlsbad, CA 92008 (US).

(72) **Inventors; and**

(75) **Inventors/Applicants** *(for US only)*: **SEENDRIPU, Kishore** [IN/US]; 7174 Pintail Drive, Carlsbad, CA 92009 (US). **MONTEMAYOR, Raymond** [US/US]; 2340 Carol View Drive #301, Cardiff by the Sea, CA 92007 (US). **YE, Sheng** [CN/US]; 3991-G Miramar Street, La Jolla, CA 92037 (US). **CHANG, Glenn** [US/US]; 30312 Anamonte, Laguna Niguel, CA 92677 (US). **LING, Curtis** [US/US]; 3162 North Mountain View, San Diego, CA 92116 (US).

(74) **Agents: HOM, Raymond, B.** et al.; Townsend and Townsend and Crew LLP, 12730 High Bluff Drive, Suite 400, San Diego, CA 92130 (US).

(81) **Designated States** *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

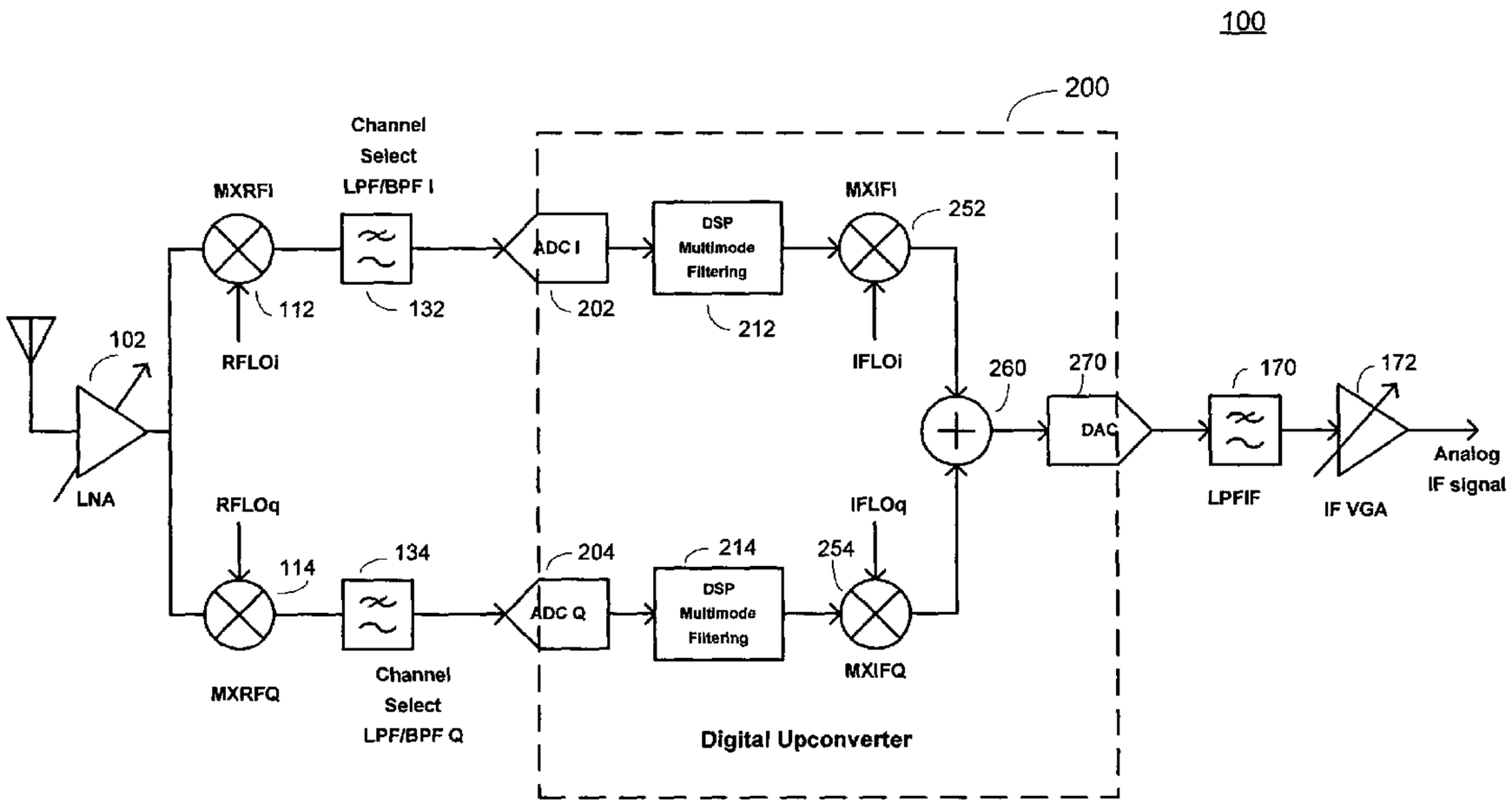
(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

(88) **Date of publication of the international search report:**
6 July 2006

[Continued on next page]

(54) **Title:** A RECEIVER ARCHITECTURE WITH DIGITALLY GENERATED INTERMEDIATE FREQUENCY



(57) **Abstract:** A receiver can be configured to include an RF front end that is configured to downconvert a received signal to a baseband signal or a low Intermediate Frequency (IF) signal. The receiver can downconvert the desired signal from an RF frequency in the presence of numerous interference sources to a baseband or low IF signal for filtering and channel selection. The filtered baseband or low IF signal can be converted to a digital representation. The digital representation of the signal can be upconverted in the digital domain to a programmable IF frequency. The digital IF signal can be converted to an analog IF signal that can be processed by legacy hardware.

WO 2006/044372 A3

WO 2006/044372 A3

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

A RECEIVER ARCHITECTURE WITH DIGITALLY GENERATED INTERMEDIATE FREQUENCY

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 60/618,240, filed October 12, 2004, entitled A RECEIVER ARCHITECTURE WITH DIGITALLY GENERATED INTERMEDIATE FREQUENCY; which is hereby incorporated herein by reference in its entirety.

BACKGROUND

[0002] The disclosure relates to electronic signal processing. More particularly, the disclosure relates to an RF receiver and receiver architecture.

[0003] In a typical frequency division multiplex communication system, multiple transmissions can simultaneously occupy a predefined operating band. The signals within the operating band can operate according to a predetermined communication standard, and thus, can have an energy within a predictable dynamic range. The communication standard can also specify a frequency spacing between adjacent channels, and the channel bandwidth. The communication standard can also specify signal parameters, such as modulation type, information rates, out of channel performance, as well as other signal parameters.

[0004] Additionally, there can be numerous signal sources operating outside of the operating band. Unlike the signals within the operating band, the out of band signals are typically not regulated by the communication standard regulating the in band signal performance. As a result, out of band signals may have substantially greater energy relative to the in-band signals, and can operate according to different signal parameters, including modulation type, out of band performance, and other parameters.

[0005] In order to tune to a desired channel, a receiver needs to substantially eliminate the effects of undesired channels, including those known interferers occurring within known operating bands as well as unanticipated interferers.

[0006] Many receiver implementations have been developed to support the various communication standards. The trend of increasing device complexity and performance

while simultaneously reducing the physical size of electronic devices imposes tremendous constraints on ongoing development.

[0007] For example, the size of cellular and cordless telephones continues to shrink while simultaneously improving the quality of the device and adding additional functionality to the device. Similarly, radios and televisions are constantly being redesigned to provide improved features and operating modes while simultaneously decreasing physical size. Although the screen size available in television receivers continues to grow, the advancement of technologies that enable flat screens and short depths greatly reduce the volume available for electronics.

[0008] It is desirable to increase the ability of a receiver to operate in multiple modes or frequency bands without compromising received signal quality. Additionally, it is desirable for a receiver implementation to minimize size, cost, and power consumption over implementations presently available.

BRIEF SUMMARY

[0009] A receiver can be configured to include an RF front end that is configured to downconvert a received signal to a baseband signal or a low Intermediate Frequency (IF) signal. The receiver can downconvert the desired signal from an RF frequency in the presence of numerous interference sources to a baseband or low IF signal for filtering and channel selection. The filtered baseband or low IF signal can be converted to a digital representation. The digital representation of the signal can be upconverted in the digital domain to a programmable IF frequency. The digital IF signal can be converted to an analog IF signal that can be processed by legacy hardware.

[0010] The disclosure includes a receiver that includes a downconverter configured to downconvert an input signal to a signal in a first frequency band, an analog to digital converter (ADC) coupled to the downconverter and configured to digitize the signal in the first frequency band to produce a digital representation of the signal in the first frequency band, and a digital upconverter configured to upconvert the digital representation of the signal in the first frequency band to a digital representation of the signal in a second frequency band.

[0011] The disclosure includes a receiver that includes a first frequency converter configured to downconvert a received signal to an in-phase baseband signal component, a

second frequency converter configured to downconvert the received signal to a quadrature baseband signal component, a first analog filter coupled to the first frequency converter and configured to perform at least partial channel selection on the in-phase baseband signal component, a second analog filter coupled to the second frequency converter and configured to perform at least partial channel selection on the quadrature baseband signal component, a first Analog to Digital Converter (ADC) coupled to the first analog filter and configured to convert the in-phase baseband signal component to a digital in-phase baseband signal component, a second ADC coupled to the second analog filter and configured to convert the quadrature baseband signal component to a digital quadrature baseband signal component, a first digital filter coupled to the first ADC and configured to digitally filter the digital in-phase baseband signal component to generate a digitally filtered in-phase baseband signal component, a second digital filter coupled to the second ADC and configured to digitally filter the digital quadrature baseband signal component to generate a digitally filtered quadrature baseband signal component, a first digital upconverter configured to digitally upconvert the digitally filtered in-phase baseband signal component to an in-phase Intermediate Frequency (IF) signal component at a desired IF, a second digital upconverter configured to digitally upconvert the digitally filtered quadrature baseband signal component to a quadrature IF signal component at the desired IF, and a digital signal combiner configured to combine the in-phase IF signal component with the quadrature IF signal component.

[0012] The disclosure includes a method of receiving a signal that includes frequency converting an input signal to an intermediate signal in a first frequency band, digitizing the intermediate signal, and digitally converting the intermediate signal to a second frequency band.

[0013] The disclosure includes a method of calibrating a quadrature receiver. The method includes injecting a calibration tone to a signal path of a quadrature receiver, detecting an amplitude and phase imbalance of the quadrature receiver, adjusting a gain of at least one of an in-phase and a quadrature signal path based on the amplitude imbalance, and adjusting a phase of at least one of the in-phase and quadrature signal paths based on the phase imbalance.

[0014] The disclosure includes a quadrature receiver calibration apparatus, that includes a tone generator configured to generate a calibration tone, a coupler configured to couple the

calibration tone to a signal path of the quadrature receiver, a detector configured to detect an in-phase and quadrature signal component when the calibration tone is coupled to the signal path, a gain feedback module configured to adjust a gain of at least one of an in-phase signal path and a quadrature signal path, and a phase feedback module configured to adjust a phase of at least one of the in-phase signal path and the quadrature signal path.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The features, objects, and advantages of embodiments of the disclosure will become more apparent from the detailed description set forth below when taken in conjunction with the drawings, in which like elements bear like reference numerals.

[0016] Figure 1 is a simplified functional block diagram of an embodiment of a receiver in a system.

[0017] Figure 2 is simplified functional block diagram of an embodiment of a receiver.

[0018] Figure 3 is a simplified functional block diagram of an embodiment of a receiver with digital frequency conversion.

[0019] Figure 4 is a simplified functional block diagram of an embodiment of a receiver with I/Q imbalance calibration.

[0020] Figure 5 is a simplified functional block diagram of an embodiment of a receiver with I/Q imbalance calibration.

[0021] Figure 6 is a simplified flowchart of a method of receiving signals.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

[0022] A receiver architecture is disclosed where the receiver performs conversion to zero Intermediate Frequency (IF) or low IF, performs anti-aliasing and partial channel selection filtering, converts the zero- or low-IF signal to the digital domain, performs frequency conversion by digital processing (for example mixing) to an arbitrary intermediate frequency, then converts the signal back to the analog domain with a digital-to-analog converter.

[0023] This approach provides the receiver with the following key advantages: an architecture suitable for single-chip implementation; flexible channel selection and IF filtering compatible with analog and digital standards; hybrid operation allowing a choice of either a low-IF or direct conversion; flexible choice of IF; substantially perfect conversion of In-phase and Quadrature signal paths to the IF as a result of the digital implementation; the option to perform digital baseband/low-IF processing; and an analog output that can be used by a wide variety of existing demodulator processors.

[0024] The disclosed receiver is configured to select a relatively narrow-band signal (the desired "channel") from among many undesired channels ("interferers"), filter out the interferers, and convert the desired channel to an arbitrary IF compatible with existing demodulators, while introducing minimal spurious signals, distortion and noise.

[0025] The receiver is configured to perform a low-IF or zero-IF conversion, which allows relatively low-power, efficient filtering to take place at the baseband or low IF. The downconverted signal is digitized. This takes advantage of natural anti-aliasing performed by any channel selection, while enabling digital signal processing downstream.

[0026] The receiver the performs upconversion in the digital domain to a desired IF. Digital upconversion allows the process to be performed with substantially no mismatches in the I and Q path, eliminating substantially all IF feedthrough and poor complex image rejection. The resulting digital IF signal can be converted to the analog domain and filtered using an on-chip anti-aliasing filter at the IF. This allows generating an analog IF signal compatible with a range of existing demodulators.

[0027] The receiver can be implemented by joining a zero- or low-IF receiver with a digital baseband portion, a digital IF generator, and a digital implementation of a transmitter where the output signal is converted back to the analog domain. The receiver architecture is particularly advantageous because the typical desired output intermediate frequency is at a sufficiently low frequency to allow data conversion to be performed by relatively low-power, low-complexity circuits.

[0028] Figure 1 is a simplified functional block diagram of an embodiment of a receiver 100 implementing digital IF generation in a system 10. The following description describes an embodiment in which the system 10 is configured to operate as a television receiver. However, the system 10 can be any of a plurality of systems. For example, the system 10 can be a television, television receiver, set top box, or television tuner integrated within a

video recorder or some other television receiver. In other embodiments, the system 10 can be a radio receiver, wireless transceiver, telephone receiver, cellular telephone, cordless telephone, or some other communication device.

[0029] The system 10 can include a source switch 12 that can be coupled to one or more signal sources. For example, a first source input can be coupled to an antenna 2 and a second source input can be coupled to a wired source, such as a cable coupled to a cable television distributor. The source switch 12 is not limited to coupling only one type of signal to the receiver 100. For example, the source switch 12 can be coupled to a television signal source, for example, via the antenna 2, and can be coupled to a radio source, for example, via the cable 4.

[0030] The source switch 12 can be configured to couple any one of the signals from any signal source to the input of the receiver 100. The receiver 100 can be, for example, configured to selectively process television signals received from a signal source, such as analog television signals formatted according to an analog television standard, such as NTSC, PAL, SECAM, or some other analog television standard. The receiver 100 can also be configured to process digital television signals, such as digital DVB-T television signals, received from one of the signal sources.

[0031] The receiver 100 can receive the RF signal from the source switch 12 and can downconvert the signal to an output IF. The output IF from the receiver 100 can be coupled to a demodulator 50 and from the demodulator 50 to a baseband processor 60. In one embodiment, the demodulator 50 can be configured to demodulate a television signal at a predetermined IF. The demodulated television signals are communicated to a baseband processor 60 that can be configured, for example, to format the signals into video and audio signals for corresponding video and audio output devices (not shown).

[0032] The system 10 can also include a mode selection module 20 that can be configured to receive a mode selection input from an external source (not shown) that can be, for example, a user selection or user control. The mode can correspond to an operating mode of the receiver 100, and can be used to determine a particular operating band, channel spacing, channel bandwidths, and output IF frequency.

[0033] The mode select module 20 can be coupled to a channel select module 30. The channel select module 30 can be coupled to the mode select module 20 and can be configured to generate the desired local oscillator (LO) control signals. The channel select

module 30 can generate the control signals needed to tune the LO frequencies of the receiver 100 to enable reception of the desired RF signal and generation of the desired output IF. The channel select module 30 can also receive one or more input signals from an external source (not shown), such as a user interface or some other module or device that can indicate a desired channel selection.

[0034] The channel select module 30 can independently control the RF and IF LOs within the receiver 100. For example, the channel select module 30 can tune the RF LO to a frequency that is based on both a mode and a desired channel. The channel select module 30 can also be configured to control the frequency of the IF LO and may be configured to control the IF LO based only on the desired mode. In other embodiments, the channel select module 30 can be configured to tune both the RF and LO frequencies for each channel.

[0035] The channel select module 30 can also be configured to control calibration of the receiver 100. The calibration can include DC offset calibration and In-phase (I) and Quadrature (Q) signal balancing. For example, the channel select module 30 can control an RF switch within the receiver 100 and can initiate the DC offset calibration. In another embodiment, a calibration module within the receiver 100 can receive the channel select signals and the filter control signals and can initiate DC offset calibration, including controlling the RF switch and filter bandwidths during the duration of the DC offset calibration.

[0036] A filter controller 40 can also be coupled to the mode select module 20. The filter controller 40 can be configured to provide the control signals to the receiver 100 that control one or more filter bandwidths within the receiver 100. The filter controller 40 can be configured to set the filter bandwidths based on the channel selectivity required in the receiver 100, which can depend on the operating mode.

[0037] The filter controller 40 can also be in communication with the channel select module 30. The filter controller 40 can be configured to control the filters within the receiver 100 to predetermined bandwidths for a predetermined calibration duration following each channel change. For example, the filter controller 40 can be configured to tune the filters to a minimal bandwidth during DC offset calibration. Alternatively, a calibration module within the receiver 100 can be configured to control the filter bandwidths during the calibration duration.

[0038] A processor 72 and associated memory 74 can be included within the system 10 and can be configured to perform one or more functions within each of the modules. For example, the memory 74 can include one or more processor 72 usable instructions in the form of software that can, when executed by the processor 72, perform some or all of the functions of the various modules within the system 10.

[0039] Figure 2 is a simplified functional block diagram of an embodiment of a receiver 100 that can be implemented on one or more substrates of one or more integrated circuits (ICs). In some embodiments, it may be advantageous to integrate the entire receiver on a single IC. In other embodiments, it may be advantageous to integrate a portion of the receiver 100 in a first IC or on a first substrate and integrate the remainder of the receiver 100 on a second IC or second substrate. The first and second substrates can be implemented in a single package or may be implemented in distinct packages. For example, a signal path within the receiver 100 can be implemented on a first substrate and one or more local oscillators can be implemented on a second substrate and couple to the first substrate through one or more interconnects.

[0040] Although the signal interconnections shown in Figure 2 appear as single ended signal interconnects, it is generally understood that some or all of the interconnections can be implemented as differential connections. It may be advantageous to implement differential interconnections, for example, for the purposes of noise reduction.

[0041] Portions of the receiver 100 can be implemented digitally, and can be configured to operate on digital representations of the signal. The digital processing of the signals within the receiver 100, and embodiments of receivers 100 having digital portions, are described in further detail in subsequent figures. The embodiment of Figure 2 does not explicitly illustrate the digital portions to allow the description to focus on the functionality of the various blocks and modules.

[0042] The receiver 100 can include an RF amplifier 102 that is configured to receive a signal at the input to the receiver 100 and amplify it. The RF amplifier 102 can be configured to receive a signal, for example, from an interconnect to an antenna or wired connection, such as a single ended wireline, a differential wireline, a twisted pair, a coaxial cable, a transmission line, a waveguide, an optical receiver configured to receive an optical signal over an optical fiber, and the like, or some other signal medium.

[0043] The RF amplifier 102 can be configured in any of several different embodiments or combination of embodiments, depending on the application. In one embodiment, the RF amplifier 102 can be a Low Noise Amplifier (LNA). In another embodiment, the RF amplifier 102 can be a variable gain amplifier, and the gain of the RF amplifier can be selected by one or more control lines (not shown) to the receiver 100. In the embodiment where the RF amplifier 102 is a variable gain amplifier, the gain of the RF amplifier 102 can be part of a gain control loop, such as an automatic gain control (AGC) loop (not shown). The RF amplifier 102 can be configured as a single amplifier stage or can include multiple amplifier stages. Where multiple amplifier stages are used, the amplifier stages can include serial, parallel, or a combination of serial and parallel amplifier configurations.

[0044] The output of the RF amplifier 102 can be coupled to inputs of first and second frequency conversion modules, here shown as a first mixer 112 and a second mixer 114. The first and second mixers 112 and 114 are shown as mixers, but can be any type of frequency conversion device. For example, the first and second mixers 112 and 114 can be double balanced mixers, double-quadrature mixers, harmonic reject mixers, interferometers, or some other type of frequency conversion device. The first and second mixers 112 and 114 can be configured to generate in-phase (I) and quadrature (Q) frequency converted signal components. The first mixer 112 is described as part of the in-phase signal path and the second mixer 114 is described as part of the quadrature signal path for purposes of discussion.

[0045] An RF LO 120 can be configured to generate a local oscillator signal to frequency convert the received RF signal to a baseband signal or a low Intermediate Frequency (IF) signal. As used herein, the term baseband signal refers to baseband signals as well as to signals that are substantially baseband signals. A signal is substantially a baseband signal if the frequency conversion process to downconvert a signal is imperfect, for example, due to LO offset errors or differences at the transmitter or receiver and errors or differences in the RF signal relative to a specified frequency of operation. For example, an RF signal may be different from a specified operating channel due to LO frequency shifts at the transmitter or Doppler shifts. Typically, the error or difference is a fraction of the baseband signal bandwidth.

[0046] A low IF signal can refer to an IF frequency that is less than twice the baseband signal bandwidth. However, in other embodiments, low IF can refer to less than 1.5, 2.5, 3,

4, 5, 10, or some other multiple of the baseband signal bandwidth. Typically, a low IF signal refers to a signal that is at a frequency sufficiently low to allow processing of the signal without additional frequency conversions.

[0047] The receiver 100 can be configured to operate using direct conversion to baseband in some operating modes while converting to a low IF in other operating modes. For example, the receiver 100 can operate in low-IF mode for analog TV applications, and zero-IF for digital applications. Using distinct frequency conversion modes for separate operating modes may be advantageous because the receiver 100 architecture can be optimized for signal characteristics.

[0048] Analog television standards such as NTSC or PAL require less channel selection and image rejection in its low-pass filtering, but are much more sensitive to DC offset which typically are present in a zero-IF implementation. This makes an analog television receiver 100 more suited for a low-IF implementation, which may suffer from poorer channel selectivity, but which also substantially eliminates the DC offset problems associated with zero-IF.

[0049] Digital TV (e.g. DVB-T) requires greater channel selection, but is less sensitive to DC offset that may be introduced by a zero-IF architecture. This makes digital TV well-suited for a zero-IF approach, which offers better channel selectivity and no image rejection limitations, but may introduce some DC offset to the signal.

[0050] The frequency of the RF LO 120 can be programmable, and the frequency can be programmed based in part on the frequency of the desired signal. In a direct conversion frequency conversion, the output of the RF LO 120 can be substantially equal to the center frequency of a double side band input signal. In other embodiments, the RF LO 120 can be tuned to a frequency that is a multiple of the desired input frequency. In the embodiment of Figure 2, the RF LO 120 can be tuned to a frequency that is substantially four times the frequency of the desired signal.

[0051] The output of the RF LO 120 can be coupled to a first phase shifter 122 that can be configured to generate at least two distinct versions of a LO signal that are in quadrature. Because inaccuracies in the quadrature LO signals can contribute to undesired signal components in the recovered signal, it is desirable to generate accurate quadrature LO signals. In one embodiment, the first phase shifter 122 can include a phase shifted signal path and a direct signal path, where the phase shifted signal path results in a signal that is

substantially 90 degrees shifted relative to the signal from the direct signal path. In another embodiment, the first phase shifter 122 can include a polyphase filter that is configured to generate the two LO signals in quadrature. In the embodiment shown in Figure 2, the first phase shifter can be implemented within the divide by four scaler.

[0052] The in-phase LO signal can be coupled to an in-phase LO buffer amplifier 116 that amplifies the in-phase LO signal and couples it to a LO input port of the first mixer 112. Similarly, the quadrature LO signal can be coupled to a quadrature LO buffer amplifier 118 that amplifies the quadrature LO signal and couples it to a LO port of the second mixer 114.

[0053] The output of the first mixer 112 can be an in-phase baseband signal that is coupled to an in-phase filter 132. The in-phase filter 132 can be programmable filter whose bandwidth can be selected based on one or more control signals (not shown) provided to the receiver 100. The bandwidth of the in-phase filter 132 can be selected, for example, based on a communication standard or mode that the receiver 100 is configured to support. Therefore, where the receiver 100 is configured to support multiple standards having different channel bandwidths, the bandwidth of the in-phase filter 132 can be selected based in part on the presently supported mode.

[0054] When the signal is a baseband signal or a low IF signal, the in-phase filter 132 can be configured as a low pass filter. Alternatively, the in-phase filter 132 can be configured as a bandpass filter if the low IF signal has sufficient bandwidth to make the use of a low pass filter undesirable.

[0055] The output of the in-phase filter 132 can be coupled to a third mixer 152 configured to frequency convert the in-phase signal to a desired output IF. In one embodiment, the output of the in-phase filter 132 is a baseband signal and the third mixer is configured to upconvert the in-phase baseband signal to an output IF.

[0056] The third mixer 152 can be driven by a programmable LO that is generated in much the same manner that is used to generate the LO for the first and second mixers 112 and 114. A programmable IF LO 140 can be configured to generate a signal that is substantially four times the desired output IF. The IF LO 140 can be programmable to allow the output IF to be selected based in part on the mode supported by the receiver 100. For example, the receiver 100 can be configured to frequency convert the input signals to a predetermined IF that can depend on the manner in which the user configures the system having the receiver 100. For example, a set top box for television signals can be configured

to generate an output signal at a predetermined IF, such as 70 MHz, or at a frequency corresponding to a television channel.

[0057] The output of the IF LO 140 can be coupled to a second phase shifter 142 that can be implemented in a divide by four circuit. An in-phase LO output from the second phase shifter 142 can be coupled to an in-phase buffer amplifier 156 that amplifies the in-phase LO signal and couples it to the LO input of the third mixer 152. The output of the third mixer 152 is an in-phase IF signal that is coupled to a first input of a signal combiner 160.

[0058] The quadrature signal path is configured to be substantially identical to the in-phase signal path. The two signal paths are typically substantially matched to reduce undesirable signal components that can be generated due to I and Q mismatches.

[0059] The output of the second mixer 114 can be a baseband quadrature signal that is coupled to an input of a quadrature filter 134. The quadrature filter 134 can be configured as a programmable low pass filter having programmable bandwidth. Typically, the configuration and bandwidths of the in-phase and quadrature filters 132 and 134 are the same such that the in-phase and quadrature signal paths remain substantially matched.

[0060] The output of the quadrature filter 134 can be coupled to an input of a fourth mixer 154 that is configured to upconvert the quadrature signal to the output IF. The fourth mixer 154 is driven by an LO signal that is generated by the IF LO 140. The output of the IF LO 140 is coupled to a second phase shifter 142 that generates a quadrature LO signal. The quadrature LO signal is coupled to a quadrature buffer amplifier 158 which amplifies the quadrature LO signal and couples it to an LO input of the fourth mixer 154. The output of the fourth mixer 154 can be a quadrature IF signal. The quadrature IF signal can be coupled to a second input of the signal combiner 160.

[0061] The signal combiner 160 can be configured to combine the in-phase and quadrature IF signals. The signal combiner 160 can be, for example, a signal summer that sums the in-phase IF signal with the quadrature IF signal. In one embodiment, the signal combiner 160 sums the two signals maintaining their phases. In another embodiment, the signal combiner 160 can invert one of the phases and sum the two signals. In yet another embodiment, the signal combiner 160 can generate the sum of the two signals and can invert the output signal.

[0062] The output of the signal combiner 160 represents the output IF signal. The output IF signal can be coupled to an output filter 170 that can be, for example, a low pass filter or bandpass filter that is configured to remove undesired signal products from the IF output signal. The output filter 170 can be configured as a fixed bandwidth filter or can be configured as a programmable bandwidth filter, where the bandwidth is determine, in part, based on a mode of the receiver 100.

[0063] The output of the output filter 170 can be coupled to an IF amplifier 172 that can be configured to amplify the output. The IF amplifier 172 can be a variable gain amplifier. The gain of the IF amplifier 172 can be controlled using one or more control inputs (not shown) on the receiver 100. The output of the IF amplifier 172 can be the output of the receiver 100.

[0064] The receiver 100 can also include a DC offset cancellation module 180 configured to substantially remove the DC component on each of the in-phase and quadrature signal paths. DC signals at the inputs to the third and fourth mixers 152 and 154 result in the generation of LO signals at the outputs of the respective third and fourth mixers 152 and 154. Because the LO signal can represent an undesired signal, the receiver 100 can incorporate a DC offset cancellation module 180 that monitors the DC offset and compensates for it to substantially remove it from both the in-phase and quadrature signal paths prior to upconversion to the output IF.

[0065] The receiver 100 can also include an I/Q calibration module 184. The receiver 100 can reduce the contribution due to undesired signals if the in-phase (I) and quadrature (Q) signal paths can be balanced. The I/Q calibration module 184 can reduce or substantially eliminate gain differences in the I and Q signal paths and can ensure that the I and Q signal paths are substantially in quadrature.

[0066] The I/Q calibration module 184 can be coupled to one or more gain stages in each of the I and Q signal paths. In the embodiment shown in Figure 2, the I/Q calibration module 184 is coupled to the filters 132 and 134 in the I and Q signal paths. The I/Q calibration module 184 can be configured to adjust the gain through one or more of the filters in order to balance the gains of the I and Q signal paths. Additionally, the I/Q calibration module 184 can be configured to adjust the phase offset contributed by the first phase shifter 122 in order to maintain the quadrature nature of the two signal paths.

[0067] It may be advantageous to implement the entire receiver 100 on a single integrated circuit, such that the processes and conditions used to manufacture the in-phase and quadrature signal components are closely matched, resulting in more closely matched I and Q signal paths. Additionally, it may be advantageous to implement the components on a single IC to minimize path length distances or variations that contribute to mismatches. A single IC implementation can also result in a smaller receiver 100 package.

[0068] Figure 3 is a simplified functional block diagram of a receiver 100 implementing a digital IF generation module 200. The receiver 100 implements some of the functionality in analog domain and other functionality in the digital domain in order to capitalize on various advantages of the respective domains. The functional block diagram of Figure 3 omits some blocks for the sake of clarity. For example, the RF and IF LOs and their respective phase shifters are not illustrated, nor are the DC offset and I/Q calibration modules illustrated.

[0069] The RF portion of the receiver 100 embodiment of Figure 3 is configured similar to that shown and described in Figure 2. An RF amplifier 102, here depicted as a variable gain LNA, is configured to receive an input signal at a desired RF frequency. The input signal can be within an operating band of possible input signals and undesired channels within the operating band may appear as interference sources.

[0070] The output of the RF amplifier 102 is coupled to first and second mixers, 112 and 114, configured to downconvert I and Q signal components, respectively, to I and Q baseband or low IF signals. The output of the first mixer 112 represents the I baseband or low IF signal. The signal is coupled to a the in-phase filter 132. The in-phase filter 132 can be configured to provide at least partial channel selection. The in-phase filter 132 can be configured to provide at least a portion of the desired channel selectivity. A remaining portion of channel selection can be implemented in the digital domain, as will be described below. The in-phase filter 132 can also operate as an anti-aliasing filter to substantially suppress aliased components after digitizing the signal.

[0071] Similarly, the output of the second mixer 114 represents the quadrature signal. The quadrature signal is coupled to the quadrature filter 134 for partial channel selection and anti-alias filtering. The shape of the in-phase and quadrature filters 132 and 134 can be determined, in part, by the amount of channel selection performed by subsequent digital

filters. Additionally, the shape of the anti-aliasing filter response can be determined in part by the sampling rate of the subsequent digitizing operation.

[0072] The output of the in-phase and quadrature filters, 132 and 134, is coupled to a digital IF generator 200 configured to digitally filter and upconvert the I and Q signals to a selectable IF. The digital IF generator 200 can also be configured to convert the digital IF signal to an analog signal representation. The digital IF generator 200 can thus be configured to accept analog I and Q signal inputs, digitally filter and upconvert the signals and combine them into a composite digital IF signal, and convert the digital IF signal to an analog IF signal. A module that interfaces with the digital IF generator 200 can be completely unaware of the digital processing performed by the digital IF generator 200.

[0073] The digital IF generator 200 includes a first Analog to Digital Converter (ADC) 202 configured to receive the downconverted in-phase signal and convert it to a digital representation. The digitized in-phase signal can be coupled to a first digital filter 212. The first digital filter 212 can be configured to perform channel selection on the digitized in-phase signal. In one embodiment, the first digital filter 212 can be configured to provide the desired channel selectivity response. In another embodiment, the first digital filter 212 can be configured to have a frequency response that operates in conjunction with the in-phase filter 132 to produce the desired channel selectivity.

[0074] The output of the first digital filter 212 can be coupled to a first digital frequency converter 252 configured to frequency convert the filtered in-phase digital signal to an in-phase digital IF. The output of the first digital frequency converter 252 is coupled to a first input of a digital signal combiner 260.

[0075] The digital IF generator 200 includes a quadrature signal path that is complementary to the in-phase signal path. A second ADC 204 is configured to accept the quadrature signal from the quadrature filter 134. The second ADC 204 converts the quadrature signal to a digital representation and couples the digital quadrature signal to a second digital filter 214.

[0076] The second digital filter 214 filters the digital quadrature signal to provide the desired channel selectivity. The filtered digital quadrature signal is coupled to a second digital frequency converter 254 configured to frequency convert the filtered quadrature digital signal to a quadrature digital IF signal. The output of the second digital frequency converter 254 is coupled to a second input of the digital signal combiner 260.

[0077] The first and second digital filters 212 and 214 can be configured with fixed bandwidths or can be configured to have controllable bandwidths and frequency responses. IN one embodiment, the bandwidths and frequency responses of the first and second digital filters 212 and 214 are substantially the same. In another embodiment, the first and second digital filters 212 and 214 can have distinct bandwidths and frequency responses. In some embodiments, the bandwidth and frequency response can be based in part on an operating mode of the receiver 100. For example, the first and second digital filters 212 and 214 can be configured with a first response if the receiver 100 is configured to process analog NTSC video signals. The first and second digital filters 212 and 214 can be configured with a second response if the receiver 100 is configured to process DVB-T signals. The filter responses can be selectively programmable to any of a plurality of predetermined frequency responses.

[0078] In one embodiment, each of the first and second digital filter 212 and 214 can be implemented as a digital signal processor (DSP) configured to provide a filter response based on one or more filter coefficients stored in a memory (not shown). The first and second digital filters 212 and 214 can be configured to store filter coefficients for a plurality of filter responses, and the DSP can be configured to select a coefficient set based, for example, on a mode or channel configuration.

[0079] The first and second digital frequency converters, 252 and 254, can be configured to perform frequency conversion according to any one of various frequency conversion techniques. For example, the first and second digital frequency converters, 252 and 254, can be configured as mixers, multipliers, rotators, or some other frequency converter.

[0080] The digital signal combiner 260 can be configured as a signal summer. Additionally, the digital signal combiner 260 can be configured to invert one or both of the digital IF signal components. The digital signal combiner 260 couples the combined, composite digital IF signal to a digital to analog converter (DAC) 270 configured to convert the digital IF signal to an analog IF signal. The analog IF signal represents the output of the digital IF generator 200.

[0081] The analog IF signal is coupled to an output filter 170 and an IF amplifier 172. The output filter 170 can be configured to remove any undesired frequency conversion products and any undesired signal components generated by the DAC 270.

[0082] Figure 4 is a simplified functional block diagram of an embodiment of a receiver 100 with digital IF generation and I/Q imbalance calibration. The receiver 100 includes a receive signal portion 400 that is configured to receive an input signal and convert it to a digital IF. An I/Q detector 460 is coupled to the output of the receive signal portion 400 and is configured to determine the relative phase and amplitude of the I and Q signal components during a calibration period. One or more feedback loops can operate to correct the amplitude and phase balance of the I and Q signal paths in order to compensate for any path mismatches or imbalances.

[0083] The receiver 100 is configured to have a signal processing mode and a calibration mode. The operation of the receiver 100 during signal processing mode is essentially the same as the receiver embodiment shown in Figure 3.

[0084] An input RF signal is coupled to the RF amplifier 102 at the input of the receive signal portion 400 of the receiver 100. The output of the RF amplifier 102 is coupled to a first multiplexer 410 that is configured to select the RF amplifier 102 output during signal processing mode. The first multiplexer 410 couples the RF amplifier 102 output to first and second mixers 112 and 114 to frequency convert the signal to I and Q baseband or low IF signal components.

[0085] An RF LO 420 having a LO generator 422 and phase shifter 424 is configured to drive the first and second mixers 112 and 114 with in-phase and quadrature LO signals, respectively. The RF LO 420 can be implemented on the same IC as the receive signal portion 400 or can be configured as a distinct module. The downconverted I and Q signals are filtered in I and Q filters 132 and 134, respectively, before being digitally converted and digitally upconverted to the desired IF.

[0086] The I signal is digitally converted using a first ADC 202 while the Q signal is digitally converted in a second ADC 204. The digital I signal is upconverted to a digital in-phase IF signal using a first digital frequency converter 252. The digital Q signal is upconverted to a digital quadrature signal using a second frequency converter 254. A second LO 440 including an LO generator 442 and phase shifter 444 is used to provide the quadrature LO signals to first and second amplifiers 452 and 454 that drive the digital frequency converters 252 and 254. The second LO 440 can be implemented on the same IC or on a module or substrate distinct from the receive signal portion 400.

[0087] The digital I and Q IF signal components are coupled to the inputs of a digital signal combiner 260 where they are combined into a composite digital IF output signal. The receive signal portion 400 of the receiver 100 is depicted as providing a digital IF output signal. However, the receiver 100 can include a DAC at the output if an analog IF signal is desired.

[0088] The receiver 100 can be configured to self calibrate in order to compensate for any imbalances in the I and Q signal paths. The receiver 100 can be configured to include an I/Q detector 460 couple to one or more feedback loops configured to provide correction signals to compensate for gain and phase imbalances in the I and Q signal paths.

[0089] The receiver 100 can perform the calibration process at distinct intervals, such as power up, channel selection, or mode selection. In another embodiment, the receiver 100 can be configured to perform calibration on a periodic basis.

[0090] During calibration, a calibration tone can be injected into the front end of the receive signal portion 400. In the embodiment shown in Figure 4, the I and Q outputs of the first LO 420 are coupled to a tone multiplexer 426. The tone multiplexer 426 is configured to select between the I and Q LO signals and couple the selected tone to a tone amplifier 412 that drives an input of the first multiplexer 410. The first multiplexer 410 is configured to select the tone input during calibration mode.

[0091] Because the tone injected into the front end of the receive signal portion is generated by the same first LO 420 that is used to generate the local oscillator signals used in the first frequency conversion, the tone and LO signals are coherent and may differ by only a phase offset. The phase offset can be substantially minimized by minimizing the path differences experienced by the LO signals, or by introducing phase delays in one or more of the LO paths to equalize the paths.

[0092] Thus, during the calibration process, the tone multiplexer 426 can be configured to selectively alternate between the in-phase and quadrature LO signals to selectively introduce in-phase and quadrature signals to the receiver 100 front end. The signal in the receive signal portion 400 will be substantially an in-phase signal component during the portion of time that the tone multiplexer selects the in-phase LO signal. Similarly, the signal in the receive signal portion 400 will be substantially a quadrature signal component during the portion of time that the tone multiplexer selects the quadrature LO signal.

[0093] When the tone multiplexer 426 selects the in-phase tone, there is substantially no quadrature signal present in the receive signal portion 400. The output of the first and second mixers 112 and 114 are DC signals representative of the phase and amplitude imbalances in the front end portion of the receiver 100. The output from the digital signal combiner 260 is substantially a signal representative of the phase and amplitude contribution introduced by the complete I and Q signal processing path.

[0094] The output of the digital signal combiner 260 is coupled to an input of an I/Q detector 460. The I/Q detector 460 includes an in-phase mixer 462 and a quadrature mixer 464 that each have one input coupled to the digital signal combiner 260 output. The LO port of the in-phase mixer 462 is driven by the in-phase LO signal from the second LO 440. The LO port of the quadrature mixer 464 is driven by the quadrature LO signal from the second LO 440. The outputs of the in-phase mixer 462 and quadrature mixer 464 are coupled to inputs of a signal combiner 466. Therefore, the I/Q detector 460 is configured to generate a DC value representative of the composite DC offset from the receiver 400. The composite DC offset is representative of the phase and amplitude imbalance of the receiver 100.

[0095] The output of the I/Q detector 460 is coupled to one or more feedback loops. For example, a first feedback lop can be configured to compensate for amplitude imbalance while a second feedback loop can be configured to compensate for phase imbalance. The output of the I/Q detector 460 is typically a DC error signal. The DC error signal is coupled to a calibration loop filter 470 that can be used to adjust the rate that the feedback loop adjusts the imbalances.

[0096] The output of the calibration loop filter 470 can be coupled to an amplifier 472 that can be used to amplify the error signal. In one embodiment, the amplifier 472 can be implemented as a comparator that is configured to toggle between two values depending on whether the DC offset is greater or less than a predetermined threshold, such as zero volts. The amplified error signal is coupled to a search module 474, such as a binary search module, that can be configured to determine a feedback value based on a search.

[0097] The search module 474 can be configured, for example, to perform a binary search to determine a DC correction value. A binary search uses the amplifier 472 or comparator output to determine if the next increment is to a greater value or a lesser value. The binary search can continue until the search converges on a value. For example, if the search

module 474 is configured to provide a 10-bit digital output, the binary search can converge in typically 11 or fewer iterations.

[0098] The output of the search module 474 is coupled to a multiplexer 476 that is configured to provide the correction value to either a gain feedback path or a phase feedback path. The gain feedback path includes a DAC 482 coupled to control the gain of the first and second amplifiers, 452 and 454, that drive the digital frequency converters 252 and 254. The phase feedback path includes a DAC 484 coupled to the digital frequency converters 252 and 254 to compensate for phase imbalances.

[0099] In one embodiment, the receiver 100 can initiate a calibration mode in which the tone multiplexer 426 selects the in-phase signal and couples the in-phase signal to the receiver 100 front end. The I/Q detector operates on the signal and causes the gain and phase feedback loops to converge upon values that are applied to the corresponding amplifier 452 and digital frequency converter 252. The tone multiplexer 426 can then be configured to select the quadrature LO signal and the process can be repeated for the quadrature amplifier 454 and frequency converter 254.

[0100] Figure 5 is a simplified functional block diagram of an embodiment of a receiver 100 having digital IF generation and I/Q imbalance calibration. The receiver 100 of Figure 5 is similar to the receiver shown in Figure 4, except that the I/Q imbalance is performed using digital signal processing I/Q calibration modules 512 and 514 positioned in series with the I and Q signal paths.

[0101] The receiver 100 is configured to have at least two operating modes including a signal processing mode and a calibration mode. The receiver 100 operation in the signal processing mode is substantially the same as that described for the receiver embodiments of Figures 3 and 4. The embodiment of Figure 5 includes an output DAC 270 and also explicitly depicts the second LO 442 and phase shifter 444 as implemented in common with the signal processing path of the receiver 100.

[0102] As was the case with the embodiment shown in Figure 4, the embodiment of Figure 5 includes a first multiplexer 410 configured to select between an RF amplifier 102 output or a tone used during calibration mode. During signal processing mode, the I/Q calibration modules 512 and 514 correct the respective I and Q signal components by gain and phase compensation values determined during the calibration mode.

[0103] During calibration mode, the I or Q calibration tone is coupled to the front end of the receiver 100. The first I/Q calibration module 512 is configured to monitor the digital I and Q signal components and is configured to adjust the gain and phase offset applied to the in-phase signal component. Similarly, the second I/Q calibration module 514 is configured to monitor the digital I and Q signal components and is configured to adjust the gain and phase offset applied to the quadrature signal component.

[0104] Figure 6 is a simplified flowchart of a method 600 of receiving a signal, such as a television signal that can be an analog television signal or a digital television signal depending on an operating mode. The method 600 can be performed by any of the receivers shown in Figures 1-5. Of course, the method 600 is not limited to processing of television signals.

[0105] The method 600 begins at block 610 where the receiver is provided a mode select control signal. The mode select signal may indicate the type of signal that is to be received, the signal source, an operating frequency range, and the like, or some combination of operating parameters. In one embodiment, the mode selection can indicate whether an analog signal, such as an NTSC television signal, or a digital signal, such as a DVB-T signal, is to be processed. The receiver can configure filters and amplifier gains based on the mode selection.

[0106] The receiver proceeds to block 620 and receives channel selection information. The receiver can be configured, for example, to receive an indication of an operating frequency band and a frequency of a desired channel or a designator of a desired channel.

[0107] The receiver proceeds to block 630 and configures the local oscillator frequencies based on the mode and channel selection information. For example, the receiver can be configured to implement downconversion to a low IF when an NTSC signal is to be received, and may be configured to implement direct downconversion to a zero-IF or baseband if a digital signal is to be received. The receiver may also configure the frequency of the second LO used for upconversion to the desired IF based on the operating mode.

[0108] After configuring the local oscillator frequencies, the receiver proceeds to block 640 and performs I/Q calibration, if I/Q calibration is incorporated into the receiver. The receiver can, for example, decouple the input signal from the receiver and introduce one or more calibration tones and correct for any I/Q imbalance based on the calibration tones.

[0109] After performing I/Q calibration, the receiver can proceed to block 650 and quadrature downconvert the desired channel to either a baseband signal or a low IF signal, depending on the mode selection. The receiver may also perform partial channel selection in order to remove some interferers and to provide anti-aliasing filtering. The receiver proceeds to block 660 and digitizes the downconverted I and Q signals.

[0110] The receiver proceeds to block 670 and digital filters the I and Q signals. The receiver can be configured to perform channel selection in the digital domain using a digital filter selected from a plurality of digital filter responses based on the mode selection.

[0111] The receiver proceeds to block 680 and digitally upconverts the I and Q signals to the desired IF. The receiver can be configured to generate a LO signal and perform the frequency conversion completely in the digital domain. As such, the balance and relationship of the I and Q signals may be tightly controlled. The receiver can combine the digital I and Q IF signal components to generate a composite digital IF signal.

[0112] The receiver can then proceed to block 690 and convert the digital IF signal to an analog IF signal for processing and demodulation. The receiver can thus interface with legacy processing devices while incorporating digital IF generation.

[0113] A receiver and method of receiving signals are described. A receiver can selectively convert a desired RF channel to a low IF or a baseband signal using a direct conversion architecture. The receiver can be configured to downconvert the desired channel to I and Q signal components. The receiver can perform partial channel selection on the downconverted I and Q signals. The receiver can digitize the filtered I and Q signals and can digitally filter each of the digitized I and Q signals to perform channel selection.

[0114] The receiver can digitally upconvert the I and Q signals to an IF. The receiver can combine the digital I and Q IF signals to generate a composite digital IF signal. The receiver can convert the digital IF signal to an analog IF signal.

[0115] The receiver may implement one or more modules that can be configured to calibrate the receiver signal paths to substantially remove any I and Q imbalance in the signal paths. The modules can include feedback modules or can be implemented as digital signal processing modules placed in series with the I and Q signal paths.

[0116] The receiver can be implemented on a single IC. Such an implementation allows the various elements to be better matched than is generally possible using discrete elements

or multiple ICs. The ability to closely match the elements of the receiver can reduce the level of DC offset error attributable to element mismatches.

[0117] The steps of a method, process, or algorithm described in connection with the embodiments disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. The various steps or acts in a method or process may be performed in the order shown, or may be performed in another order. Additionally, one or more process or method steps may be omitted or one or more process or method steps may be added to the methods and processes. An additional step, block, or action may be added in the beginning, end, or intervening existing elements of the methods and processes.

[0118] The above description of the disclosed embodiments is provided to enable any person of ordinary skill in the art to make or use the disclosure. Various modifications to these embodiments will be readily apparent to those of ordinary skill in the art, and the generic principles defined herein may be applied to other embodiments without departing from the spirit or scope of the disclosure. Thus, the disclosure is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

WHAT IS CLAIMED IS:

1. A receiver comprising:

a downconverter configured to downconvert an input signal to a signal in a first frequency band;

an analog to digital converter (ADC) coupled to the downconverter and configured to digitize the signal in the first frequency band to produce a digital representation of the signal in the first frequency band; and

a digital upconverter configured to upconvert the digital representation of the signal in the first frequency band to a digital representation of the signal in a second frequency band.

2. The receiver of Claim 1, wherein the first frequency band comprises one of a baseband frequency band or a low Intermediate Frequency (IF) band based on a mode of the receiver.

3. The receiver of Claim 1, wherein the downconverter comprises:

an in-phase downconverter configured to downconvert an in-phase component of the input signal to the first frequency band; and

a quadrature downconverter configured to downconvert a quadrature component of the input signal to the first frequency band.

4. The receiver of Claim 1, wherein the downconverter comprises:

an in-phase downconverter configured to downconvert an in-phase component of the input signal to substantially a baseband in-phase signal; and

a quadrature downconverter configured to downconvert a quadrature component of the input signal to substantially a baseband quadrature signal.

5. The receiver of Claim 1, wherein the downconverter comprises:

an in-phase downconverter configured to downconvert an in-phase component of the input signal to a in-phase low Intermediate Frequency (IF) signal; and

a quadrature downconverter configured to downconvert a quadrature component of the input signal to a quadrature low IF signal.

6. The receiver of Claim 1, further comprising a filter configured to perform at least partial channel selection of the signal in the first frequency band prior to the ADC.

7. The receiver of Claim 1, further comprising a digital filter configured to perform channel selection of the digital representation of the signal in the first frequency band.

8. The receiver of Claim 1, wherein the digital upconverter comprises:

a first digital upconverter configured to digitally upconvert an in-phase component of the input signal to an in-phase digital signal at a desired Intermediate Frequency (IF); and

a second digital upconverter configured to digitally upconvert a quadrature component of the input signal to a quadrature digital signal at the desired IF.

9. The receiver of Claim 8, further comprising a digital signal combiner configured to combine the in-phase digital signal at the desired IF with the quadrature digital signal at the desired IF.

10. A receiver comprising:

a first frequency converter configured to downconvert a received signal to an in-phase baseband signal component;

a second frequency converter configured to downconvert the received signal to a quadrature baseband signal component;

a first analog filter coupled to the first frequency converter and configured to perform at least partial channel selection on the in-phase baseband signal component;

a second analog filter coupled to the second frequency converter and configured to perform at least partial channel selection on the quadrature baseband signal component;

a first Analog to Digital Converter (ADC) coupled to the first analog filter and configured to convert the in-phase baseband signal component to a digital in-phase baseband signal component;

a second ADC coupled to the second analog filter and configured to convert the quadrature baseband signal component to a digital quadrature baseband signal component;

a first digital filter coupled to the first ADC and configured to digitally filter the digital in-phase baseband signal component to generate a digitally filtered in-phase baseband signal component;

a second digital filter coupled to the second ADC and configured to digitally filter the digital quadrature baseband signal component to generate a digitally filtered quadrature baseband signal component;

a first digital upconverter configured to digitally upconvert the digitally filtered in-phase baseband signal component to an in-phase Intermediate Frequency (IF) signal component at a desired IF;

a second digital upconverter configured to digitally upconvert the digitally filtered quadrature baseband signal component to a quadrature IF signal component at the desired IF; and

a digital signal combiner configured to combine the in-phase IF signal component with the quadrature IF signal component.

11. A method of receiving a signal, the method comprising:

frequency converting an input signal to an intermediate signal in a first frequency band;

digitizing the intermediate signal; and

digitally converting the intermediate signal to a second frequency band.

12. The method of Claim 11, wherein frequency converting the input signal comprises:

downconverting the input signal to an in-phase baseband signal component; and

downconverting the input signal to a quadrature baseband signal component.

13. The method of Claim 11, wherein the intermediate signal comprises:

an in-phase baseband signal component; and

a quadrature baseband signal component.

14. The method of Claim 11, further comprising performing partial channel selection on the intermediate signal.

15. The method of Claim 11, wherein digitizing the intermediate signal comprises:

digitizing an in-phase signal component of the intermediate signal; and

digitizing a quadrature signal component of the intermediate signal.

16. The method of Claim 11, wherein digitally converting the intermediate signal comprises:

digitally upconverting an in-phase signal component of the intermediate signal to an in-phase Intermediate Frequency (IF) component at a desired IF;

digitally upconverting a quadrature signal component of the intermediate signal to a quadrature IF component at the desired IF; and

combining the in-phase IF component with the quadrature IF component.

17. A method of calibrating a quadrature receiver, the method comprising:

injecting a calibration tone to a signal path of a quadrature receiver;

detecting an amplitude and phase imbalance of the quadrature receiver;

adjusting a gain of at least one of an in-phase and a quadrature signal path based on the amplitude imbalance; and

adjusting a phase of at least one of the in-phase and quadrature signal paths based on the phase imbalance.

18. The method of Claim 17, wherein injecting the calibration tone comprises injecting one of a quadrature or an in-phase Local Oscillator (LO) signal to the signal path.

19. The method of Claim 18, wherein the one of the quadrature or in-phase LO signal is synchronized with a LO signal used to downconvert the calibration tone to a DC signal.

20. The method of Claim 17, wherein detecting the amplitude and phase imbalance of the quadrature receiver comprises:

downconverting an in-phase Intermediate Frequency (IF) signal component to a first DC signal;

downconverting a quadrature IF signal component to a second DC signal;

combining the first and second DC signals to generate a combined DC signal; and

determining the phase imbalance based on the combined DC signal.

21. A quadrature receiver calibration apparatus, the apparatus comprising:

a tone generator configured to generate a calibration tone;

a coupler configured to couple the calibration tone to a signal path of the quadrature receiver;

a detector configured to detect an in-phase and quadrature signal component when the calibration tone is coupled to the signal path;

a gain feedback module configured to adjust a gain of at least one of an in-phase signal path and a quadrature signal path; and

a phase feedback module configured to adjust a phase of at least one of the in-phase signal path and the quadrature signal path.

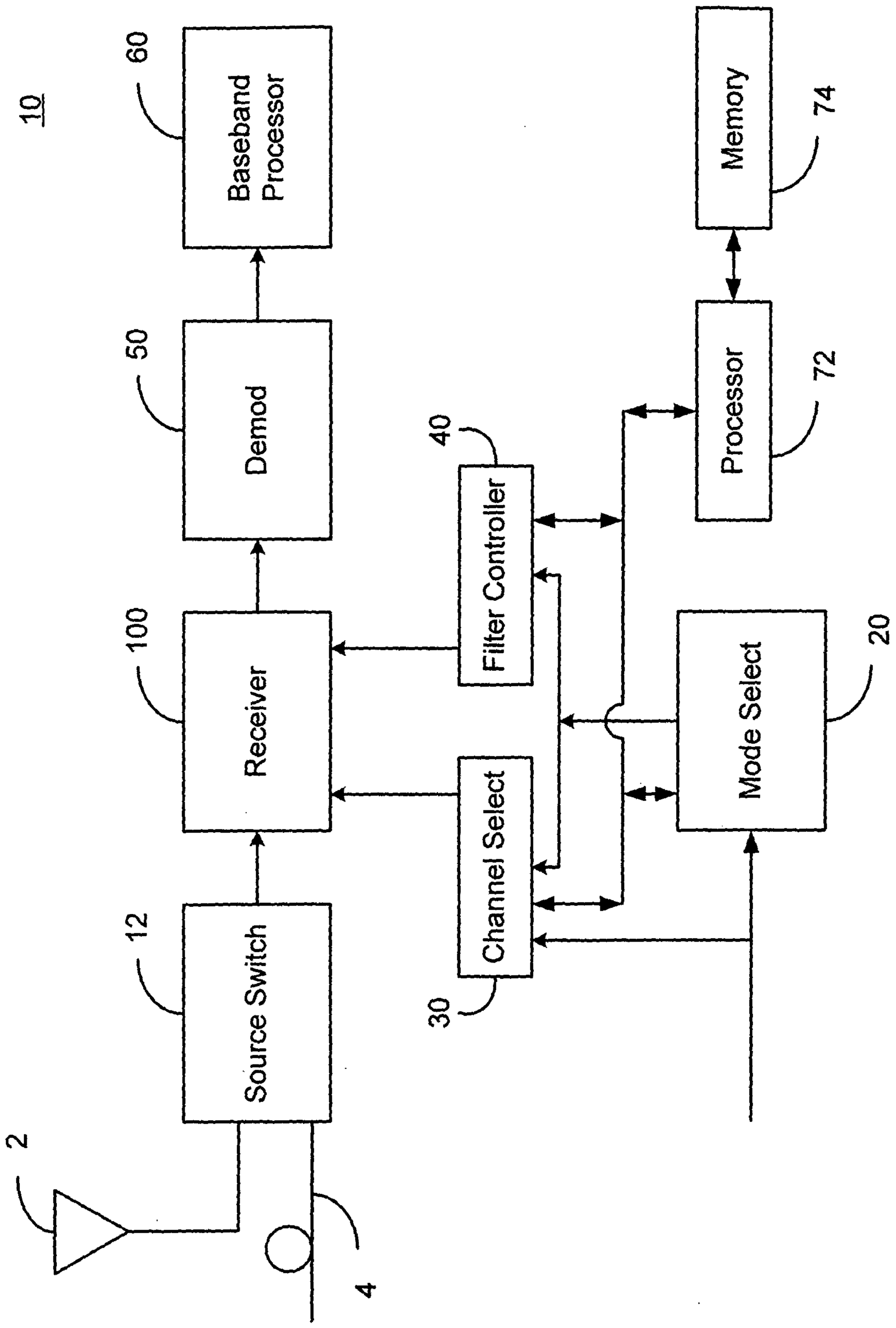

10
60
Baseband Processor
50
Demod
100
Receiver
12
Source Switch
2
4
40
Filter Controller
30
Channel Select
Memory
74
Processor
72
Mode Select
20

FIG. 1

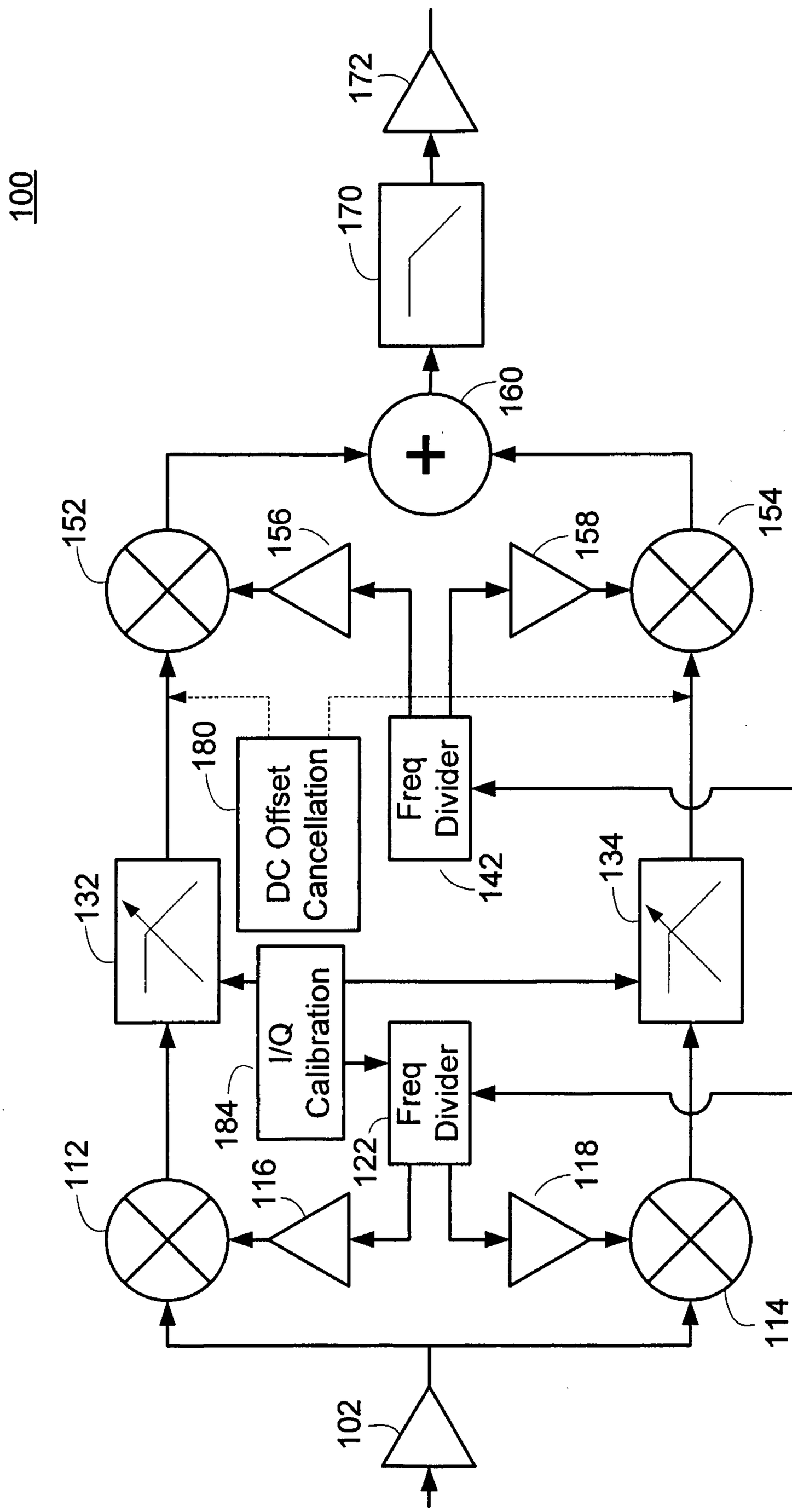

100
102
112
114
116
118
120
122
132
134
140
142
152
154
156
158
160
170
172
180
184
DC Offset Cancellation
Freq Divider
I/Q Calibration

FIG. 2

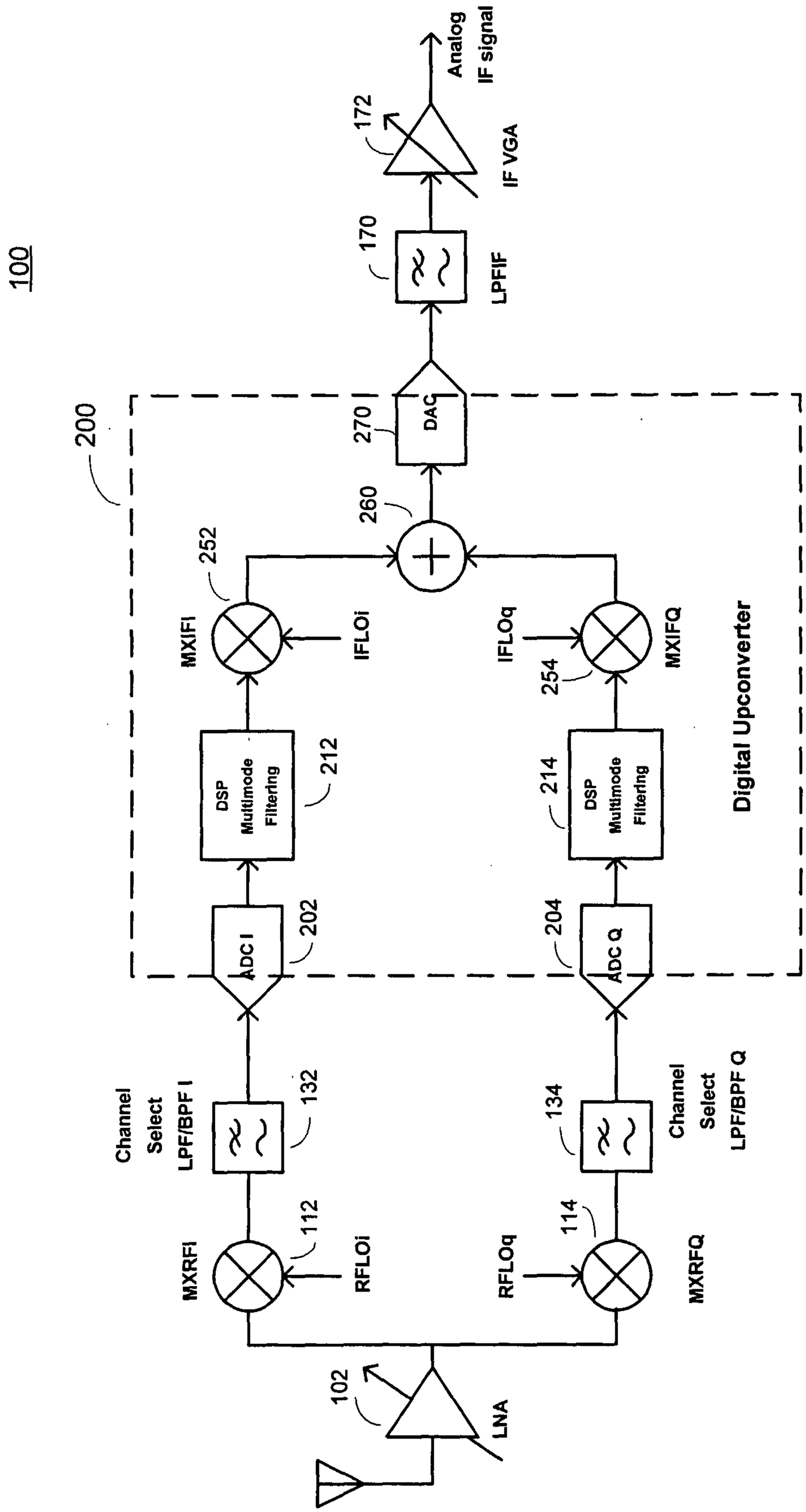

100
200
Analog IF signal
172
IF VGA
170
LPFIF
270
DAC
260
252
MXIFI
IFLOi
IFLOq
254
MXIFQ
Digital Upconverter
DSP Multimode Filtering
212
214
DSP Multimode Filtering
ADC I
202
ADC Q
204
Channel Select LPF/BPF I
132
Channel Select LPF/BPF Q
134
112
MXRFI
RFLOi
RFLOq
114
MXRFQ
102
LNA

FIG. 3

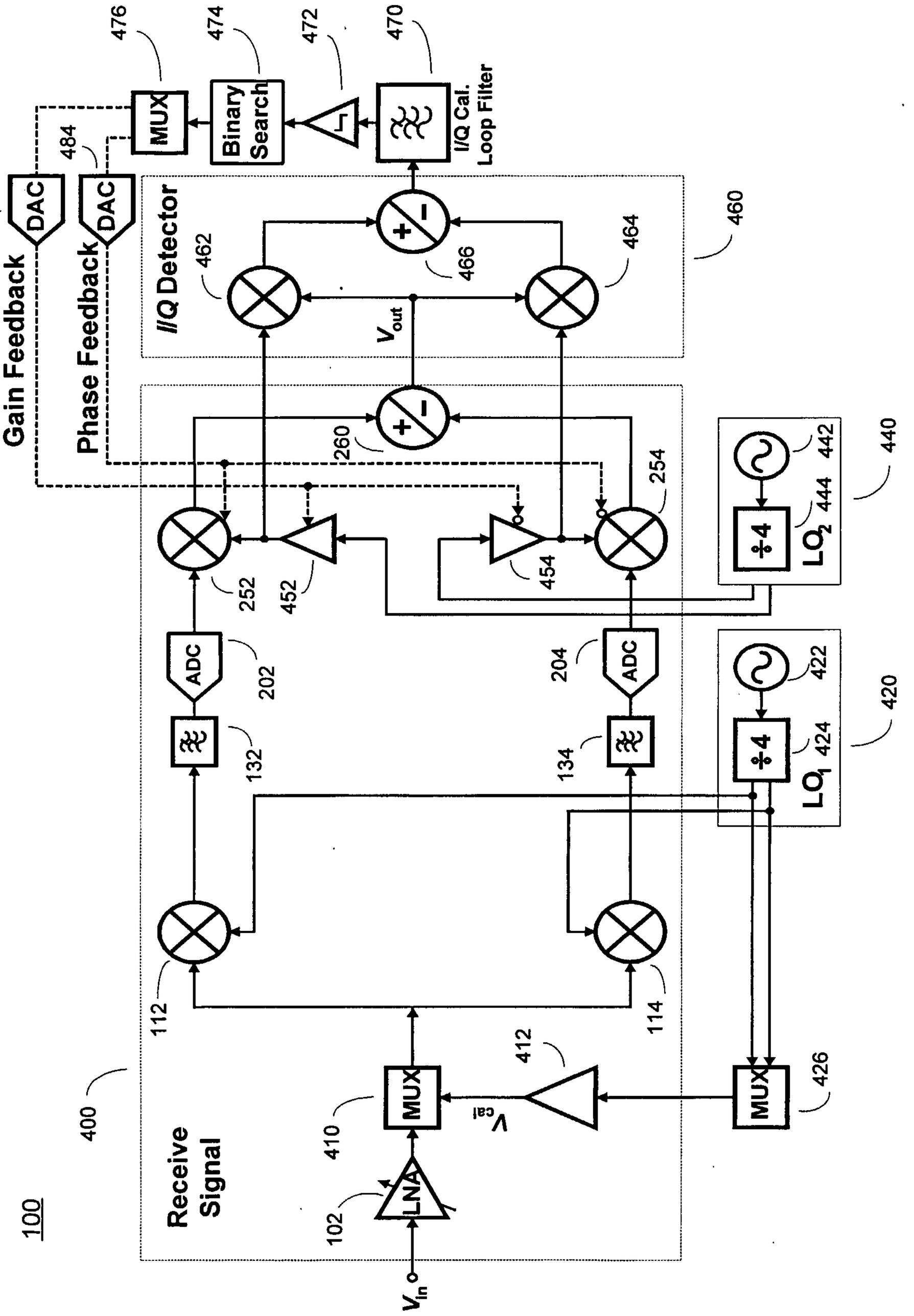

100
400
Receive Signal
102
LNA
410
MUX
V_{cal}
412
V_{in}
112
114
252
254
260
452
454
460
I/Q Detector
462
464
466
V_{out}
470
I/Q Cal. Loop Filter
472
Binary Search
474
MUX
476
482
Gain Feedback
DAC
484
Phase Feedback
DAC
132
134
202
204
ADC
ADC
420
LO_1
422
÷4
424
440
LO_2
442
÷4
444
426
MUX

FIG. 4

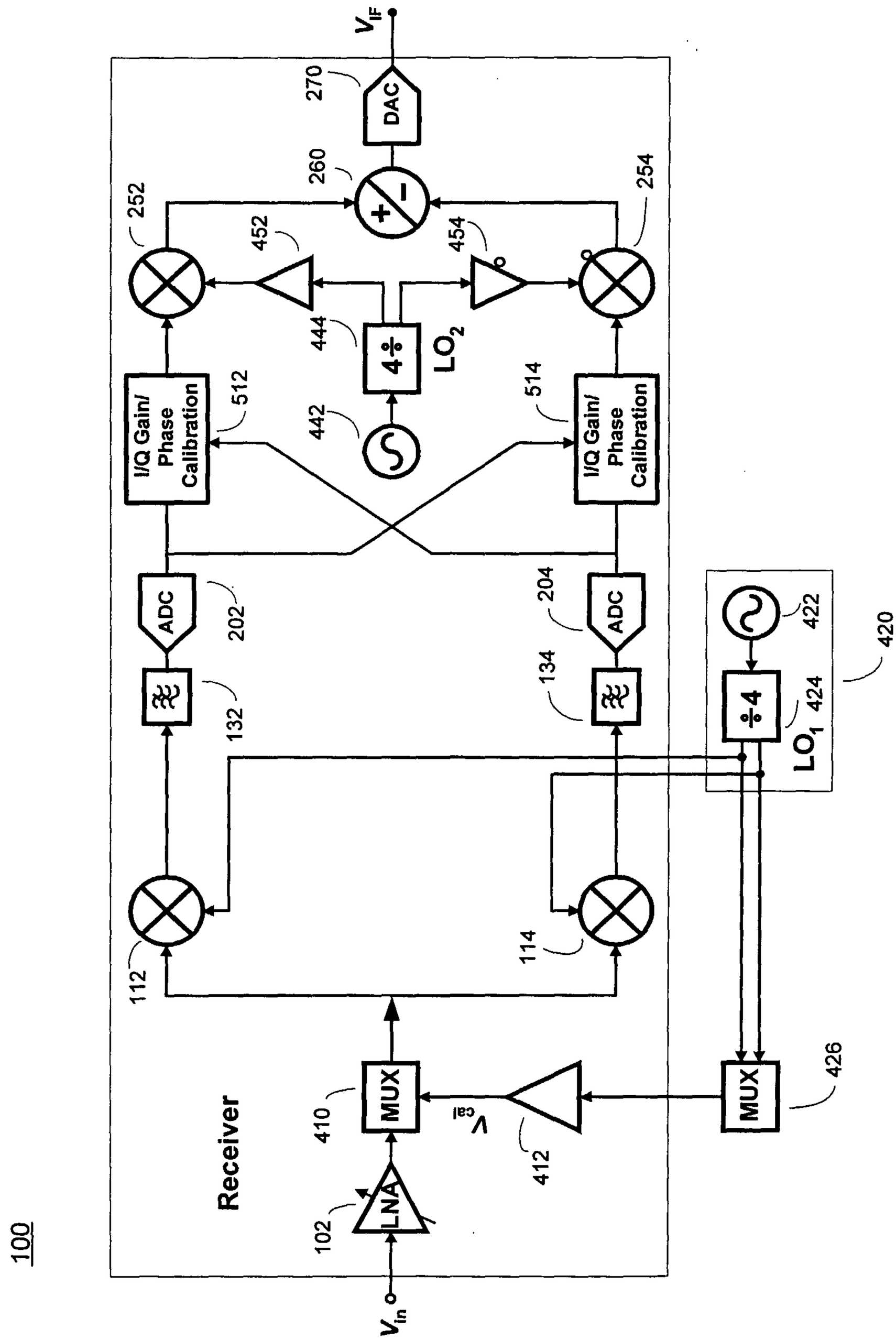

100
Receiver
V_{IF}
270
DAC
260
252
254
452
454
444
LO_2
442
512
514
I/Q Gain/ Phase Calibration
I/Q Gain/ Phase Calibration
ADC
ADC
202
204
132
134
112
114
410
MUX
MUX
426
V_{cal}
412
102
LNA
V_{in}
420
422
424
LO_1

FIG. 5

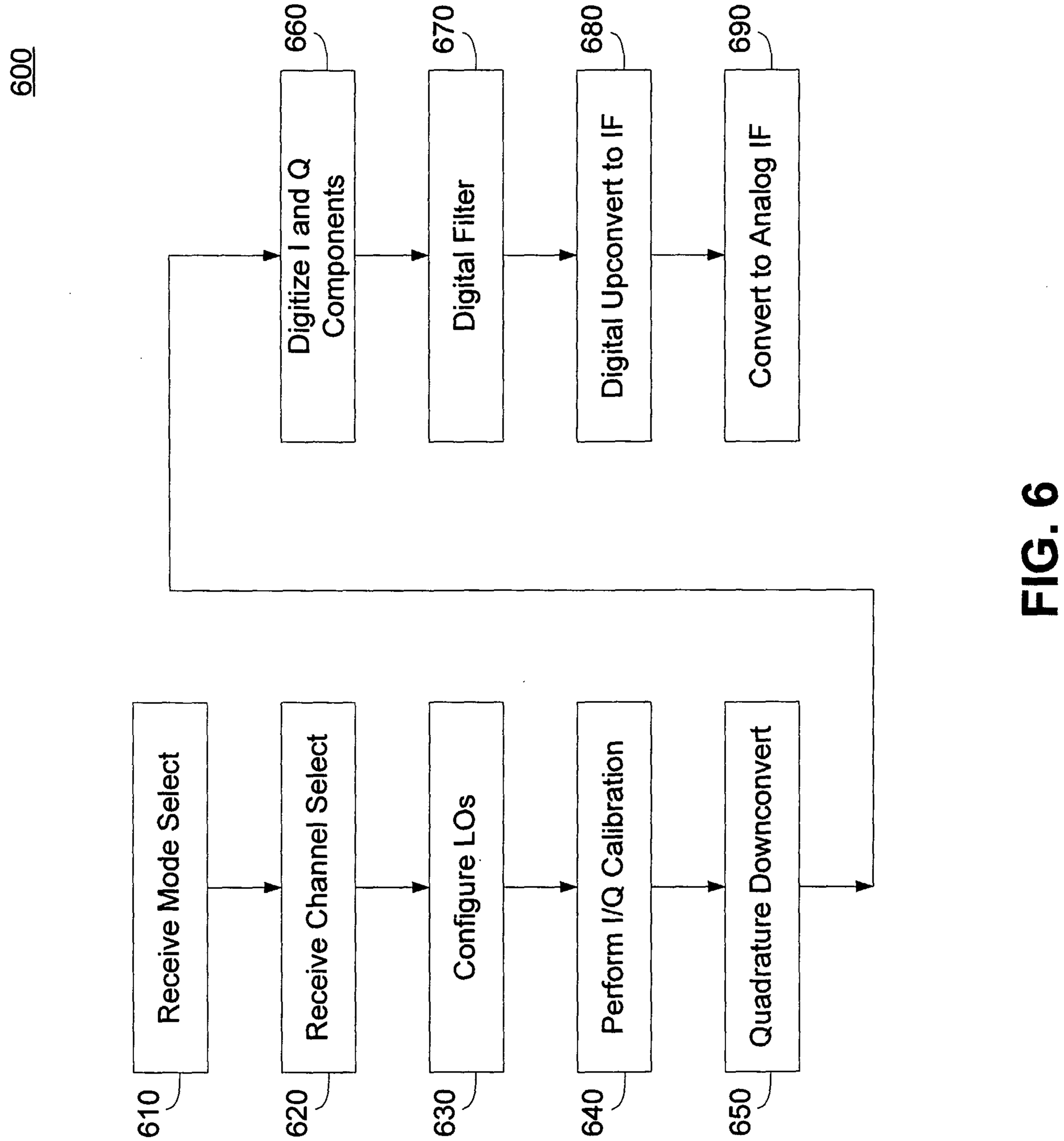
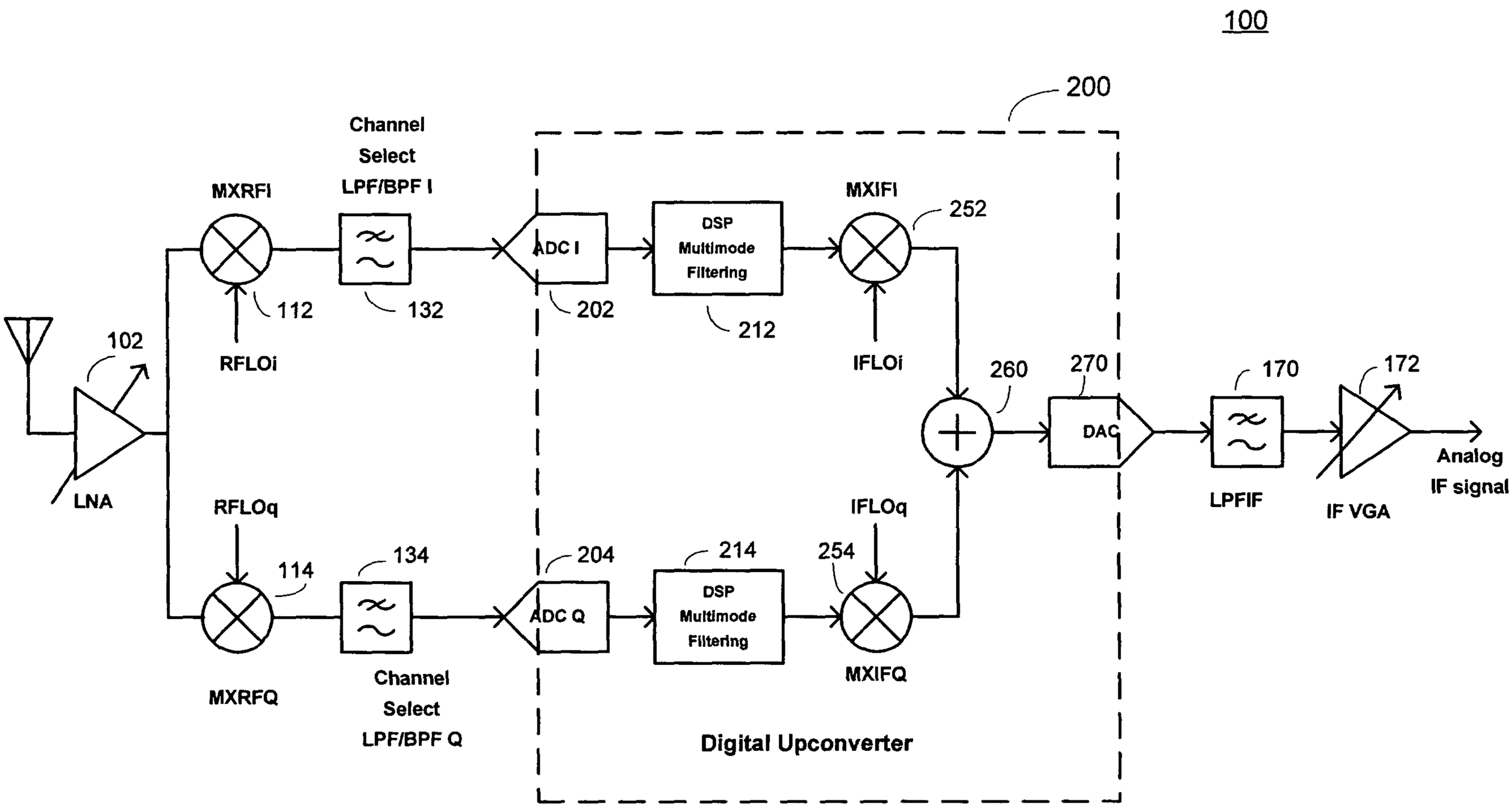

600
610
Receive Mode Select
620
Receive Channel Select
630
Configure LOs
640
Perform I/Q Calibration
650
Quadrature Downconvert
660
Digitize I and Q Components
670
Digital Filter
680
Digital Upconvert to IF
690
Convert to Analog IF

FIG. 6


100
200
Channel
Select
LPF/BPF I
MXRFI
MXIFI
252
DSP
Multimode
Filtering
ADC I
112
132
202
212
RFLOi
IFLOi
102
260
270
170
172
DAC
LNA
LPFIF
IF VGA
Analog
IF signal
RFLOq
IFLOq
114
134
204
214
254
DSP
Multimode
Filtering
ADC Q
MXRFQ
MXIFQ
Channel
Select
LPF/BPF Q
Digital Upconverter