

(51) International Patent Classification:
H03M 1/70 (2006.01) *H03G 3/00* (2006.01)(21) International Application Number:
PCT/IB2009/052497(22) International Filing Date:
11 June 2009 (11.06.2009)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
08104422.4 16 June 2008 (16.06.2008) EP

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

[Continued on next page]

(54) Title: DIGITAL-TO-ANALOGUE CONVERTER

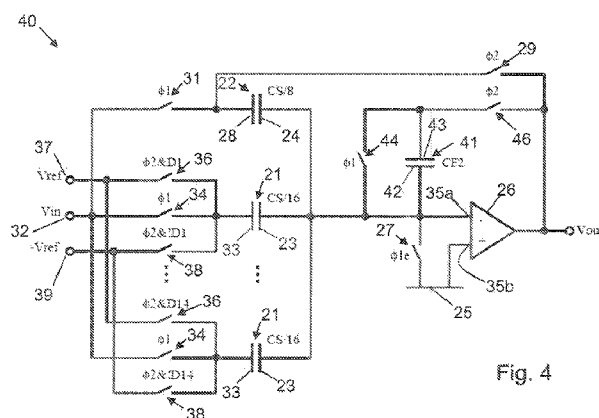


Fig. 4

(57) Abstract: A multiplying digital-to-analogue converter circuit for a stage of a pipelined analogue-to-digital converter, the multiplying digital-to-analogue circuit comprising: an operational amplifier (28); at least one sampling capacitor (21) having a first plate (23) connected to an input of the operational amplifier; a first feedback capacitor {22} having a first plate {24} connected to the input of the operational amplifier, a second plate (33, 28) of the at least one sampling capacitor and the first feedback capacitor being switchably connected to an analogue signal input (32) according to a first clock signal to permit sampling of an analogue signal, the second plate (33) of the at least one sampling capacitor (21) being additionally switchably connected to a reference voltage (37, 39) according to a second clock signal in combination with a digital signal to permit differencing of a sampled analogue signal and an analogue representation of the digital signal, and the second plate of the first feedback capacitor being switchably connected to an output of the operational amplifier according to the second clock signal; and a second feedback capacitor (41) having a first plate (42) connected to the input to the operational amplifier, and a second plate (43) switchably connected to the input of the operational amplifier according to the first clock signal, the second plate being switchably connected to the output of the operational amplifier according to the second clock signal.



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Published:

- *with international search report (Art. 21(3))*

DIGITAL-TO-ANALOGUE CONVERTER

The invention relates to a multiplying digital-to-analogue converter (MDAC) circuit for use in a stage of a pipelined analogue-to-digital converter (ADC).

Pipelined ADCs are a common class of ADC. Figure 1 shows a block schematic representation of a stage of a pipelined ADC 10. An input analogue signal V_{in} is sampled and held 11 before being encoded 12 into a preset number of bits of the final output of the ADC. The preset number of bits are output to other parts of the pipelined ADC, such as a digital post-processing circuit 13 for calibration and encoding of the final ADC output. The encoded bits are also converted back to an analogue voltage representation of the encoded bits using a digital-to-analogue converter (DAC) 14. The analogue voltage representation is then differenced 16 with the sampled analogue signal to provide a residue voltage. The residue voltage is then amplified 17 and passed to subsequent stages of the pipelined ADC for use in encoding the remaining bits of the final output of the ADC.

The term "residue voltage" when related to a stage of a pipelined ADC relates to the proportion of the analogue signal remaining after the stage has encoded the predetermined number of bits of the ADC output.

Typically, the function of encoding the preset number of bits is undertaken in an analogue-to-digital sub-converter (ADSC) 12. The remaining operations of sampling 11, digital to analogue conversion 14, differencing 16 and amplification 17 are undertaken by an MDAC circuit.

In a switched-capacitor MDAC the conversion takes place in two separate phases; a first phase where an input capacitance is charged with an analogue input voltage, and a second phase where feedback is applied to an operational amplifier circuit to give the amplified residue voltage.

Typically in a pipeline stage using an N-bit ADSC, the gain is 2^{N-1} . Therefore, as explained in detail below, the output signal range of a typical pipeline stage is equal to its input signal range.

In a pipelined ADC it is power efficient to implement a large signal range in the front-end pipeline stages and a smaller signal range in the back-end pipeline stages.

This is because the input signal ranges of the second and subsequent stages are constrained by the supply voltage. The input signal range of the first stage is typically maximized for maximal signal-to-noise-ratio (SNR), to enable a power-efficient realization of high SNR at a low supply voltage. Thus there exists a need for a pipeline stage in which the gain is other than 2^{N-1} for an N-bit ADSC.

For example if the gain of an MDAC circuit is reduced, the gain bandwidth product of an operational amplifier in an MDAC circuit can be reduced by an amount proportional to the reduction in gain of the circuit, whilst achieving the same circuit speed. This translates into a reduction in power as gain bandwidth product is roughly proportional to power. Moreover the slew rate requirements are also relaxed with a reduction in circuit gain, also translating into a proportional power reduction.

The term "input range" when applied to a stage of a pipelined ADC relates to the maximum range of an analogue signal which may be presented to the input of the stage, or alternatively the maximum signal range that can be digitized by the stage. The term "output range" relates to the range of the output signal of the stage, or alternatively the maximum signal range that can be digitized by a subsequent stage. The output range of a stage may be governed by the gain of the MDAC circuit. Range scaling may therefore be defined as being when the input and output ranges of a stage are different.

Additionally, the settling speed of the circuit and therefore the residue voltage depends on the feedback factor. A high feedback factor is desirable since it gives a shorter settling time, shortening the overall conversion time of a pipelined ADC.

According to a first aspect of the invention there is provided a multiplying digital-to-analogue converter circuit for a stage of a pipelined analogue-to-digital converter, the multiplying digital-to-analogue converter circuit comprising:

- an operational amplifier;
- at least one sampling capacitor having a first plate connected to an input of the operational amplifier;
- a first feedback capacitor having a first plate connected to the input of the operational amplifier,
- a second plate of the at least one sampling capacitor and the first feedback capacitor being switchably connected to an analogue signal input according to a first clock signal to permit sampling of an analogue signal,

the second plate of the at least one sampling capacitor being additionally switchably connected to a reference voltage according to a second clock signal in combination with a digital input, the second plate of the first feedback capacitor being switchably connected to an output of the operational amplifier according to the second clock signal; and

a second feedback capacitor having a first plate connected to the input to the operational amplifier, and a second plate switchably connected to the input of the operational amplifier according to the first clock signal, the second plate being switchably connected to the output of the operational amplifier according to the second clock signal.

The second plate of the second feedback capacitor may be switchably connected to the a fixed voltage node (e.g. electrical ground or a fixed voltage supply), the fixed voltage node being itself switchably connected to the input of the operational amplifier. Alternatively, the second plate of the second feedback capacitor may be switchably connected directly to the input of the operational amplifier.

The inclusion of the second feedback capacitor allows control of the gain of the MDAC such that the output range can be controlled relative to the input range. As mentioned above and described in detail below, an input range greater than the output range is desirable as this improves the power efficiency of a pipeline stage.

Moreover, some applications, e.g. 14-bit ADC for cellular phone base stations, require a 2V peak-to-peak input range. This high signal range can not be accommodated at the output of a pipelined ADC stage, i.e. the output of an operational amplifier, when using a supply in the order of 1.2V.

The second feedback capacitor also alters the feedback factor of the MDAC circuit. Increasing the feedback factor allows the settling time of the stage to be reduced, thereby improving the time of conversion of the pipeline ADC.

The configuration of the second feedback capacitor means that the capacitor is reset, i.e. discharged, when the first clock signal connects the second plate of the second feedback capacitor to the input of the operational amplifier. The second feedback capacitor is then switched in when the second clock signal connects the second plate of the second feedback capacitor to the output of the operational amplifier. This configuration means that the second feedback capacitor is able to affect the total feedback capacitance of the circuit.

The input of the operational amplifier may be switchably connected to a fixed voltage node (e.g. electrical ground or a fixed voltage supply) according to a third clock signal, such that any operational amplifier noise added to the voltage over the sampling capacitor is minimised or removed, and the signal to noise ratio is improved. Alternatively, the inverting and non-inverting inputs of the operational amplifier may be switchably connected together according to the third clock signal to achieve the same effect.

The invention may include a plurality of sampling capacitors arranged in parallel, each sampling capacitor corresponding to a bit of a digital signal input to the circuit.

The digital signal input to the MDAC circuit may be the output from the comparators of an ADSC circuit. By providing a plurality of sampling capacitors, each of which corresponds to a bit of the digital signal, multi-bit digital signals may be accommodated by the circuit. A larger number of bits (or an increased resolution) in a pipeline stage results in a larger gain of the stage and a decrease in input-related noise and non-linearity of subsequent stages. This is to be traded off with a larger number of comparators, resulting in a larger capacitive load at the input.

The value of each of the sampling capacitors may be substantially the same. Alternatively, values of the sampling capacitors may be weighted.

The use of different weighting schemes for the sampling capacitors means that different types of coded signal from the ADSC may be accommodated. For instance a digital signal received from an ADSC may be encoded such that each bit of the digital signal has equal weight. In this case sampling capacitors of equal value may be used in the MDAC circuit. Alternatively, the digital signal received from an ADSC may be binary coded in which case weighted capacitor values may be used.

The first feedback capacitor and the second feedback capacitor may be of equal value. This results in an MDAC circuit the gain of which is reduced by a half when compared to a circuit containing no second feedback resistor. This feature permits range scaling, thereby increasing power efficiency of the circuit.

The use of equal value first and second feedback capacitors also increases the feedback factor k of the circuit, which results in a reduction in the conversion time of the pipelined ADC.

5 The values of the first and the second feedback capacitors may be different, thereby permitting different gains to be implemented to suit circuit requirements.

10 According to a second aspect of the invention there is provided a method for providing an amplified residue voltage in a stage of a pipelined analogue-to-digital converter using a multiplying digital-to-analogue converter circuit according to the first aspect, the method comprising the steps of:

- a) sampling an analogue signal presented at the analogue signal input of the circuit;
- 15 b) holding a charge corresponding to an instantaneous value of the sampled analogue signal on the second plate of the at least one sampling capacitor;
- c) differencing the sampled analogue signal with an analogue representation of a digital signal presented to the circuit to provide a residue voltage; and
- d) amplifying the residue voltage to provide an output signal to a further stage of a pipelined analogue-to-digital converter.

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Amplification of the residue voltage such that the input range of the circuit is different to the output range of the circuit provides the advantage that the circuit may be more power efficient. In addition the increase in the feedback factor for the circuit may reduce the conversion time of the pipelined ADC.

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Step a) of the invention may include connecting the second plate of the at least one sampling capacitor and the first feedback capacitor to the analogue signal input to sample an analogue signal, while connecting the second plate of the second feedback capacitor to the input of the operational amplifier. This step allows the second feedback capacitor to be reset or discharged ready for use in the feedback loop of the operational amplifier while the analogue input signal is sampled. The second feedback capacitor is thereby able to be periodically discharged between samples.

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Step b) may include disconnecting the second plate of the at least one sampling capacitor and the first feedback capacitor from the analogue signal input, while disconnecting the second plate of the second feedback capacitor from the input of the operational amplifier. This step removes the short circuit across the two plates of the

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second feedback capacitor by disconnecting the second plate from the input to the operational amplifier. The second feedback capacitor is then ready to be incorporated into the operational amplifier feedback loop.

5 Step c) may include, after disconnecting the second plate of the at least one sampling capacitor and the first feedback capacitor from the analogue signal input, connecting the second plate of the at least one sampling capacitor to the reference voltage according to the level of a bit of a digital signal.

10 Step d) may include connecting the second plate of the first and second feedback capacitors to the output of the operational amplifier to provide an amplified residue voltage representing the difference between the sampled analogue signal and an analogue representation of the digital signal. This step switches the second feedback capacitor into the feedback loop of the operational amplifier during amplification of the
15 difference voltage. As explained in greater detail below the second feedback capacitor is therefore able improve the feedback factor of the circuit by increasing the feedback capacitance.

Steps c) and d) above in combination result in an amplified difference, and in
20 practice take place at substantially the same moment. The mechanism for this is described in terms of charge transfer relationships detailed below.

There now follows a description of preferred embodiments of the invention, by way of non-limiting example, with reference being made to the accompanying drawings
25 in which:

figure 1 shows a block schematic diagram of a pipeline stage of a pipelined ADC;

figure 2 shows an MDAC circuit for use in a stage of a pipelined ADC;

figure 3 shows a timing diagram representing a relationship between exemplary clock signals used in operating an MDAC circuit;

30 figure 4 shows an exemplary MDAC circuit for use in a stage of a pipelined ADC including a second feedback capacitor;

figure 5 shows a further exemplary MDAC circuit for use in a stage of a pipelined ADC including a second feedback capacitor;

figure 6 shows a modified version of the MDAC circuit of figure 4, including a
35 charge-reset switch arrangement; and

figure 7 shows a timing diagram of the sequence of switches for the circuit of figure 6.

Figure 2 shows a single-ended equivalent representation of an $N = 4$ bit MDAC circuit 20 where N is the number of bits in a digital signal received by the MDAC circuit from and ADSC (not shown). The circuit may in practice be implemented as a differential circuit.

A total sampling capacitance C_s is split into $2^N = 16$ equally sized unit capacitances 21. It will be appreciated by the skilled worker that the number of unit capacitances will differ dependent on the number of bits encoded by the ADSC. The number of unit capacitances may be equal to 2^N .

The example in figure 2 employs unit capacitances, each having an equal capacitance value, as the digital signal to be received by the MDAC circuit is intended to be a thermometer coded digital signal. Alternative capacitor configurations may be employed if other types of encoded digital signal are to be presented to the MDAC circuit. For example when binary coded data is used binary weighted capacitor values may be employed.

In the example shown in figure 2, two of the unit capacitances are combined to provide a feedback capacitor 22. It will be appreciated by the skilled worker that other MDAC circuit configurations may be employed e.g. in some circuits only one of the unit capacitances may be used as feedback capacitor 22.

The remaining unit capacitors form the sampling capacitors 21 of the MDAC circuit. Each sampling capacitor 21 corresponds to a bit of the encoded digital signal received from the ADSC.

A first plate 23 of each of the sampling capacitors 21 and a first plate 24 of the feedback capacitor 22 are connected to the inverting input 35a of an operational amplifier 26. The inverting input 35a is also connected to electrical ground 25 through a switch 27. The non-inverting input 35b of operational amplifier 26 is connected to electrical ground 25.

A second plate 28 of feedback capacitor 22 is connected to the output of operational amplifier 26 through switch 29. The second plate 28 of feedback capacitor 22 is also connected through switch 31 to an analogue signal input 32.

Second plates 33 of sampling capacitors 21 are connected through switches 34 to the analogue signal input 32. The second plates 33 of sampling capacitors 21 are also connected through switches 36 to a positive reference voltage 37, and through switches 38 to a negative reference voltage input 39.

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Switch 27 is opened and closed according to a clock signal ϕ_{1e} . Switches 31 and 34 are opened and closed according to a clock signal ϕ_1 . Switch 29 is opened and closed according to a clock signal ϕ_2 . Switches 36 and 38 are opened and closed according to clock signal ϕ_2 in combination with the encoded digital signal received by the MDAC circuit from an ADSC. Switches 36 are closed when ϕ_2 is high and D_i is high, and switches 38 are closed when ϕ_2 is high and D_i is low, where $D_i = 0|1$ ($i = 1-14$) and is the output of the comparators of an ADSC

Clock signals ϕ_1 and ϕ_2 constitute a non-overlapping clocking scheme and ϕ_{1e} is a slightly advanced version of clock signal ϕ_1 . In the example shown in figure 2 the switches 27, 29, 31, 34, 36, 38 are closed when the relevant clock signals are high.

An analogue input signal V_{in} is presented to the MDAC circuit 20 at the analogue signal input 32 and positive and negative reference voltages V_{ref} , $-V_{ref}$ are presented to the reference voltage inputs 37 and 39 respectively.

Figure 3 shows an exemplary timing diagram depicting each of the three clock signals ϕ_1 , ϕ_2 and ϕ_{1e} implemented in operation of the circuits shown in figures 2, 4 and 5. Times t_0 , t_1 , t_2 and t_3 are sequential discrete times which relate to different stages of the operation of the MDAC circuit 20. The first clock signal ϕ_1 transitions from high to low in advance of the second clock signal ϕ_2 transitioning from low to high, and the second clock signal ϕ_2 transitions from high to low in advance of the first clock signal ϕ_1 transitioning from low to high. The third clock signal ϕ_{1e} is a slightly advanced version of the first clock signal, such that high to low and low to high transitions of ϕ_{1e} always occur in advance of those of ϕ_1 . This advanced clock signal ϕ_{1e} allows for a sample to be acquired from the signal input 32 by opening switch 27 in advance of opening switches 31, 34, thereby minimizing errors and distortion due to signal-dependent sampling timing.

At time t_0 ϕ_1 and ϕ_{1e} are high and switches 27, 31 and 34 are closed, and ϕ_2 is low and switches 29, 36 and 38 are open. The voltage across the total sampling capacitance C_s tracks the analogue input signal V_{in} .

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At time t_1 , $\phi 1_s$ goes low and switch 27 is opened. The inverting input to operational amplifier 26 is no longer connected to electrical ground and the input signal V_{in} is sampled on C_S . The sampled analogue signal V_{in} is therefore held as a charge on the total sampling capacitance C_S .

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At time t_2 $\phi 1$ goes low disconnecting the analogue input signal 32 from the sampling capacitors 21 and the feedback capacitor 22 by opening switches 31 and 34.

The above steps are commonly referred to as bottom-plate sampling, in which switch 27 performs the sampling action. Switch 27 effectively has a fixed voltage at both its source and drain (when using a MOSFET transistor switch), which improves the linearity of the sampling action.

At time t_3 $\phi 2$ goes high, connecting the second plates 33 of 14 of the 16 unit capacitances i.e. the sampling capacitors 21, to either the positive reference voltage 37 or the negative reference voltage 39 depending on the value of D_i . If D_i is high then the second plates 33 are connected to the positive reference voltage 37 and if D_i is low then the second plates 33 are connected to the negative reference voltage 39.

The remaining capacitance i.e. the feedback capacitor 22 is connected in a feedback configuration across operational amplifier 26 when switch 29 is closed.

The output of the MDAC circuit 20 is an amplified residue voltage between the sampled analogue signal and an analogue voltage representation of the encoded digital signal received from the ADSC.

The charge transfer in the MDAC circuit 20 can be written as:

$$\begin{aligned}
 C_S V_{in} &= D_1 \frac{C_S}{16} V_{ref} + (1 - D_1) \frac{C_S}{16} (-V_{ref}) \\
 &+ \dots \\
 &+ D_{14} \frac{C_S}{16} V_{ref} + (1 - D_{14}) \frac{C_S}{16} (-V_{ref}) \\
 &+ \frac{C_S}{8} V_{out}
 \end{aligned}$$

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And with D defined as:

$$D = \frac{1}{14} \sum_{i=1}^{14} D_i$$

The input to output relationship of the MDAC circuit 20 is:

$$V_{out} = 8(V_{in} + (1 - 2D)\frac{14}{16}V_{ref})$$

The switched capacitor MDAC circuit for a pipeline stage of a pipelined ADC shown in figure 2 therefore has a gain of 8 and a subtraction of the analogue input signal from the analogue voltage representation of the encoded digital signal according to $-(1 - 2D)V_{ref}$.

In the N-bit MDAC circuit for a pipeline stage shown in figure 2 the gain is equal to $2^{(N-1)} = 8$.

The input range of the MDAC circuit 20 is divided by $2^N = 16$, and the residue voltage is amplified by 8. Thus, without redundancy, the input range of the circuit 20 is scaled down by a factor 2.

However, in typical pipelined ADCs half of the total output range is redundant such that offsets in the comparators of the ADSC, and operational amplifier 26 offset do not result in the output of the MDAC circuit 20 being outside the output range. Therefore the output range of the stage is equal to the input range.

The feedback factor k of the MDAC circuit 20 is calculated by:

$$k = \frac{C_{feedback}}{C_{total}}$$

Where $C_{feedback}$ is the value of the feedback capacitor 22, which is connected in feedback configuration with operational amplifier 26 at time t_3 , and C_{total} is the total capacitance in the circuit i.e. the sum of all of sampling capacitors 21 and the feedback capacitor 22.

A high feedback factor is desirable since it gives a shorter settling time of the MDAC circuit 20, shortening the overall conversion time of the pipelined ADC.

The (4 bit) MDAC circuit shown in Fig. 2 has a feedback factor of:

$$\frac{C_s/8}{C_s} = \frac{1}{8}$$

MDAC circuit 20 is restricted to a gain factor of 8 by the relative values of the capacitances used. There are circumstances such as when range scaling is required when a different gain factor may be advantageous.

Figure 4 shows a single-ended equivalent representation of an embodiment of an MDAC circuit 40 according to the invention, in which a second feedback capacitor 41 is included. As with the circuit shown in figure 2, this may in practice be implemented as a differential circuit.

A first plate 42 of second feedback capacitor 41 is connected to the inverting input 35a of operational amplifier 26.

A second plate 43 of second feedback capacitor 41 is connected through switch 44 to the inverting input of operational amplifier 26. As in figure 2, the inverting input of operational amplifier 26 is connected to electrical ground through switch 27. The second plate 43 of second feedback capacitor 41 is also connected, through switch 46, to the output of operational amplifier 26.

The following description of the operation of the circuit represented in figure 4 refers also to the timing diagram of figure 3.

At time t_0 $\phi 1$ and $\phi 1_e$ are high and switches 27, 31, 34 and 44 are closed. Switches 44 and 46 are controlled by clock signals $\phi 1$ and $\phi 2$ respectively. Clock signal $\phi 2$ is low and switches 29, 36, 38 and 46 are open. The voltage across the total sampling capacitance C_s tracks the analogue input signal V_{in} . Additionally, the second plate 43 of second feedback capacitor 41 is discharged through switches 44 and 27 to electrical ground. This removes any charge remaining on second feedback capacitor 41 from previous processing by the MDAC circuit 40.

At time t_1 $\phi 1_e$ goes low and switch 27 is opened. The inverting input to operational amplifier 26 and the second plate 43 of second feedback capacitor 41 are no longer connected to electrical ground and the input signal V_{in} is sampled on C_s i.e. the sampling capacitors 21 and the first feedback capacitor 22. The sampled analogue signal is therefore held as a charge on total sampling capacitance C_s .

At time t_2 $\phi 1$ goes low disconnecting the analogue input signal from the sampling capacitors 21 and the feedback capacitor 22 by opening switches 31 and 34. Additionally, second plate 43 of second feedback capacitor 41 is disconnected from the non-inverting input of operational amplifier 26 as switch 44 is opened.

At time t_3 $\phi 2$ goes high, connecting second plates 33 of 14 of the 16 unit capacitances i.e. sampling capacitors 21, to either a positive reference voltage 37 or the negative reference voltage 39 depending on the value of D_i . If D_i is high then the second plates 33 are connected to the positive reference voltage 37 and if D_i is low then the second plates 33 are connected to the negative reference voltage 39.

The remaining capacitance i.e. the first feedback capacitor 22 is connected in a feedback configuration across operational amplifier 26. Second feedback capacitor 41 is also connected in a feedback configuration across operational amplifier 26 as switch 46 is closed.

The charge transfer in the MDAC circuit 40 can be written as:

$$\begin{aligned}
 C_s V_{in} &= D_1 \frac{C_s}{16} V_{ref} + (1 - D_1) \frac{C_s}{16} (-V_{ref}) \\
 &+ \dots \\
 &+ D_{14} \frac{C_s}{16} V_{ref} + (1 - D_{14}) \frac{C_s}{16} (-V_{ref}) \\
 &+ \frac{C_s}{8} V_{out} \\
 &+ C_{f2} V_{out}
 \end{aligned}$$

The input to output relationship of the MDAC circuit 40 shown in figure 3 is therefore:

$$V_{out} = \frac{C_s}{\frac{C_s}{8} + C_{f2}} (V_{in} + (1-2D) \frac{14}{16} V_{ref})$$

The value of second feedback capacitor 41 may be set to $C_s/8$ and the input to output relationship can then be written as:

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$$V_{out} = 4(V_{in} + (1-2D) \frac{14}{16} V_{ref})$$

Therefore MDAC circuit 40 may have a gain of 4 and a subtraction of the analogue input signal from the analogue representation of the encoded digital signal according to $-(1-2D)V_{ref}$. The gain of MDAC circuit 40 is therefore half that of MDAC circuit 20. As in MDAC circuit 20, the analogue input signal is divided by $2^N = 16$ when sampling, but the residue voltage in MDAC circuit 40 is amplified by 4. Therefore, including redundancy, the input range of MDAC circuit 40 is scaled down by a factor 2.

15 Therefore MDAC circuit 40 results in a range scaling of the input range to output range by a factor of 2.

It will be appreciated that through selection of alternative values of second feedback capacitor 41, different gains may be realised using MDAC circuit 40.

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The connection of second feedback capacitor 41 in a feedback configuration across operational amplifier 26 increases the value of $C_{feedback}$ and therefore increases the feedback factor of the MDAC circuit 40.

25 The speed of the circuit is characterized by its -3dB-frequency, $f_{3dB} = k * GBW$, where GBW is the gain-bandwidth product of the amplifier. The speed thus is proportional to the feedback factor, making a high feedback factor desirable.

The feedback factor of MDAC circuit 40 can be calculated as:

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$$k = \frac{C_s/8 + C_{f2}}{C_s + C_{f2}}$$

Where C_{12} is the capacitance of second feedback capacitor 41. If second feedback capacitor 41 is set to have a capacitance equal to $C_s/8$, the feedback factor of MDAC circuit 40 can be calculated as:

$$k = \frac{\frac{C_s}{8} + \frac{C_s}{8}}{C_s + \frac{C_s}{8}} = \frac{2}{9}$$

MDAC circuit 40 therefore exhibits an increased feedback factor over MDAC circuit 20. This results in a shorter settling time of the MDAC circuit

The sum of capacitance values of the first feedback capacitor 22 and the sampling capacitors should be equal to C_s for the MDAC stage to perform the required functions of sampling, digital to analogue conversion, differencing and amplification. The same effect as described above could not therefore be achieved simply by increasing the size of the first feedback capacitor 22.

In switched-capacitor MDAC circuits the settling speed is proportional to the feedback factor. This invention describes an MDAC circuit using an N-bit ADSC, capable of realising various required gains, and with an up to 20% speed improvement as compared to typical MDAC circuits.

Shown in figure 5 is an alternative embodiment of an MDAC circuit 50 according to the invention, in which the inverting input 35a of the operational amplifier 26 is instead switchably connected to a fixed voltage node 51. The second plate 43 of the second feedback capacitor 41 is also switchably connected to the same fixed voltage node. The operation of the circuit in figure 5 is essentially identical to that of figure 4, as described above, with the only difference being that the second feedback capacitor 41 is discharged directly to the fixed voltage node 51 via switch 44.

In other alternative embodiments, switch 27 may be connected between the inverting 35a and non-inverting 35b inputs of the operational amplifier.

As described above in relation to the embodiments shown in figures 4 and 5, the range-scaling function of the MDAC is implemented with an additional second feedback capacitor 41. When the value of this capacitor equals $C_s/8$, and the open-loop gain A_{OL} of the operational amplifier 26 is high, the signal range of the output is scaled by a factor

of 2 compared with the input. The introduction of the second feedback capacitor requires some attention to be paid to maintain linearity. A non-linear portion of the charge sampled by the total input capacitance C_s is transferred to the second feedback capacitor 41. When the input capacitance is reconnected to the input to acquire the next sample, its remaining charge could cause distortion due to inter-symbol interference (ISI). In order to avoid this, a charge-reset switch arrangement 61 can be implemented in the pipeline stage circuit 60, as shown in figure 6. The circuit 60 of figure 6 is otherwise similar to the circuit shown in figure 4. The charge-reset switch arrangement 61 comprises a plurality of switches, each switch connected between a plate of each of the sampling capacitors 22, 21 and a fixed voltage node 62, which may be held at ground or a fixed voltage supply.

Figure 7 shows an exemplary timing diagram for the switches 61 of figure 6. Operation (i.e. closing) of the switches 61 is triggered by a clock signal R, causing the input capacitors to be reset. A further clock signal ϕ_{1R} then causes the input switches to close, shortly after the switches 61 are opened. The remaining operation of the circuit 60 is similar to that described above in relation to figure 4.

Adding the charge-reset switching arrangement 61 to the input stage of the circuit 60 avoids the need for a dummy input sampling capacitance (for example as disclosed by P. Bogner et al., in "A 14b 100MS/s digitally self-calibrated pipelined ADC in 0.13 μ m CMOS," ISSCC Dig. Tech. Papers, pp. 224-225, Feb. 2006), thereby saving a significant amount of power needed to drive the capacitive loading on the circuit.

The invention may be applied in the design of 14-bit 125-MS/s ADCs for high-speed analogue-to-digital and digital-to-analogue conversion. Future products possibly incorporating the invention are e.g. a standalone 14-bit ADC for communication infrastructure and an embedded 12-bit ADC for consumer products.

Other embodiments are intentionally within the scope of the invention, as defined by the appended claims.

CLAIMS

1. A multiplying digital-to-analogue converter circuit for a stage of a pipelined analogue-to-digital converter, the multiplying digital-to-analogue circuit comprising:

an operational amplifier;

at least one sampling capacitor having a first plate connected to an input of the operational amplifier;

a first feedback capacitor having a first plate connected to the input of the operational amplifier,

a second plate of the at least one sampling capacitor and the first feedback capacitor being switchably connected to an analogue signal input according to a first clock signal to permit sampling of an analogue signal,

the second plate of the at least one sampling capacitor being additionally switchably connected to a reference voltage according to a second clock signal in combination with a digital input, the second plate of the first feedback capacitor being switchably connected to an output of the operational amplifier according to the second clock signal; and

a second feedback capacitor having a first plate connected to the input to the operational amplifier, and a second plate switchably connected to the input of the operational amplifier according to the first clock signal, the second plate being switchably connected to the output of the operational amplifier according to the second clock signal.

2. The multiplying digital-to-analogue converter circuit of claim 1, wherein the input of the operational amplifier is switchably connected to a fixed voltage node according to a third clock signal.

3. The multiplying digital-to-analogue converter circuit of claim 1 wherein the non-inverting and inverting inputs of the operational amplifier are switchably connected together according to a third clock signal.

4. The multiplying digital-to-analogue converter circuit of claim 1 wherein the second plate of the second feedback capacitor is switchably connected directly to the input of the operational amplifier according to the first clock signal.

5. The multiplying digital-to-analogue converter circuit of claim 2 wherein the second plate of the second feedback capacitor is switchably connected to the fixed voltage node according to the first clock signal.

6. The multiplying digital-to-analogue converter circuit of claim 1 including a plurality of sampling capacitors arranged in parallel, each sampling capacitor corresponding to a bit of the digital signal input.

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7. The multiplying digital-to-analogue converter circuit of claim 6 wherein the value of each of the sampling capacitors is the same.

8. The multiplying digital-to-analogue converter circuit of claim 6 wherein the values of the sampling capacitors are binary weighted.

9. The multiplying digital-to-analogue converter circuit of any preceding claim wherein the value of the first feedback capacitor and the second feedback capacitor are the same.

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10. The multiplying digital-to-analogue converter circuit of any preceding claim wherein the first plate of each of the at least one sampling capacitor is switchably connected to a fixed voltage node according to a third clock signal.

11. A pipelined analogue-to-digital converter including a multiplying digital-to-analogue converter circuit according to any preceding claim.

12. A method for providing an amplified residue voltage in a stage of a pipelined analogue-to-digital converter using a multiplying digital-to-analogue converter circuit according to claim 1, the method comprising the steps of:

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a) sampling an analogue signal presented at the analogue signal input of the circuit;

b) holding a charge corresponding to an instantaneous value of the sampled analogue signal on the second plate of the at least one sampling capacitor;

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c) differencing the sampled analogue signal with an analogue representation of a digital signal presented to the circuit to provide a residue voltage; and

d) amplifying the residue voltage to provide an output signal to a further stage of a pipelined analogue-to-digital converter.

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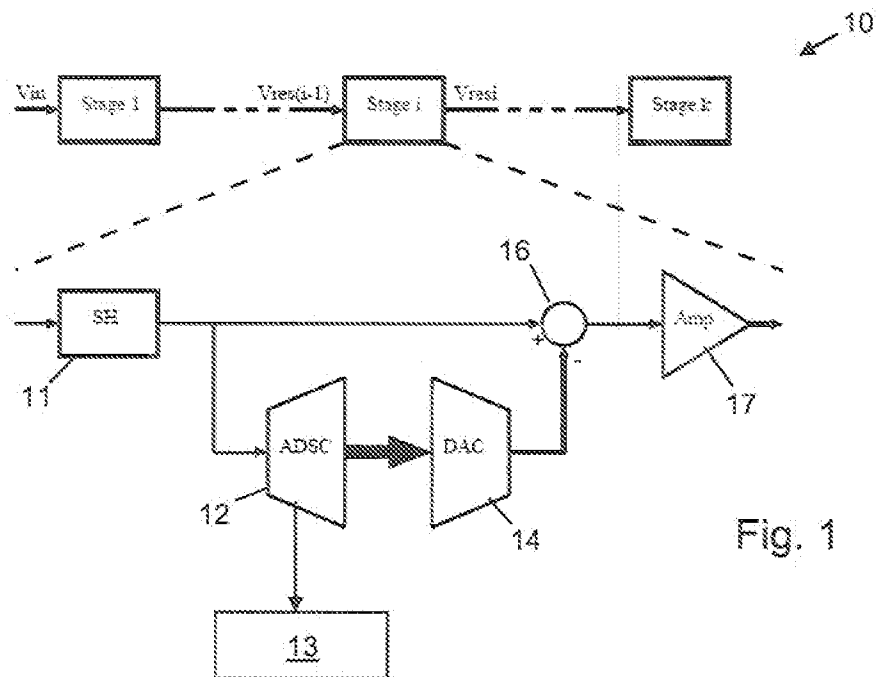


Fig. 1

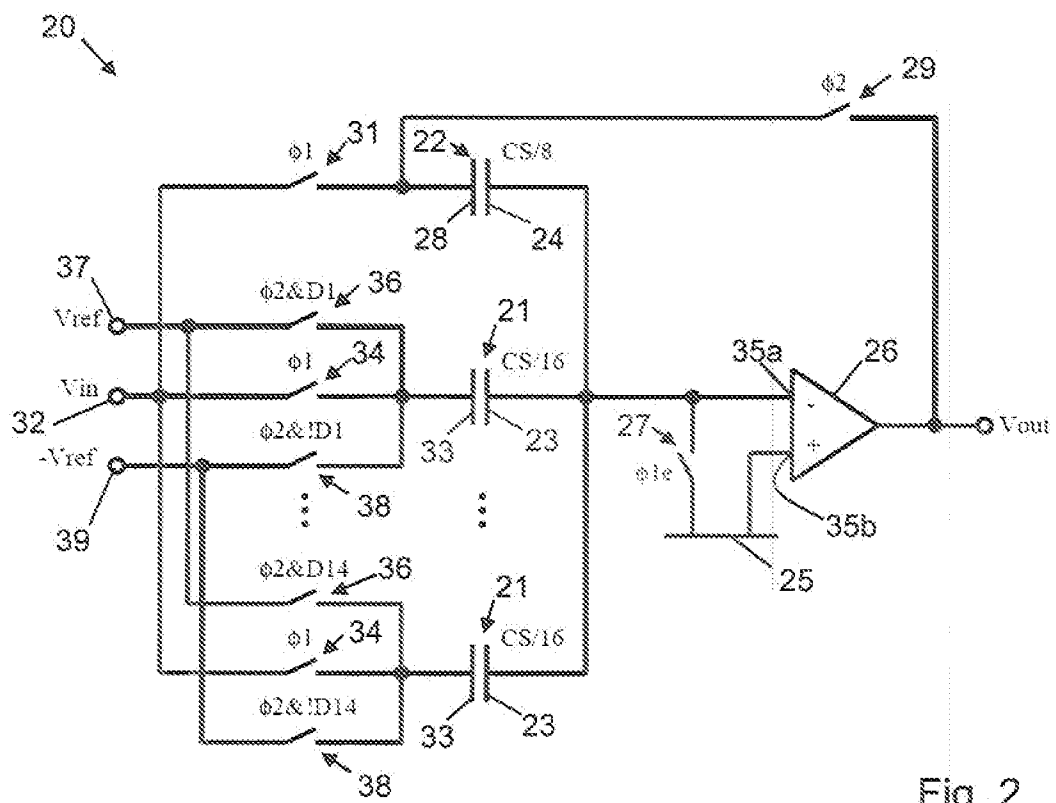


Fig. 2

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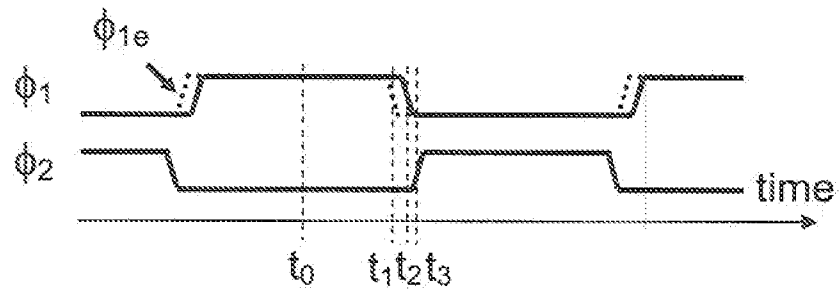


Fig. 3

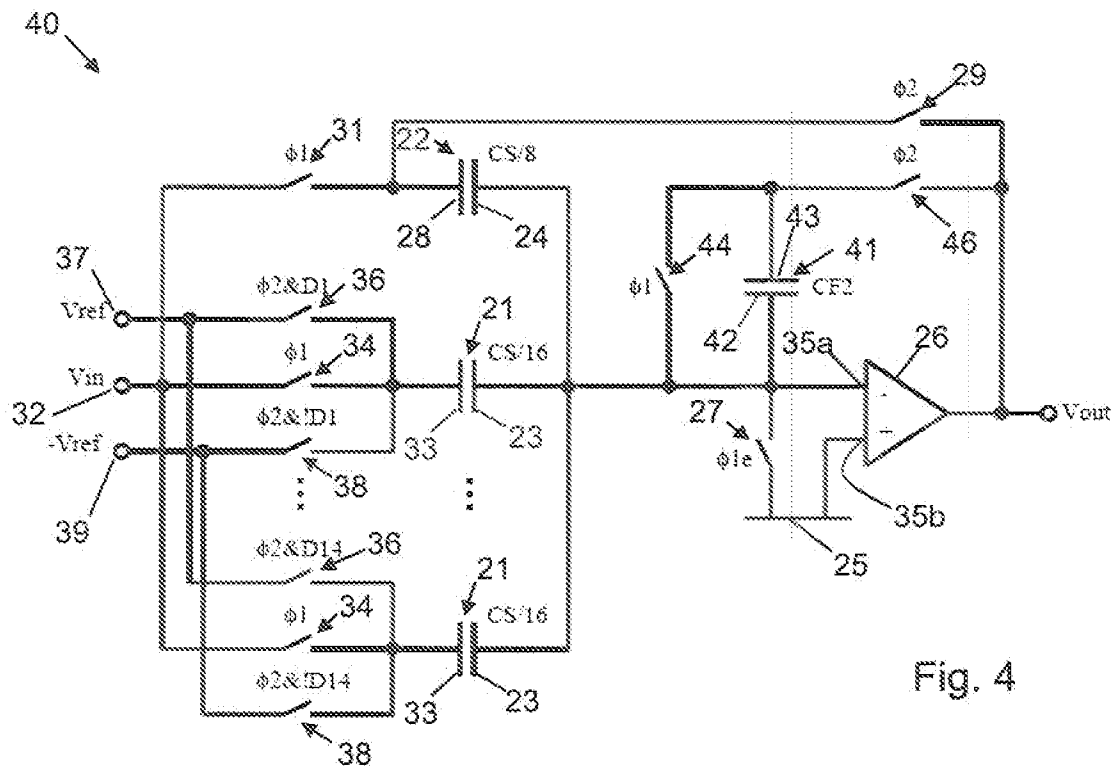


Fig. 4

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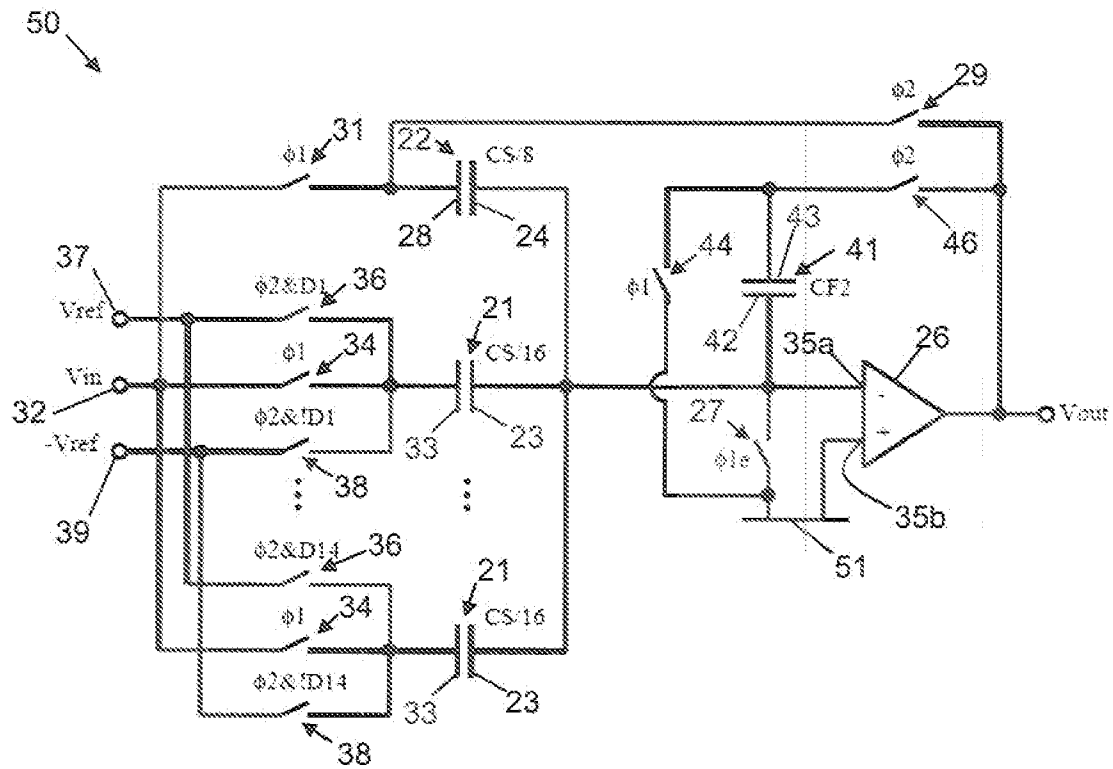


Fig. 5

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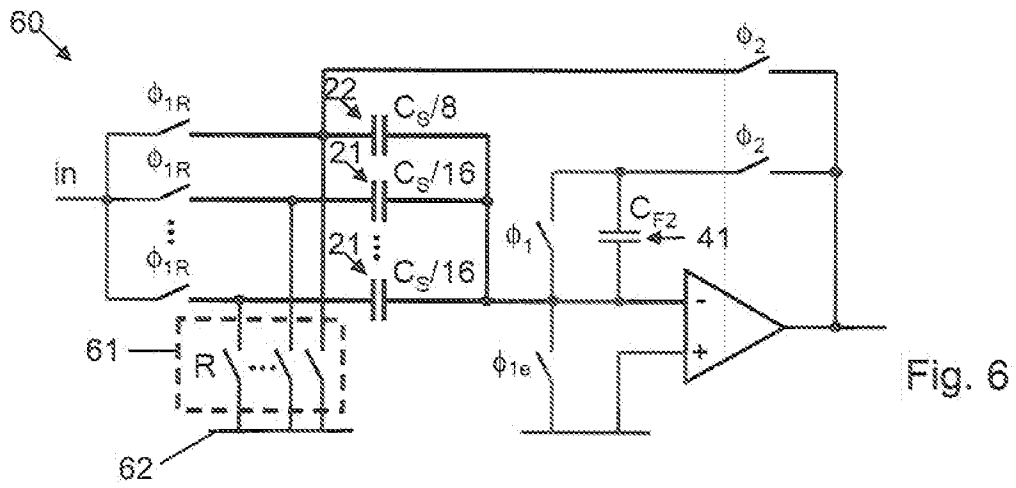


Fig. 7

INTERNATIONAL SEARCH REPORT

International application No

PCT/IB2009/052497

A. CLASSIFICATION OF SUBJECT MATTER
 INV. H03M1/70 H03G3/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03M H03G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 499 027 A (KARANICOLAS ANDREW N [US] ET AL) 12 March 1996 (1996-03-12)	1,5-7, 10-12
Y	column 8, line 58 - column 9, line 3; claims 13,14; figures 10A,10B	2-4,8-9
Y	US 2007/290914 A1 (MATSUSHITA MASATOSHI [JP] ET AL) 20 December 2007 (2007-12-20) figures 5,7,9	1-3,6-8, 10-12
Y	US 2007/290915 A1 (MORIMOTO YASUO [JP]) 20 December 2007 (2007-12-20) figure 7	1-3,6-8
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Further documents are listed in the continuation of Box C.



See patent family annex.

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X document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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Date of the actual completion of the international search

19 October 2009

Date of mailing of the international search report

02/11/2009

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Müller, Uta

INTERNATIONAL SEARCH REPORT

International application No

PCT/IB2009/052497

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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Y	BOGNER P: "A 28mW 10b 80MS/s pipelined ADC in 0.13[μ]m CMOS" PROCEEDINGS - IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS - 2004 IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS - PROCEEDINGS; VOLUME I OF V: ANALOG SIGNAL PROCESSING 2004 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS INC. US, vol. 1, 2004, pages I17-I20, XP002551101 paragraph; figure 2.2	1-4,6-9, 11-12
Y	JP 2004 336197 A (CANON KK) 25 November 2004 (2004-11-25) abstract; figures 1-3	1,11-12
Y	US 7 102 557 B1 (FRITH PETER [GB]) 5 September 2006 (2006-09-05) column 4, lines 23-27; figures 8a, 8b	1,6-8, 11-12
Y	DATABASE INSPEC [Online] THE INSTITUTION OF ELECTRICAL ENGINEERS, STEVENAGE, GB; 2000, HUI LIU ET AL: "Components of a 12-bit 50 Ms/s non-radix 2 pipeline analog-to-digital converter" XP002551102 Database accession no. 7145791 abstract; figure 8	1-4, 10-12
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International application No

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