

[54] MAJORITY LOGIC SYSTEM

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[51] Int. Cl.G06f 11/08, H03k 19/42
[58] Field of Search.....307/210, 204, 211, 307/220-225, 219, 232, 242, 243, 262, 269; 328/92, 96, 104, 103, 110, 60-63, 120; 325/41

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[57] ABSTRACT

Each of three redundant multiphase signal generating circuits provides a six phase square wave modulated driving pulse train that is adapted for driving the gates of a number of inverters of a standby power supply system. For each of the six phases of each channel, a simultaneous majority logic is employed to enforce agreement among like phase square waves of the several channels. Each channel operates independently of each other channel but monitors the outputs of the other channels. When and only when an individual channel finds itself in disagreement with two other channels, then such individual channel forces itself into agreement with the others. Thus three redundant six-phase signals are retained if the trigger input to one channel is lost. Even with total loss of one channel, the remaining two will continue normal operation.

21 Claims, 5 Drawing Figures

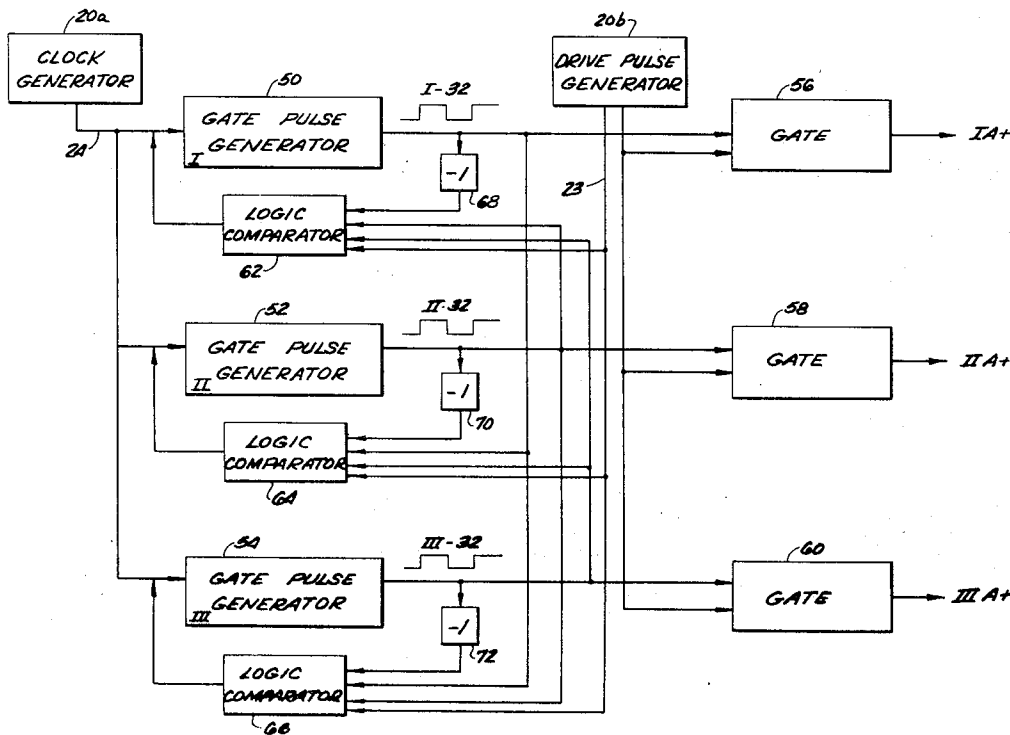
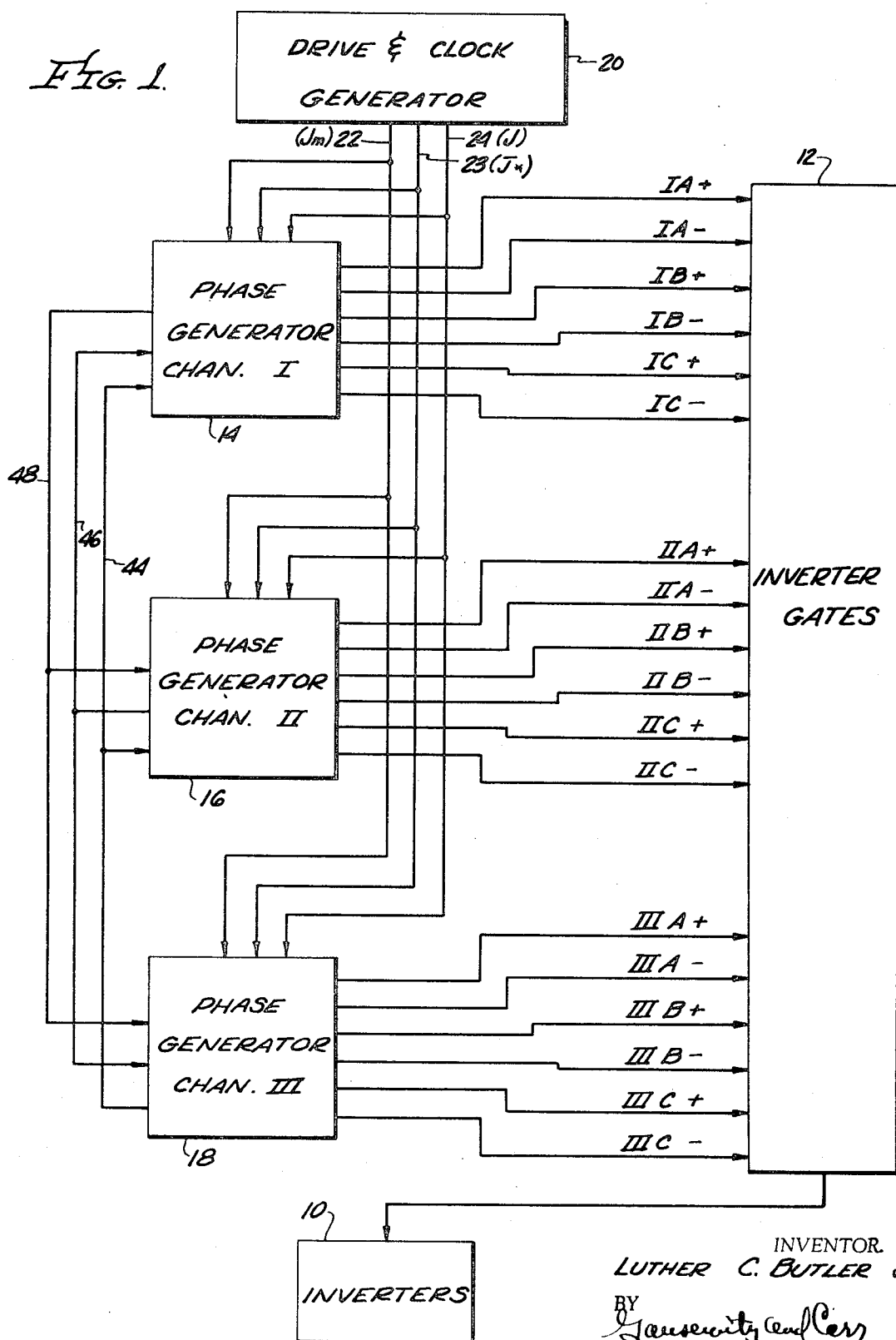


FIG. 1.



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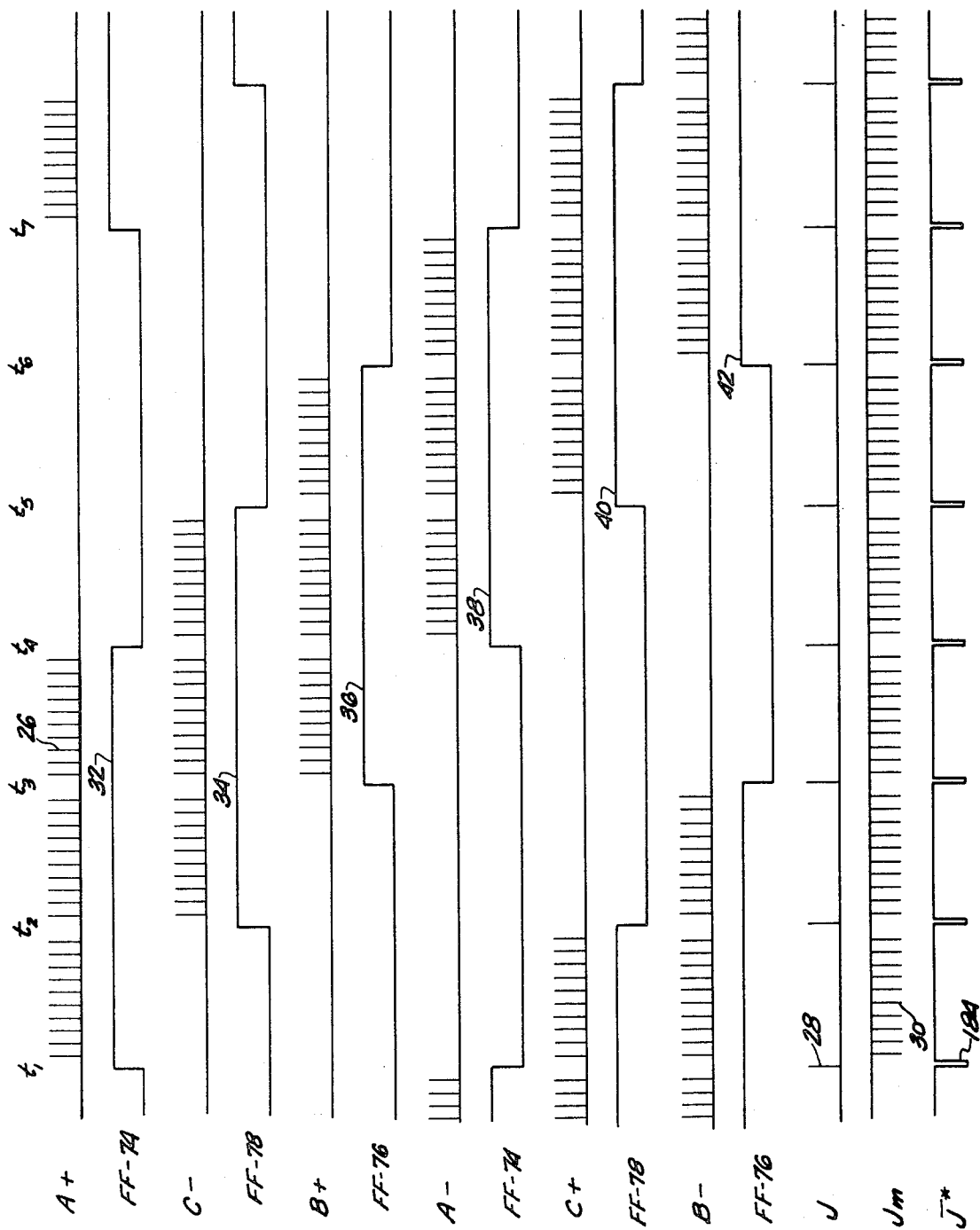


FIG. 2.

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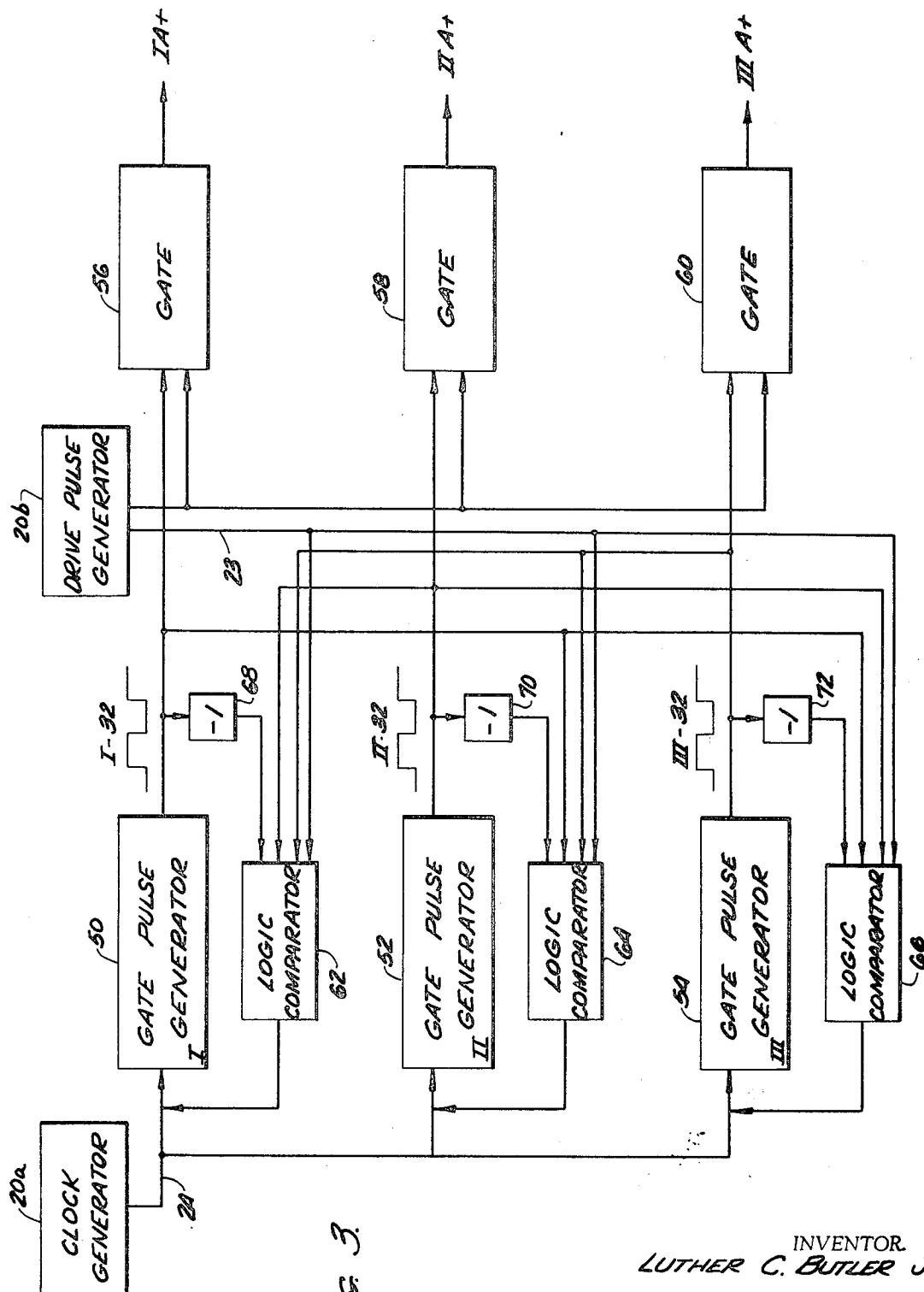


FIG. 3

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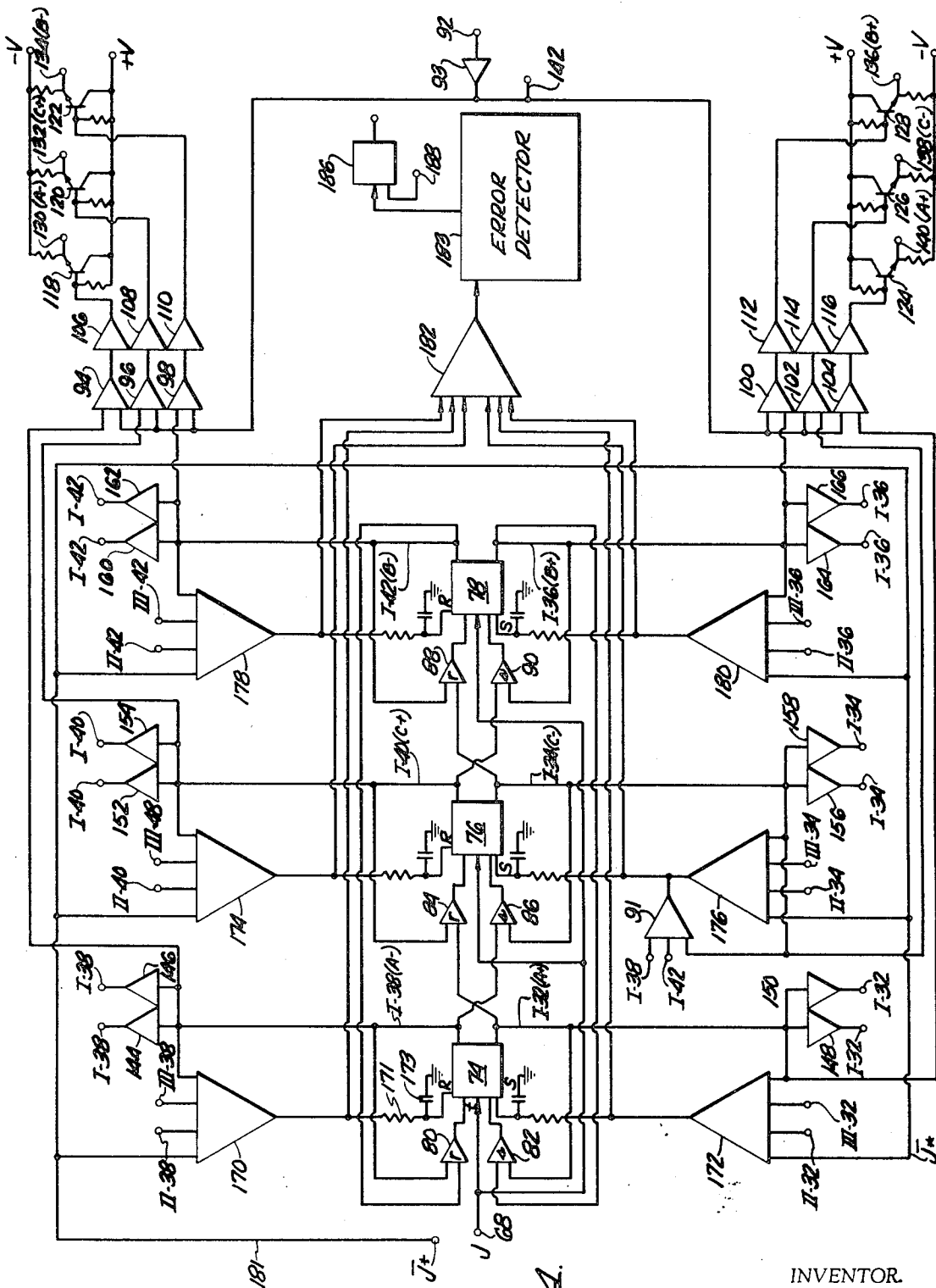


FIG. 4.

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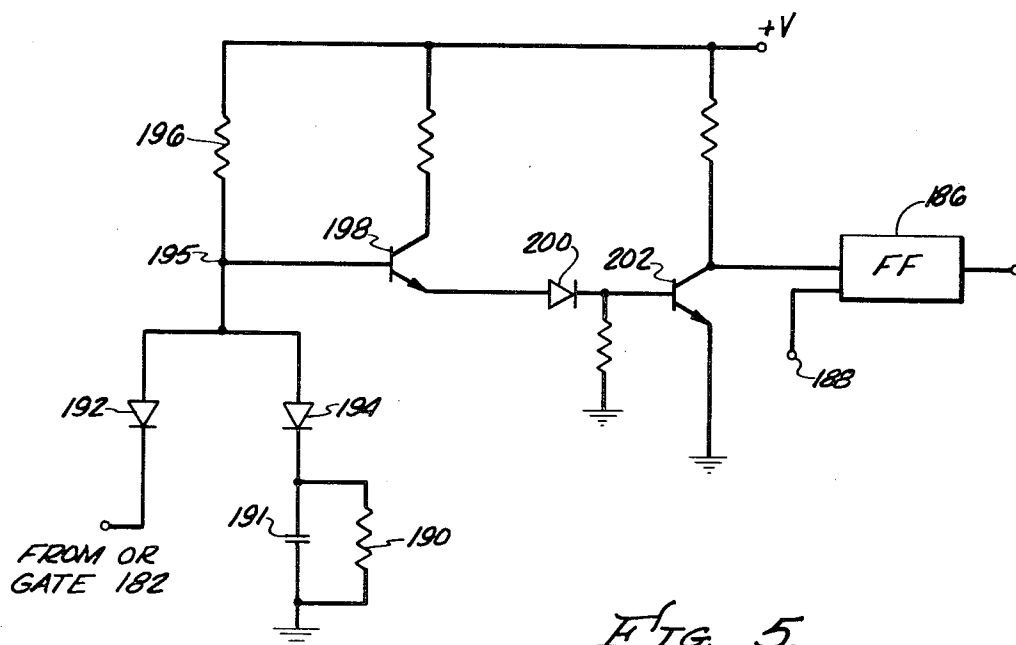


FIG. 5.

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MAJORITY LOGIC SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to redundant signal generators and more particularly concerns multiphase, multichannel generators of maximized reliability.

2. Description of Prior Art

Redundancy of control, information handling, or signal generating has long been employed where maximum reliability is required and where the expense, weight, and bulk of the redundant structures can be tolerated. Optimally, in such redundant systems, each channel individually should be capable of assuming the entire burden alone. That is, if one or all or a group of the redundant channels of control or signal generation should fail, the desired result still should be available by the use of the remaining channel or channels. With such an arrangement, the failed channel or channels are simply ignored and the system may continue to operate. However, in some systems, as for example, in those where multichannel control signals are employed for driving precision frequency sensitive systems, it is necessary, in addition to obtaining redundancy, to insure synchronization between and among the several channels of information. This is necessary in order to obtain a true redundancy wherein information from any channel can be employed together with or in place of information from other channels without loss of frequency or phase. In order to enforce such synchronization in redundant channels, it has been suggested in the past that one channel be employed as a master with the others slaved to synchronism with and from the master channel. In such an arrangement, of course, it is necessary to provide synchronizing control information from the master channel to the slave channel whereby if such interchannel control information would be lost or subject to error one or more of the redundant channels is lost or its accuracy destroyed. A similar drawback exists in those systems wherein some logic circuit outside of all channels looks at all three channels and then enforces a simultaneous synchronization upon all these channels. This use of interchannel control signals severely comprises the relative independence of operation of each of the channels, a mode of operation that is highly desirable in reliable redundant systems. Furthermore, the loss of an interchannel synchronizing signal from, in the one case the master channel, or in an alternate case the external logic circuit, may result in loss of one or more of the channels. Prior systems have introduced additional complexities and added circuitry for majority operation. A basic goal of reliable systems is the minimization of components, circuitry, and length and number of connecting lines, wherefor the simplest majority system is advantageous.

SUMMARY OF THE INVENTION

The present invention, in accordance with a preferred embodiment thereof employs a number of channels of bi-state signal generating circuitry, each being triggered for nominal synchronization of their outputs. In order to ensure synchronization of both phase and frequency among the output signals of the several channels despite the fact that all channels are triggered in synchronism, each channel compares its own output with the outputs of at least two other channels to ascertain synchronism of frequency and phase. However, in

order to maintain maximum independence of each channel, no action is taken in any channel except upon ascertaining that the instant channel disagrees with at least two other channels. If, and only if, any one channel finds that its own output disagrees with the outputs of two other channels, then and only then, such individual channel changes its output to conform to the other two channels. With this arrangement, synchronization of phase and frequency of all three channels is maintained with least compromise of independence of operation of any individual channel. No cross-channel control lines are required, and each channel may continue to operate even though another channel has failed. Alternatively, if a channel loses its triggering input, it will take its synchronization from a pair of other operating channels.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a multiphase, multichannel phase generating system according to the present invention.

FIG. 2 is a synchrograph of wave forms produced at the output of one of the channels of FIG. 1 together with signal inputs to such channel.

FIG. 3 illustrates majority logic or interchannel synchronization for one phase of all three channels.

FIG. 4 shows a typical one of the several redundant channels including details of circuitry for generating a six-phase signal and the major synchronizing circuit for such one channel, and

FIG. 5 depicts circuitry of an error detector employed in the described system.

DESCRIPTION OF THE PREFERRED EMBODIMENT

General System

Although the system of the present invention is applicable to many different situations wherein multichannel redundant multiphase signal generation and control is required, principles of the invention will be described in connection with an embodiment that has been incorporated in an uninterruptible power supply system of the type shown and described in detail in an application of Luther C. Butler, Jr., Thomas W. Grasmehr, and Robert S. Jamieson for Multichannel Control Circuit filed Feb. 5, 1970, Serial No. 8,877, now U.S. Pat. No. 3,619,661, which is incorporated by reference herein. Shown and claimed in said application for Multichannel Control Circuit is a system for generating three redundant channels of timing signals that are synchronized in frequency and phase. The present invention embodies a specific mechanization, for bi-state or multiphase signal generators or shift registers, of the invention, or aspects thereof, shown and claimed in said application for Multichannel Control Circuit, and invented jointly by Luther C. Butler, Jr., Thomas W. Grasmehr, and Robert S. Jamieson.

As illustrated in FIG. 1, such a standby, uninterruptible power supply system, includes a group of inverters 10 driven by a number of inverter gates 12 under control of three redundant channels of six phase information provided by a channel I phase generator 14, a channel II phase generator 16, and a channel III phase generator 18. The several phase generator channels are supplied with a train J_m of inverter gate drive or "comb" pulses and a train J of timing or clock pulses from a drive and clock generator 20 via lines 22 and 24.

A third pulse train $\bar{J}^*$ on line 23 is also provided to all channels from the generator 20 for purposes to be described below. Each phase generator channel provides a six phase output to the inverter gates, identified as the plus and minus phases of A, B, and C, respectively, with the output of each channel being also identified by the I, II, or III representing the individual channel.

Many types of circuits for producing fixed repetition rate pulse trains such as the trains J, $\bar{J}^*$, and J_m are well known in the art wherefore no detailed description of such pulse generators is necessary. Typical pulse generating circuits of a type that may be employed herein for generating separate sets of comb and clock pulses for each channel are shown and described in the aforesaid application for Multichannel Control Circuit, Ser. No. 8,877, now U.S. Pat. No. 3,619,661.

Although but a single drive and clock pulse generator are described herein for purposes of exposition, in an actual system embodying the present invention each phase generator channel has its own drive and clock pulse generators and these are maintained in synchronism by delayed majority logic circuitry as more particularly described in the aforesaid application for Multichannel Control Circuit.

In this standby power system, and as described in the aforesaid co-pending application, the inverter gates are driven in three-phase operation each by a pair of mutually opposite phase square wave modulated gate drive pulses. Thus it is a function of the embodiment of the invention described herein for purposes of exposition to provide a six-phase square wave modulated pulse train identified as A+, A-, B+, B-, C+, and C- in FIG. 2. For example, the modulated train of gate drive pulses (herein some times designated as comb pulses) exists or is "on" from the time identified at t_1 to t_4 , the first half cycle of this modulated signal, and is "off" for the second half cycle of the signal from t_4 to t_7 . At the latter instant, t_7 , the modulated signal A+ begins its next cycle. The time instants t_1 through t_7 , etc., are controlled by a train J of clock pulses 28 also illustrated in FIG. 2. For use with a six-phase signal that is to be produced at the outputs of each of the three channels illustrated in FIG. 1, the clock pulses 28 have a repetition rate that is six times the repetition rate of the modulating square wave of the gate drive signal A+. For an N phase signal, the train of clock pulses has a repetition rate of N times the repetition rate of the multiphase signal. In other words where, as illustrated in the drawing, one full cycle of a modulated signal of one phase is repeated every 360°, the phase interval between consecutive ones of the clock pulses in 60°. Preferably the clock pulse train J comprises one pulse 28 for every predetermined integral number of comb pulses 30 of the train J_m . The input train J_m of comb pulses is shown in FIG. 2 as comprising a series of negative going pulses 30 of which pulses occurring at each clock pulse are suppressed for reasons to be set forth below. In the embodiment described herein, the comb pulses have a frequency of 14.4 kilohertz, this number being selected as integral multiple of a nominal 360 hertz frequency of the clock pulse train J.

It will be seen, as illustrated in FIG. 2, that each modulated comb signal lags the preceding phase modulated comb signal by 60 degrees, that is, by one time interval such as $t_1 - t_2$. In other words, if the first phase of the modulated signal be considered as A+, the second phase signal C-, is initiated at t_2 and is on until t_5 . It is

then off for the next three time intervals and then on again. So too, the third phase signal B+ is initiated 60° later at time t_3 and remains on for three of the 60° intervals. This signal like each of the others is on for 180° and off for 180°. The fourth signal A- is initiated at time t_4 , and as will be noted is of opposite phase with respect to the signal A+. The fifth signal C+ is of opposite phase with respect to the modulated signal C- and is initiated at time t_5 . The last of the six phase signals B- is of opposite phase with respect to the signal B+ and is initiated at time t_6 in the illustration of FIG. 2.

Thus there is required for the inverter gates 12 and inverter 10 of FIG. 1, and concomitantly, there is provided by each of the redundant phase generator channels 14, 16, and 18, the indicated set of six phase signals comprising modulated comb pulses in six phases successively shifted by 60°. It will be readily appreciated that a six phase drive is required for a three phase output of the inverters, each of such three phases being displaced by 120 degrees from the others.

As previously indicated, the present invention is concerned with the several channels of phase generator 14, 16 and 18 illustrated in FIG. 1. The various gates, inverters, and comb and clock generator 20 are briefly illustrated solely to afford a better understanding of the nature and requirement or the particular phase modulated output of the type illustrated in FIG. 2. Each phase generator channel produces a number of phase control or modulator gate pulses indicated at 32, 34, 36, 38, 40, and 42 in FIG. 2 for the respective phases A+, C-, B+, A-, C+, and B- of the modulated signals.

The inverters and gates for which the present plural channel phase generating system is specifically designed require redundant channel multiphase signals, with the signals of the several channels being exactly in phase and at the same frequency as compared to corresponding signals of each of the other channels. Accordingly, each phase generator channel sends out its own output signal to each of the other channels via lines 44, 46, and 48 (FIG. 1). It will be readily understood that although but a single line is shown connecting each channel to the other two channels, the indicated flow of information occurs for each phase of the multiphase signal produced by the channel. This arrangement will be described in greater detail in connection with the detailed illustrations of FIG. 4.

The phase generator of each channel normally operates independently of each other in response to the comb and clock signals provided to it directly via lines 22 and 24. Nevertheless, each channel by means of information conveyed on lines 44, 46, and 48 monitors the operation of the other two channels. If, and only if, any one channel, channel II for example, should find that its phase control signal for any of its six phases is not in agreement with the corresponding phase control signal from both of the other channels then such channel, channel II in this example, will change its phase control pulse of such particular phase in order to conform with the corresponding signals of the other channels. However, should the individual channel find a disagreement with but one of the other channels then no action is taken and the disagreement is ignored.

Majority Logic — Three Channels, One Phase

Majority synchronizing logic for synchronizing phase and frequency of one phase of the output of all three channels is illustrated in FIG. 3. The several channels

for one phase of the signals generated thereby include a channel gate pulse generator 50, 52, and 54, respectively, providing square wave signals, such as that illustrated in FIG. 2 and indicated at 32, to channel modulator gates 56, 58, and 60, respectively. The gate pulse generators are triggered by clock pulses provided on line 24 from the clock generator 20a which forms a part of the drive and clock generator 20 of FIG. 1. Gates 56, 58, and 60 each has a second input thereto from the common line 22 on which appear the comb or inverter gate drive pulses from the drive pulse generator 20b that forms a part of the drive and clock generator 20 of FIG. 1. Each phase generator channel also includes a logic comparator 62, 64, and 66 and an inverting circuit 68, 70, and 72, respectively. Each logic comparator comprises a coincidence gate having first and second inputs thereto from the outputs of the other two channels. The third input to the logic comparator is provided from the output of its own channel via the inverting circuit. Thus, for example, logic comparator 62 of channel I receives as a first input the signal II-32 from channel II, and as a second input the third channel output III-32. The third input to logic comparator 62 comprises the inverted version of its own channel output I-32.

The output of each logic comparator is fed back to the input of the corresponding gate pulse generator to effect a change of state of the flip-flop forming part of the generator when the comparator provides an output indicating disagreement of its own channel output with the outputs of two other channels. For example, if all channels are in synchronism and in phase, logic comparator 62 receives a high input from the signal II-32 and a high input from the third channel signal III-32. Via the inversion circuit 68, it receives a low input from the high channel I signal I-32. Accordingly, the coincidence circuit 62 provides no actuating output. However, should the channel I signal I-32 be low when the other two like phase signals are high, the comparator 62 receives three high inputs and thus provides an actuating input to the gate pulse generator to force the generator of this channel into agreement with the other two channels. The operation of the logic comparators 64 and 66 for channels II and III is the same as that described in connection with channel I whereby each of these channels II and III continuously monitors the outputs of both of the other channels and when it finds itself to be in disagreement with both of the other channels forces a change in its own gate pulse generator to enforce agreement between or among all of the channels.

Monitoring action must be inhibited during the time of normal switching in response to clock pulse J although it is desirable to carry out the monitoring as soon as possible after the signal that is to be controlled, if at all, by the monitoring has become true or gone high. Accordingly, each of the logic comparators 62, 64, and 66 has a fourth input via line 23 from the clock generator that momentarily disables the logic comparator during the clock pulse and for an instant immediately following occurrence of a clock pulse on line 24. Thus, the monitoring is inhibited during the clock pulse and for a time sufficient to complete the switching that may occur in response to the clock pulse.

Each of the comb pulses 30 that occurs in coincidence with one of the clock pulses 28 is suppressed. Suppression of the comb pulse at 360 cycle intervals

ensures against the use of possibly weakened inverter gate drive pulse since such pulse, in going through the gate 56, 58, or 60, may be severely attenuated or shortened if it occurs at a time when the modulating square wave comprising the second input to such gate is changing.

Details of One Channel Six Phases

Illustrated in FIG. 4 are details of one complete channel including gate pulse generator and modulator gate together with the logic comparators for each of the six phases of an exemplary channel, channel I. It will be understood that each of the other two channels, channels II and III, is identical in every respect to channel I illustrated in these figures.

The gate pulse generator comprises a conventional shift register known as "Johnson" or "Switch-tail" counter including flip-flops or bi-stable multivibrators 74, 76, and 78. The flip-flops are conventional circuits which provide mutually exclusive outputs in any one condition as is well known. Each flip-flop has direct set and reset terminals S and R which, when low, will shift and hold the flip-flop in its set or reset state respectively providing at the two flip-flop output terminals, respectively, high and low outputs for the set condition of the flip-flop and respectively low and high outputs for the reset condition of the flip-flop. In addition to the direct set and reset terminals responsive to low or negative signals, each flip-flop has a clock input, t , and a set and reset input gate indicated at s and r . Each of the set and reset input gates has two inputs which, when high, enable the input gates and allow the flip-flop to be toggled or to change its state when the clock or triggering input goes low. That is, upon the fall of the clock input t , the set or reset gate that is enabled by a high at its two inputs will provide a signal that allows the flip-flop to be set or reset if it is not already in such condition. Thus, the direct set and reset terminals are responsive to steady-state low signals, and the set and reset input gates are enabled by high signals to cause the flip-flop to be toggled on the fall of the clock signal thereto. Typical flip-flops of the type employed in the described system are available as microcircuit chips designated MC945F, G, MC845F,P,G, MC948F,G, MC848F,P,G, described in "Integrated Circuit Data Book," First Edition, August, 1968, Motorola Semi-Conductor Products, Inc. Thus flip-flop 74 provides at one output terminal the A-phase signal I-38, and at its second output terminal, the opposite phase A+ signal I-32. Similarly, flip-flop 76 provides the opposite phase outputs I-40 (C+) and I-34 (C-), and flip-flop 78 provides the opposite phase outputs I-42 (B-) and I-36 (B+).

The train J of positive clock pulses 28 is provided to each channel at input terminal 68, whence it is fed to each of the set and reset input gates 80, 82 of flip-flop 74. Each of the flip-flops has a similar pair of reset and set input gates, 84, 86 for flip-flop 76, and 88, 90 for flip-flop 78, and each flip-flop receives as its triggering input clock pulses from the input clock pulse train J. The outputs of each flip-flop are fed to respectively opposite side input gates of the succeeding flip-flop of this shift register, and the outputs of the final flip-flop 78 are fed back to the same side input gates of the first flip-flop 74, as shown in the drawings. Each of the input gates 80 through 90 of the several flip-flops receives as its second input a feedback signal from the output on the same side of the same flip-flop. With the illustrated

connection of these flip-flops, the states of the shift register (at the A+, C-, and B+ outputs) will be as indicated in the following table:

Count	FF74 A+	FF76 C-	FF78 B+
1	1	0	0
2	1	1	0
3	1	1	1
4	0	1	1
5	0	0	1
6	0	0	0
7	1	0	0

It will be seen that the shift register flip-flops assume the indicated series of states for the first six counts of input clock pulses, and then upon the seventh clock pulse, resume the initial state and start counting anew. These states correspond to the flip-flop outputs illustrated in FIG. 2 where the pulse 32, the output of flip-flop 74, is true for the first three counts and is false for the next three counts. Phase control pulse 36, the output of flip-flop 78, is false for the first two counts, true for the next three counts, and false for the next two counts. Likewise, phase control pulse 34, the output of flip-flop 76, is false for the first count as illustrated in FIG. 2, true for the next three counts, and false for the next three counts. Each pulse is, of course, true for three counts and false for three counts where each count represents 60° of a cycle and each signal exists in one state for one half cycle. The opposite phase signals 38, 40, and 42 have states opposite to those indicated in the above table.

In order to prevent the counter from getting into or remaining in its two unused counts, namely, 0 1 0 and 1 0 1, a NAND gate 91 is provided, having inputs (via connecting leads not shown) from I-38 and I-42 of flip-flops 74 and 78 and a third input via the illustrated lead from I-34 of flip-flop 76. This gate provides an output to set flip-flop 76 whereby the two unused counts are avoided. NAND 91 and all of the NAND gates illustrated herein are "Not AND" circuits that provide a low output when all inputs are high and provide a high output when any input is low.

The comb signal, a train of negative going pulses 30 as illustrated in FIG. 2, is fed to each channel at an input terminal 92 and thence inverted in a gate 93 and fed as one input to each of six modulator NAND gates 94, 96, 98, 100, 102, and 104 of the several phases. Each of the six phase control pulse outputs of the three flip-flops is fed as a second input to a different one of the modulator gates 94 through 104, whereby the output of each of these gates, fed through a series of NAND gates 106 through 116 and through a set of emitter follower transistors 118 through 128, provides at channel output terminals 130 through 140 the six phase signals IA+, IA-, IB+, IB-, IC+, and IC- as illustrated in FIG. 1. Thus the modulated comb signal of FIG. 2 is produced by combining the phase control outputs of the flip-flops with the comb signal in the several modulator gates 94 through 104. An input terminal 142 is employed to suppress the comb signal within the system during startup and shutdown of the inverter system.

In order to provide information for the monitoring of channel I phases by each of the other two channels, each flip-flop output is fed via a pair of inverting buffer circuits or NAND gates 144 and 146, 148 and 150, 152 and 154, 156 and 158, 160 and 162; and 164 and 166, to logic comparators of the other two channels. Thus, for example, the output of flip-flop 74, I-38, is fed to

NAND gates 144 and 146 from whence it is sent via lines (not shown in FIG. 4) to each of channels II and III, respectively. Similarly, the other output of flip-flop 74 identified as the signal I-32 is fed via inverting circuits 148 and 150 to the comparator of each of the channels II and III that compares the phase control pulse signal which is of the same phase as the signal 32.

Just as each output of each flip-flop of the channel I shift register is fed via the indicated inverting circuits to each of the other channels, so too each output of each flip-flop of the shift registers of each other channel is fed to the logic comparison circuits of the channel I phase generator. These logic comparison circuits comprise four input NAND gates 170 through 180, each receiving a first input from the corresponding side of the flip-flop of its own channel, second and third inputs from the inverted outputs of the corresponding side of the corresponding flip-flops of like phase of the other two channels, and a fourth input comprising a momentary disabling signal on line 181 to be described hereinafter.

The inverting buffer gates 144 through 166 feed the state of the several flip-flops in a given channel to the other two channels. The coincidence gates 170 through 180 force majority agreement among the three shift registers. Each of these gates monitors outputs from the other two channels and compares these with the output of its own corresponding flip-flop. It provides no actuating signal when all agree. Where there is a unanimous agreement in coincidence gate 170, for example, the input from channel II, the signal indicated as II-38, and the input from channel III, indicated as III-38, are both high, having been inverted by their corresponding output buffer gates, whereas the signal from flip-flop 74, I-38, is low. Thus no switching output is provided from the coincidence gate 170. If, on the other hand, when the inputs II-38 and III-38 are both high, the third input to this gate, the signal I-38, is also high, a disagreement exists. That is, the channel I signal is in disagreement with both of the other two channels. In this situation, unless the gate disabling signal appears on line 181, gate 170 provides a negative signal into the direct reset terminal of flip-flop 74 to reset this flip-flop thereby forcing it into agreement with the corresponding flip-flops of the other two channels. This same logic comparison arrangement is repeated for the direct reset input sides of the other two flip-flops 76 and 78 of the channel and is also repeated for all of the direct set terminals of all flip-flops so that majority agreement is enforced upon each of the six phases.

The signal on line 181 which is applied as the fourth input to each of the coincidence gates 170 through 180 comprises the train $\bar{J}^*$ of negative pulses 184 illustrated in FIG. 2. These pulses 184 are produced in synchronism with and of opposite phase relative to the pulses of clock pulse train J. The pulses 184 are, in effect, inverted and stretched versions of the clock pulses. The pulses are stretched (extended in time) by conventional circuitry so that switching of the flip-flop cannot be forced by the majority logic until the flip-flop has had a chance to be switched by the clock pulses J and the circuit has had time to establish a quiescent state.

Accordingly, the clock pulse train J, when it goes low, normally sets or resets each of the three flip-flops into its correct state, that is, causes the flip-flop to change in accordance with the logic provided by the set and reset input gates 80 through 90. If this clock pulse

is absent or if a malfunction occurs in the set or reset input gate to the flip-flop, the latter may not have achieved its proper state. In such a situation, the majority action of the coincidence gate acting upon the direct set or direct reset inputs forces agreement. Immediately after the termination of the clock pulse 28 and before the next one of the comb pulses 30 (it will be recalled that the comb pulses occurring in coincidence with clock pulses J have been suppressed), the pulse 184 on line 181 goes high to enable the coincidence gate 170 which then provides a negative going signal to the direct reset input of the flip-flop and forces it into agreement with the corresponding flip-flops of the other two channels. The pulse train $\bar{J}^*$ is a stretched and inverted version of the clock pulse train. Nevertheless, these pulses are short enough so that the forced agreement will occur before the first comb pulse appears at the input terminal 92.

The enabling pulse train $\bar{J}^*$ is fed via line 181 as the fourth input to each of the coincidence gates 170 through 180 whereby all of the logic comparators act in a substantially similar manner. Accordingly, this phase generator channel may continue to contribute to the production of modulated comb pulses via its output emitter followers even if the clock pulse input thereto is absent or if the input circuits of the several flip-flops fail to operate properly.

Alarm

A multiple input OR gate 182 has an input from the outputs of each of the coincidence logic gates 170 through 180, and accordingly, monitors the occurrence of disagreements of this channel with the other two channels. The output of gate 182 is high when any one of its inputs is low. Otherwise, when all inputs are high, this output is low. This will be recognized as the operation of the circuit of the described NAND gates which provide a logical OR function and inversion. If disagreement occurs upon one or two or three successive ones of clock pulses 28, no action need be taken. However, if the disagreement continues beyond three clock pulses or, if the output of any one of the coincidence gates 170 through 180 is continuously high, an error detector 183 having an input from the output of OR gate 182 will provide an error signal to an alarm flip-flop 186 which produces an out-of-synchronism alarm for this phase generator channel. By application of a signal at terminal 188, the error flip-flop 186 may be reset.

The error detector circuit 183 (FIG. 5) is a timing or counting circuit having a parallel resistance capacitance circuit comprising a resistor 190 and a capacitor 191 connected between ground and the input of a substantially conventional coincidence gate. If a predetermined number, four or more for example, of pulses at the 360 hertz clock rate appear at the output of OR gate 182, capacitor 191 is charged sufficiently to cause the timing circuit 183 to produce an output that sets the error flip-flop, and thus turns in the out-of-synchronization alarm.

As illustrated in FIG. 5, pulses from the output of OR gate 182 are fed to the cathode of a diode 192 that provides a first of two inputs to the coincidence part of this circuit. The second input is provided from capacitor 191 to a second input diode 194. The common connection of the diode anodes, point 195, is connected via a resistor 196 to a positive potential +V and also to the

base of an NPN transistor 198 having its collector resistively connected to +V. The emitter of transistor 198 is connected via a diode 200 to the base of a second NPN transistor 202 having its collector resistively connected to +V and its emitter connected to ground. The output of this circuit, at the collector of transistor 202, is connected to trigger the alarm flip-flop 186.

When no out-of-synchronization signal is detected by OR gate 182, the cathode of diode 192 is low, this diode conducts through resistor 196, point 195 is low, and diode 194 is back biased. Capacitor 191 receives no charge. Upon detection of an out-of-synchronization signal, the output of OR gate 182 goes high, diode 192 is cut off, and diode 194 momentarily conducts through resistor 196 to add an increment of charge to capacitor 191. Point 195 remains below the level at which the normally cut off transistor 198 will conduct. Second and third successive out-of-synchronization signals add second and third charge increments to capacitor 191. The values of circuit components and potentials are so chosen that such a third successive charge increment provides a high signal on the cathode of diode 194 that is substantially equivalent to a logical one for this coincidence circuit. Therefore, if a fourth successive out-of-synchronization signal should occur, both input diodes 192 and 194 are now back biased, point 195 goes high, and transistor 198, normally cut off, conducts. This causes conduction of normally cut off transistor 202 to provide an alarm signal to the flip-flop 186. It will be understood that this circuit will also provide an alarm upon occurrence of a continuous high at the cathode of diode 192. Of course, the parameters may be chosen to cause an alarm upon occurrence of a number of out-of-synchronization signals other than the number four, chosen for purposes of exposition.

To ensure operation of the OR gate 182, pulse lengthening RC networks are incorporated between the direct reset and set lines of each of the three flip-flops and the outputs of logic comparator gates 170 through 180. Thus, for example, on the reset input side of flip-flop 74 there is included a resistor 171 connected between the output of gate 170 and the direct reset input to the flip-flop. A capacitor 173 is connected between this input and ground. The time constant of this RC network is chosen such that an error signal, a low at the output of gate 170, will be retained for a period of time sufficient to operate and pass through OR gate 182. Each of the other five inputs to the direct set and reset terminals of these three flip-flops have similar RC networks with similarly chosen time constants. This integrating circuit is employed because the flip-flops switch very rapidly and a signal at the output of the comparators may be too short to pass through the OR gate 182.

SUMMARY OF THE INVENTION

There has been described an improved multiphase redundant signal generator wherein each channel of the multiphase generator has a maximum independence and freedom from each other channel, but nevertheless, monitors each of the others to enforce synchronization of frequency and phase among the channels. If any one channel finds itself in disagreement with both the other channels, it changes to force itself into agreement. However, if the other two channels which are being compared do not agree with each other, no action is taken. Thus each channel may continue to operate even though one of the others suffers

from a malfunction, wherefore optimum reliability is attained.

The foregoing detailed description is to be clearly understood as given by way of illustration and example only, the spirit and scope of this invention being limited solely by the appended claims.

I claim:

1. A majority logic system comprising a plurality of channels of shift registers, means for triggering said shift registers to generate signals in synchronism, and means for comparing signals from the shift register of one of said channels with signals from the shift registers of two of the other said channels to effect synchronism of all of the compared signals.
2. A majority logic system comprising a plurality of redundant multiphase signal generating means, each comprising means for generating a bi-state signal having components of mutually different phase, means for transmitting each component of said signal to at least two of the other generating means, means for comparing the states of each component of signals received from other signal generating means with the states of each corresponding component of its own bi-state signal, and means for changing the state of any one component of its own bi-state signal when it does not agree with the state of the corresponding components of two other signals.
3. A majority logic system comprising a plurality of redundant and nominally synchronous bi-state signal handling circuits, and logic means within each individual circuit responsive to the outputs of at least two of the other circuit outputs for changing the state of the output of such individual circuit only when it differs from the state of the output of more than one of the other circuits.
4. The system of claim 2 including a source of clock signals, each circuit comprising
 - a first flip-flop connected to be set and reset in synchronism by said clock signals, said logic means for each individual circuit comprising
 - a coincidence gate responsive to a signal of one state from the flip-flop of such individual circuit and to signals of opposite states from the flip-flops of at least two other circuits, and
 - means for momentarily disabling said coincidence gate for a time during and immediately following each of said clock signals.
5. The system of claim 4 including a source of drive pulses, each circuit comprising
 - a second and third flip-flop,
 - means for connecting said flip-flops to change state upon each fourth clock signal to provide a three phase output,
 - second and third logic means for said second and third flip-flops, each substantially similar to said first mentioned logic means and each connected with second flip-flops and third flip-flops of a plurality of said circuits in the same manner as said first mentioned logic means is connected with said first flip-flops,
 - a plurality of drive pulse coincidence gates, each having a first input from an individual one of the flip-flops of one of said signal handling circuits, and each having a second input from said source of drive pulses whereby a plurality of redundant sets

of multiphase modulated drive pulses is provided from said drive pulse gates.

6. A multiphase signal handling circuit comprising means for providing clock signals, means for providing a drive signal comprising a train of drive pulses, and a plurality of modulating channels responsive to said clock and drive signals for providing a number of redundant sets of said drive signals modulated with mutually different phases, each said channel comprising means for generating a plurality of modulator gate signals of respectively different phases, means for comparing modulator gate signals of like phase from at least three of said channels and mutually synchronizing compared signals, and means for modulating the drive signal by each said gate signal.
7. A redundant multiphase signal handling system comprising
 - means for providing a train of clock pulses at a repetition rate of N times the repetition rate of said multiphase signal,
 - where N is the number of phases of said multiphase signal, and
 - a plurality of channels of phase generators each comprising
 - means responsive to said clock pulses for generating N phase control pulses each being phase displaced from a phase control pulse of earlier phase by the interval between clock pulses,
 - logic means for each individual phase of phase control pulses for comparing such individual pulse with a corresponding pulse of at least two other channels, and
 - means responsive to said logic means for changing such individual pulse when disagreement with said two other channel compared pulses occurs.
8. The system of claim 7 including
 - means for providing a train of drive pulses, each said channel including
 - a plurality of modulators, each modulator having a first input from said drive pulses, and a second input from a different phase of said phase control pulses.
9. The system of claim 8 wherein each channel includes
 - means for monitoring the output of said logic means, and
 - means responsive to said monitoring means for indicating occurrence of said disagreement at a plurality of successive clock pulses.
10. The system of claim 9 wherein said means for indicating occurrence of disagreement comprises
 - a capacitor for storing signals indicating disagreement, and means responsive to a predetermined charge on said capacitor for generating an alarm signal.
11. The system of claim 7 wherein said phase control pulse generating means of each channel comprises
 - a shift register having a triggering input from said clock pulses and having a plurality of stages, each stage having outputs providing two of said phase control pulses of mutually opposite phase, said logic means for each individual channel comprising a first coincidence gate for each of said shift register stages having inputs from one of said stage outputs and from corresponding outputs of corresponding stages of said two other channels, and

a second coincidence gate for each of said shift register stages having inputs from the other of said stage outputs and from corresponding outputs of corresponding stages of said two other channels, said means for changing an individual pulse comprising means responsive to each of the coincidence gates for changing the state of the corresponding shift register stage.

12. The system of claim 11 including means for momentarily disabling each said coincidence gate during and immediately after each clock pulse.

13. The system of claim 11 wherein each channel includes an OR gate responsive to each said coincidence gate for providing an out of synchronization signal, first and second input diodes having first and second input terminals and having output terminals connected in common, said second input terminal being connected to said OR gate to receive said out of synchronization signal, a switching device having an output terminal and having an input connected to said commonly connected diode output terminal, and a parallel capacitor-resistor circuit connected to the input terminal of said first diode, whereby a signal of predetermined character at the input terminal of the second diode will charge the capacitor sufficiently to provide an input to the first diode.

14. A multichannel, multiphase signal circuit comprising a source of clock pulses, a source of drive pulses, and a plurality of channels of phase generators, each channel comprising first, second, and third flip-flops connected to form a shift register that shifts in a predetermined sequence in response to an input from said clock pulse source, each flip-flop having a direct set and reset input, and a first and second output, a plurality of modulator gates, each having a first input from said source of drive pulses, and a second input from a respective one of said first and second outputs of said first, second, and third flip-flops, a plurality of output gates responsive to a first output of each flip-flop for transmitting said first output of such flip-flop to each of the other channels, a plurality of output gates connected to the second output of each flip-flop for transmitting the second output of such flip-flop to each of the other channels, a coincidence gate for each direct input of each flip-flop, each coincidence gate having an output connected to one of the direct inputs of the flip-flop, a first input from the first output of the flip-flop, and second and third inputs from corresponding outputs of corresponding flip-flops of each of two other channels.

15. The circuit of claim 14 including means for disabling each of said coincidence gates of each channel for an interval that begins with each

clock pulse and that terminates before the next one of said drive pulses.

16. The circuit of claim 14 wherein said drive pulses have a repetition rate that is a multiple of the repetition rate of said clock pulses, and wherein each drive pulse that occurs in coincidence with a clock pulse is suppressed.

17. The system of claim 14 including an OR gate having an input from each of the outputs of each of the coincidence gates, and a timing circuit having an input from the output of the OR gate for providing a synchronization error output signal upon receipt of a predetermined minimum number of pulses from the OR gate or upon receipt of any continuous output signal from the OR gate.

18. The system of claim 17 including an integrating circuit connected between the output of each of said coincidence gates and said OR gate.

19. A redundant majority logic system comprising a plurality of redundant channels of signal generating circuits, means for triggering each of said circuits to generate signals in mutual synchronism, means for comparing signals from the circuit of one of said channels with signals from the circuits of two of the other said channels, and means responsive to said comparing means for enforcing synchronism of the signal of said one channel with the signals of said other two channels when the signal of said one channel is out of synchronism with the signals from both of said other two channels.

20. A majority logic system comprising a plurality of channels of shift registers, means for triggering said shift registers to generate signals in synchronism, and means for comparing signals from the shift registers of one of said channels with signals from the shift registers of two of the other of said channels to effect synchronism of all of the compared signals, said last-mentioned means comprising means for changing the signal from said one channel only when it is out of synchronism with signals from both of said other channels.

21. A multiphase signal handling circuit comprising means for providing clock signals, means for providing a drive signal comprising a train of drive pulses, and a plurality of modulating channels responsive to said clock and drive signals for providing a number of redundant sets of said drive signals modulated with mutually different phases, each said channel comprising means for generating a plurality of modulator gate signals of respectively different phases, means for comparing modulator gate signals of like phase from at least three of said channels and mutually synchronizing compared signals, and means for modulating the drive signal by each said gate signal, each said comparing means comprising comparator means within each individual channel for generating a disagreement signal only when the gate signal of such individual channel fails to agree with the gate signals of like phase from at least two other channels, and means responsive to said disagreement signal for changing the gate signal of such individual channel to agree with said signals of like phase from said other channels.

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