United States Patent

Zeph

[15] 3,699,763

[45] Oct. 24, 1972

[54] **24-HOUR DIGITAL CLOCK**

[72] Inventor: **David L. Zeph,** Indianapolis, Ind.

[73] Assignee: **The United States of America as represented by the Secretary of the Navy**

[22] Filed: **July 6, 1971**

[21] Appl. No.: **159,856**

[52] **U.S. Cl.** .....**58/23 R,** 58/50, 235/92 T, 340/373

[51] **Int. Cl.** **G04c 3/00,** G04b 19/30

[58] **Field of Search**...58/23 R, 23 A, 24 R, 34, 50 R; 235/92 T

[56] **References Cited**

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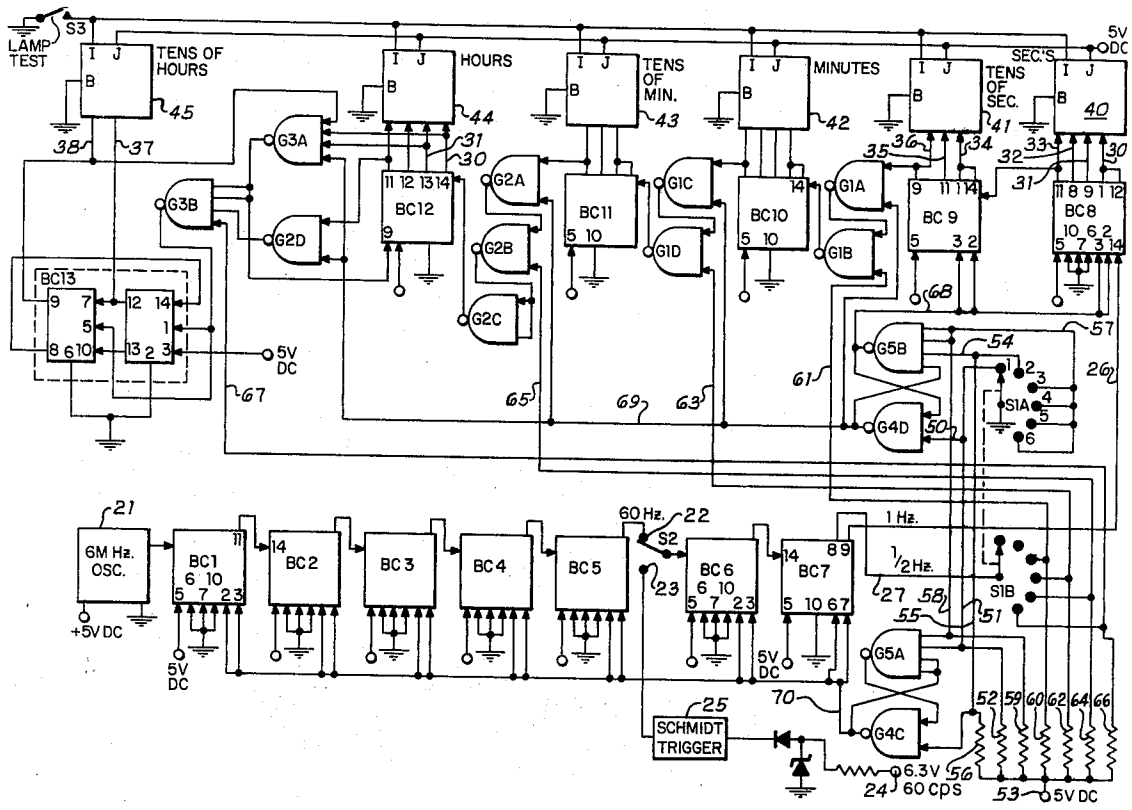
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[57] **ABSTRACT**

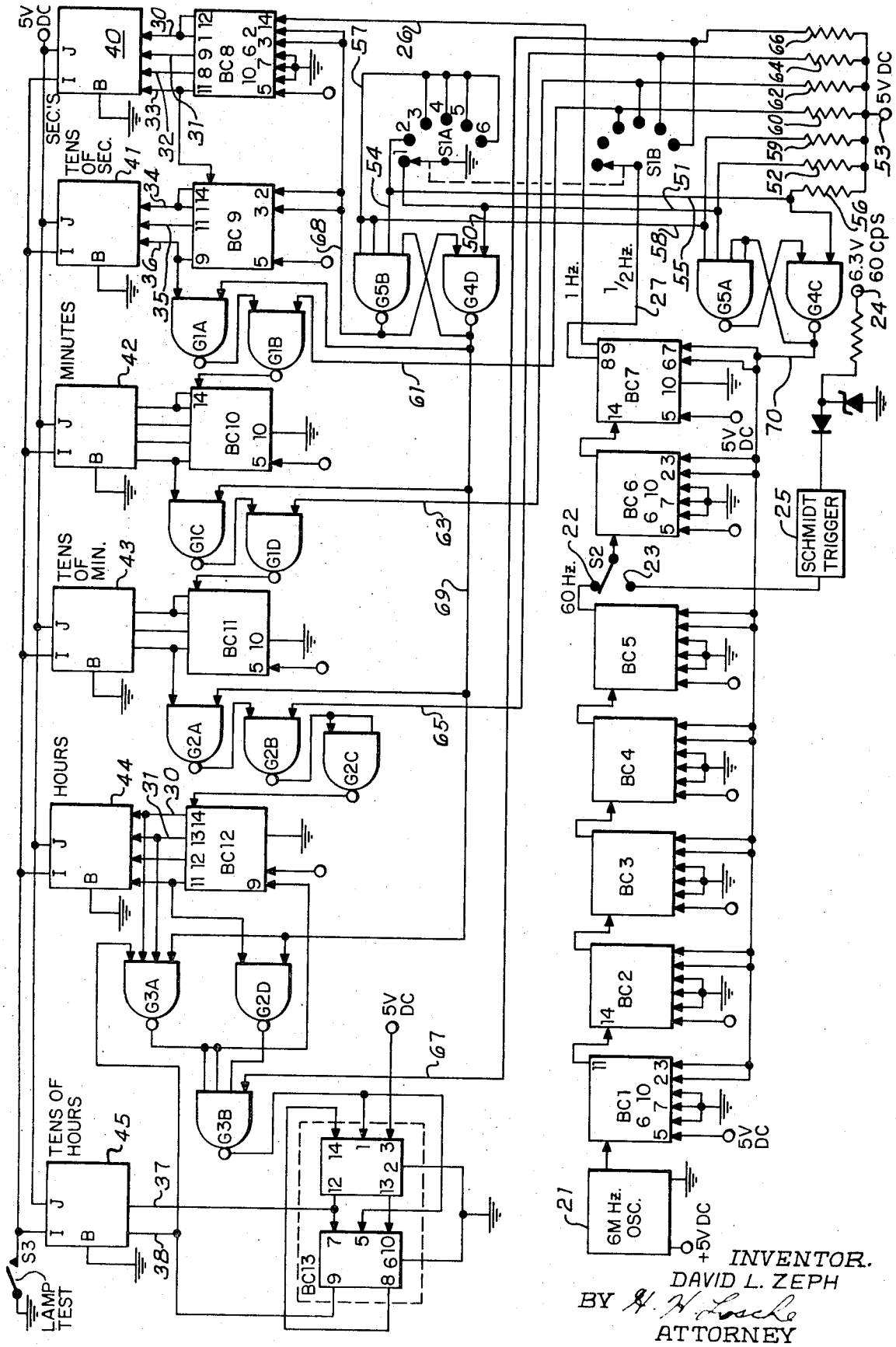
A 24-hour digital clock having a plurality of division counters driven from a stable frequency which are coupled to seven line segment decoder-drivers. A selector switch coupled to the counters allows setting of the minutes, tens of minutes, hours, and tens of hours to a precise time signal while resetting all other counters.

9 Claims, 1 Drawing Figure



PATENTED OCT 24 1972

3,699,763



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24-HOUR DIGITAL CLOCK

STATEMENT OF GOVERNMENT INTEREST

The invention described herein may be manufactured and used by or for the Government of the United States of America for governmental purposes without the payment of any royalties thereon or therefor.

BACKGROUND OF THE INVENTION

This invention relates to digital display time pieces and more particularly to solid state micro-miniature circuited digital readout clocks of high accuracy which are readily settable in time readout and operable accurately in hostile environments.

The present recording sets for receivers of meteorological data and the like utilize digital clocks with mechanical movements which are extremely susceptable to vibrations encountered in a vehicle environment, such as in an aircraft or on shipboard. Available electronic clocks require multiple rotary, toggle, or pushbutton switches to control circuitry to "set" the clock to desired time readout. These are very troublesome disadvantages in the operation of the receiver equipment often destroying simplicity when it is needed most.

SUMMARY OF THE INVENTION

In the present invention a plurality of division binary counters are used coupled to a high frequency stable oscillator to divide the high frequency count down to 60 cycles per second and thence down to one cycle and one-half cycle per second. At the 60- cycle point in the division counter series is included a switch to alternately switch in low voltage house current which will be further divided down to one cycle per second providing a semiprecision external source to drive the digital clock. The one cycle per second frequency is applied to the first of a series of decoder, driver binary counter circuits which add up the frequency pulses in a decade counter, the 10s output of which is added in a divide-by-six binary counter to obtain the count of seconds and tens of seconds to add to a maximum of 59 and then reset to zero. The series of decoder/drivers in like manner provide the count for the minutes, 10s of minutes, hours, and 10s of hours, the latter of which is specially circuited by NAND gates to reset from 23 hours to zero hours on the pulse following 59 minutes and 59 seconds. A six-contact, double-gang selector switch is used to reset the minutes and hours of the digital clock. The digital readouts of hours, minutes, and seconds are from decade digital readout devices which give a visual running time readout that is not disturbed by vibrations, being solid state, and which are as accurate as the stabilized or external frequency inputs. It is accordingly a general object of this invention to provide a 24-hour digital clock that will provide digital readout of high precision that can be "set" to desired times with a single six-position selector switch.

BRIEF DESCRIPTION OF THE DRAWING

These and other objects and the attendant advantages, features and uses will become more apparent to those skilled in the art as a more detailed description proceeds when considered along with the single FIGURE of drawing illustrating in block circuit schematic of the invention with arrows indicating the direction of information.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to the FIGURE of drawing, the circuit is started with a 6 magahertz (MHz) precision crystal oscillator **21** having its output coupled to the first of a series of binary counters BC1 through BC5 which form a divide by 100,000 chain producing a 60 Hz on the output of BC5 at contact **22** of a switch S2. The binary counters BC1 through BC5 are commercially available flatpacs, one type being available from Texas Instrument, Incorporated under the catalogue number of SN7490 N and will not be discussed further in their internal operation since they are well-known to have the function of counting. The second frequency input to switch S2 contact **23** is from an input terminal **24** to which is adapted to be applied a 60 cycles per second (cps) at any desirable voltage, herein shown to be 6.3 volts. This 60 cps frequency is applied through a Schmidt trigger **25** to provide a 60 Hz square wave voltage at terminal **23**. The switch S2 may therefore be switched to contact **22** to obtain an internal precision 60 Hz frequency or to terminal **23** to obtain a semiprecision 60 cps frequency for the system. The switch blade of switch S2 is coupled as an input to two series coupled binary counters BC6 and BC7, the output on terminal **9** of BC7 being divided down further to produce a precision 1 Hz frequency output on conductor **26**. The output terminal **8** of BC7 produces a one-half Hz frequency on the output conductor **27**. Binary counters BC6 and BC7 may also be obtained from the Texas Instrument, Incorporated having part numbers SN7490N and SN7492N, respectively, although other binary counters of other companies may be equally useful and adaptable to the clock circuit of this invention.

The 1 Hz output signal on the output conductor **26** is applied as an input to the first of a series of counters BC8 through BC13. These counters may likewise be purchased on the open market from Texas Instrument, Incorporated, BC8 and BC10 having the part numbers SN7490N while the counters BC9 and BC11 have part numbers SN7492N. BC12 is a counter obtainable from Fairchild Semiconductor Company having a part number U6B931059X. The counter BC13 is a dual J-K flipflop circuit obtainable from Texas Instrument, Incorporated under the part number SN7473N

The counter BC8 provides a seconds counter up to 9, the 10th count of which will be applied as an input to BC9. BC8 has four outputs **30**, **31**, **32**, and **33**, providing the four binary digits to obtain the 10 count as a decade counter. As the decade counter BC8 counts the 1 Hz frequency pulses over input **26** at terminal **14** thereto, the binary digits will add up until the binary count of 1 0 0 1 equals a count of 9 which will return to binary 0 0 0 0 at the same time that a "1" to "0" transition is applied to terminal **14** of BC9. BC9 is a divide-by-six counter which will give the 10 of seconds count on the three outputs **34**, **35**, and **36**. The fifth pulse input from BC9 will produce a binary count of 1 0 1 and the next pulse input will produce a binary 0 0 In this manner a count of **59** can be run up on the seconds and tens of seconds counters of BC8 and BC9, the 16 pulse, or 60 seconds, causing these counters to return to "0." The outputs **30** through **33** from BC8 are applied to a seconds digital display means **40** while the outputs **34** through **36** from BC9 will be applied to a 10

of seconds digital display means **41**. The output from the binary counter **BC9** is applied through two NAND gates in series **G1A** and **G1B** to the input terminal **14** of **BC10**. The output of **BC10** is coupled in series through NAND gates **G1C** and **G1D** in series to **BC11** and the output of **BC11** is coupled in series through NAND gates **G2A, G2B,** and **G2C** to the binary counter **BC12**. **BC10** adds up the minutes and is a decade counter counting up to 10 and each 10th count is applied to **BC11** which adds up the 10s of minutes to the count of six since **BC11**, like **BC9**, is a divide-by-six counter. **BC10** is coupled by four leads to a digital readout means **42** in the same manner as for the seconds, and **BC11** is coupled by three leads carrying the three binary counts to a 10s of minutes digital display means **43**. Like the seconds and 10s of seconds counters, the minutes and 10s of minutes counters will add up to **59** and the next input pulse will return these two counters to zero in like manner as for the seconds and 10s of seconds counter.

BC12 is a decade counter which has its four binary digit leads coupled to a digital readout means **44** for displaying the hours count whereas **BC13** is coupled by two leads **37** and **38** to a 10s of hours digital display means **45**. The digital display means **40** through **45** are produced by many manufacturers and are well-known as a marketed item and will not be discussed further in structure herein. Since the counters **BC12** and **BC13** must operate in a unique manner to count only to **23** and then be returned to "0 " on the next input pulse, **BC12** and **BC13** are coupled to provide this result. **BC12** has its output terminal **11** coupled through a NAND gate **G2D** as an input to a NAND gate **G3B**, the output of which is to terminals **1** and **5** of **BC13**. The output terminals **13** and **14** being output conductors **30** and **31** are coupled as inputs to a NAND gate **G3A** the output of which is coupled as an input to NAND gate **G3B** and also as a feedback to input terminal **9** of **BC12**. The output terminal **9** of **BC13** is coupled by conductor **38** to the 10s of hours digital display **45** and also coupled back as a feedback input to NAND gate **G3A**. Output terminal **12** of **BC13** is coupled as the second input **37** to the digital readout means **45**. By this coupling arrangement **BC12** being a decade counter will count up to 10 at which time an output will pass through **G2D** and **G3B** NAND gates to flip the flipflop circuit **BC13** to produce a binary 1 on the output **37**. The second count of 10 out of **BC12** will likewise pass through NAND gates **G2D** and **G3B** through **BC13** to produce a binary count of two (1 0) on outputs **38, 37**, respectively. This also produces a "1" input on **G3A** together with two "1 " inputs from lines **30** and **31** on the output of **BC12** [when **BC12** is at 3 (0 0 1 1)]which will produce a "0" on the output of **G3A** returned to terminals **9** of **BC12** changing this from a decade counter mode of operation to a synchronous parallel entry mode which will cause **BC12** to return to "**0**" upon the next count impulse from **BC11**. When **BC12** returns to "**0**" it sends a pulse via **G3A** and **G3B** which causes **BC13** to return to "0)L " Accordingly, **BC12** and **BC13** will add up to the displayed output on **45** and **44** to **23** and when the **24** hours has been reached by an impulse of **BC11** the **23** count will return to "o. " Accordingly, it may be seen that a count of 23:59:59 can be reached on the digital display means 40 through 45 at which time the next one second count or Hz pulse will return the counters and digital display means to "0's" at which time the seconds counter will begin to count towards 0 1 0 0.

In order to set the 24-hour digital clock to any desired starting time a two-gang switch **S1A** and **S1B** having six contact positions thereon is used. The switch **S1** is a non-shorting rotary switch which together with NAND gate latches **G4C, G4D, G5A,** and **G5B** are used. **G4C** and **G5A** are cross-coupled from output to input and in like manner **G4D** and **G5D** are cross-coupled from output to input. The rotary switch contact of **S1A** is coupled directly to a fixed potential, such as ground, while the rotary switch contact of **S1B** is coupled to the output conductor **27** from **BC7** on which is applied the one-half Hz frequency. Terminal **1** of **S1A** is coupled as the second input of NAND gate **G4D** by conductor **50** and also by branch conductor **51** as one of the inputs to NAND gate **G5A**. Conductor **51** is also coupled through a resistor **52** to a terminal input **53** to which a DC voltage source may be applied, herein illustrated as being 5 volts. Contact **2** of **S1A** is coupled by conductor **54** as an input to NAND gate **G5B** and by way of branch conductor **55** as a second input to NAND gate **G4C**. Branch conductor **55** is also coupled through a resistor **56** to the DC source **53**. Contacts **3, 4, 5,** and **6** of **S1A** are coupled in parallel by conductor **57** as another input to NAND gate **G5B** and also by branch conductor **58** as an input to NAND gate **G5A** as well as through a resistor **59** to the DC supply at terminal **53**. Terminals **1** and **2** of **S1B** are open. Terminal **3** of **S1B** is coupled through resistor **60** to the DC source **53** and also by way of conductor **61** as a second input to the NAND gate **G1B**. Terminal **4** of **S1B** is coupled through a resistor **62** to source **53** and by way of conductor **63** as a second input to NAND gate **G1D**. Terminal **5** of **S1B** is coupled through resistor **64** to the source **53** and by way of conductor **65** as a second input to NAND gate **G2B**. Terminal **6** of **S1B** is coupled through resistor **66** to the DC source **53** and also by way of conductor **67** as an input to NAND GATE **G3B**. The output of NAND gate **G5B** is by way of conductor **68** to input terminals **2** and **3** of both **BC8** and **BC9** in parallel as well as the second input to NAND gate **G4D**, as hereinbefore stated. The output of NAND gate **G4D** on conductor **69** is applied as a second input to NAND gate **G1A**, as a second input to NAND gate **G1C**, as a second input to NAND gate **G2A**, as one of the inputs to NAND gate **G3A**, and as a second input to NAND gate **G2D**, as well as the cross-coupled input to NAND gate **G5B** hereinbefore stated. The output of **G4C** on conductor **70** is in parallel to terminals **2** and **3** or terminals **6** and **7**, as appropriate, to all the binary counters **BC1** through **BC7**. The other terminals, such as terminal **5** of the binary counters, are coupled to the DC voltage source while other terminals of the binary counters **BC1** through **BC7** are coupled to ground, as herein illustrated for the desired operation of these counters. In like manner the binary counters **BC8** through **BC13** and the digital display means **40** through **45** each have appropriate voltages applied thereto as shown in the Figure of drawing. Where it is desirable to make a lamp test of the digital display means **40** through **45** a switch **S3** may be placed between ground and the terminals I in parallel to all the display means to test digital display lamps.

OPERATION

In the statement of operation of the 24-hour digital clock hereinabove described, TABLE I herein below will be used in going through the various switched operations.

TABLE I

Latching NAND gates	SWITCH POSITIONS run 1 i out n	hold 2 i out n	minutes 3 i out n	tens of minutes 4 i out n	hours 5 i out n	tens of hours 6 i out n
G5B						
	1	1	0	0	0	0
0 - Run	1 0	1	0	0	0	0
1 - Hold	1	0 1	1 1	1 1	1 1	
	i	0	0	0	0	0 G4D
0 - Disables	0	1	1	1	1	1
1 - Enables	0 1	1 0	1 0	1 0	1 0	1 0
	1	1	0	0	0	0
G5A	0	1	1	1	1	1
	0 1	1 0 0 1		0 1	0 1	0 1
	0	1	0	0	0	0
G4C						
0 - Counts	1	1	1	1	1	1
1 - Zeroed	1 0	0 1	1 0	1 0 tg	1 0	1 0

When switch S1 is switched to contacts **1**, this will be the "run" position such that the 6 MHz oscillator **21** is applying frequency through contact **22** of switch S2 producing a 1 Hz output on **26** to the seconds counter BC8. In this contact **1** position or "run" position all inputs to NAND gate G5B will be binary 1's on the inputs from top to bottom, as indicated in TABLE I. The two top inputs will be 1 since contacts **3** through **6** are open and voltage is applied over conductor **58** from source **53** through resistor **59** applying 5 volts substantially to the top two inputs to NAND gate G5B. The third input down to G5B is via conductor **55** and resistor **56** from the 5 volts DC source **53** since contact **2** of S1A is open. Since the lower input to NAND gate G4D is "**0**" by virtue of S1A being on contact **1** via conductor **50**, the output of G4D will be "1" regardless of whether the second input of G4D is a "1" or a "0. " Accordingly, the fourth input to G5B is a "1" thereby producing a "0" output on conductor **68** to the counters BC8 and BC9 allowing counters BC8 and BC9 to count normally. Also since the output of G4D is "**1**," as hereinbefore stated, NAND gates G1A, G1C, G2A, G2D, and G3A are enabled, except that G3A is disabled by the input from conductor **38**. Looking to NAND gate G5A, the top input is a "**1**" since 5 volts stands on conductor **58** but the second input from the top on conductor **51** is a "**o**" since conductor **1** of S1A is grounded. NAND gate G4C has the bottom input coupled directly to the conductor **55** which is open at contact **2** of S1A and therefore has a 5 volt DC through resistor **56** applied which will produce an output on **70** of "0" regardless of whether the second input is a "1" or a "0."Since output **70** is "0" the bottom two inputs to G5A are "0's " producing a "1" output from G5A as a second input to G4C. Accordingly, in the "run" position of the device shown in FIG. **1** the outputs of the NAND gate latching gates will be as shown in the "run" position of TABLE I. BC8 through BC13 are thereby enabled to continue count up through 23 hours, 59 minutes and 59 seconds at which time the next 1 second count will return the counter to "0" to start a new count from "1" count up to 23 hours, 59 minutes and 59 seconds.

In resetting this clock it is preferable to first set the hours and then the minutes but the seconds will be reset automatically in all but the "run" position. Switch S1 is rotated to position **6**. This will set up the capability of setting the tens of hours counter at which time the outputs of the latching NAND gates G5B, G4D, G5A, and G4C will be 1 0 1 0, respectively, as shown in TABLE I, which outputs are established by the inputs as shown. Since G4C is at "0, " BC1 through BC7 will be enabled to count normally. G5B is at "1" which resets BC8 and BC9 to "0." G5D is at "0" disabling gates G1A, G1C, G2A, G2D, and G3A such that BC10 through BC13 are isolated from one another. In switch position **6** the one-half Hz frequency is applied through S1B to G3B causing BC13 to count at a one-half Hz rate. As soon as the count in BC13 reaches the desired starting point in tens of hours, the switch S1 is rotated to the fifth position setting up the latching NAND gate outputs to 1 0 1 0 as shown in the hours, column **5** of TABLE I. This now places the one-half Hz signal as an input through G2B to the hours counter which can be run up at the one-half Hz rate until the desired hours count is reached. This same procedure is used for the 10s of minutes count on contact **4** and the minutes count on contact **3** of switch S1 to preset the tens of minutes and minutes counters BC11 and BC10 which will be digitally read out on **42** and **43**, respectively.

After each of the four significant decade counters is preset to the desired 10s of hours, 10s of minutes and minutes, switch S1 is rotated to the "hold" position contact **2**. In this position G4C output goes to a "1" resetting counters BC1 through BC7 to "0" count. G4D remains at "0" isolating the preset counters BC10 through BC13 while G5B remains at "1" resetting BC8 and BC9 to count "0. " At the appropriate time switch S1 is rotated to the first contact position or "run" position and all counters are allowed to resume normal operation of counting time, as hereinabove described.

The one-half Hz frequency used as a "preset forcing pulse" was considered the fastest allowable frequency since it is necessary for the operator to switch to the next decade as soon as the count reaches the desired value in the decade being preset as a faster "preset forcing pulse" would require a reaction probably exceeding that of a normal person. Only a single simple switch S1 is required to preset the four most significant decades of the digital clock and immediate and continuous readout is provided by the digital readout means **40** through **45** so that precise setting of the clock may be accomplished and accurate timing is provided. If it is desirable to use an external source such as from house current, terminal **24** may be coupled to a 60 cycle source and the voltage regulated to some low voltage, herein shown to be 6.3 volts, and this external source can then be used by switching S2 to contact **23** to provide at least a semiprecision count by a clock means of this invention.

While many modifications may be made by the application of different voltages or the use of different flatpacs requiring different voltages, it is to be understood that I desire to be limited in the spirit of my invention only by the scope of the appended claims.

I claim:

1. A 24- hour digital clock comprising:

a stable oscillator of high frequency having an output;

a series string of binary counters having the first of the series string coupled to the output of said oscillator and coupled in series to divide said oscillator frequency to a frequency of one cycle per second on an output thereof;

a series of two pairs of binary counters, each pair including a decade counter having its output coupled to a divide-by-six counter with the first of said series decade counter having its input coupled to the output of said series string of binary counters, the first pair of decade and divide-by-six counters being coupled through a first set of NAND gates and said second of said pair of decade counter and divide-by-six counter being coupled through a second set of NAND gates;

a decade counter and a J-K flipflop circuit with the decade counter input coupled through a third set of NAND gates to the output of the last in the series of binary pairs and coupled together through a fourth set of NAND gates;

a selector switch of two gangs having a plurality of positions, the switchable contact of one gang being coupled to a fixed potential and the switchable contact of the other gang being coupled to a very low frequency source, the plurality of contacts of said one gang being coupled through a first NAND latching gate to said first through four NAND gates and the contacts of said other gang being coupled to a direct current voltage source through resistors and to said first through four NAND gates, and a second NAND latching gate coupled to said first NAND latching gate, to said direct current voltage source through said resistors, and to said series string of binary counters to provide setting of said two pairs of binary counters to zero, setting of said decade counter and J-K flipflop to zero, and setting of said series string of binary counters to start a new count by selected positions of said selector switch; and

digital readout means coupled to each binary decade counter, divide-by-six counter, and J-K flip-flop to provide numerical display of seconds, 10s of seconds, minutes, 10s of minutes, hours, and 10s of hours whereby a precise time piece is provided that is readily settable for time changes without vibration interference.

2. A 24-hour digital clock as set forth in claim **1** wherein

said series string of binary counters each produce frequency division to one point in the coupling producing 60 cycles per second at which coupling point includes a frequency selector switch to alternately select the frequency through said series string of binary counters and an external supply of 60 cycle per second frequency.

3. A 24-hour digital clock as set forth in claim **2** wherein

said series string of binary counters produces in the last binary counter said one cycle per second output and a one-half cycle per second output coupled to said switch contact of said other gang constituting said very low frequency source.

4. A 24 hour digital clock as set forth in claim **3** wherein

said first NAND latching gate consists of two NAND gates cross coupled from output to one input, all but one of said one gang of switch contacts being coupled as inputs to one of said two NAND gates and the one contact of said one gang of switch contacts being an input to the other of said two NAND gates.

5. A 24-hour digital clock as set forth in claim **4** wherein

said second NAND latching gate consists of two NAND gates cross coupled from the output to one input, all but a second of said contacts of said one gang switch contacts being coupled to one of said NAND gates of said second NAND latching gates, the second of said contacts being coupled to the other NAND gate of said second NAND latching gates, said output of said second NAND latching gates being from said other NAND gate.

6. A 24- hour digital clock as set forth in claim **5** wherein

said external supply of sixty cycles per second frequency coupled to said frequency selector switch is through a Schmidt trigger to provide a square wave input from said supply.

7. A 24-hour digital clock as set forth in claim **6** wherein

said fourth set of NAND gates include three NAND gates, the first and second thereof being coupled as inputs to the third thereof, the output of the latter being said coupling to said J-K flip-flop, the output of said J-K flipflop being fed back as an input to said first NAND gate of said fourth set and the output of said first NAND gate of said fourth set being fed back to said decade counter for said hours count, and said first NAND gate having inputs coupled to the outputs of said hours decade counter in a manner whereby said J-K flipflop will count in tens of hours to two and the hours counter will count to three and both counters will be reset to zero on the next input to said hours decade counter.

8. A 24- hour digital clock as set forth in claim **7** wherein

said coupling of each seconds and minutes decade counter to the corresponding digital readout means has the digit of the least significant bit coupled back to the decade counter and the fourth most significant bit constituting said output to said corresponding divide-by-six counter.

9. A 24- hour digital clock as set forth in claim **8** wherein

said coupling of each 10s of seconds and 10of minutes divide-by-six counters has the least significant digital bit coupled back as an input to itself and the third most significant bit constituting said output to the next higher order counter.

* * * * *

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(5/69)

UNITED STATES PATENT OFFICE

CERTIFICATE OF CORRECTION

UNDER RULE 322

Patent No. 3,699,763 Dated October 24, 1972

Inventor(s) DAVID L. ZEPH

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In the Patent, Column 2, line 62, change "0 0"

To Read:

0 0 0

Column 3, line 62, change "0)L"

To read:

0

Column 5, TABLE I, under "Latching NAND Gates" above "0-Disables" insert -- G4D --

Under "Tens of Hours", delete the vertical column of figures and letters and add:

0
0
1 1
0

1
1 0

0
1
0 1
0

1
1 0

Under "tens of Minutes" delete "tg"

Signed and sealed this 13th day of March 1973.

(SEAL)
Attest:

EDWARD M.FLETCHER,JR.
Attesting Officer

ROBERT GOTTSCHALK
Commissioner of Patents

PO-1050
(5/69)

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0
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0

1
1 0

0
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0 1
0

1
1 0

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