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(54) **Title**: TRENCH VERTICAL DOUBLE DIFFUSED METAL OXIDE SEMICONDUCTOR TRANSISTOR

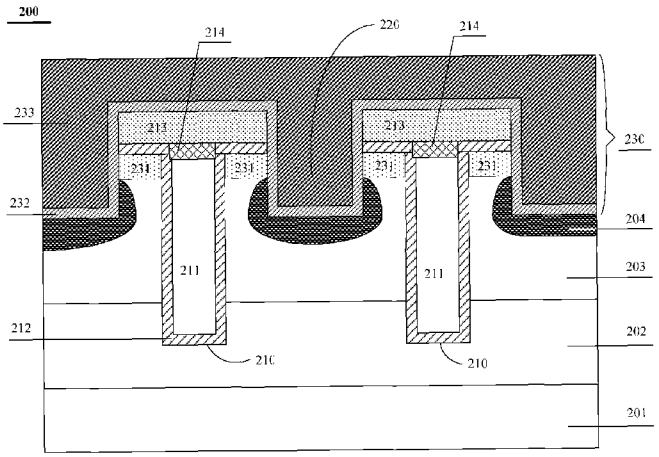

Fig.2

(57) **Abstract**: A trench vertical double diffused metal oxide semiconductor transistor includes, in part, a semiconductor substrate, an epitaxial layer formed above the substrate, a well region formed in the epitaxial layer, a multitude of trenches formed in the well region with each trench having formed therein a gate oxide layer and a polysilicon gate, a multitude of contact holes formed in the well region wherein each contact hole is positioned between a pair of adjacent trenches and has a metal disposed therein, a multitude of body contact regions positioned below the contact holes, and a multitude of source regions formed in the well region. Each source region is positioned between a trench and a contact hole. The substrate, the epitaxial layer, and the source regions are of the first conductivity type. The well region and the body contact regions are of the second conductivity type opposite the first conductivity type.

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TRENCH VERTICAL DOUBLE DIFFUSED METAL OXIDE SEMICONDUCTOR TRANSISTOR

Background of the Disclosure

[0001] The present invention relates to a transistor structure, and in particular to a trench vertical double diffused metal oxide semiconductor transistor structure.

[0002] Double diffused metal oxide semiconductor (DMOS) transistors are known. Compared with a bipolar power device, a DMOS transistor provides a number of advantages, such as high input impedance, low drive current, fast switching speed, negative current temperature coefficient, better current self-regulation capability, better thermal stability, better voltage breakdown characteristic, and the like. DMOS transistors are widely used in electronic devices, and are beginning to find increasing uses in high voltage, high current applications where bipolar power devices have traditionally been dominant.

[0003] One type of DMOS transistor, commonly referred to as a trench double diffused metal oxide semiconductor (TDMOS) transistor, includes a vertical channel with a gate formed therein that extends between its source and the drain regions. A vertical trench transistor provides a lower on-resistance than a conventional DMOS transistor. The source and drain regions of a TDMOS transistor are located at the opposing sides of the substrate in which the transistor is formed. The source region of a TDMOS is usually located at the top side of the substrate. Source regions of multiple TDMOS transistors are often connected together. The drain region of a TDMOS is located at the bottom of the substrate and is coupled to a metal layer formed on the bottom the substrate. More information about conventional TDMOS transistors is provided in US patent Nos. 5,541,425 and 5,072,266.

[0004] Figure 1 is a cross-sectional view of a conventional TDMOS transistor 100, as known in the prior art. As shown in Figure 1, TDMOS transistor 100 includes an N+ semiconductor substrate 101, an N- epitaxial layer 102, a P-type well region 103, polysilicon gate 130 formed in a trench extending to epitaxial layer 102, N+ doped source region 111, and gate oxide layer 131. The drain of TDMOS transistor 100 is coupled to metal layer 120 formed on the backside of substrate 101. The source of TDMOS transistor 100 is coupled to metal layer 110 formed on the surface of source region 111 and p-type well 103. Since P-well 103 is relatively lightly doped, its contact with metal layer 110 results in various parasitic effects that adversely affects transistor

100's performance.

Summary of the Disclosure

[0005] A trench vertical double diffused metal oxide semiconductor transistor (alternatively referred to herein as transistor), in accordance with one embodiment of the present invention, includes, in part, a semiconductor substrate, an epitaxial layer formed above the substrate, a well region formed in the epitaxial layer, a multitude of trenches formed in the well region with each trench having formed therein a gate oxide layer and a polysilicon gate, a multitude of contact holes formed in the well region wherein each contact hole is positioned between a pair of adjacent trenches and has a metal disposed therein, a multitude of body contact regions positioned below the contact holes, and a multitude of source regions formed in the well region. Each source region is positioned between a trench and a contact hole. The substrate, the epitaxial layer, and the source regions are of the first conductivity type. The well region and the body contact regions are of the second conductivity type opposite the first conductivity type.

[0006] In one embodiment, each contact hole has an opening of 0.5μm to 1μm and a depth of 0.35μm to 1μm. The depth of each contact hole is greater than an ion injection depth of the source region and is less than a depth of the trenches. In one embodiment, the doping concentration of the body contact regions is greater than the doping concentration of the well region. In one embodiment, the gate oxide layer disposed in each trench extends outwardly to cover a surface of the source region adjacent that trench.

[0007] In one embodiment, the transistor further includes, in part, an oxide layer formed above the polysilicon gates of the trenches. In one embodiment, the transistor further includes, in part, a dielectric layer formed over the oxide layer covering the surfaces of the source regions. The dielectric layer is also formed over the oxide layer covering the surfaces of the polysilicon gates. In one embodiment, the insulation dielectric layer is a borophosphosilicate glass layer.

[0008] In one embodiment, the transistor further includes, in part, a first metal layer formed over the insulation dielectric layer. The first metal layer is also used to fill the contact holes. In one embodiment, the first metal layer is a laminated layer that includes, in part, a bonding layer and a second metal layer. In one embodiment, the bonding layer includes a Ti/TiN laminated layer. In one embodiment, the second metal layer is an AlSiCu alloy. In one embodiment, the first conductivity type is N type and the second conductivity type is P type. In yet another embodiment, the first conductivity type is P type semiconductor and the second conductivity type is N type.

Brief Description of the Drawings

[0009] Figure 1 is a cross-sectional view of a trench vertical double diffused metal oxide semiconductor transistor, as known in the prior art.

[0010] Figure 2 is a cross-sectional view of a trench vertical double diffused metal oxide semiconductor transistor, in accordance with one embodiment of the present invention.

Detailed Description of the Embodiments

[0011] Figure 2 is a cross-sectional view of a trench vertical double diffused metal oxide semiconductor (TDMOS) transistor 200, in accordance with one embodiment of the present invention. TDMOS transistor 200 is shown as including a semiconductor substrate 201 having a first conductivity type, an epitaxial layer 202 having the first conductivity type and formed above substrate 201, a well region 203 of a second conductivity type formed in epitaxial layer 202, and a multitude of trenches 210 formed in well region 203. As shown, trenches 210 extend into the epitaxial layer 202. Each trench 210 includes a gate oxide layer 212 formed along the walls and bottom of that trench, and a polysilicon gate 211. TDMOS transistor 200 is also shown as including a multitude of contact holes 220 extending in well region 203. Each contact hole 220 is positioned between a pair of adjacent trenches 210 and includes a first metal layer 230 coupled to source regions of TDMOS 200. TDMOS transistor 200 is also shown as including a multitude of body contact regions 204 of the second conductivity type. Each body contact region 204 is positioned along the bottom as well along the sides near the bottom of an associated contact hole 220. TDMOS transistor 200 is also shown as including a multitude of source regions 231 of the first conductivity type formed in well region 203. Each source region 231 is positioned between a trench 210 and a contact hole 220.

[0012] In accordance with one exemplary embodiment of the present invention, substrate 201 and source regions 231 of the TDMOS transistor are heavily doped. The doping concentration of source regions 231 is less than that of substrate 201. Epitaxial layer 202 is relatively lightly doped and has a doping concentration that is less than that of source regions 231. Body contact regions 204 are heavily doped. Well region 203 is lightly doped and has a doping concentration that is less than that of body contact regions 204.

[0013] In accordance with one exemplary embodiment of the present invention, contact holes 220 of the TDMOS transistor have an opening between 0.5μm to 1μm and a depth between 0.35μm and 1μm. The depth of contact holes 220 is greater than the ion

injection depth of source region 231 (i.e., the depth that the impurities reach after they are implanted in the source and then diffused) and less than the depth of trenches 210. In one embodiment, contact holes 220 have an opening of 0.75μm and a depth of 0.7μm. Contact holes 220 are formed in well region 203 and have a depth that is less than the depth of well region 203.

[0014] In accordance with one exemplary embodiment of the present invention, gate oxide layer 212 of the TDMOS transistor extends outwardly to cover the surface of source regions 231, as shown in Figure 2. In such embodiments, the upper surface of polysilicon gate 211 is covered with an oxide layer 214. In such embodiments, an insulating dielectric layer 213 is formed over gate oxide layer 212 and oxide layer 214, as shown. In some embodiments, dielectric layer 213 is a borophosphosilicate glass (BPSG).

[0015] In accordance with yet another exemplary embodiment of the present invention, the oxide layer covering the surfaces of source regions 231, and polysilicon gates 211 of the TDMOS transistor are covered with a relatively thin layer of oxide 214. Accordingly, in such embodiments, oxide layer 214 overlays gate oxide layer 212 (covering the surface of source regions 231) as well as polysilicon gates 211.

[0016] As shown in Figure 2, a first metal layer 230 is formed over dielectric layer 213 and in contact holes 220. In some embodiments, first metal layer 230 is of a laminated layer structure and includes a bonding layer 232 and a second metal layer 233. In some embodiments, bonding layer 232 is a Ti/TiN laminated layer. Bonding layer 232 connects source regions 231 and body contact regions 204 to one another. As shown, bonding layer 232 also covers insulating layers 213. Ti/TiN has an excellent filling capability and forms a strong bond with silicon body. Ti/TiN bonds strongly with insulation dielectric layer 213 so as to significantly improve the stability of the metal structure. In some embodiments, second metal layer 233 is an AlSiCu alloy used for connecting the source regions to an external source.

[0017] In accordance with one embodiment of the present invention, the first conductivity type is N type, and the second conductivity type is P type. Accordingly, in such embodiments, substrate 201 which forms the drain region of TDMOS transistor 200 is of N type conductivity. Epitaxial layer 202 which has a lower doping concentration than substrate 201 is also of N type conductivity. Source region 231 is a heavily doped N type region. Accordingly, in such embodiments, TDMOS transistor 200 is a P-channel vertical trench MOS transistor. The channel of such a transistor is a lightly doped P-type region extending from N+ type source region 231 along the side

walls of trenches 210 to N type epitaxial layer 202. To form a channel in such embodiments, a positive voltage V_{GS} greater than threshold voltage Vt is applied between the gate region 211 and source region 231. The application of this voltage causes the P-type channel to be inverted to an N-type so as to form a conductive path between source region 231 and drain region 201. When the voltage of the drain is higher than the voltage of the source (i.e. $V_{DS}>0$ is applied between the source and drain regions) electrons in the N-type source region reach the drain region via the conductive channel region, thereby causing a drain-source current to flow from the drain to the source. The larger the value of V_{GS} is, the smaller the corresponding channel resistance will be, and under the same V_{DS} bias, the larger the drain source current will be. After flowing through the channel, the current reaches semiconductor substrate 201 (the drain of TDMOS transistor 200) and received by drain metal layer 120.

[0018] In accordance with another embodiment of the present invention, the first conductivity type is P type, and the second conductivity type is N type. Accordingly, in such embodiments, substrate 201 which forms the drain region of TDMOS transistor 200 is of P type conductivity. Epitaxial layer 202 which has a lower doping concentration than substrate 201 is also of P type conductivity. Source region 231 is a heavily doped P type region. Accordingly, in such embodiments, TDMOS transistor 200 is an N-channel vertical trench MOS transistor. The channel of such a transistor is a lightly doped N-type region extending from P+ doped source region 231 along the side walls of trenches 210 to P-type epitaxial layer 202. To form a channel in such embodiments, a negative voltage V_{GS} whose absolute value is greater than the absolute value of the threshold voltage Vt is applied between the gate region 211 and source region 231. The application of this voltage causes the N-type channel to be inverted to a P-type so as to form a conductive path between source region 231 and drain region 201. When the voltage of the drain is lower than the voltage of the source (i.e. $V_{DS}<0$ is applied between the source and drain regions), holes in the P-type source region reach the drain region via the conductive channel region, thereby causing a source-drain current to flow from the source to the drain. The more negative is the value of V_{GS}, the smaller the corresponding channel resistance will be, and under the same V_{DS} bias, the larger the drain source current will be. After flowing through the channel, the current reaches semiconductor substrate 201 (the drain of TDMOS transistor 200) and received by drain metal layer 120.

[0019] In accordance with one embodiment of the present invention, as described above, metal layer 230 fills contact holes 220. Each contact hole 220 is shown as being positioned between a pair of source regions 231. A heavily doped body contact

region 204 is formed along the bottom as well along the sides near the bottom of its associated contact hole 220. Accordingly, contacts between metal layer 230 and the silicon body as well as contacts between metal layer 230 and the source regions are made through contact holes 220. Source regions 231 make contacts with metal layer 230 via the side walls of contact holes 220. The silicon body forms contacts with metal layer 230 via the bottom as well as the sides of the contact holes 220 and heavily doped regions 204. Consequently contacts between the source regions and the silicon body are made via metal layer 230. In other words, in various embodiments of a TDMOS transistor of the present invention, silicon body regions that contact metal layer 230 are all heavily doped, thereby effectively minimizing various parasitic effects.

[0020] The above embodiments of the present invention are illustrative and not limitative. Various alternatives and equivalents are possible. Other additions, subtractions or modifications are obvious in view of the present invention and are intended to fall within the scope of the appended claim.

CLAIMS

1. A trench vertical double diffused metal oxide semiconductor transistor comprising:

a semiconductor substrate of a first conductivity type;

an epitaxial layer formed above the substrate and having a first conductivity type;

a well region formed inside the epitaxial layer and having a second conductivity type;

a plurality of trenches formed in the well region, each trench comprising a gate oxide layer and a polysilicon gate;

a plurality of contact holes formed in the well region, each contact hole positioned between a pair of adjacent trenches and having disposed therein a first metal;

a plurality of body contact regions positioned below the plurality of contact holes and having a second conductivity type; and

a plurality of source regions formed in the well region and having the first conductivity type, each source region positioned between one of the plurality of trenches and one of the plurality of contact holes.

2. The trench vertical double diffused metal oxide semiconductor transistor of claim 1 wherein each contact hole has an opening between 0.5μm and 1μm and a depth between 0.35μm and 1μm, wherein a depth of each contact hole is greater than an ion injection depth of the source region and less than a depth of the trenches.

3. The trench vertical double diffused metal oxide semiconductor transistor of claim 1 wherein a doping concentration of the body contact regions is greater than a doping concentration of the well region.

4. The trench vertical double diffused metal oxide semiconductor transistor of claim 1 wherein the gate oxide layer disposed in each trench extends outwardly to cover a surface of a source region adjacent the trench.

5. The trench vertical double diffused metal oxide semiconductor transistor of claim 4

wherein the trench vertical double diffused metal oxide semiconductor transistor further comprises an oxide layer formed above the polysilicon gates of the plurality of trenches.

6. The trench vertical double diffused metal oxide semiconductor transistor of claim 5 wherein the trench vertical double diffused metal oxide semiconductor transistor further comprises a dielectric layer formed over the oxide layer covering surfaces of the source regions, said dielectric layer being also formed over the oxide layer covering surfaces of the polysilicon gates.

7. The trench vertical double diffused metal oxide semiconductor transistor of claim 6 wherein said insulation dielectric layer is a borophosphosilicate glass layer.

8. The trench vertical double diffused metal oxide semiconductor transistor of claim 6 wherein said trench vertical double diffused metal oxide semiconductor transistor further comprises a first metal layer formed over the insulation dielectric layer and in the contact holes.

9. The trench vertical double diffused metal oxide semiconductor transistor of claim 8 wherein the first metal layer is a laminated layer comprising a bonding layer and a second metal layer.

10. The trench vertical double diffused metal oxide semiconductor transistor of claim 9 wherein the bonding layer comprises a Ti/TiN laminated layer.

11. The trench vertical double diffused metal oxide semiconductor transistor of claim 9 wherein the second metal layer is an AlSiCu alloy.

12. The trench vertical double diffused metal oxide semiconductor transistor of claim 1 wherein the first conductivity type is N type and the second conductivity type is P type.

13. The trench vertical double diffused metal oxide semiconductor transistor of claim 1 wherein the first conductivity type is P type semiconductor and the second conductivity type is N type.

14. A method of forming a trench vertical double diffused metal oxide semiconductor transistor, the method comprising:

providing a semiconductor substrate of a first conductivity type;

forming an epitaxial layer of a first conductivity type above the substrate;

forming a well region of a second conductivity type in the epitaxial layer;

forming a plurality of trenches in the well region, each trench comprising a gate oxide layer and a polysilicon gate;

forming a plurality of contact holes in the well region, each contact hole positioned between a pair of adjacent trenches and having disposed therein a first metal;

forming a plurality of body contact regions around bottoms of the plurality of contact holes, said body regions being of a second conductivity type; and

forming a plurality of source regions of the first conductivity type in the well region, each source region positioned between one of the plurality of trenches and one of the plurality of contact holes.

15. The method of claim 14 wherein each contact hole has an opening between 0.5μm and 1μm and a depth between 0.35μm and 1μm, wherein a depth of each contact hole is greater than an ion injection depth of the source region and less than a depth of the trenches.

16. The method of claim 14 wherein a doping concentration of the body contact regions is greater than a doping concentration of the well region.

17. The method of claim 14 wherein the gate oxide layer disposed in each trench extends outwardly to cover a surface of a source region adjacent the trench.

18. The method of claim 17 further comprising:

forming an oxide layer above the polysilicon gates of the plurality of trenches.

19. The method of claim 18 further comprising:

forming a dielectric layer over the oxide layer covering surfaces of the source regions; and

forming the dielectric layer over the oxide layer covering surfaces of the polysilicon gates.

20. The method of claim 18 further comprising:

forming a first metal layer over the insulation dielectric layer and in the contact holes.

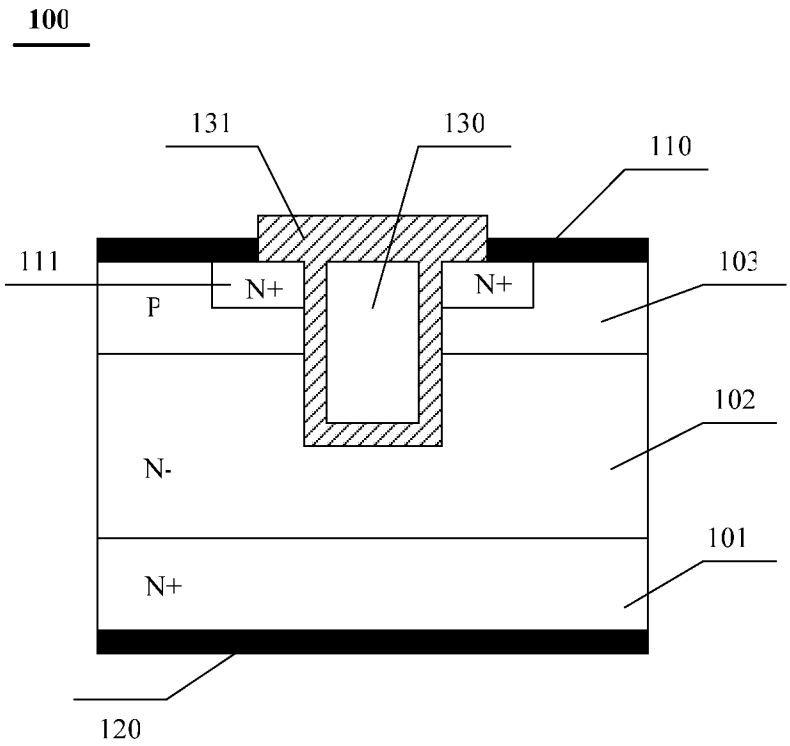
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Fig.1

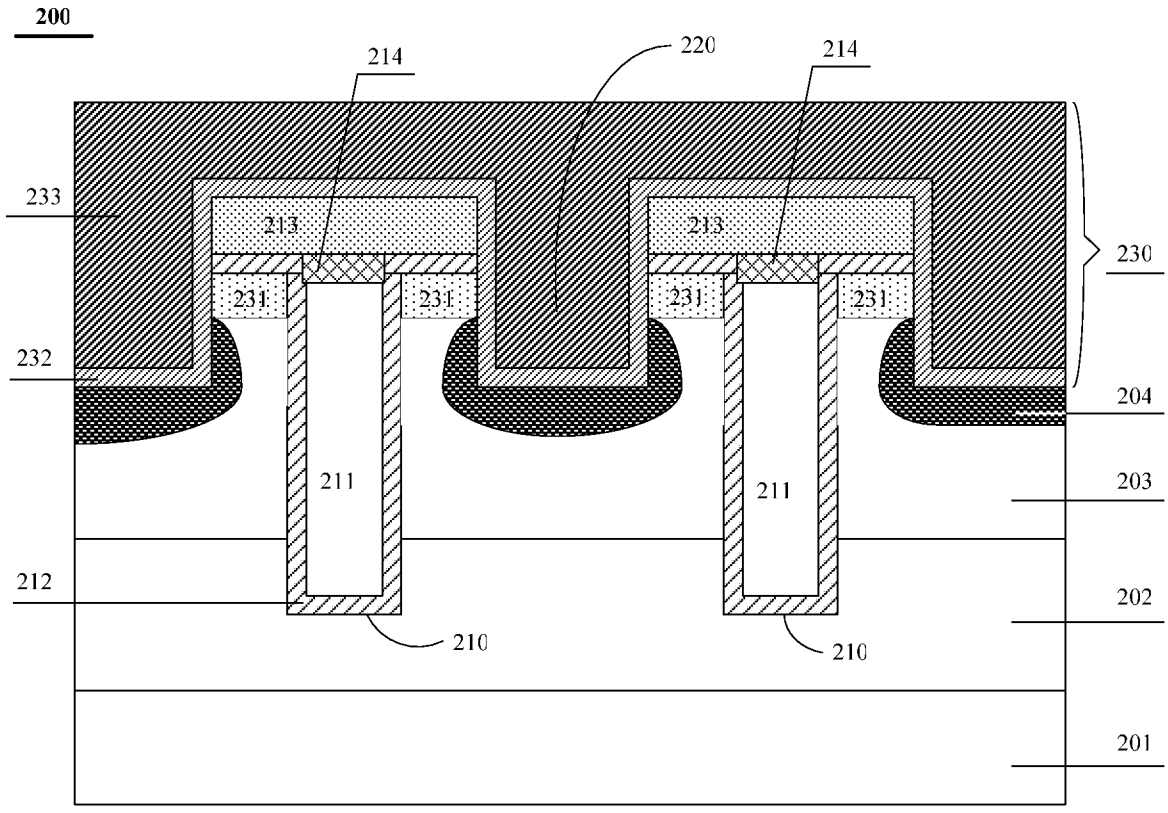
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Fig.2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2011/070950

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/78 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC:H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI;EPODOC; CNPAT; CNKI: DMOS, UMOS, TDMOS, PLUG, CONTACT

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim
X	US2004/0021174A1 (KOBAYASHI, Kenya) 05 Feb.2004(05.02.2004) Description paragraphs 51-65, Figs.3-8C	1-20
X	US2008/0073714A1 (SHIRAI, Nobuyuki et al.) 27 Mar.2008 (27.03.2008) Description paragraphs 64-97, Fig.10	1-20
X	JP2000-223708A (TOSHIBA CORP.) 11 Aug.2000(11.08.2000) Description paragraphs 7-26, Figs.1-2	1-20
X	US2010/0025759A1 (ROHM CO., LTD.) 04 Feb.2010(04.02.2010) Description paragraphs 51-119, Figs.1-2	1-20
X	US2009/0315104A1(FORCE MOS TECHNOLOGY CO., LTD.) 24 Dec.2009(24.12.2009) Description paragraph 27, Fig. 2	1-20
X	US2010/0200912A1 (FORCE MOS TECHNOLOGY CO., LTD.) 12 Aug.2010(12.08.2010) Description paragraph 21, Fig. 2	1-20

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"&"document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28.Apr.2011(28.04.2011)	**23 Jun. 2011 (23.06.2011)**
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer SHAO, Ye Telephone No. (86-10)62413923

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2011/070950

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