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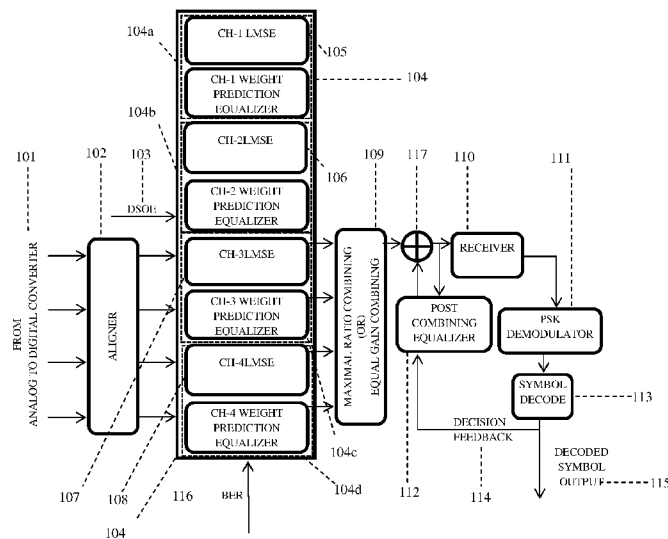


Figure 2

(57) Abstract: The present invention is a multilevel equalizer bearing dual equalizer units for performing equalization operations before and after the combination of multipath signals. The Pre-Combining Equalizer functions on the basis of the Least Mean Square (LMS) Criterion and the Linear Predictive Filtering method by use of the Bit Error Rate (BER) code of the final output, which minimizes the errors caused by multipath delays and Inter-Symbol Interferences (ISI). The post-combining equalizer effectively reduces the errors that are induced as a result of imperfect combining. Such a system can suitably function by the employment of Forward Error Correction (FEC) having lower code rate that can be effective for obtaining higher bandwidth.



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DYNAMIC COEFFICIENT STORAGE EQUALIZER

FIELD OF THE INVENTION

This invention relates to telecommunication systems, Multiple Input Multiple Output (MIMO) in particular that can align and equalize the multipath signals thereby reducing the effects of ISI induced due to increased data rates during the transmission.

BACKGROUND OF THE INVENTION

The conventional telecommunication systems involving Multiple Input Multiple Output (MIMO) arrangements require the installation of several antennas for transmitting and receiving the signals in order to obtain the final output signal with better Signal-to-Noise (S/N) ratio. Moreover, the multiple signals are associated with varying time delay in the path which creates the need for a system which can align and equalize the multipath signals to avoid the loss of data caused by intensity attenuation of the input stream. In addition, the bulk data contained in the multiple input waves can be subjected to Inter-Symbol Interference (ISI) due to the overlapping of the symbols included in the signal data with each other that gives rise to distortion patterns.

Dual equalizing units can resolve the above-stated issues by performing the equalization operations before and after the combination of multipath input data. The Pre-Combining Equalizer ensures that the effects of the Inter-Symbol Interference (ISI) and multipath dispersion are minimal whereas the Post-Combining equalizer will reduce the net errors after the combination process.

DISCUSSION OF PRIOR ART

The systems involving Multiple Input Multiple Output (MIMO), related to the telecommunication devices require various arrangements for processing the multiple input signals so as to render the final output to be free of errors that may have been induced due to the phenomenon such as multipath fading, Inter-symbol Interference, multipath dispersion, degraded Carrier-to-Noise Ratio. The

arrangement includes units that deal with aligning, equalization and combination steps for processing these multipath signals.

US 3633107 A titled “*Adaptive signal processor for diversity radio receivers*” discloses “a signal processor in a diversity receiver for the digital data transmitted over dispersive and fading radio channels performs the functions of demodulation, diversity signal combining, delay equalization, multipath distortion equalization and timing jitter elimination. Transversal equalizers, one in each diversity channel, are made adaptive to a common, time-varying mean-square error signal derived from the combined post detection output data.” (*Sic US Publication No. US 3633107 A*).

US 3879664 A titled “*High speed digital communication receiver*” discloses “a high speed digital communications receiver used in a diversity receiver system in which the pre-detection combiner of the receiver operates on a forward adaptive filter equalizer, having multiple weighting sections, in each of the diversity channels to process each received bandpass diversity signals prior to demodulation. The combined weighted output signal from the pre-detection combiner is then demodulated and the data therein appropriately reconstructed and an error signal is generated. The error signal thus obtained is modulated and restricted for use in an adaptive control circuitry which provides appropriate adaptive weighting signals for use in the processing of the received diversity signals at each of the forward filter equalizers. The un-modulated error signal is applied in a backward adaptation control circuit for providing appropriate adaptive weighting signals for use in a single backward filter equalizer which suitably processes the reconstructed data to form a cancellation signal which is used to eliminate inter-symbol interference and source correlation effects in the demodulated combined weighted output signal. A novel adaptive timing system is disclosed which permits the receiver clock to follow transmitter clock variations. Further, a novel automatic gain control system at the input IF receiver amplifiers are used to reduce the dynamic range requirements of the forward filter weight components.” (*Sic US Publication No. US 3879664 A*).

US 4890298 A titled "*Troposcatter modem receiver*" discloses "The Troposcatter Modem Receiver includes a combiner, demodulator, baseband filter, a complex coefficient forward equalizer, a detector and a feedback circuit. The combiner is a linear maximal-ratio combiner and receives a plurality of input signals at an intermediate frequency and generates a combined output signal for presentation to the demodulator. The demodulator produces a demodulated signal which is filtered by the baseband filter prior to being presented to a first input of the equalizer. The output of the equalizer is forwarded to the detector which produces an output signal. The signal is fed back by way of the feedback circuit to a second input of the equalizer to modify the output signal."(Sic US Publication No. US 4890298 A).

US 5068873A titled "*Equalizer*" discloses "An adaptive equalizer comprising a computer unit which receives a known signals sequence to estimate transmission channel characteristics and effect compensatory control of tap coefficients by use of a first algorithm that has fast convergence property, and a tap coefficient computing unit for making compensation for relatively slow changes in a random data input after the compensation for the transmission channel characteristics, which either employs an algorithm that involves a relatively low computational complexity or intermittently executes computation." (Sic US Publication No. US 5068873 A).

US 5175747 A titled "*Equalizer*" discloses "an adaptive equalizer comprising a computing unit which receives a known signal sequence to estimate transmission channel characteristics and effect compensatory control of tap coefficients by use of a first algorithm that has fast convergence property, and a tap coefficient computing unit for making compensation for relatively slow changes in a random data input after the compensation for the transmission channel characteristics, which either employs an algorithm that involves a relatively low computational complexity or intermittently executes computation which contains an interpolation of consecutive sets of tap coefficients between intermittent intervals."(Sic US Publication No. US 5175747 A).

US 6590933 B1 titled "*Adaptive decision-feedback equalizer with error-predictor for improved convergence*" discloses "a method for use in data communications equipment for improving convergence of a hybrid decision feedback apparatus including an adaptive feed-forward equalizer and an adaptive decision feedback equalizer. An independent error predictor component is used for better convergence and then is eliminated by converting, using z-transformations, the adaptive feed-forward equalizer and adaptive decision feedback equalizer to an equivalent feed forward equalizer and an equivalent decision feedback equalizer, respectively, in which the error predictor is embedded or incorporated therein. The smaller system with a reduced number of FFE-DFE coefficients has a faster convergence rate."(Sic US Publication No. US 6590933 B1).

The above stated prior arts employ various techniques to improvise the carrier-to-noise ratio (CNR)/signal-to noise ratio (SNR) mainly involved in the Multiple-Input Multiple-Output (MIMO) system. In one of the prior art, the difference between the input and output of the slicer are applied to compute the error signal which in-turn is used to update the weights, whereas in the proposed invention the weights are updated independently on each channel before the combining. Another technique equalizes and combines in the passband (i.e. before demodulation). In the available invention, a Post-Combining Equalizer structure in which there are feed-forward and feedback filters is proposed. Both these filter structure are inter-dependent. Also, the weight update is based on LMS algorithm in both the filters.

In the available prior arts, the equalization and combining is done in the passband while the present technique is done in the baseband. Also, the prior-art proposes Post-Combining Equalizer structures in which there are feed-forward and feedback filters, both these filter structures are inter-dependent. The weight updation is based on LMS algorithm in both the filters whereas in the proposed invention, the weights are updated independently in the Pre-Combining Equalizer

using LMS and a prediction algorithm, and for Post-Combining Equalizer, weights are updated using a decision feedback equalizer.

SUMMARY OF THE INVENTION

The present invention describes a Multilevel Equalizer consisting of two equalizer
5 units for a single carrier. In the dual equalizer system, the equalization operation
is performed before and after combining the signals. The incoming signals from
analog to digital converters are passed through an Aligner unit having multiple
individual channels that perform a pilot detection on each channel. The pilot is a
tone that occurs periodically and detected using standard methods. The signal is
10 then passed through a Chain Aligner unit that uses the pilot tone for finally
obtaining the time-aligned signal. The so-aligned signal is then set to proceed to
the Pre-Combining Equalizer comprising a Weight Prediction Equalizer module
and a storage-based Pilot Aided LMS Equalizer. The Equalizer contains a
Predictive Weight Computer that can efficiently update the weight history of the
15 samples in the system memory after its effective processing, thereby resulting in
the faster convergence of Least Mean Square Error (LMSE) and the requirement
of fewer samples of the pilot transmission, thus conserving bandwidth. This is
done using a module unlike in traditional equalizer systems which depend on the
periodically occurring desired data (pilot data) for correcting the errors in the
20 channel. The module functions by computing the initial weights based on Least
Mean Square (LMS) criterion and storing these weights until some threshold
value of Bit Error Rate (BER) is received from the final decode output. Once the
desired threshold of BER is attained, the module switches to linear predictive
filter method for upgrading the next weights, this predictive filter does not depend
25 on the pilot data.

After the initial equalization, the system performs the diversity combining by
means of methods like Maximal Ratio Combining or Equal Gain Combining,
from where it is further sent to a receiving system connected to a Phase-Shift
Keying (PSK) demodulator. The errors further in the combined signal are rectified
30 employing a second equalization process after the Combiner. The second

equalizer system ensures the removal of the net errors in the system, thereby performing improved equalization of the samples that could be decoded even with a lower code rate Forward Error Correction (FEC) enabling higher data bandwidth. The Output of PSK Demodulator is fed to a FEC Decoder and Descrambler, which retrieves the original information. A signal is also fed as Decision Feedback to a Post-Combining Equalizer, which minimizes the errors after the combining process. The decode output signal, after the FEC Decoder and Scrambler is also used to estimate the Bit Error Rate (BER) information that is used by the module of the Predictive Weight Computer present in the Pre-Combining Equalizer module for retaining the information related to the final weights on attainment of the steady state.

The system consists of an Aligner, a Pre-Combining Equalizer module, a Combiner that applies Maximal Ratio Combining or Equal Gain Combining, a Receive module, a Phase-Shift Keying (PSK) demodulator, a Post-combining Equalizer and a Forward Error Correction (FEC) Decoder and Descrambler. The Pre-Combining Equalizer module includes a set of Weight Prediction Equalizer and Least Mean Square Equalizer for each Channel. The system introduces a known Pilot data which is a distinct Pilot tone after the Modulator at a fixed interval. These aids to detect these Pilot Data without the need for a complete decode. A Field-Programmable Gate Array (FPGA) acquires the Analog-to-Digital Converter (ADC) samples that serve as input to the Aligner.

In the present invention a Multilevel Equalizer Aided Channel Combining and Decode system having a Weight Prediction Equalizer in each receive channel for the effective operation in any channel condition consists of an Aligner, a Pre-combining Equalizer, a Combiner, a Receiver, a Phase-Shift Keying (PSK) Demodulator, a Post-Combining Equalizer, a Symbol Decode, an Adder, a Desired Signal Occurrence Estimate (DSOE), a Decision Feedback, a Decoded Symbol output, a Bit Error Rate (BER), one or more Raw samples and a FEC Decoder. The Pre-combining equalizer includes multiple Weight Prediction Equalizers, CH-1 Weight Prediction Equalizer, CH-2 Weight Prediction

Equalizer, CH-3 Weight Prediction Equalizer, CH-4 Weight Prediction Equalizer, multiple Least Mean Squared Error Equalizers (LMSE), CH-1 LMSE, CH-2 LMSE, CH-3 LMSE, CH-4 LMSE, one Weight Prediction Equalizer and one Least Mean Squared Error Equalizer for each of the receive channels. The Raw
5 Samples comprising a Pilot Data and information to be transmitted are captured from one of the Analog to Digital Converters. The Aligner is comprised of a Time Aligner and a Phase Aligner. The Desired Signal Occurrence Estimate (DSOE) is an estimate of a next desired signal in terms of receiver sample clocks. The Pre-combining Equalizer observes the Bit Error Rate (BER) coming from the FEC
10 Decoder and switches between the LMSE Equalizer and Weight Prediction Equalizer for each receive channel. The corresponding Weight Prediction Equalizer takes the history of weights to compute the next weight. The LMSE Equalizer in which samples from each of the Analog to Digital Converter are weighed independently, and each output signal is compared with the Desired
15 Signal sample to generate error signals. The Combiner performs merging of multiple inputs. The Receiver is a part of a decision device and performs an initial set of signal processing such as DC offset removal and a small phase rotation. The PSK Demodulator is also a part of the decision device comprising most of signal processing control loops such as Pilot Symbol Detection, Symbol Timing
20 Recovery, and Carrier Recovery control loops. The Post-Combining Equalizer is a decision feedback equalizer, in which output of the Symbol Decode is given to an array of delay elements where each output is weighed, and the weighted sum is fed to control the output of the Combiner. The Symbol Decode converts samples into Symbols and combines In-Phase (I) symbols and Quadrature-Phase (Q)
25 symbols into bits. The Decision Feedback is a feedback given to the Post-Combining Equalizer. The Decoded Symbol Output is symbol output from the Symbol Decode. The Bit Error Rate (BER) corresponds to number of bit errors observed over a pre-defined pilot length. The Adder performs a numeric signed addition of the two inputs, and the sum is given out as the output.

In this invention, the Pilot Data is a pre-defined tone that occurs at a known interval and is a “Desired Signal” and is distinctly distinguishable by the Receiver. One or more signals received by different receive channels encounter different path delays and the signals received by the different receive channels encounter different phase rotations. A Time Aligner time aligns all the signals received at different receive channels by adding appropriate delays. A Phase Aligner is responsible for aligning phase of all the received signals. The corresponding Weight Prediction Equalizer takes the history of the weights and tries standard interpolation and prediction methods including the application of a Kalman Filter to compute the next weight, the LMSE Equalizer in which the samples from each of the Analog to Digital Converter are weighed independently, and each output signal is compared with a Desired Signal sample to generate the error signals. This along with the input samples and a Step Size is used to compute the next set of weights. The Combiner uses Maximal Ratio Combining or Equal Gain Combining.

The Pre-combining Equalizer further comprises one or more Standard Delay Elements, a Multiplier, a Weight Prediction Equalizer, a Switcher, a Weight Update module, a Desired Signal and a Bit Error Rate (BER). The standard delay element provides one sample clock delay to incoming samples that is when output of the Standard Delay Element is previous sample, and then input of the Standard Delay Element would be current sample. The Multiplier performs numeric signed multiplication of the two inputs, and the product is given as the output. The Weight Prediction Equalizer refers to any one of the CH-1 Weight Prediction Equalizer, CH-2 Weight Prediction Equalizer, CH-3 Weight Prediction Equalizer, CH-4 Weight Prediction Equalizer. The Switcher observes the Bit Error Rate (BER) coming from the FEC Decoder and switches between the CH-1 Weight Prediction Equalizer or CH-1 Least Mean Squared Error Equalizer on Receive Channel-1, CH-2 Weight Prediction Equalizer or CH-2 Least Mean Squared Error Equalizer on Receive Channel-2, CH-3 Weight Prediction Equalizer or CH-3 Least Mean Squared Error Equalizer on Receive Channel-3 and CH-4 Weight

Prediction Equalizer or CH-4 Least Mean Squared Error Equalizer on Receive Channel-4. The Weight Update module performs standard weight update computations including Least Mean Square (LMS). The Desired Signal is the known data (known to both transmitter and the receiver) that is transmitted at
5 identified intervals.

The Post-combining Equalizer is a decision feedback equalizer, further comprises a Decision Feedback, a Multiplier, a Weight Update module and one or more standard delay elements. The Decision Feedback is a feedback given to the Post-
10 Combining Equalizer. The standard delay element provides one sample clock delay to the incoming samples that is when the output of the Standard Delay Element is the previous sample, then the input of the Standard Delay Element would be the current sample. The Multiplier performs numeric signed multiplication of the two inputs, and the product is given as the output. The
15 Weight Update module performs standard weight update computations including Least Means Square (LMS).

The method of the present invention, having a Weight Prediction Equalizer in each receive channel for effective operation in any channel condition that consists of an Aligner, a Pre-combining Equalizer, multiple Weight Prediction Equalizers,
20 CH-1 Weight Prediction Equalizer, CH-2 Weight Prediction Equalizer, CH-3 Weight Prediction Equalizer, CH-4 Weight Prediction Equalizer, multiple Least Mean Squared Error Equalizers (LMSE), CH-1 LMSE, CH-2 LMSE, CH-3 LMSE, CH-4 Least LMSE, a Combiner, a Receiver, a Phase-Shift Keying (PSK) Demodulator, a Post-Combining Equalizer, a Symbol Decode, an Adder, a
25 Desired Signal Occurrence Estimate (DSOE), a Decision Feedback, a Decoded Symbol output, a Bit Error Rate (BER), one or more Raw samples, one or more final weights, one or more streams that correspond to the output of the Aligner and a FEC Decoder. comprising the steps of: a) Acquiring digital signal from multiple Analog to Digital Converter simultaneously, through the Aligner, b)
30 Subjecting the received signal to identical processing, for detection of the start of

the Desired Signal frame at the multiple receive channels, c) Employing the respective Desired Signal detection circuits in the receive channel for a detection process, d) Initiating a clock counter in the respective Desired Signal Detection circuit, once the first Desired Signal is detected in any one of the channels and
5 applying the same process to the detection of the Desired Signal in the other channel at the respective Desired Signal detection circuit, e) Terminating the clock counters in the previous channels upon detection of the Desired Signal in the last channel, f) Estimating the next occurrence of the Desired Signal tone after alignment wherein the clock count value is called the Desired Signal Occurrence
10 Estimate (DSOE) and is a number of receive clock cycles after which the next pilot tone is expected to occur, called a Delay Computation Path, g) Filling and flushing of system buffer based on the Desired Signal Occurrence Estimate, the arrival of which is kept track by a counter that expires on start of the Desired
15 Signal, to check if desired signal estimations are aligned, h) Generating the Desired Signal Occurrence estimate where the signal is time-aligned as a Chain Delay Counter consists of pre-determined time delay for the channels such that precision of alignment is limited by a resolution of time-base and jitter of the
20 clock, i) Transmitting the time-aligned signal in each channel to the corresponding Pre-Combining Equalizer, which stores weight-related data of the Desired Signal Occurrence Estimate in a system buffer, j) Initiating an LMSE equalization process once the filling stops in the LMSE Equalizers and is done for a desired
25 signal sample length, k) Combining the equalized signal by a multipath Combiner to increase the signal-to-noise (S/N) ratio of the signal received, l) Processing the combined signal by the Receiver and PSK Demodulator, m) Performing Post-Combining equalization by the Post-Combining Equalizer that equalizes the
30 signal and eliminates residual error that may either be introduced or remaining during the combination process, and n) Sending the output of the FEC Decoder, the Bit Error Rate, to the Pre-Combining Equalizer for switching between Ch-1 Least Mean Squared Error Equalizer and CH-1 Weight Prediction Equalizer, CH-2 Least Mean Squared Error Equalizer and CH-2 Weight Prediction Equalizer, CH-3 Least Mean Squared Error Equalizer and CH-3 Weight Prediction

Equalizer, CH-4 Least Mean Squared Error Equalizer and CH-4 Weight Prediction Equalizer.

One or more final weights are applicable for the samples acquired after this calculation and are valid till the next set of weights are computed based on Pilot
5 indicator state. For the first pilot detected, buffered samples are equalized, and simultaneously the other stream passes through the equalizer transparently without any modifications where once the weights are computed, the same are applied to the stream data by convolution. The above step is repeated for each Desired Signal detected in received stream, and the previous weights are used as
10 initial weights for every subsequent equalization process. A weight array is created for every Desired Signal passing through the equalizer as copy of weights obtained from the equalizer is stored in another buffer. The Bit Error Rate is computed using standard methods, once the signal is decoded which are fed to the equalizer and the process continues until an acceptable threshold of the Bit Error
15 Rate is achieved. Upon attainment of the acceptable BER value, weight update process switches from the LMSE Equalizers to the corresponding Weight Prediction Equalizer. The estimated results of the CH-1 Least Mean Squared Error Equalizer is replaced with CH-1 Weight Prediction Equalizer, CH-2 Least Mean Squared Error Equalizer is replaced with CH-2 Weight Prediction Equalizer, CH-
20 3 Least Mean Squared Error Equalizer is replaced with CH-3 Weight Prediction Equalizer and CH-4 Least Mean Squared Error Equalizer is replaced with CH-4 Weight Prediction Equalizer weights in the system thereby assisting the system to adapt weights to changing channel in the absence of the new weights from the LMSE and also to aid faster convergence to steady state for LMSE. The channel
25 with the signal that is responsible for the termination of clock counters in the other channels is the reference channel and all other channels are referenced to this channel. The count on each of the clock counters corresponds to the path delay experienced by the signal received at the respective antenna. Desired Signal Occurrence Estimate (DSOE) is a pre-determined number of receive clock cycles
30 after which the next pilot tone is expected to occur. Identification of the reference

channel is responsible for the change in the signal path from Delay computation path flow to Data Path flow. The Combiner incorporates maximal ratio combining (MRC) or equal gain combining (EGC) method. A periodic Desired Signal tone that once aligned makes it possible to estimate the next occurrence in terms of receive clocks. The clock count value is called Desired Signal Occurrence Estimate (DSOE) and is a number of receive clock cycles after which the next pilot tone is expected to occur. Identification of the reference channel is responsible for the change in the signal path to Data Path flow. Upon achieving steady state, the final weights computed depending on the Bit Error Rate output is retained, and the process of switching of the weights is avoided.

One of the key aspects of the present invention is placing the predictive filter on each receive channel. Two types of communication systems benefit from this phenomena. In over the horizon Communication systems, radio waves encounter the lower boundaries of the atmosphere where the atmospheric conditions can affect the Radio channel. However, these conditions are cyclic in nature and a predictive filter can leverage the cyclic nature to converge faster. In extremely high-frequency communications systems, radio waves operate at a center-frequency as high as 20 GHz to 80GHz. At such high frequencies, the radio channel is susceptible to even minor environmental changes such as mist and seasonal humidity. The predictive filter helps counter this.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows the overall block diagram for a Modem system equipped with an Encode Transmission and Decode unit.

Figure 2 shows the Multilevel Equalizer Aided Channel Combining and Decode system.

Figure 3 shows the various logical components of the Pre-Combining Equalizer.

Figure 4 shows the various logical components of the Post-Combining Equalizer.

Figure 5 shows the flowchart of the dual equalization process.

Figure 6 shows the flowchart representation of the computational process of the weight prediction by the Linear Weight Prediction module using an algorithm such as Kalman Filter.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

5 **Figure 1** shows the overall block diagram for a Modem system equipped with an Encode transmission and Decode unit. The system consists of a PC **500**, a System Ethernet interface **501**, a Receive block **R**, a Transmit block **T**, an Oven-Controlled Crystal Oscillator (OCXO) **522** and a Clock Distribution **524**. The PC **500** is connected via the System Ethernet interface **501** to the Receive block **R** and the Transmit block **T**. The Transmit block **T** consists of a Scrambler **535**, an FEC Encoder **534**, a Burst Modulator **533**, a DAC driver **531**, a Digital to Analog Converter (DAC) **528**, a DAC DATACLK Generator **529**, a Low Pass Filter **527**, an IQ-Modulator **526**, an IQ-Modulator LO Generator **523**, an IF Front-end **525**, a Splitter **519** and Transmission channels **517**, **518**. The Receive block **R** consists of

10 Receive Channel-1 **516a**, Receive Channel-2 **516b**, Receive Channel-3 **516c** and Receive Channel-4 **516d**, Intermediate Frequency (IF)Front-end-1 **515a**, Intermediate Frequency (IF) Front-end-2 **515b**, Intermediate Frequency (IF) Front-end-3 **515c** and Intermediate Frequency (IF)Front-end-4 **515d**, IQ Demodulators **514a**, **514b**, **514c**, **514d**, Signal Conditioning **513a**, **513b**, **513c**,

15 **513d**, Analog to Digital Converters (ADC) **512a**, **512b**, **512c**, **512d**, a Multilevel Equalizer Aided Channel Combining and Demodulator **511**, a Forward Error Correction (FEC) Decoder **508**, a Descrambler**507**, a 4x IQ DEMOD LO Generator**520** and a 4×ADC CLK Generator **521**.

The PC **500** is any computing device that is capable of transmitting and receiving

25 an Ethernet data. The System Ethernet Interface **501** refers collectively to the Ethernet data processing system consisting of hardware ports and computing logic that acts on the data received from the PC **500** and given by the device to the PC **500**.Input bits **501x** are to be transmitted over the Intermediate Frequency (IF) interface. Bit Output **507x** is decoded from the signal received over the

30 Intermediate Frequency (IF) interface. The Descrambler **507** is responsible for

Descrambling of data that is scrambled by the Scrambler **535**. If the Scrambler **535** is disabled, the Descrambler **507** has to be bypassed. Scrambled Bit Output **508x** corresponds to the bits that are an output of the FEC Decoder **508** and are input to the Descrambler **507**. The FEC Decoder **508** is responsible for decoding of data that is encoded by the FEC Encoder **534** on the Transmit side. If the FEC Encoder **534** is disabled on the Transmit side, the FEC Decoder **508** has to be bypassed. Bit Error Rate (BER) **116** corresponds to the number of bit errors observed over a pre-defined pilot length. The Encoded and Scrambled Bit Output **510** are the bits prior to being sent to the FEC Decoder **508**. The Multilevel Equalizer Aided Channel Combining and Demodulator **511** are responsible for acquiring the data from multiple Analog to Digital Converters **512a..d**, does co-phasing, subsequently diversity combining, equalizes and demodulates the signal to obtain the data. The Analog to Digital Converters **512a..d** converts the analog signal from the Signal Conditioning **513a..d** to proportional multi-bit parallel digital values. The Signal Conditioning **513a..d** performs amplification and DC level shifting of the Analog signal to the levels appropriate to each of the Analog to Digital Converters **512a..d**. The IQ Demodulators **514a..d** converts the bandpass signal at Intermediate Frequency to a baseband signal. The IF Front End **515a..d** comprises a pair of Saw Filter Networks, Digital Step Attenuators and Low Noise Amplifiers. The multiple Receive Channels **516a..d** refers to the IF signal that is given to each of the IF Front End **515a..d**. The Transmit Out-1 **517**, Transmit Out-2 **518**, refers to the Analog Signal that is the IF output of the system. The Splitter **519** is a device that divides the signal from TX IF Front End **525** into two and hands over to Transmit Out-1 **517** and Transmit Out-2 **518**.

The input clocks are from the clock regenerators, the IQ Demodulator LO Generator **520** for the IQ Demodulators **514a..d**, the ADC Clock Generator **521** for Analog to Digital Converter **512a..d**, the IQ-Modulator LO Generator **523** for the IQ-Modulator **526**, the DAC Clock generator **529** for Digital to Analog Converter **528**. The Oven Controlled Crystal Oscillator (OCXO) **522** is an Ultra-Low Jitter 10MHz clock which forms the “Station Clock” of the system. The

Clock Distribution **524** allocates the OCXO **522** clock to the other clock generators in the system. The TX IF Front End **525** comprises a Saw Filter network, Attenuators and Low Noise Amplifiers of the Transmit side. The IQ-Modulator **526** converts the baseband In-Phase (I) and Quadrature-Phase (Q) signal to bandpass signal at Intermediate Frequency (IF). The Low Pass Filter **527** is used to remove the harmonics present in the output of the Digital to Analog Converter **528** and conserve the overall system bandwidth requirement. The Digital to Analog Converter **528** produces an analog waveform proportional to the digital value on the transmit data. It accepts a parallel digital data and produces an analog voltage proportional to the digital value. The DACDATACLK Generator **529** is clock regenerators that will clock the Digital to Analog Converter **528**. The DAC Driver **531** converts the data from the Burst Modulator **533** suitable for the Digital to Analog Converter **528**. The Burst Modulator **533** converts the data bits to In-Phase (I) and Quadrature-Phase (Q) data of appropriate levels. The FEC Encoder **534** does the forward error correction encoding on the data. Encoded and Scrambled Input Bits **534x** are the bits after the scrambling and FEC encoding processes. The Scrambler **535** is used for the following purposes, (a) to enable accurate timing recovery on the receiver without resorting to redundant line coding and (b) to disperse the energy on the carrier. It disperses the data to meet the maximum power spectral density requirements. Scrambled Input Bits **535x** refers to the bits to be transmitted after the scrambling process.

Figure 2 is the Multilevel Equalizer Aided Channel Combining and Decode system that consists of an Aligner **102**, a Pre-Combining Equalizer **104**, a Combiner **109**, a Receiver **110**, a PSK Demodulator **111**, a Post-Combining Equalizer **112**, a Symbol Decode **113** and an Adder **117**. The Pre-Combining Equalizer **104** includes multiple Weight Prediction Equalizers, CH-1 Weight Prediction Equalizer **104a**, CH-2 Weight Prediction Equalizer **104b**, CH-3 Weight Prediction Equalizer **104c**, CH-4 Weight Prediction Equalizer **104d**, multiple Least Mean Squared Error Equalizers (LMSE), CH-1 LMSE **105**, CH-2 LMSE **106**, CH-3 LMSE **107**, CH-4 Least LMSE **108**. There is one Weight Prediction

Equalizer and one Least Mean Squared Error Equalizer for each of the receive channels. Raw Samples **101** from each of the Analog to Digital Converters **512a..d** is captured. The Raw Samples **101** comprises a Pilot Data and the information to be transmitted. This Pilot Data is a pre-defined tone that occurs at a known interval. The Pilot Data is the “Desired Signal” and is distinctly distinguishable by the Receiver **110**. The Aligner **102** contains two portions which are a Time Aligner and a Phase Aligner. The signals received by the different receive channels encounters different path delays. The Time Aligner time aligns all the signals received at the different receive channels by adding appropriate delays. The signals received by the different receive channels encounter different phase rotations. The Phase Aligner is responsible for aligning the phase of all the received signals. A Desired Signal Occurrence Estimate (DSOE) **103** is the estimate of the next desired signal **305** in terms of the receiver sample clocks. The Pre-Combining Equalizer **104** observes a Bit Error Rate (BER) **116** coming from the FEC Decoder **508** and switches between the LMSE Equalizer and Weight Prediction Equalizer for each receive channel. The respective Weight Prediction Equalizer **104a..d** takes the history of the weights and try standard interpolation or prediction algorithms (like Kalman Filter) to compute the next weight. The LMSE Equalizer **105, 106, 107, 108** in which the samples from each of the Analog to Digital Converter **512a..d** is weighed independently, and each output signal is compared with a Desired Signal **305** sample to generate the error signals. These error signals, along with the input samples and a Step Size are used to compute the next set of weights. The Combiner **109** that can be a Maximal Ratio Combining or an Equal Gain Combining performs merging of the multiple inputs.

The Receiver **110** is a part of the decision device and performs an initial set of signal processing such as DC offset removal and a small phase rotation. The PSK Demodulator **111** is also a part of the decision device. The PSK Demodulator **111** comprises most of the signal processing control loops such as Pilot Symbol Detection, Symbol Timing Recovery, and Carrier Recovery control loops. The Post-Combining Equalizer **112** is a decision feedback equalizer, in which the

output of the Symbol Decode **113** is given to an array of delay elements where each output is weighed, and the weighted sum is fed to control the output of the Combiner **109**. The Symbol Decode **113** converts the samples into Symbols and combines the In-Phase (I) symbols and Quadrature-Phase (Q) symbols into bits.

5 Decision Feedback **114** is the feedback given to the Post-Combining Equalizer **112**. Decoded Symbol Output **115** is the symbol output from the Symbol Decode **113**. The Bit Error Rate (BER) **116** corresponds to the number of bit errors observed over a predefined pilot length. The Adder **117** performs a numeric signed addition of the two inputs, and the sum is given out at the output.

10 **Figure 3** includes the various logical components of the Pre-Combining Equalizer. A Standard Delay Element **300** provides one sample clock delay to the incoming samples that is when the output of the Standard Delay Element **300** is the previous sample, then the input of the Standard Delay Element **300** would be the current sample. The Multiplier **301** performs numeric signed multiplication of

15 the two inputs, and the product is given as the output. The Weight Prediction Equalizer **308** refers to any one of the CH-1 Weight Prediction Equalizer **104a**, CH-2 Weight Prediction Equalizer **104b**, CH-3 Weight Prediction Equalizer **104c**, CH-4 Weight Prediction Equalizer **104d**. The Switcher **303** observes the Bit Error Rate (BER) **116** coming from the FEC Decoder **508** and switches between the

20 CH-1 Weight Prediction Equalizer **104a** or CH-1 Least Mean Squared Error Equalizer **105** on Receive Channel-1, CH-2 Weight Prediction Equalizer **104b** or CH-2 Least Mean Squared Error Equalizer **106** on Receive Channel-2, CH-3 Weight Prediction Equalizer **104c** or CH-3 Least Mean Squared Error Equalizer **107** on Receive Channel-3 and CH-4 Weight Prediction Equalizer **104d** or CH-4

25 Least Mean Squared Error Equalizer **108** on Receive Channel-4. The Weight Update **304** performs standard weight update computations (e.g. LMS). The Desired Signal **305** is the known data (known to both transmitter and the receiver) that is transmitted at identified intervals. The Bit Error Rate **116** corresponds to the number of bit errors observed over a predefined pilot length.

Figure 4 includes the various logical components of the Post-combining Equalizer. The Receiver **110** is a part of the decision device and performs an initial set of signal processing such as DC offset removal and a small phase rotation. The PSK Demodulator **111** is also a part of the decision device and
5 comprises most of the signal processing control loops such as Pilot Symbol Detection, Symbol Timing Recovery and Carrier Recovery control loops. The Adder **117** performs numeric signed addition of the two inputs, and the sum is given out at the output. The Symbol Decode **113** converts the samples into
10 symbols into bits. The Post-Combining Equalizer **112** is a decision feedback equalizer, in which the output of the Symbol Decode **113** is given to an array of delay elements where each output is weighed, and the weighted sum is fed to control the output of the Combiner **109**. The Decision Feedback **114** is the feedback given to the Post-Combining Equalizer **112**. The Decoded Symbol
15 Output **115** is the symbol output from the Symbol Decode **113**.

Figure 5 shows the flowchart of the Dual Equalization process. The process starts **1** by the acquisition of the digital signal **2** from the multiple Analog to Digital Converter **512a..d** simultaneously **3** through the Aligner **102**. Desired Signal **305** is a tone that occurs periodically and detected using standard methods. The
20 received signal is subjected to identical processing **5**, for the detection of the start of the Desired Signal frame at the multiple receive channels **4**. The respective Desired Signal **305** detection circuits in the receive channel are employed for the detection process **6**. Once the first Desired Signal **305** is detected in any one of the channels, the clock counter in the respective Desired Signal Detection circuit is
25 initiated **7**. The same process applies to the detection of the Desired Signal **305** in the other channel at the respective Desired Signal detection circuit **8**. Upon detection of the Desired Signal **305** in the last channel, the clock counters in the previous channels are terminated **9**. The channel with the signal that is responsible for the termination of clock counters in the other channels is the reference
30 channel. All other channels are referenced to this channel. The count on each of

the clock counters corresponds to the path delay experienced by the signal received at the respective antenna. As the Desired Signal **305** tone is periodic, once aligned it is possible to estimate the next occurrence in terms of the receive clocks **10**. The Desired Signal Occurrence Estimate (DSOE) **103** is a pre-determined number of receive clock cycles after which the next pilot tone is expected to occur. The above flow is called the Delay Computation Path. Identification of the reference channel is responsible for the change in the signal path from Delay Computation Path flow to Data Path flow.

The Desired Signal Occurrence Estimate **103** is used to fill and flush the system buffer, and the arrival is kept track by a counter that expires on the start of the Desired Signal **305**, checks if the desired signal estimations are aligned **11**. If they are aligned then, the Desired Signal Occurrence estimate **103** is generated **12**. Here the signal is time-aligned as the Chain Delay Counter consists of pre-determined time delay **13** for channels. The precision of alignment is limited by the resolution of time-base and the jitter of the clock. The time-aligned signal in each channel is transmitted **14** to the corresponding Pre-Combining Equalizer **104**, which stores the weight-related data of the Desired Signal Occurrence Estimate **103** in a system Buffer **15**. Once the filling process stops, the LMSE equalization process begins **18** in the LMSE Equalizers **105**, **106**, **107**, **108** and is done for a desired signal sample length. One or more final weights, thus obtained will be applicable for the samples acquired after this calculation and are valid till the next set of weights are computed based on the Pilot indicator state. For the first pilot detected, the buffered samples are being equalized, and simultaneously the other stream passes through the equalizer transparently without any modifications. However, once the weights are computed, the same are applied to the stream data by convolution. This process is repeated for each Desired Signal detected in the received stream, and the previous weights are used as the initial weights for every subsequent equalization process. A weight array is created for every Desired Signal passing through the equalizer as the copy of weights obtained from the Equalizer is stored in another buffer. The Bit Error Rate **116** is

computed using standard methods once the signal is decoded **27**, which are fed to the equalizer and the process continues until an acceptable threshold of the Bit Error Rate **116** is achieved. Upon attainment of the acceptable BER value, the weight update process switches **16** from the LMSE Equalizers **105, 106, 107, 108** to the corresponding Weight Prediction Equalizer **104a..d**. This leads to the requirement of fewer instances of the pilot and thus increases the overall bandwidth of the system. The estimated results of the CH-1 Least Mean Squared Error Equalizer **105** is replaced with CH-1 Weight Prediction Equalizer **104a**, CH-2 Least Mean Squared Error Equalizer **106** is replaced with CH-2 Weight Prediction Equalizer **104b**, CH-3 Least Mean Squared Error Equalizer **107** is replaced with CH-3 Weight Prediction Equalizer **104c** and CH-4 Least Mean Squared Error Equalizer **108** is replaced with CH-4 Weight Prediction Equalizer **104d** weights in the system **17**. Thus, helps to adapt weights to the changing channel in the absence of the new weights from the LMSE and also to aid faster convergence to steady state for LMSE.

Once, the steady state is achieved, which will be after some iteration, the final weights computed depending on the Bit Error Rate **116** output is retained, and the process of switching of the weights is evaded. The equalized signal is combined by a multipath Combiner that incorporates either the maximal ratio combining (MRC) or equal gain combining (EGC) methods **19**, so as to increase the signal-to-noise (S/N) ratio of the signal received. The combined signal is processed **20** by the Receiver **110** and PSK Demodulator **111**, followed by the process of post-combining equalization **21** by the Post-Combining Equalizer that equalizes the signal and eliminates the residual error that may be introduced or remaining during the combination process. The Decision Feedback **114** is the feedback given to the Post-Combining Equalizer **112**. The original information is then extracted from the Post-Combining Equalizer **112** by the FEC Decoder **508** and a Descrambler **507** at **22**. The output of the FEC Decoder **23**, the Bit Error Rate, **116** is given to the Pre-Combining Equalizer **104** for switching between Ch-1 Least Mean Squared Error Equalizer **105** and CH-1 Weight Prediction Equalizer

104a, CH-2 Least Mean Squared Error Equalizer **106** and CH-2 Weight Prediction Equalizer **104b**, CH-3 Least Mean Squared Error Equalizer **107** and CH-3 Weight Prediction Equalizer **104c**, CH-4 Least Mean Squared Error Equalizer **108** and CH-4 Weight Prediction Equalizer **104d** which ends the
5 Process **24**.

Figure 6 shows the flowchart representation of the computational process of the weight prediction by the Linear Weight Prediction using an algorithm such as Kalman Filter. The algorithm starts **401** with the acquisition of the observation vector 'V' which corresponds to the actual weight that is obtained from the Least
10 Mean Square Error (LMSE) method and defining a control vector 'u', which defaults to zero value while deriving the obtained value 'z' **402**. The next step includes the initialization of the system matrix involving the state transition matrix 'A', input matrix 'B' and the observation matrix 'H', with a default value of 1 for each matrix. This step also initializes other parameters like process noise
15 covariance 'Q' and measurement noise covariance 'R' at **403**, followed by verifying if x, P are available. If available skips **405**, else executes at **404**. Since the values of x and P are not available, the algorithm will estimate an initial value for 'x' and 'P' **405**. The next step **406** involves consecutively computing the predictions for the state vector 'x'. Then compute the Co-variance Matrix P **407**.
20 Further computes the Kalman Gain **408**, compute the correction based on the observation for the state estimate **409** and computes the correction based on the observation for the Covariance Matrix **410**. The computed x is iteratively fed **406** to reduce the error **411** and thus ends the process **412**.

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CLAIMS

1. A Multilevel Equalizer Aided Channel Combining and Decode system having a Weight Prediction Equalizer in each receive channel for effective operation in any channel condition consists of (a) an Aligner **102**,(b) a Pre-combining Equalizer **104**, (c) a Combiner **109**, (d) a Receiver **110**,(e) a Phase-Shift Keying (PSK) Demodulator **111**, (f) a Post Combining Equalizer **112**, (g) a Symbol Decode **113**, (h) an Adder **117**, (i) a Desired Signal Occurrence Estimate (DSOE) **103**, (j) a Decision Feedback **114**, (k) a Decoded Symbol output **115**, (l) a Bit Error Rate (BER) **116**, (m) one or more Raw samples **101** and (n) a FEC Decoder **508**, wherein:
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- a. The Pre-combining equalizer **104** includes multiple Weight Prediction Equalizers, CH-1 Weight Prediction Equalizer **104a**, CH-2 Weight Prediction Equalizer **104b**, CH-3 Weight Prediction Equalizer **104c**, CH-4 Weight Prediction Equalizer **104d**, multiple Least Mean Squared Error Equalizers (LMSE), CH-1 LMSE **105**, CH-2 LMSE **106**, CH-3 LMSE **107**, CH-4 Least LMSE **108**, one Weight Prediction Equalizer and one Least Mean Squared Error Equalizer for each of the receive channels;
 - b. The Raw Samples **101** comprising a Pilot Data and information to be transmitted are captured from each of the Analog to Digital Converters **512a..d**;
 - c. The Aligner **102** is comprised of (a) a Time Aligner and (b) a Phase Aligner;
 - d. The Desired Signal Occurrence Estimate (DSOE) **103** is an estimate of a next desired signal **305** in terms of receiver sample clocks;
 - e. The Pre-combining Equalizer **104** observes the Bit Error Rate (BER) **116** coming from the FEC Decoder **508** and switches between the LMSE Equalizer and Weight Prediction Equalizer for each receive channel;

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- f. The corresponding Weight Prediction Equalizer **104a..d** takes the history of weights to compute the next weight;
 - g. The LMSE Equalizer **105, 106, 107, 108** in which samples from each of the Analog to Digital Converter **512a..d** are weighed independently, and each output signal is compared with the Desired Signal **305** sample to generate error signals;
 - h. The Combiner **109** performs merging of multiple inputs;
 - i. The Receiver **110** is a part of a decision device and performs an initial set of signal processing such as DC offset removal and a small phase rotation;
 - j. The PSK Demodulator **111** is also a part of the decision device comprising most of signal processing control loops such as Pilot Symbol Detection, Symbol Timing Recovery, and Carrier Recovery control loops;
 - k. The Post Combining Equalizer **112** is a decision feedback equalizer, in which output of the Symbol Decode **113** is given to an array of delay elements where each output is weighed, and the weighted sum is fed to control the output of the Combiner **109**;
 - l. The Symbol Decode **113** converts samples into Symbols and combines In-Phase (I) symbols and Quadrature-Phase (Q) symbols into bits;
 - m. The Decision Feedback **114** is a feedback given to the Post Combining Equalizer **112**;
 - n. The Decoded Symbol Output **115** is symbol output from the Symbol Decode **113**;
 - o. The Bit Error Rate (BER) **116** corresponds to number of bit errors observed over a pre-defined pilot length; and
 - p. The Adder **117** performs a numeric signed addition of the two inputs, and the sum is given out as the output.

2. A Multilevel Equalizer Aided Channel Combining and Decode system of Claim 1, wherein the Pilot Data is a pre-defined tone that occurs at a known interval and is a “Desired Signal” and is distinctly distinguishable by the Receiver **110**.
- 5 3. A Multilevel Equalizer Aided Channel Combining and Decode system of Claim 1, wherein one or more signals received by different receive channels encounter different path delays and the signals received by the different receive channels encounter different phase rotations wherein:
- 10 a. A Time Aligner time aligns all the signals received at different receive channels by adding appropriate delays; and
- b. A Phase Aligner is responsible for aligning phase of all the received signals.
4. A Multilevel Equalizer Aided Channel Combining and Decode system of Claim 1, wherein the corresponding Weight Prediction Equalizer **104a..d**
- 15 takes the history of the weights and tries standard interpolation and prediction methods including the application of a Kalman Filter to compute the next weight, the LMSE Equalizer **105, 106, 107, 108** in which the samples from each of the Analog to Digital Converter **512a..d** are weighed independently, and each output signal is compared with a Desired Signal
- 20 **305** sample to generate the error signals, this along with the input samples and a Step Size is used to compute the next set of weights.
5. A Multilevel Equalizer Aided Channel Combining and Decode system of Claim 1, wherein the Combiner **109** uses Maximal Ratio Combining.
- 25 6. A Multilevel Equalizer Aided Channel Combining and Decode system of Claim 1, wherein the Combiner **109** uses Equal Gain Combining.
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7. A Multilevel Equalizer Aided Channel Combining and Decode system of Claim 1, wherein the Pre-combining Equalizer further comprises (a) one or more Standard Delay Elements **300**, (b) a Multiplier **301**, (c) a Weight Prediction Equalizer **308**, (d) a Switcher **303**, (e) a Weight Update module **304**, (f) a Desired Signal **305** and (g) a Bit Error Rate (BER) **116** wherein:
- a. The standard delay element **300** provides one sample clock delay to incoming samples that is when output of the Standard Delay Element is previous sample, then input of the Standard Delay Element would be current sample;
 - b. The Multiplier **301** performs numeric signed multiplication of the two inputs, and the product is given as the output;
 - c. The Weight Prediction Equalizer **308** refers to any one of the CH-1 Weight Prediction Equalizer **104a**, CH-2 Weight Prediction Equalizer **104b**, CH-3 Weight Prediction Equalizer **104c**, CH-4 Weight Prediction Equalizer **104d**;
 - d. The Switcher **303** observes the Bit Error Rate (BER) **116** coming from the FEC Decoder **508** and switches between the CH-1 Weight Prediction Equalizer **104a** or CH-1 Least Mean Squared Error Equalizer **105** on Receive Channel-1, CH-2 Weight Prediction Equalizer **104b** or CH-2 Least Mean Squared Error Equalizer **106** on Receive Channel-2, CH-3 Weight Prediction Equalizer **104c** or CH-3 Least Mean Squared Error Equalizer **107** on Receive Channel-3 and CH-4 Weight Prediction Equalizer **104d** or CH-4 Least Mean Squared Error Equalizer **108** on Receive Channel-4;
 - e. The Weight Update module **304** performs standard weight update computations including Least Means Square (LMS); and
 - f. The Desired Signal **305** is the known data (known to both transmitter and the receiver) that is transmitted at identified intervals.

8. A Multilevel Equalizer Aided Channel Combining and Decode system of Claim 1 wherein the Post-combining Equalizer **112** is a decision feedback equalizer, further comprises (a) a Decision Feedback **114**, (b) a Multiplier **301**, (c) a Weight Update module **304** and (d) one or more standard delay elements **300**, wherein:
- a. The Decision Feedback **114** is a feedback given to the Post Combining Equalizer **112**;
 - b. The standard delay element **300** provides one sample clock delay to the incoming samples that is when the output of the Standard Delay Element is the previous sample, then the input of the Standard Delay Element would be the current sample;
 - c. The Multiplier **301** performs numeric signed multiplication of the two inputs, and the product is given as the output; and
 - d. The Weight Update module **304** performs standard weight update computations including Least Means Square (LMS).
9. A Multilevel Equalizer Aided Channel Combining and Decoding method having a Weight Prediction Equalizer in each receive channel for effective operation in any channel condition that consists of (a) an Aligner **102**, (b) a Pre-combining Equalizer **104**, (c) multiple Weight Prediction Equalizers, CH-1 Weight Prediction Equalizer **104a**, CH-2 Weight Prediction Equalizer **104b**, CH-3 Weight Prediction Equalizer **104c**, CH-4 Weight Prediction Equalizer **104d**, (d) multiple Least Mean Squared Error Equalizers (LMSE), CH-1 LMSE **105**, CH-2 LMSE **106**, CH-3 LMSE **107**, CH-4 Least LMSE **108**, (e) a Combiner **109**, (f) a Receiver **110**, (g) a Phase-Shift Keying (PSK) Demodulator **111**, (h) a Post Combining Equalizer **112**, (i) a Symbol Decode **113**, (j) an Adder **117**, (k) a Desired Signal Occurrence Estimate (DSOE) **103**, (l) a Decision Feedback **114**, (m) a Decoded Symbol output **115**, (n) a Bit Error Rate (BER) **116**, (o) one or more Raw samples **101**, (p) one or more final weights, (q) one or more streams that correspond to the output of the Aligner and (r) a FEC Decoder **508**, comprising the steps of:

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- a. Acquiring **1** digital signal **2** from multiple Analog to Digital Converter **512a..d** simultaneously **3**, through the Aligner **102**;
 - b. Subjecting the received signal **4** to identical processing **5**, for detection of the start of the Desired Signal frame at the multiple receive channels;
 - c. Employing the respective Desired Signal **305** detection circuits in the receive channel for a detection process **6**;
 - d. Initiating **7** a clock counter in the respective Desired Signal Detection circuit, once the first Desired Signal **305** is detected in any one of the channels and applying the same process to the detection of the Desired Signal **305** in the other channel at the respective Desired Signal detection circuit **8**;
 - e. Terminating **9** the clock counters in the previous channels upon detection of the Desired Signal **305** in the last channel;
 - f. Estimating the next occurrence of the Desired Signal **305** tone after alignment wherein the clock count value is called the Desired Signal Occurrence Estimate (DSOE) **103** and is a number of receive clock cycles after which the next pilot tone is expected to occur, called a Delay Computation Path;
 - g. Filling and flushing of system buffer based on the Desired Signal Occurrence Estimate **103**, the arrival of which is kept track by a counter that expires on start of the Desired Signal **305**, to check if desired signal estimations are aligned **11**;
 - h. Generating **12** the Desired Signal Occurrence estimate **103** where the signal is time-aligned as a Chain Delay Counter consists of pre-determined time delay for the channels **13** such that precision of alignment is limited by a resolution of time-base and jitter of the clock;

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- i. Transmitting the time-aligned signal in each channel **14** to the corresponding Pre-Combining Equalizer **104**, which stores weight-related data of the Desired Signal Occurrence Estimate **103** in a system buffer **15**;
 - j. Initiating an LMSE equalization process **18** once the filling stops in the LMSE Equalizers **105**, **106**, **107**, **108** and is done for a desired signal sample length;
 - k. Combining the equalized signal **19** by a multipath Combiner to increase the signal-to-noise (S/N) ratio of the signal received;
 - l. Processing the combined signal **20** by the Receiver **110** and PSK Demodulator **111**;
 - m. Performing post-combining equalization **21** by the Post-Combining Equalizer **112** that equalizes the signal and eliminates residual error that may either be introduced or remaining during the combination process; and
 - n. Sending the output of the FEC Decoder **23**, the Bit Error Rate, **116** to the Pre-Combining Equalizer **104** for switching **18** between CH-1 Least Mean Squared Error Equalizer **105** and CH-1 Weight Prediction Equalizer **104a**, CH-2 Least Mean Squared Error Equalizer **106** and CH-2 Weight Prediction Equalizer **104b**, CH-3 Least Mean Squared Error Equalizer **107** and CH-3 Weight Prediction Equalizer **104c**, CH-4 Least Mean Squared Error Equalizer **108** and CH-4 Weight Prediction Equalizer **104d**, **24**.
10. A Multilevel Equalizer Aided Channel Combining and Decoding method of Claim 9 having an improved, bandwidth conserving weight prediction equalizer wherein:
- a. One or more final weights are applicable for the samples acquired after this calculation and are valid till the next set of weights are computed based on Pilot indicator state;

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- b. For the first pilot detected, buffered samples are equalized, and simultaneously the other stream passes through the equalizer transparently without any modifications where once the weights are computed, the same are applied to the stream data by convolution;
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- c. Step b is repeated for each Desired Signal detected in received stream, and the previous weights are used as initial weights for every subsequent equalization process;
- d. A weight array is created for every Desired Signal **305** passing through the equalizer as copy of weights obtained from the equalizer is stored in another buffer;
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- e. The Bit Error Rate **116** is computed using standard methods, once the signal is decoded **27** which are fed to the equalizer and the process continues until an acceptable threshold of the Bit Error Rate **116** is achieved;
- f. Upon attainment of the acceptable BER value, weight update process switches **16** from the LMSE Equalizers **105, 106, 107, 108** to the corresponding Weight Prediction Equalizer **104a..d**; and
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- g. The estimated results of the CH-1 Least Mean Squared Error Equalizer **105** is replaced with CH-1 Weight Prediction Equalizer **104a**, CH-2 Least Mean Squared Error Equalizer **106** is replaced with CH-2 Weight Prediction Equalizer **104b**, CH-3 Least Mean Squared Error Equalizer **107** is replaced with CH-3 Weight Prediction Equalizer **104c** and CH-4 Least Mean Squared Error Equalizer **108** is replaced with CH-4 Weight Prediction Equalizer **104d** weights in the system **17** thereby assisting the system to adapt weights to changing channel in the absence of the new weights from the LMSE and also to aid faster convergence to steady state for LMSE.
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11. A Multilevel Equalizer Aided Channel Combining and Decoding method of Claim 9, wherein:
- a. The channel with the signal that is responsible for the termination of clock counters in the other channels is the reference channel and all other channels are referenced to this channel;
 - b. The count on each of the clock counters corresponds to the path delay experienced by the signal received at the respective antenna;
 - c. Desired Signal Occurrence Estimate (DSOE) **103** is a pre-determined number of receive clock cycles after which the next pilot tone is expected to occur; and
 - d. Identification of the reference channel is responsible for the change in the signal path from Delay computation path flow to Data Path flow.
12. A Multilevel Equalizer Aided Channel Combining and Decoding method of Claim 9, wherein the Combiner **109** incorporates maximal ratio combining (MRC).
13. A Multilevel Equalizer Aided Channel Combining and Decoding method of Claim 9, wherein the Combiner **109** incorporates equal gain combining (EGC) method **19**.
14. A Multilevel Equalizer Aided Channel Combining and Decoding method of Claim 9, having a Delay computation path wherein:
- a. A periodic Desired Signal **305** tone that once aligned makes it possible to estimate the next occurrence in terms of receive clocks **10**;
 - b. The clock count value is called Desired Signal Occurrence Estimate (DSOE) **103** and is a number of receive clock cycles after which the next pilot tone is expected to occur; and
 - c. Identification of the reference channel is responsible for the change in the signal path to Data Path flow.

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15. A Multilevel Equalizer Aided Channel Combining and Decoding method of Claim 9, wherein upon achieving steady state, the final weights computed depending on the Bit Error Rate **116** output is retained, and the process of switching of the weights is avoided.

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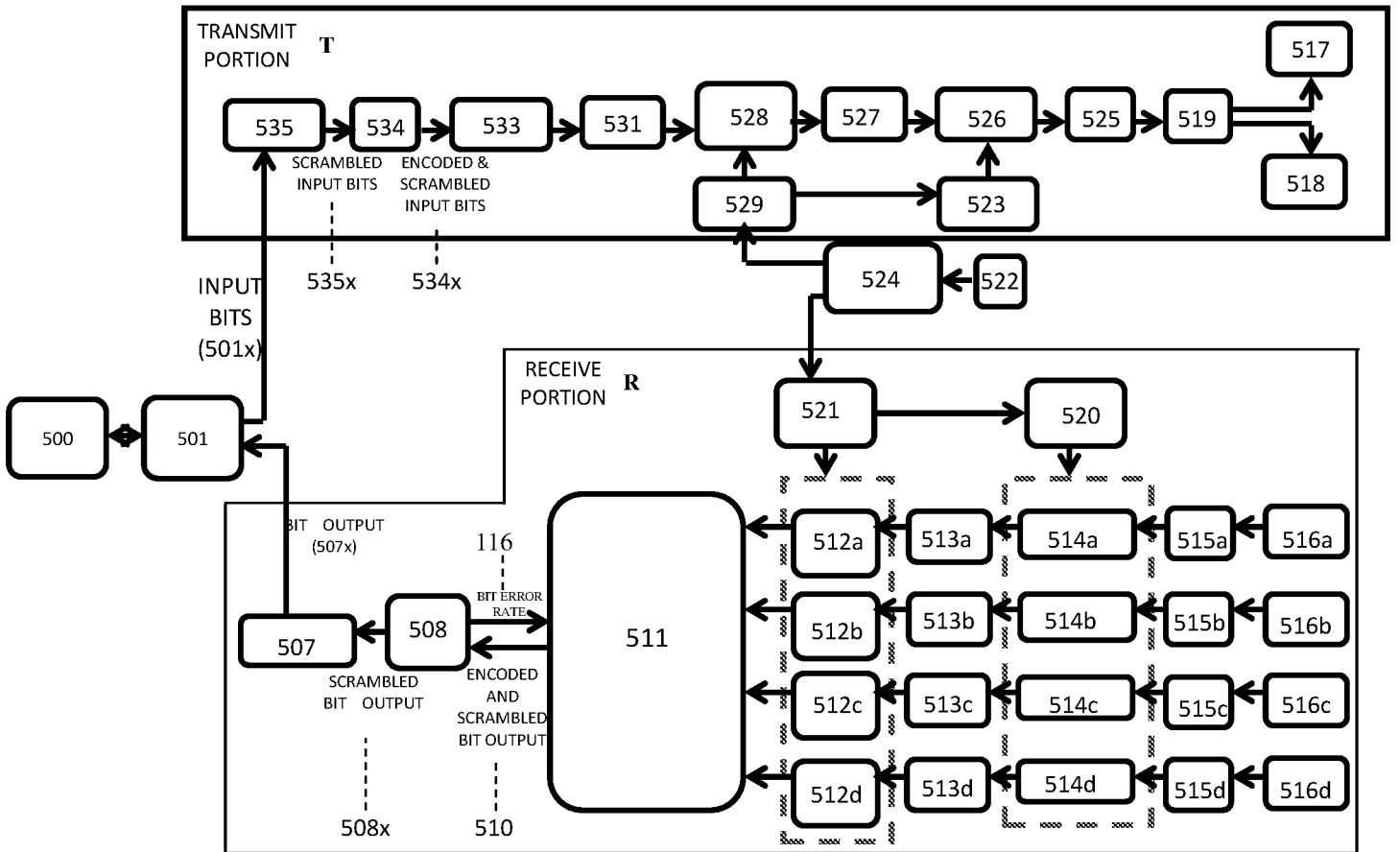


Figure 1

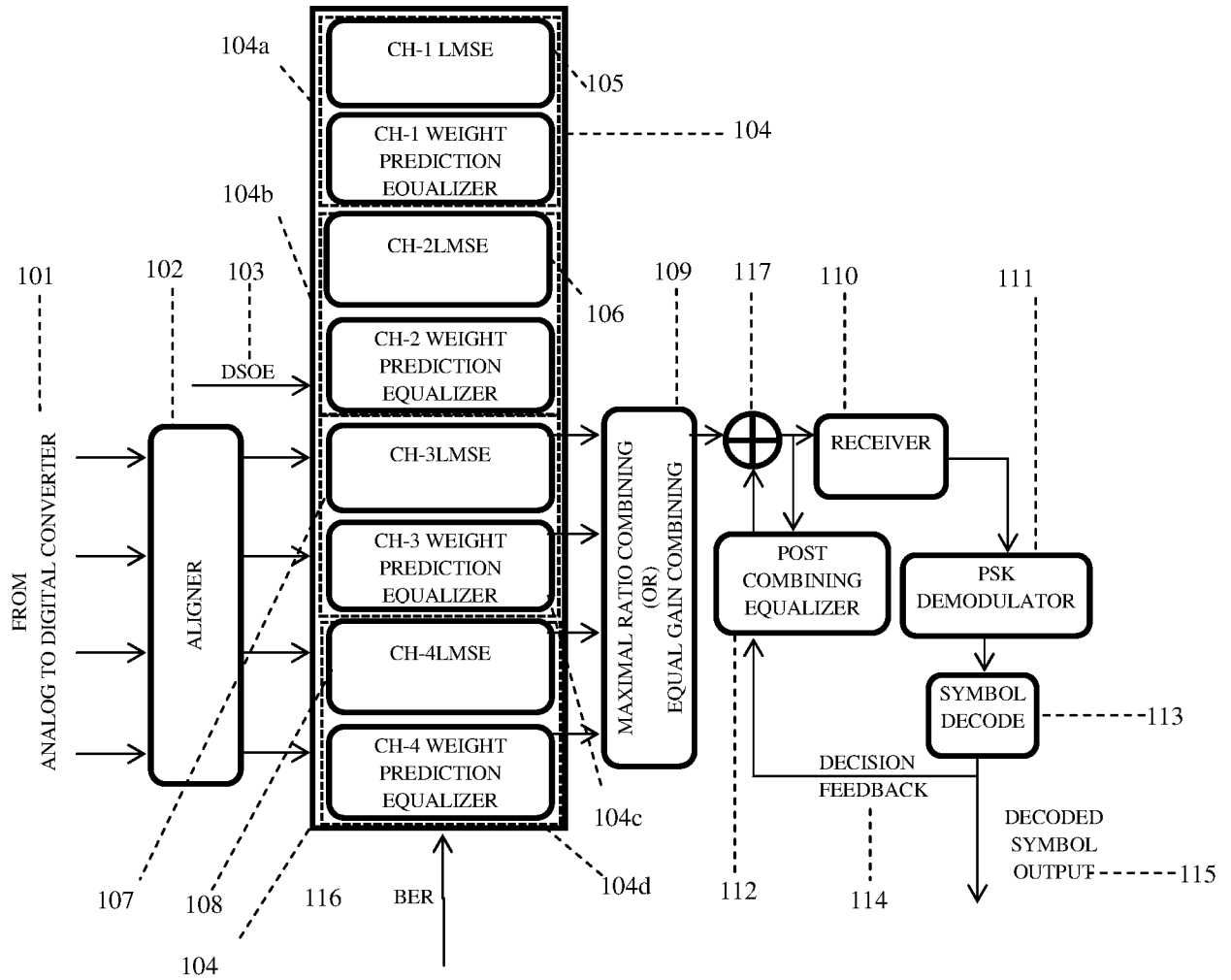


Figure 2

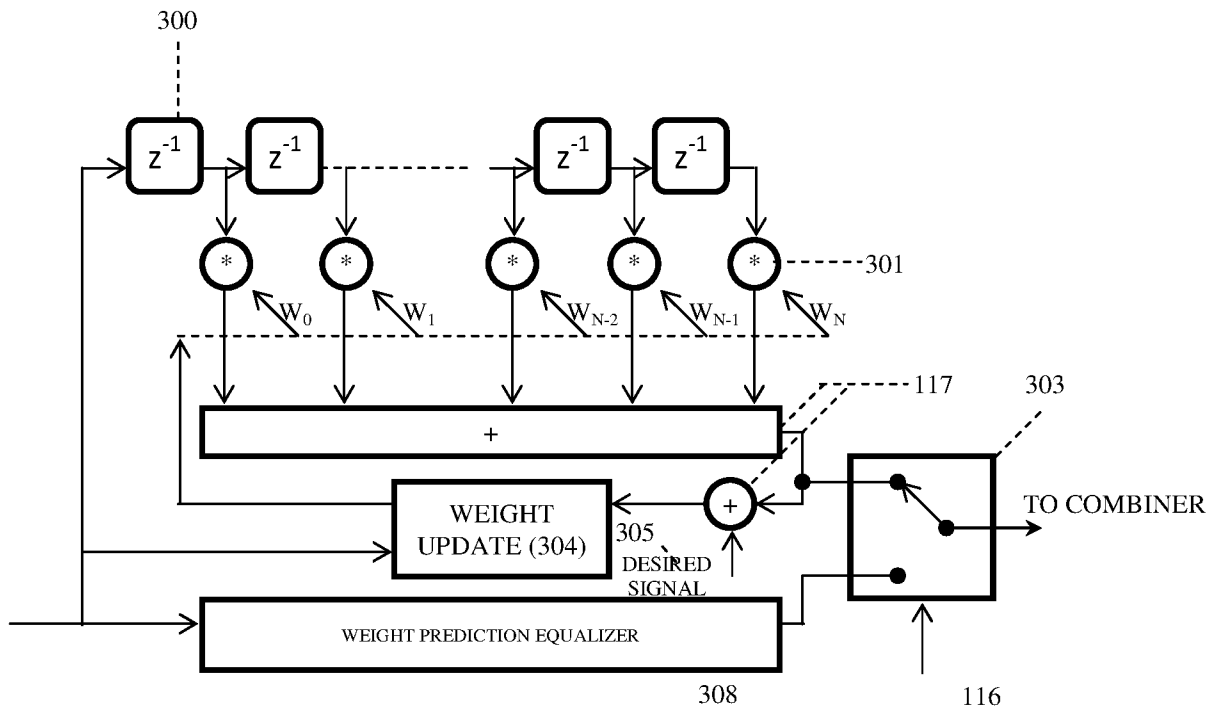


Figure 3

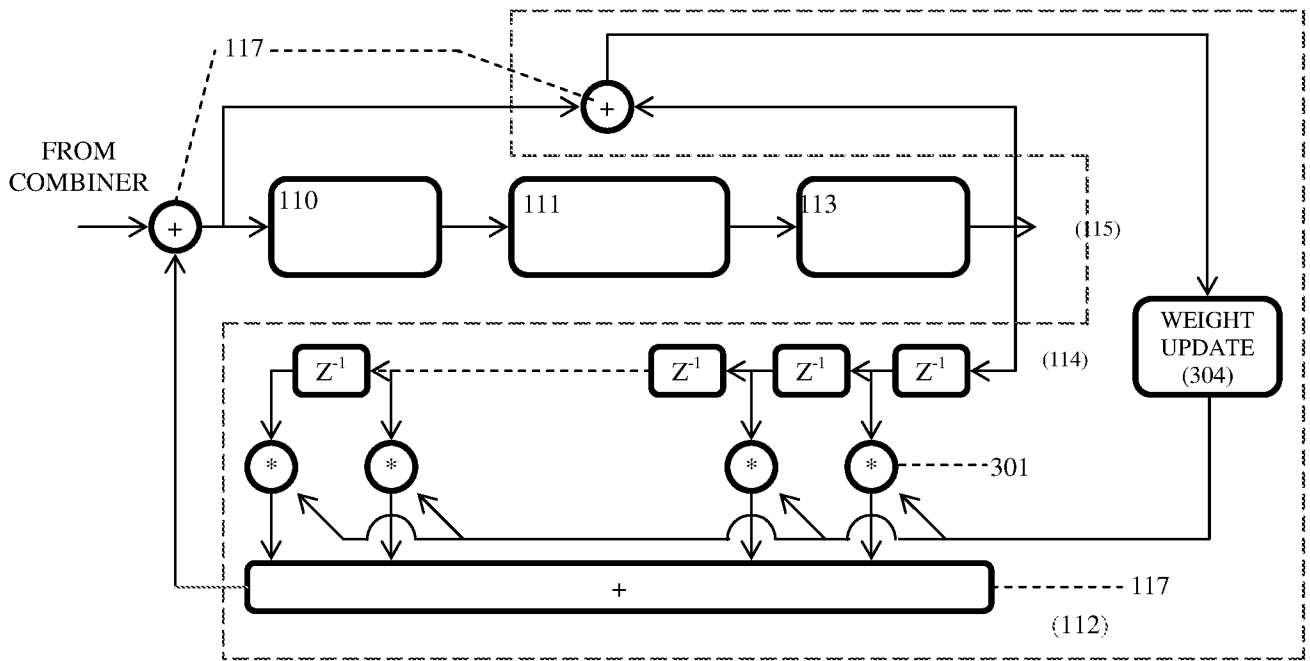
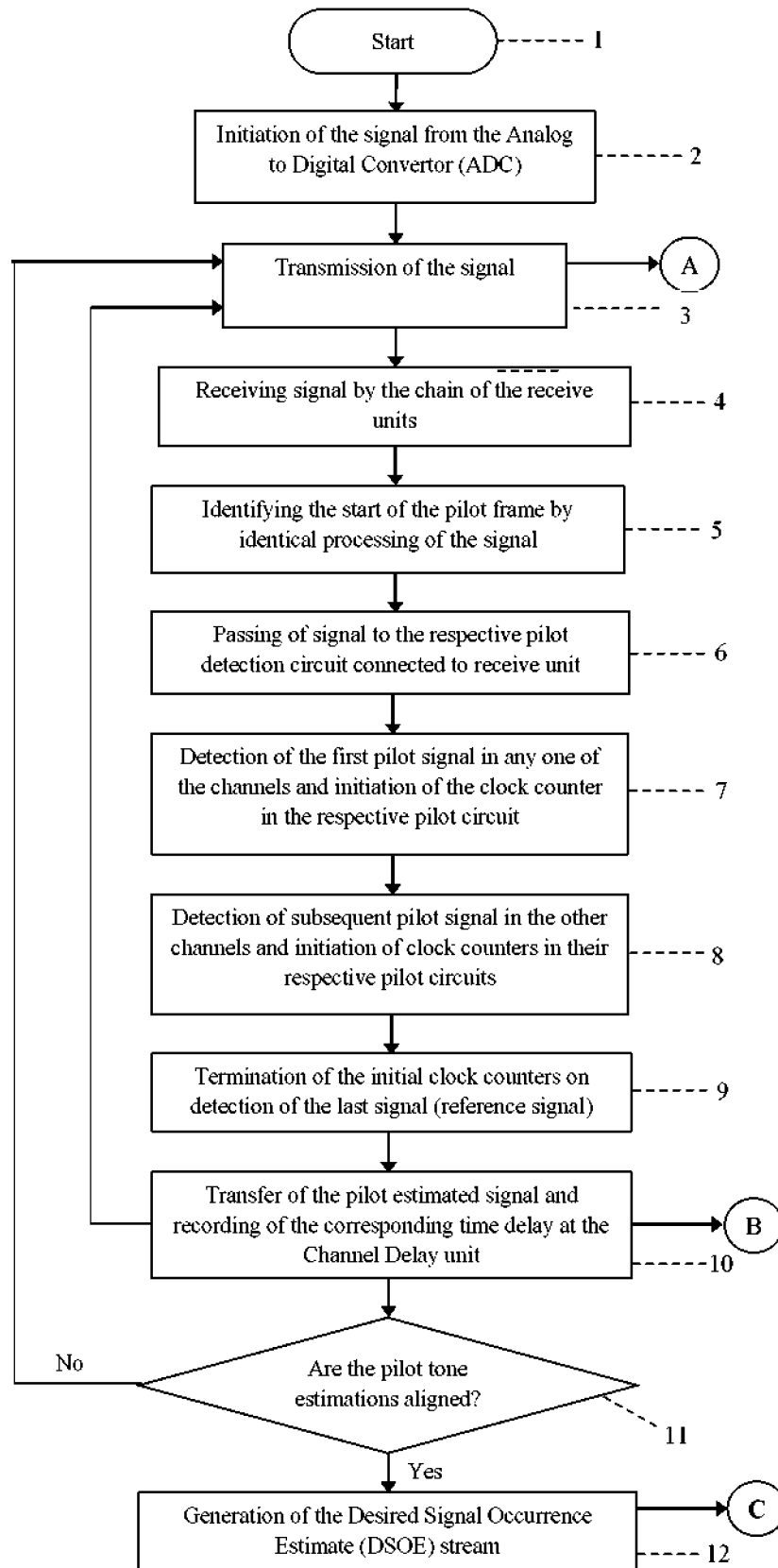


Figure 4



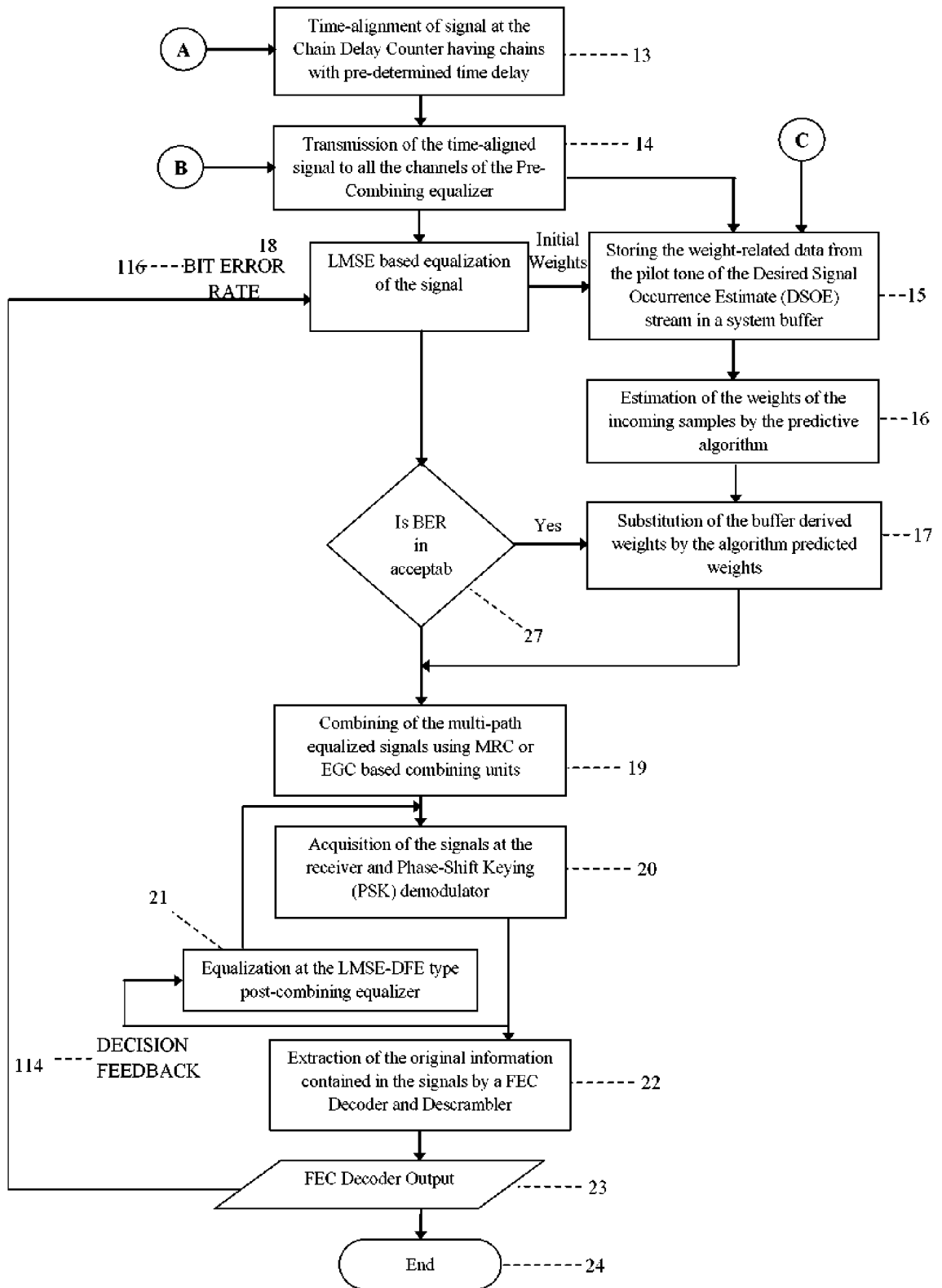


Figure 5

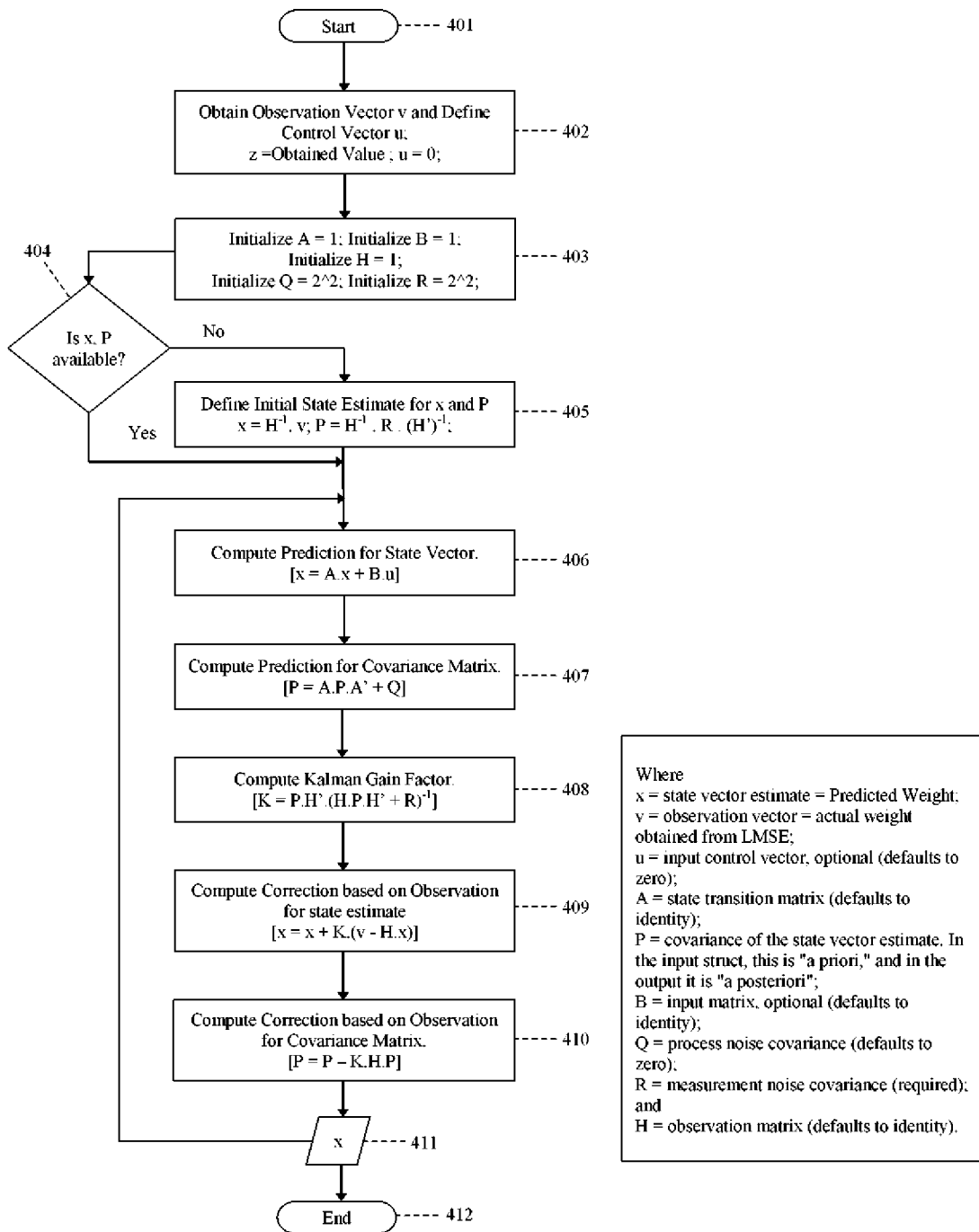


Figure 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IN2016/050153

A. CLASSIFICATION OF SUBJECT MATTER
H04L25/00,H04L27/00 Version=2016.01

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Databases:Patseer, IPO Internal Database
Search terms:multilevel equalizer,bandwidth,linear predictive filtering

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	D1: US6862315 B1 (ADVANCED MICRO DEVICES, INC.) 01 MARCH 2005 (01-03-2005) Page 2, line 15-page3, line38; page4, line62-page5, line 20;	1-15

Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier application or patent but published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 09-09-2016	Date of mailing of the international search report 09-09-2016
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