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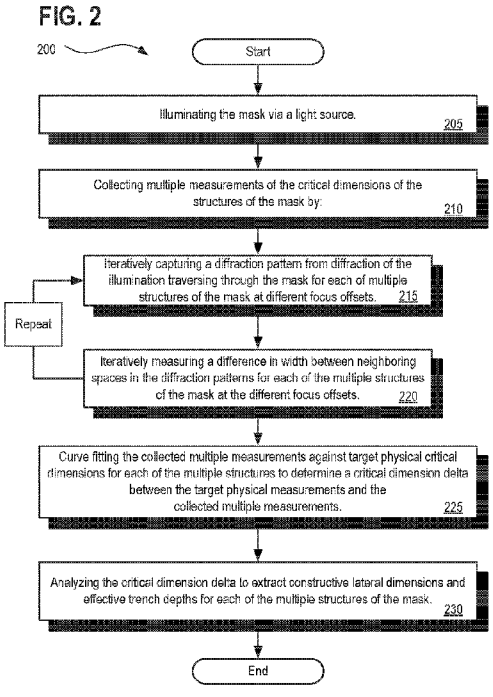
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(54) **Title**: SYSTEMS, METHODS, AND APPARATUSES FOR IMPLEMENTING CRITICAL DIMENSION (CD) AND PHASE CALIBRATION OF ALTERNATING PHASE SHIFT MASKS (APSM) AND CHROMELESS PHASE LITHOGRAPHY (CPL) MASKS FOR MODELING

FIG. 2



(57) **Abstract**: In accordance with disclosed embodiments, there are provided methods, systems, and apparatuses for implementing critical dimension (CD) and phase calibration of alternating phase shift masks (APSM) and chromeless phase lithography (CPL) masks for modeling. For instance, in accordance with one embodiment, there are means described for identifying critical dimensions of structures of a mask via means for illuminating the mask via a light source; collecting multiple measurements of the critical dimensions of the structures of the mask by iteratively: (i) capturing a diffraction pattern from diffraction of the illumination traversing through the mask for each of multiple structures of the mask at different focus offsets, and (ii) measuring a difference in width between neighboring spaces in the diffraction patterns for each of the multiple structures of the mask at the different focus offsets; curve fitting the collected multiple measurements against target physical critical dimensions for each of the multiple structures to determine a critical dimension delta between the target physical measurements and the collected multiple measurements; and analyzing the critical dimension delta to extract constructive lateral dimensions and effective trench depths for each of the multiple structures of the mask. Other related embodiments are disclosed.

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SYSTEMS, METHODS, AND APPARATUSES FOR IMPLEMENTING CRITICAL DIMENSION (CD) AND PHASE CALIBRATION OF ALTERNATING PHASE SHIFT MASKS (APSM) AND CHROMELESS PHASE LITHOGRAPHY (CPL) MASKS FOR MODELING

CLAIM OF PRIORITY

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TECHNICAL FIELD

[0003] The subject matter described herein relates generally to the field of semiconductor and electronics manufacturing, and more particularly, to systems, methods, and apparatuses for implementing critical dimension (CD) and phase calibration of alternating phase shift masks (APSM) and chromeless phase lithography (CPL) masks for modeling.

BACKGROUND

[0004] The subject matter discussed in the background section should not be assumed to be prior art merely as a result of its mention in the background section. Similarly, a problem mentioned in the background section or associated with the subject matter of the background section should not be assumed to have been previously recognized in the prior art. The subject matter in the background section merely represents different approaches, which in and of themselves may also correspond to embodiments of the claimed subject matter.

[0005] Conventional techniques used for three-dimension mask metrologies are either physically destructive to the masks being evaluated or are now insufficiently accurate as semiconductor manufacturing techniques necessitate increasingly strict tolerances and smaller

physical dimensions.

[0006] Conventional methodologies measure Critical Dimensions (CDs) using Critical Dimension Scanning Electron Microscopy (CDSEM). The measured critical dimensions vary as a function of CDSEM image acquisition and algorithm settings as well as the three-dimensional profile of the mask, which in turn, may negatively affect the OPC model accuracy.

[0007] In addition, complementary techniques that measures that three-dimensional profile of the mask required the physical destruction of the mask itself in order to obtain the measurements which themselves carry significant uncertainty due to the complex profile of the mask and its dimensions. The measurements required are extremely small and simply cannot be measured with sufficient precision using the presently available techniques.

[0008] Additionally, the masks being evaluated are not necessarily perfectly perpendicular or flat as they are cut for the purpose of obtaining the measurements, which therefore increases the difficulty of relating the measurements of the physical mask back to the OPC model thus increasing inaccuracies and uncertainty due to such variances.

[0009] The accuracy of these measurements and the accuracy of the model is of utmost importance because any variation of the OPC model translates to a variation of dimensions on the final semiconductors chip produced.

[0010] When the physical dimensions of the manufactured semiconductors were greater, such inaccuracies and uncertainty were manageable due to the greater margins. However, as the physical size of these manufactured semiconductors is reduced farther into the nanometer realm of manufacturing, it becomes necessary to operate using increasingly accurate models if manufacturing yields are to remain economically viable.

[0011] The present state of the art may therefore benefit from the systems, methods, and apparatuses for implementing critical dimension (CD) and phase calibration of alternating phase shift masks (APSM) and chromeless phase lithography (CPL) masks for modeling as described herein.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Embodiments are illustrated by way of example, and not by way of limitation, and will be more fully understood with reference to the following detailed description when considered in connection with the figures in which:

[0013] **Figure 1A** depicts an SEM image grating with a 160 nanometer pitch printed on a wafer using a narrow-line illumination 125 in accordance with which embodiments may operate;

[0014] **Figure 1B** depicts a flow diagram in accordance with described embodiments;

[0015] **Figure 1C** shows an equation by which to calculate the intensity slice at image plane for three-beam interference in accordance with described embodiments;

[0016] **Figure 1D** depicts a plot generated via a Rigorous Lithography Simulator calculation in accordance with described embodiments;

[0017] **Figure 1E** depicts a plot of actual measurement data points with curve fitting in accordance with described embodiments;

[0018] **Figure 1F** depicts the maximum critical dimension delta through focus plotted against the drawn width in nanometers in accordance with described embodiments;

[0019] **Figure 1G** depicts a plot of a focus offset which has zero resist critical dimension delta in accordance with described embodiments;

[0020] **Figure 2** is a flow diagram illustrating a method for implementing critical dimension (CD) and phase calibration of alternating phase shift masks (APSM) and chromeless phase lithography (CPL) masks for modeling in accordance with described embodiments;

[0021] **Figure 3** illustrates a computing device in accordance with one embodiment; and

[0022] **Figure 4** illustrates an interposer that includes one or more embodiments as described herein.

DETAILED DESCRIPTION

[0023] Described herein are systems, methods, and apparatuses for implementing critical dimension (CD) and phase calibration of alternating phase shift masks (APSM) and chromeless phase lithography (CPL) masks for modeling. For instance, in accordance with one embodiment, there are means described for identifying critical dimensions of structures of a mask via means for illuminating the mask via a light source; collecting multiple measurements of the critical dimensions of the structures of the mask by iteratively: (i) capturing a diffraction pattern from diffraction of the illumination traversing through the mask for each of multiple structures of the mask at different focus offsets, and (ii) measuring a difference in width between neighboring spaces in printed on wafer for each of the multiple structures of the mask at the different focus offsets; curve fitting the collected multiple measurements against rigorous optical lithography simulations based on target physical critical dimensions for each of the multiple structures to determine a critical dimension delta between the target physical measurements and the collected multiple measurements; and analyzing the critical dimension delta to extract optically effective lateral dimensions and effective trench depths for each of the multiple structures of the mask.

[0024] The methodologies described herein provide improvements to OPC model

accuracy which may then be applied to a variety of lithography processes.

[0025] Optical Proximity Correction (OPC) models require accurate mask layout dimensions as input parameters. The greater the accuracy, the more useful and accurate the resulting model will be for the semiconductor manufacturing processes. Described herein are techniques which utilize an optical interference method to bridge the gap between measurements obtained via standard metrology techniques and the required input parameters for optical modeling. According to described embodiments, the measured critical dimensions are compared to what an optical model "sees" by curve-fitting so as to obtain a critical dimension delta between the physical measurement and the optical model. The critical dimension delta can then be applied to the mask layout to provide a more accurate input for OPC modeling, and as a result, the model accuracy is greatly improved.

[0026] Alternating Phase Shift Masks (APSM) and Chromeless Phase Lithography (CPL) masks print one-dimensional mask patterns at half-pitch on wafers when perfect image balance is achieved. This happens when the zeroth-order of diffraction is completely cancelled out. The specific line width/pitch ratios and mask phase depth conditions for which perfect image balance is achieved can be calculated through rigorous simulation. The results of the rigorous simulations can then be compared with critical dimensions and phase depths measured by standard metrology, such as CDSEM and Atomic Force Microscopy (AFM) to obtain an offset based on the critical dimension delta between the physical measurement and the optical measurements.

[0027] The offset between measured and optical measurements can then be compensated for within the OPC model.

[0028] Present models measure mask critical dimensions for use as OPC model input parameters for model calibration via by CDSEM from the top, middle, or bottom of trenches. However, the delta between the measured critical dimensions and the model input parameters requires compensation which is conventionally accommodated by applying a global sizing onto the mask layout. Through trial and error, improved global sizing adjustments to the mask layout may be obtained, however, the method is both time consuming and imprecise due to the simple fact that the adjustment is a global correction and fails to recognize the variability of deltas between the critical dimensions and the model beyond those which may be adjusted for through a single global sizing correction.

[0029] Measurements based on optical interference provide more accurate critical dimension and phase depth measurements for OPC modeling and therefore have the capability to better associate actual fabrication measurements with the modeling parameters. Through the more accurate modeling input parameters, accuracy is greatly improved, especially when the

sidewall of the mask is not perfectly vertical and exhibits a complicated profile.

[0030] In order to improve the OPC model's predictive capabilities it is necessary to provide it with more accurate mask dimensions. Because the mask is a three dimensional structure it simply is not feasible to measure the features of the mask directly as such features do not represent simple straight one dimensional lines. Rather, the features are a complex shape with a profile, a width, and a slope. Conventional methodologies taking physical measurements not only require destruction of the mask, but introduce inaccuracy into the OPC model when the measurements are used as input parameters because the measurement of the critical dimension will vary with location from which the measurement is taken. For instance, for a feature having a slope, the width will vary with depth, and thus, some uncertainty remains regardless of the point from which the measurement is taken.

[0031] In the following description, numerous specific details are set forth such as examples of specific systems, languages, components, etc., in order to provide a thorough understanding of the various embodiments. It will be apparent, however, to one skilled in the art that these specific details need not be employed to practice the embodiments disclosed herein. In other instances, well known materials or methods have not been described in detail in order to avoid unnecessarily obscuring the disclosed embodiments.

[0032] In addition to various hardware components depicted in the figures and described herein, embodiments further include various operations which are described below. The operations described in accordance with such embodiments may be performed by hardware components or may be embodied in machine-executable instructions, which may be used to cause a general-purpose or special-purpose processor programmed with the instructions to perform the operations. Alternatively, the operations may be performed by a combination of hardware and software.

[0033] Any of the disclosed embodiments may be used alone or together with one another in any combination. Although various embodiments may have been partially motivated by deficiencies with conventional techniques and approaches, some of which are described or alluded to within the specification, the embodiments need not necessarily address or solve any of these deficiencies, but rather, may address only some of the deficiencies, address none of the deficiencies, or be directed toward different deficiencies and problems which are not directly discussed.

[0034] **Figure 1A** depicts an SEM image 110 grating with a 160 nanometer pitch printed on a wafer using a narrow-line illumination 125 source in accordance with which embodiments may operate. Within SEM image 110, phase pi 115 and phase 0 120 are observed.

[0035] In order to qualify Chromeless Phase Lithography (CPL) reticles and ensure the

functionality as designed, mask critical dimension and phase depth are used as criteria of reticle qualification. Critical Dimension Scanning Electron Microscopy (CDSEM) and Atomic Force Microscopy (AFM) provide physical measurements of these two metrics while optical interference methods provide measurements of "effective" critical dimension and phase depth as optical model input parameters.

[0036] Depicted SEM image 110 is a one-dimensional grating with various widths and pitches drawn on a CPL reticle. Using point source illumination 125, image balance (here phase 0 (element 120) and phase pi (element 115) has the same resist critical dimension) occurs at a specific drawn width/pitch ratio when the zeroth-order diffraction is completely cancelled out.

[0037] The printed resist pitch is half of the mask pitch (1x), and image balance holds through different focus offsets. Compared with Rigorous Lithography Simulation (RLS), the "effective" width and pitch for image balance is obtained and used as input of OPC model calibration.

[0038] This technique is especially useful when an etched sidewall of mask glass is not vertical or perpendicular which makes it exceedingly difficult to determine which part of a cross-sectional width should used as model input as there is variability in the measurement with depth of the non-vertically cut mask.

[0039] In accordance with one embodiment, detection occurs at a point where the sinusoidal curve touches zero and with zero crossing observed. Because the curve is very steep the measurement is extremely precise. In accordance with the described embodiments, a change in the measured critical dimension will result in a change in the location of the crossing, at a point other than zero, or a change in the width, such as a larger width between the waves.

[0040] In accordance with a particular embodiment, determining where the sinusoidal curve touches zero, with zero crossing is detected, constitutes part of the process for measuring the critical dimensions of a mask. In accordance with an alternative embodiment, determining where the sinusoidal curve touches zero, with zero crossing is detected, constitutes a monitoring process for manufactured silicon wafers or for in-process masks in which the measurement is compared to an expected result to verify the manufactured product is within specified tolerances. Because the measurements are possible without destroying the mask, the monitoring may be conducted on product yields from the manufacturing process without damaging them.

[0041] According to certain embodiments the image resulting from illumination of the mask is transferred from the image side and imprinted onto photo resist coated wafers at which point the dimensions of the photo resist trenches may be measured. In alternative embodiments, the image is transferred onto a charge-coupled device (CCD), Complementary metal–oxide–semiconductor (CMOS), or other electronic image capture device from which the trenches may

be measured via software or other computerized processing. In another embodiment, the image is transferred through a magnifier onto a photo resist or onto an array of photo detectors, from which the trenches may be measured from the magnified transferred image with greater accuracy.

[0042] In accordance with described embodiments, mask critical dimension and phase depth measurement using SEM image 110 include at least the following operations according to the depicted method flow 101:

[0043] **Figure 1B** depicts a flow diagram 101 in accordance with described embodiments.

[0044] As is depicted at block 150 of **Figure 1B**, a one-dimensional (1D) grating is printed on wafers with various widths and pitches using a narrow-line illumination 125 source mimicking a point source in one direction. According to such embodiments, the grating direction is parallel to the illumination 125 as is depicted at **Figure 1A**.

[0045] According to certain embodiments, an optical print is used to observe optical or phasing interference. By measuring constructive and destructive interference patterns at a far field at the end of the optics, the corresponding dimensions within the phase of the mask can be measured with a very high degree of precision.

[0046] Illumination is provided at the mask side in such a way that three diffraction orders are generated. Each of the three diffraction orders interferes with one another and as the focus of the optics is changed, the interference pattern develops very unique and abrupt signatures. The target dimension of the pattern on the mask and illumination and imaging system is adjusted so that the center beam or zero order is very weak.

[0047] At block 155 of **Figure 1B**, three-beam interference is used to calculate the intensity slice at image plane. In accordance with particular embodiments, the three-beam interference is calculated according to the equation 102 as set forth by **Figure 1C**. Note at the equation 102 the first order and the negative diffraction order is equal to each other.

[0048] In accordance with certain embodiments, the arrangement is made in such a way that the three beams are generated but the center order is very weak and consequently, nearly all of the resulting signal is generated by the first order and the negative order which generates a sinusoidal pattern on the imager side. Due to the non-zeroth-order beams, the sinusoidal wave form is slightly shifted up causing an imbalance between neighboring patterns.

[0049] Stated differently, given a sinusoidal wave, the resulting sinusoidal pattern will be symmetric across zero, such that, for all the distance the wave travels up, it travels an equal distance down, from its zero symmetry. Conversely, the orders have a slight DC shift such that the wave travels slightly higher from zero and travels a slightly lesser amount down from zero.

This shift, or offset, can be very precisely measured by measuring the neighboring spaces.

[0050] Consequently, the different diffraction measurements may thus be captured by measuring the neighboring space's dimension on the imager side, without regard to the absolute dimension of the space itself. The DC shift amount will change in both magnitude and design as the beam goes from a focused state through defocusing to a defocused state.

[0051] At block 160 of **Figure 1B**, the critical dimension delta between phase pi (element 115 of Figure 1A) and phase 0 (element 120 of Figure 1A) are measured through different focus offsets. For instance, **Figure 1D** depicts a plot 103 generated via a Rigorous Lithography Simulation (RLS) calculation showing the relation between focus offset on the horizontal axis 131 and the absolute delta critical dimension between phase pi and phase 0 on the vertical axis 132.

[0052] As depicted at **Figure 1D**, there is a signal interference and the center beam zeroth order shifts up. According to a particular embodiment, the zeroth order generates a perfectly symmetrical sinusoidal wave and then added to the zeroth order is a DC shift, either up or down. According to a particular embodiment, the intensity of the of the wave is measured. As depicted, one wave peak is larger than the other because the square of the up-shift of the sine curve is rendered resulting in the neighboring peak being a different height. This difference in height is referred to as an imbalance. The imbalance or the difference in the height of the neighboring peaks changes in proportion to the focus. According to described embodiments, the difference in height or the imbalance between the peaks is measured as it is known that as a function of focus the amount of imbalance changes.

[0053] According to a particular embodiment, the absolute critical dimension is determined by identifying where the imbalance between the peaks is at its minimum. Stated differently, when the width is at its narrowest after progressing through a series of different focus offsets 131, the critical dimension of the mask feature being measured is deduced based on the focus offset 131 which results in the least amount of imbalance in the waves.

[0054] According to a particular embodiment, multiple focus offsets are observed and their imbalance is iteratively measured and the focus offset which yields the least amount of imbalance is identified. According to such an embodiment, the focus offset which yields the least amount of imbalance is then utilized to deduce the effective critical dimension for a mask feature being measured.

[0055] Such a method returns a more accurate measurement of the effective critical dimension compared to the conventional techniques. For instance, conventional techniques may return a result of 100nm for the measured critical dimension, however, the technique described above may return a result of 103nm. While such a delta (e.g., of ~3.0 to 3.5 nm) is seemingly

miniscule, it nevertheless has a large affect on the predictability of the model due to the very small sizes and dimensions being dealt with. As such, any improvement in the measurement of the critical dimension, regardless of how small, provides for improved prediction capabilities of the model when translated on to the physical mask.

[0056] The plot 104 at **Figure 1E** depicts actual measurement data points with curve fitting using the indicated focus offset on the horizontal axis 131.

[0057] If image balanced is achieved by completely cancelling out the zeroth-order diffraction, indicated by t=0 in Equation 102 at **Figure 1C**, then a flat line should be observed. As depicted, however, there is small amount zeroth-order diffraction remaining and thus, the line is not completely flat. Critical dimension delta sensitivity to the focus is minimized when zeroth-order diffraction is minimized.

[0058] By measuring each of several consecutive images at different states from focused through the defocusing of the beams, changes to the consecutive images permits the extraction of the zeroth order strength from which it can then be deduced the dimensions as well as the space of the mask's trenches and the mask's geometries through simulations.

[0059] In such a way, the "effective" critical dimension defining the width of the features on the mask is measured indirectly. The actual features of the mask are extremely complex and the true critical dimension depend upon perspective and reference point. The critical dimensions may yield different results depending upon how deep into a three dimensional profile of the mask the measurements are observed.

[0060] Embodiments described herein therefore determine what patterns are needed on the mask to create a certain pattern on the wafer and the wafer is then measured to determine the effective mask critical dimensions. Because of optical interference, there is only one effective mask critical dimension that will yield the particular wave pattern sought.

[0061] At block 165 of **Figure 1B**, the maximum resist critical dimension delta between phase pi (element 115 of Figure 1A) and phase 0 (element 120 of Figure 1A) is extracted and plotted versus grating width. Refer to the plot 106 at **Figure 1F** which depicts the maximum critical dimension delta through focus on the vertical axis 107 plotted against the drawn width in nanometers on the horizontal axis 108. Note that the solid lines are calculated whereas the squares represent actual measurement points taken.

[0062] Within the mask there are multiple three-dimensional features and structures which may be measured and evaluated to determine their critical dimensions. One important measurement is the trench depth for any given feature. The trench depth generates a phase shift between neighboring features and measuring the effective phase depth is useful as it is the effective depth which generates the destructive interference. At 180-degrees the effective phase

shift will generate perfect cancellation of the orders through destructive interference which is important for imaging performance.

[0063] Although the features have an actual trench depth corresponding to their physical depth within the three-dimensional mask, it is the effective trench depth which matters for the purposes of generating the destructive interference to cancel the orders.

[0064] As depicted at **Figure 1F**, the center line corresponding to a depth of 195 nanometers is taken using conventional techniques which requires destruction of the mask to obtain the measurements indicated by the black squares. However, as can be seen, depth 195 nm is not the best fit and the effective phase depth is likely to be different and can be measured more accurately using the techniques described herein. Conventional methods sometimes correct for the non-180 degree result by calculating the geometric phase depth in order to achieve a 180 degree result, however, the effective phase depth may be different due to scattering of the mask sidewall.

[0065] The bottom curve which goes down almost to zero corresponding to a depth of 193 nm results in an effective phase of 180 degrees meaning that the 193 nm depth is the best depth to operate with. As before, while the difference between 195 nm and 193 nm is incredibly small, the more accurate measurement will nevertheless yield better model predictability.

[0066] At block 165 of **Figure 1B**, the maximum critical dimension delta through focus is plotted against the drawn width. **Figure 1G** depicts a plot 111 of a focus offset which has zero resist critical dimension delta which has been extracted and plotted versus grating width in accordance with the described embodiments. In particular, there is depicted a focus offset that has 0 delta on the vertical axis 112 plotted against the drawn width in nanometers on the horizontal axis 113. As before, the solid lines are calculated whereas the squares represent actual measurement points taken.

[0067] With overlap of RLS calculation results and measurement data points with 3.5-nm grating critical dimension offset, the measurement data agrees with the phase depth of 195 degrees the best as can be seen from the plot 111 of **Figure 1G**. Such a result thus implies that a 3.5 nm critical dimension delta from drawn lateral dimension and a 195-degree phase depth should be used for the OPC model calibration. This number is close to the actual sizing used for via layer model calibration. The plots 106 and 111 additionally show that 93 nm of grating width for a 160-nm-pitch results in the most balanced image, meaning minimum zeroth-order diffraction.

[0068] Plot 111 depicts a measurement graph deduced from the measurements depicted at Figures 1D and 1E. The lines of **Figure 1G** are rendered by simulation but provide for an extra point of measurement and provides a validation of the determined phase of the trench

depth. According to described embodiments, the simulation finds, for each drawn width 113, which mask size as conventionally measured has an offset value with 0 delta on the vertical axis 112. As can be seen here, by fitting the curve it is possible to deduce what the actual physical depth of a trench would be to then validate the determined phase of the trench depth. In this case, the mask as measured by this technique results in a 195 nm measured trench depth which is very close to the 195 nm trench depth to be operated on as described above.

[0069] The described techniques have been laboratory demonstrated to provide an improved model fit for the mask critical dimensions over mask CDSEM measurements and the application of a global bias through extrapolation of the mask's critical dimension delta in the manner described above.

[0070] **Figure 2** is a flow diagram illustrating a method 200 for implementing critical dimension (CD) and phase calibration of alternating phase shift masks (APSM) and chromeless phase lithography (CPL) masks for modeling in accordance with described embodiments. Some of the blocks and/or operations listed below are optional in accordance with certain embodiments. The numbering of the blocks presented is for the sake of clarity and is not intended to prescribe an order of operations in which the various blocks must occur. Additionally, operations from method 200 may be utilized in a variety of combinations.

[0071] At block 205 the method for identifying critical dimensions of structures of a mask begins with illuminating the mask via a light source.

[0072] At block 210 the method includes collecting multiple measurements of the critical dimensions of the structures of the mask by iteratively: (i) capturing a diffraction pattern from diffraction of the illumination traversing through the mask for each of multiple structures of the mask at different focus offsets (block 215) and (ii) measuring a difference in width between neighboring spaces in the diffraction patterns for each of the multiple structures of the mask at the different focus offsets (block 220). Operations 215 and 220 repeat as necessary for each of the multiple measurements of the critical dimensions of the structures of the mask.

[0073] At block 225 the method includes curve fitting the collected multiple measurements against target physical critical dimensions for each of the multiple structures to determine a critical dimension delta between the target physical measurements and the collected multiple measurements.

[0074] At block 230 the method includes analyzing the critical dimension delta to extract constructive lateral dimensions and effective trench depths for each of the multiple structures of the mask.

[0075] In accordance with another embodiment of method 200, illuminating the mask includes illuminating the mask via a single point source of illumination.

[0076] In accordance with another embodiment of method 200, illuminating the mask via a single point source of illumination includes illuminating the mask via the single point source and causing the single point source of illumination to diffract at the mask into three diffraction orders, a first order, a zeroth-order, and a negative order.

[0077] In accordance with another embodiment of method 200, illuminating the mask includes illuminating the mask via a double point source of illumination.

[0078] In accordance with another embodiment of method 200, illuminating the mask includes illuminating the mask via a four or fewer points of illumination.

[0079] In accordance with certain embodiments, multiple point sources of illumination are utilized, however, the described methodology works best with a small number of points of illumination being shone upon the mask, such as one, two, or four points of illumination. While greater numbers of points of illumination are theoretically feasible, the complexity increases dramatically with greater numbers of illumination points and the improvement in accuracy diminishes and therefore fails to justify the increased complexity.

[0080] In accordance with another embodiment of method 200, the illumination is determined based on the mask property and the structure of the mask to be measured.

[0081] In accordance with another embodiment of method 200, the mask is one of a binary mask, an Attenuated Phase-Shift Mask (APSM mask), or a Chromeless Phase Lithography (CPL) mask.

[0082] The methodology is applicable to all presently available mask types and is expected to also be applicable to future mask types not yet available to the market place.

[0083] In accordance with another embodiment of method 200, the structure of the mask includes a one-dimensional or two-dimensional grating pattern.

[0084] The diffraction grating by the structures of the mask create an optical component with a periodic structure, which splits and diffracts light into several beams travelling in different directions. The directions of these beams depend on the spacing of the grating and the wavelength of the light so that the grating acts as the dispersive element.

[0085] In accordance with another embodiment of method 200, the mask includes multiple structures, each structure having dimensions of a non-linear profile, a width, a slope, and a depth. According to such an embodiment, measuring the difference in width between neighboring spaces in the diffraction pattern includes performing the measuring on different ones of the structures of different dimensions through different focus offsets.

[0086] In accordance with another embodiment of method 200, illumination includes a wavelength in a visible range. Illuminating the mask may be performed within the visible light range, however, any wavelength of illumination may be utilized in accordance with the described

embodiments.

[0087] In accordance with another embodiment of method 200, capturing the diffraction pattern from diffraction of the illumination traversing through the mask includes transferring an image of the illuminated mask onto a photo resist.

[0088] In accordance with another embodiment of method 200, measuring the difference in width between neighboring spaces in the diffraction pattern includes measuring the difference in width between neighboring spaces from the image of the mask transferred onto the photo resist via Critical Dimension Scanning Electron Microscopy (CDSEM).

[0089] In accordance with another embodiment of method 200, capturing the diffraction pattern from diffraction of the illumination traversing through the mask includes transferring an image of the illuminated mask onto a photo resist coated silicon wafer According to such an embodiment, the method further includes capturing a Scanning Electron Microscope (SEM) image of the photo resist coated silicon wafer after exposure to the image of the illuminated mask and further in which measuring the difference in width between neighboring spaces in the diffraction pattern includes measuring the difference in width between neighboring spaces from the captured SEM image of the photo resist coated silicon wafer.

[0090] A photoresist is a light-sensitive material common to various industrial processes including photolithography and photoengraving to form a patterned coating on a surface. In the production of semiconductor circuits, a photoresist loses its resistance or its susceptibility to attack by an etchant or solvent when exposed to light.

[0091] In accordance with another embodiment of method 200, capturing the diffraction pattern from diffraction of the illumination traversing through the mask includes electronically capturing an image as transferred through the mask via charge-coupled device (CCD); and in which the method further includes storing the captured image.

[0092] In accordance with another embodiment of method 200, measuring the difference in width between neighboring spaces in the diffraction pattern includes measuring the difference in width between neighboring spaces from the captured and stored image via software image processing.

[0093] In accordance with another embodiment, method 200 further includes performing simulations to identify zero crossing and to extrapolate constructive lateral dimensions for each of the multiple structures and a mask phase depth for each of the multiple structures.

[0094] In accordance with another embodiment, method 200 further includes determining effective trench depth for each of the multiple structures and a mask phase depth for each of the multiple structures.

[0095] In accordance with a particular embodiment there is a non-transitory computer

readable storage medium having instructions stored thereupon that, when executed by a processor, the instructions cause the processor to perform operations for identifying critical dimensions of structures of a mask, in which operations include: illuminating the mask via a light source; collecting multiple measurements of the critical dimensions of the structures of the mask by iteratively: (i) capturing a diffraction pattern from diffraction of the illumination traversing through the mask for each of multiple structures of the mask at different focus offsets, and (ii) measuring a difference in width between neighboring spaces in the diffraction patterns for each of the multiple structures of the mask at the different focus offsets; curve fitting the collected multiple measurements against target physical critical dimensions for each of the multiple structures to determine a critical dimension delta between the target physical measurements and the collected multiple measurements; and analyzing the critical dimension delta to extract constructive lateral dimensions and effective trench depths for each of the multiple structures of the mask.

[0096] According to another embodiment of the non-transitory computer readable media, capturing the diffraction pattern from diffraction of the illumination traversing through the mask includes transferring an image of the illuminated mask onto a photo resist; and in which measuring the difference in width between neighboring spaces in the diffraction pattern includes measuring the difference in width between neighboring spaces from the image of the mask transferred onto the photo resist via Critical Dimension Scanning Electron Microscopy (CDSEM).

[0097] According to another embodiment of the non-transitory computer readable media, capturing the diffraction pattern from diffraction of the illumination traversing through the mask includes transferring an image of the illuminated mask onto a photo resist coated silicon wafer; in which the method further includes capturing a Scanning Electron Microscope (SEM) image of the photo resist coated silicon wafer after exposure to the image of the illuminated mask; and in which measuring the difference in width between neighboring spaces in the diffraction pattern includes measuring the difference in width between neighboring spaces from the captured SEM image of the photo resist coated silicon wafer.

[0098] Described embodiments may be formed or carried out on a substrate, such as a semiconductor substrate. In one implementation, the semiconductor substrate may be a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium antimonide, or other combinations of group III-V or group IV materials.

Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the described embodiments.

[0099] A plurality of transistors, such as metal-oxide-semiconductor field-effect transistors (MOSFET or simply MOS transistors), may be fabricated on the substrate. In various described embodiments, the MOS transistors may be planar transistors, nonplanar transistors, or a combination of both. Nonplanar transistors include FinFET transistors such as double-gate transistors and tri-gate transistors, and wrap-around or all-around gate transistors such as nanoribbon and nanowire transistors. Although the implementations described herein may illustrate only planar transistors, it should be noted that the described embodiments may also be carried out using nonplanar transistors.

[00100] Each MOS transistor includes a gate stack formed of at least two layers, a gate dielectric layer and a gate electrode layer. The gate dielectric layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide (SiO_2) and/or a high-k dielectric material. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate dielectric layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric layer to improve its quality when a high-k material is used.

[00101] The gate electrode layer is formed on the gate dielectric layer and may consist of at least one P-type workfunction metal or N-type workfunction metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer may consist of a stack of two or more metal layers, where one or more metal layers are workfunction metal layers and at least one metal layer is a fill metal layer.

[00102] For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a workfunction that is between about 4.9 eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals such as hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum

carbide. An N-type metal layer will enable the formation of an NMOS gate electrode with a workfunction that is between about 3.9 eV and about 4.2 eV.

[00103] In some implementations, the gate electrode may consist of a "U"-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In another implementation, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In further described embodiments, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

[00104] In some embodiments, a pair of sidewall spacers may be formed on opposing sides of the gate stack that bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process operations. In an alternate implementation, a plurality of spacer pairs may be used, for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

[00105] As is well known in the art, source and drain regions are formed within the substrate adjacent to the gate stack of each MOS transistor. The source and drain regions are generally formed using either an implantation/diffusion process or an etching/deposition process. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate to form the source and drain regions. An annealing process that activates the dopants and causes them to diffuse further into the substrate typically follows the ion implantation process. In the latter process, the substrate may first be etched to form recesses at the locations of the source and drain regions. An epitaxial deposition process may then be carried out to fill the recesses with material that is used to fabricate the source and drain regions. In some implementations, the source and drain regions may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some implementations the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In further embodiments, the source and drain regions may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. And in further embodiments, one or more layers of metal and/or metal alloys may be used to form the source and drain regions.

[00106] One or more interlayer dielectrics (ILD) are deposited over the MOS transistors.

The ILD layers may be formed using dielectric materials known for their applicability in integrated circuit structures, such as low-k dielectric materials. Examples of dielectric materials that may be used include, but are not limited to, silicon dioxide (SiO_2), carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. The ILD layers may include pores or air gaps to further reduce their dielectric constant.

[00107] **Figure 3** illustrates a computing device 300 in accordance with described embodiments. The computing device 300 houses a board 302. The board 302 may include a number of components, including but not limited to a processor 304 and at least one communication chip 306. The processor 304 is physically and electrically coupled to the board 302. In some implementations the at least one communication chip 306 is also physically and electrically coupled to the board 302. In further implementations, the communication chip 306 is part of the processor 304.

[00108] Depending on its applications, computing device 300 may include other components that may or may not be physically and electrically coupled to the board 302. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

[00109] The communication chip 306 enables wireless communications for the transfer of data to and from the computing device 300. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 306 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 300 may include a plurality of communication chips 306. For instance, a first communication chip 306 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 306 may be

dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[00110] The processor 304 of the computing device 300 includes an integrated circuit die packaged within the processor 304. In some described embodiments, the integrated circuit die of the processor includes one or more devices, such as MOS-FET transistors built in accordance with described embodiments. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[00111] The communication chip 306 also includes an integrated circuit die packaged within the communication chip 306. In accordance with other described embodiments, the integrated circuit die of the communication chip includes one or more devices, such as MOS-FET transistors built in accordance with described embodiments.

[00112] In further implementations, another component housed within the computing device 300 may contain an integrated circuit die that includes one or more devices, such as MOS-FET transistors built in accordance with described embodiments.

[00113] In various implementations, the computing device 300 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 300 may be any other electronic device that processes data.

[00114] **Figure 4** illustrates an interposer 400 that includes one or more described embodiments. The interposer 400 is an intervening substrate used to bridge a first substrate 402 to a second substrate 404. The first substrate 402 may be, for instance, an integrated circuit die. The second substrate 404 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer 400 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 400 may couple an integrated circuit die to a ball grid array (BGA) 406 that can subsequently be coupled to the second substrate 404. In some embodiments, the first and second substrates 402/404 are attached to opposing sides of the interposer 400. In other embodiments, the first and second substrates 402/404 are attached to the same side of the interposer 400. And in further embodiments, three or more substrates are interconnected by way of the interposer 400.

[00115] The interposer 400 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further

implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

[00116] The interposer may include metal interconnects 408 and vias 410, including but not limited to through-silicon vias (TSVs) 412. The interposer 400 may further include embedded devices 414, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 400. In accordance with described embodiments, apparatuses or processes disclosed herein may be used in the fabrication of interposer 400.

[00117] While the subject matter disclosed herein has been described by way of example and in terms of the specific embodiments, it is to be understood that the claimed embodiments are not limited to the explicitly enumerated embodiments disclosed. To the contrary, the disclosure is intended to cover various modifications and similar arrangements as would be apparent to those skilled in the art. Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements. It is to be understood that the above description is intended to be illustrative, and not restrictive. Many other embodiments will be apparent to those of skill in the art upon reading and understanding the above description. The scope of the disclosed subject matter is therefore to be determined in reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

[00118] It is therefore in accordance with the described embodiments that:

[00119] According to an embodiment there is a method for identifying critical dimensions of structures of a mask, wherein the method comprises: illuminating the mask via a light source; collecting multiple measurements of the critical dimensions of the structures of the mask by iteratively: (i) capturing a diffraction pattern from diffraction of the illumination traversing through the mask for each of multiple structures of the mask at different focus offsets, and (ii) measuring a difference in width between neighboring spaces in the diffraction patterns for each of the multiple structures of the mask at the different focus offsets; curve fitting the collected multiple measurements against target physical critical dimensions for each of the multiple structures to determine a critical dimension delta between the target physical measurements and the collected multiple measurements; and analyzing the critical dimension delta to extract constructive lateral dimensions and effective trench depths for each of the

multiple structures of the mask.

[00120] According to an embodiment, illuminating the mask comprises illuminating the mask via a single point source of illumination.

[00121] According to an embodiment, illuminating the mask via a single point source of illumination comprises illuminating the mask via the single point source and causing the single point source of illumination to diffract at the mask into three diffraction orders, a first order, a zeroth-order, and a negative order.

[00122] According to an embodiment, illuminating the mask comprises illuminating the mask via a double point source of illumination.

[00123] According to an embodiment, illuminating the mask comprises illuminating the mask via a four or fewer points of illumination.

[00124] According to an embodiment, the illumination is determined based on the mask property and the structure of the mask to be measured.

[00125] According to an embodiment, the mask is one of a binary mask, an Attenuated Phase-Shift Mask (APSM mask), or a Chromeless Phase Lithography (CPL) mask.

[00126] the structure of the mask comprises a one-dimensional or two-dimensional grating pattern.

[00127] According to an embodiment, the mask comprises multiple structures, each structure having dimensions of a non-linear profile, a width, a slope, and a depth; and wherein measuring the difference in width between neighboring spaces in the diffraction pattern comprises performing the measuring on different ones of the structures of different dimensions through different focus offsets.

[00128] According to an embodiment, illumination comprises a wavelength in a visible range.

[00129] According to an embodiment, capturing the diffraction pattern from diffraction of the illumination traversing through the mask comprises transferring an image of the illuminated mask onto a photo resist.

[00130] According to an embodiment, measuring the difference in width between neighboring spaces in the diffraction pattern comprises measuring the difference in width between neighboring spaces from the image of the mask transferred onto the photo resist via Critical Dimension Scanning Electron Microscopy (CDSEM).

[00131] According to an embodiment, capturing the diffraction pattern from diffraction of the illumination traversing through the mask comprises transferring an image of the illuminated mask onto a photo resist coated silicon wafer; wherein the method further comprises capturing a Scanning Electron Microscope (SEM) image of the photo resist coated silicon wafer

after exposure to the image of the illuminated mask; and wherein measuring the difference in width between neighboring spaces in the diffraction pattern comprises measuring the difference in width between neighboring spaces from the captured SEM image of the photo resist coated silicon wafer.

[00132] According to an embodiment, capturing the diffraction pattern from diffraction of the illumination traversing through the mask comprises electronically capturing an image as transferred through the mask via charge-coupled device (CCD); and wherein the method further comprises storing the captured image.

[00133] According to an embodiment, measuring the difference in width between neighboring spaces in the diffraction pattern comprises measuring the difference in width between neighboring spaces from the captured and stored image via software image processing.

[00134] According to an embodiment, the method further comprises: performing simulations to identify zero crossing and to extrapolate constructive lateral dimensions for each of the multiple structures and a mask phase depth for each of the multiple structures.

[00135] According to an embodiment, the method further comprises: determining effective trench depth for each of the multiple structures and a mask phase depth for each of the multiple structures.

[00136] According to an embodiment there is a system for identifying critical dimensions of structures of a mask, wherein the system comprises: a light source to illuminate the mask; an image capture device to collect multiple measurements of the critical dimensions of the structures of the mask by iteratively capturing a diffraction pattern from diffraction of the illumination traversing through the mask for each of multiple structures of the mask at different focus offsets, and an analysis unit to measure a difference in width between neighboring spaces in the diffraction patterns for each of the multiple structures of the mask captured by the image capture device at the different focus offsets; the analysis unit to curve fit the collected multiple measurements against target physical critical dimensions for each of the multiple structures to determine a critical dimension delta between the target physical measurements and the collected multiple measurements; and the analysis unit to determine constructive lateral dimensions and effective trench depths for each of the multiple structures of the mask based on the critical dimension deltas.

[00137] According to an embodiment, the light source comprises one of: a single point source of illumination; a double point source of illumination; or a four or fewer point source of illumination.

[00138] According to an embodiment, the light source is determined based on the mask property and the structure of the mask to be measured; and wherein the mask is one of a binary

mask, an Attenuated Phase-Shift Mask (APSM mask), or a Chromeless Phase Lithography (CPL) mask.

[00139] According to an embodiment, the system to iteratively capture the diffraction pattern from diffraction of the illumination traversing through the mask comprises the system to transfer an image of the illuminated mask onto a photo resist.

[00140] According to an embodiment, measuring the difference in width between neighboring spaces in the diffraction pattern comprises measuring the difference in width between neighboring spaces from the image of the mask transferred onto the photo resist via Critical Dimension Scanning Electron Microscopy (CDSEM).

[00141] According to an embodiment, the system to iteratively capture the diffraction pattern from diffraction of the illumination traversing through the mask comprises the system to transfer an image of the illuminated mask onto a photo resist coated silicon wafer; the system is to further capture a Scanning Electron Microscope (SEM) image of the photo resist coated silicon wafer after exposure to the image of the illuminated mask; and wherein measuring the difference in width between neighboring spaces in the diffraction pattern comprises the system to measure the difference in width between neighboring spaces from the captured SEM image of the photo resist coated silicon wafer.

[00142] According to an embodiment, the system to iteratively capture the diffraction pattern from diffraction of the illumination traversing through the mask comprises the system to electronically capture an image as transferred through the mask via charge-coupled device (CCD); and wherein the system further comprises storage media to store the captured image.

[00143] According to an embodiment, the system to measure the difference in width between neighboring spaces in the diffraction pattern comprises the system to measure the difference in width between neighboring spaces from the captured and stored image via software image processing.

[00144] According to an embodiment there is non-transitory computer readable storage media having instructions stored thereupon that, when executed by a processor, the instructions cause the processor to perform operations for identifying critical dimensions of structures of a mask, wherein operations comprise: illuminating the mask via a light source; collecting multiple measurements of the critical dimensions of the structures of the mask by iteratively: (i) capturing a diffraction pattern from diffraction of the illumination traversing through the mask for each of multiple structures of the mask at different focus offsets, and (ii) measuring a difference in width between neighboring spaces in the diffraction patterns for each of the multiple structures of the mask at the different focus offsets; curve fitting the collected multiple measurements against target physical critical dimensions for each of the multiple structures to determine a critical

dimension delta between the target physical measurements and the collected multiple measurements; and analyzing the critical dimension delta to extract constructive lateral dimensions and effective trench depths for each of the multiple structures of the mask.

[00145] According to an embodiment, capturing the diffraction pattern from diffraction of the illumination traversing through the mask comprises transferring an image of the illuminated mask onto a photo resist; and wherein measuring the difference in width between neighboring spaces in the diffraction pattern comprises measuring the difference in width between neighboring spaces from the image of the mask transferred onto the photo resist via Critical Dimension Scanning Electron Microscopy (CDSEM).

[00146] According to an embodiment, capturing the diffraction pattern from diffraction of the illumination traversing through the mask comprises transferring an image of the illuminated mask onto a photo resist coated silicon wafer; wherein the method further comprises capturing a Scanning Electron Microscope (SEM) image of the photo resist coated silicon wafer after exposure to the image of the illuminated mask; and wherein measuring the difference in width between neighboring spaces in the diffraction pattern comprises measuring the difference in width between neighboring spaces from the captured SEM image of the photo resist coated silicon wafer.

CLAIMS

What is claimed is:

1. A method for identifying critical dimensions of structures of a mask, wherein the method comprises:

illuminating the mask via a light source;

collecting multiple measurements of the critical dimensions of the structures of the mask by iteratively:

(i) capturing a diffraction pattern from diffraction of the illumination traversing through the mask for each of multiple structures of the mask at different focus offsets, and

(ii) measuring a difference in width between neighboring spaces in the diffraction patterns for each of the multiple structures of the mask at the different focus offsets;

curve fitting the collected multiple measurements against target physical critical dimensions for each of the multiple structures to determine a critical dimension delta between the target physical measurements and the collected multiple measurements; and

analyzing the critical dimension delta to extract constructive lateral dimensions and effective trench depths for each of the multiple structures of the mask.

2. The method of claim 1, wherein illuminating the mask comprises illuminating the mask via a single point source of illumination.

3. The method of claim 2, wherein illuminating the mask via a single point source of illumination comprises illuminating the mask via the single point source and causing the single point source of illumination to diffract at the mask into three diffraction orders, a first order, a zeroth-order, and a negative order.

4. The method of claim 1, wherein illuminating the mask comprises illuminating the mask via a double point source of illumination.

5. The method of claim 1, wherein illuminating the mask comprises illuminating the mask via a four or fewer points of illumination.

6. The method of claim 1, wherein the illumination is determined based on the mask property and the structure of the mask to be measured.

7. The method of claim 1, wherein the mask is one of a binary mask, an Attenuated Phase-Shift Mask (APSM mask), or a Chromeless Phase Lithography (CPL) mask.

8. The method of claim 1, wherein the structure of the mask comprises a one-dimensional or two-dimensional grating pattern.

9. The method of claim 1:

wherein the mask comprises multiple structures, each structure having dimensions of a non-

linear profile, a width, a slope, and a depth; and

wherein measuring the difference in width between neighboring spaces in the diffraction pattern comprises performing the measuring on different ones of the structures of different dimensions through different focus offsets.

10. The method of claim 1, wherein illumination comprises a wavelength in a visible range.

11. The method of claim 1, wherein capturing the diffraction pattern from diffraction of the illumination traversing through the mask comprises transferring an image of the illuminated mask onto a photo resist.

12. The method of claim 11, wherein measuring the difference in width between neighboring spaces in the diffraction pattern comprises measuring the difference in width between neighboring spaces from the image of the mask transferred onto the photo resist via Critical Dimension Scanning Electron Microscopy (CDSEM).

13. The method of claim 1:

wherein capturing the diffraction pattern from diffraction of the illumination traversing through the mask comprises transferring an image of the illuminated mask onto a photo resist coated silicon wafer;

wherein the method further comprises capturing a Scanning Electron Microscope (SEM) image of the photo resist coated silicon wafer after exposure to the image of the illuminated mask; and

wherein measuring the difference in width between neighboring spaces in the diffraction pattern comprises measuring the difference in width between neighboring spaces from the captured SEM image of the photo resist coated silicon wafer.

14. The method of claim 1:

wherein capturing the diffraction pattern from diffraction of the illumination traversing through the mask comprises electronically capturing an image as transferred through the mask via charge-coupled device (CCD); and

wherein the method further comprises storing the captured image.

15. The method of claim 14, wherein measuring the difference in width between neighboring spaces in the diffraction pattern comprises measuring the difference in width between neighboring spaces from the captured and stored image via software image processing.

16. The method of claim 1, further comprising:

performing simulations to identify zero crossing and to extrapolate constructive lateral dimensions for each of the multiple structures and a mask phase depth for each of the multiple structures.

17. The method of claim 1, further comprising:

determining effective trench depth for each of the multiple structures and a mask phase depth for each of the multiple structures.

18. A system for identifying critical dimensions of structures of a mask, wherein the system comprises:

a light source to illuminate the mask;

an image capture device to collect multiple measurements of the critical dimensions of the structures of the mask by iteratively capturing a diffraction pattern from diffraction of the illumination traversing through the mask for each of multiple structures of the mask at different focus offsets, and

an analysis unit to measure a difference in width between neighboring spaces in the diffraction patterns for each of the multiple structures of the mask captured by the image capture device at the different focus offsets;

the analysis unit to curve fit the collected multiple measurements against target physical critical dimensions for each of the multiple structures to determine a critical dimension delta between the target physical measurements and the collected multiple measurements; and

the analysis unit to determine constructive lateral dimensions and effective trench depths for each of the multiple structures of the mask based on the critical dimension deltas.

19. The system of claim 18, wherein the light source comprises one of:

a single point source of illumination;

a double point source of illumination; or

a four or fewer point source of illumination.

20. The system of claim 18:

wherein the light source is determined based on the mask property and the structure of the mask to be measured; and

wherein the mask is one of a binary mask, an Attenuated Phase-Shift Mask (APSM mask), or a Chromeless Phase Lithography (CPL) mask.

21. The system of claim 18, wherein the system to iteratively capture the diffraction pattern from diffraction of the illumination traversing through the mask comprises the system to transfer an image of the illuminated mask onto a photo resist.

22. The system of claim 21, wherein measuring the difference in width between neighboring spaces in the diffraction pattern comprises measuring the difference in width between neighboring spaces from the image of the mask transferred onto the photo resist via Critical Dimension Scanning Electron Microscopy (CDSEM).

23. The system of claim 18:

wherein the system to iteratively capture the diffraction pattern from diffraction of the

illumination traversing through the mask comprises the system to transfer an image of the illuminated mask onto a photo resist coated silicon wafer;

the system is to further capture a Scanning Electron Microscope (SEM) image of the photo resist coated silicon wafer after exposure to the image of the illuminated mask; and

wherein measuring the difference in width between neighboring spaces in the diffraction pattern comprises the system to measure the difference in width between neighboring spaces from the captured SEM image of the photo resist coated silicon wafer.

24. The system of claim 18:

wherein the system to iteratively capture the diffraction pattern from diffraction of the illumination traversing through the mask comprises the system to electronically capture an image as transferred through the mask via charge-coupled device (CCD); and

wherein the system further comprises storage media to store the captured image.

25. The system of claim 24, wherein the system to measure the difference in width between neighboring spaces in the diffraction pattern comprises the system to measure the difference in width between neighboring spaces from the captured and stored image via software image processing.

26. Non-transitory computer readable storage media having instructions stored thereupon that, when executed by a processor, the instructions cause the processor to perform operations for identifying critical dimensions of structures of a mask, wherein operations comprise:

illuminating the mask via a light source;

collecting multiple measurements of the critical dimensions of the structures of the mask by iteratively:

(i) capturing a diffraction pattern from diffraction of the illumination traversing through the mask for each of multiple structures of the mask at different focus offsets, and

(ii) measuring a difference in width between neighboring spaces in the diffraction patterns for each of the multiple structures of the mask at the different focus offsets;

curve fitting the collected multiple measurements against target physical critical dimensions for each of the multiple structures to determine a critical dimension delta between the target physical measurements and the collected multiple measurements; and

analyzing the critical dimension delta to extract constructive lateral dimensions and effective trench depths for each of the multiple structures of the mask.

27. The non-transitory computer readable media of claim 26, wherein capturing the diffraction pattern from diffraction of the illumination traversing through the mask comprises transferring an image of the illuminated mask onto a photo resist; and

wherein measuring the difference in width between neighboring spaces in the diffraction pattern comprises measuring the difference in width between neighboring spaces from the image of the mask transferred onto the photo resist via Critical Dimension Scanning Electron Microscopy (CDSEM).

28. The non-transitory computer readable media of claim 26:

wherein capturing the diffraction pattern from diffraction of the illumination traversing through the mask comprises transferring an image of the illuminated mask onto a photo resist coated silicon wafer;

wherein the method further comprises capturing a Scanning Electron Microscope (SEM) image of the photo resist coated silicon wafer after exposure to the image of the illuminated mask; and

wherein measuring the difference in width between neighboring spaces in the diffraction pattern comprises measuring the difference in width between neighboring spaces from the captured SEM image of the photo resist coated silicon wafer.

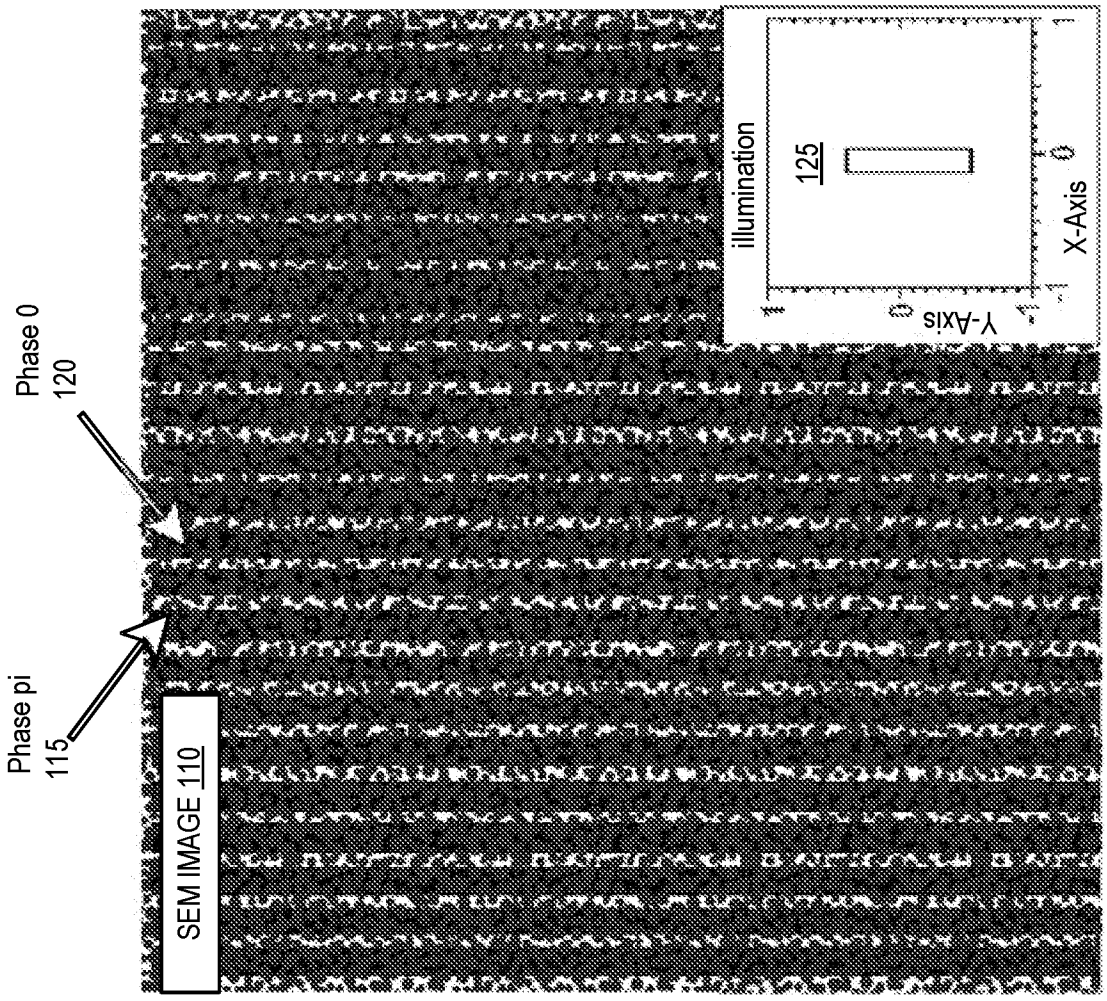

Phase 0
120
Phase pi
115
SEM IMAGE 110
illumination
125
Y-Axis
X-Axis

Fig. 1A

FIG. 1B

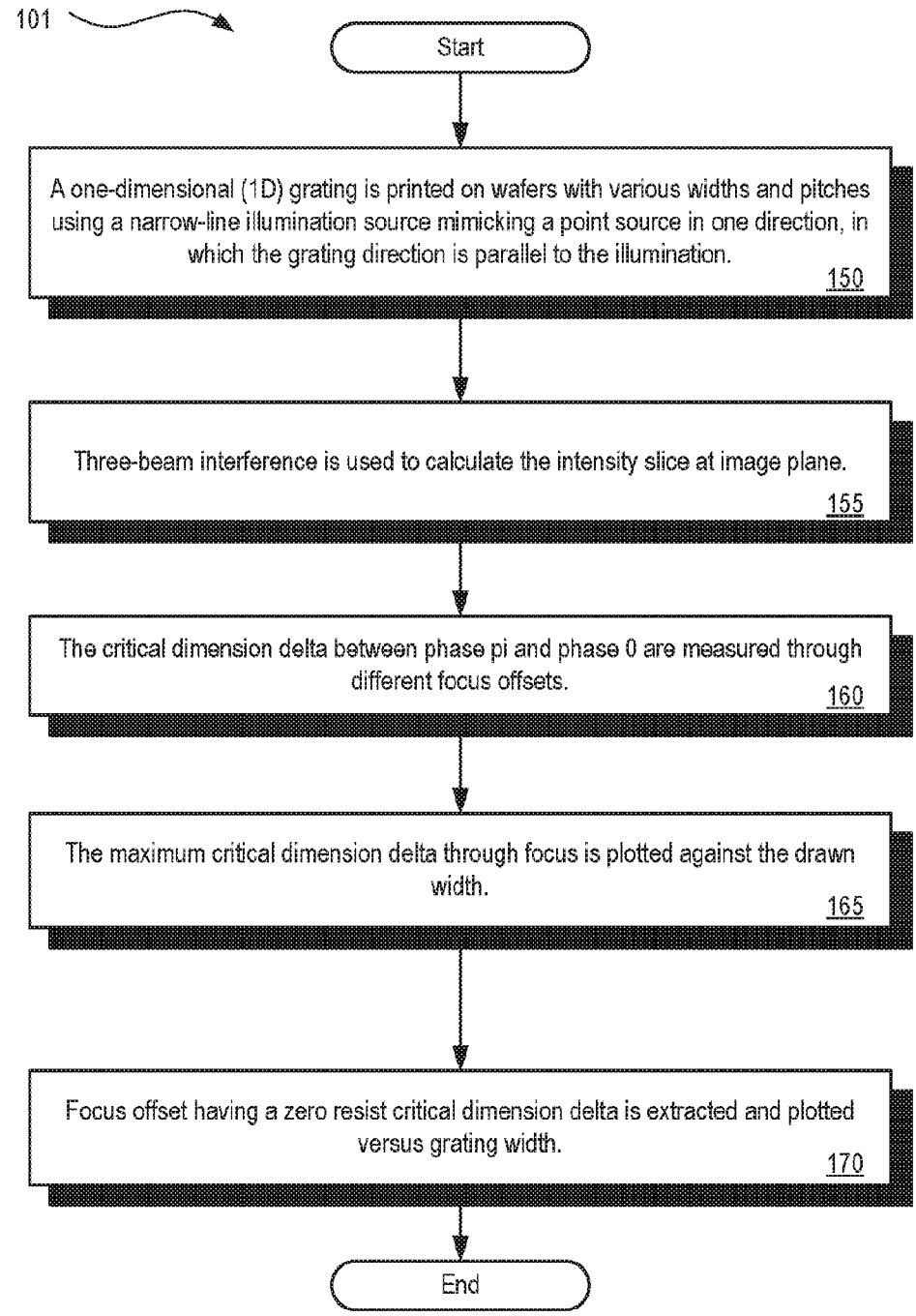

101
Start
A one-dimensional (1D) grating is printed on wafers with various widths and pitches using a narrow-line illumination source mimicking a point source in one direction, in which the grating direction is parallel to the illumination.
150
Three-beam interference is used to calculate the intensity slice at image plane.
155
The critical dimension delta between phase pi and phase 0 are measured through different focus offsets.
160
The maximum critical dimension delta through focus is plotted against the drawn width.
165
Focus offset having a zero resist critical dimension delta is extracted and plotted versus grating width.
170
End

FIG. 1C

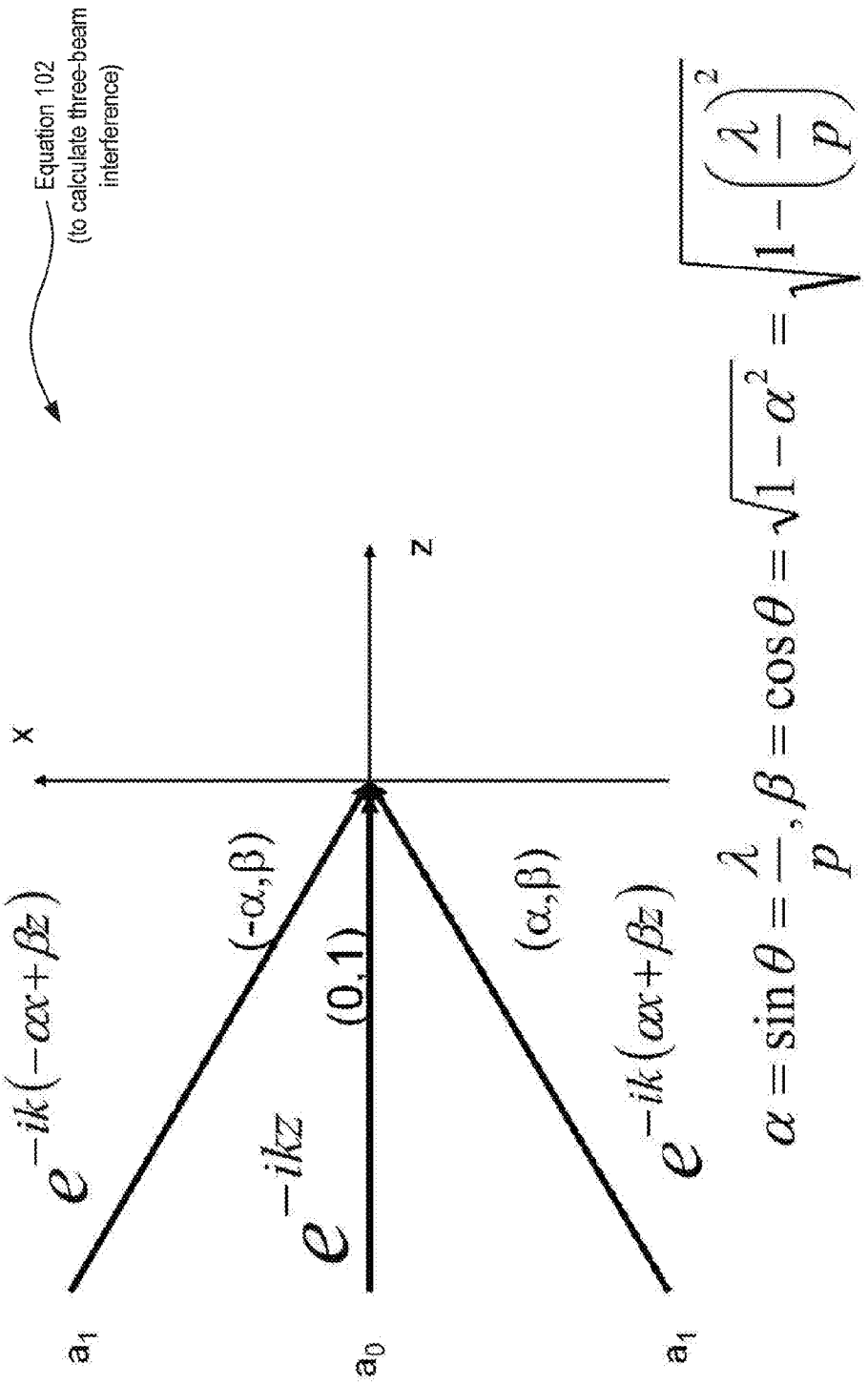
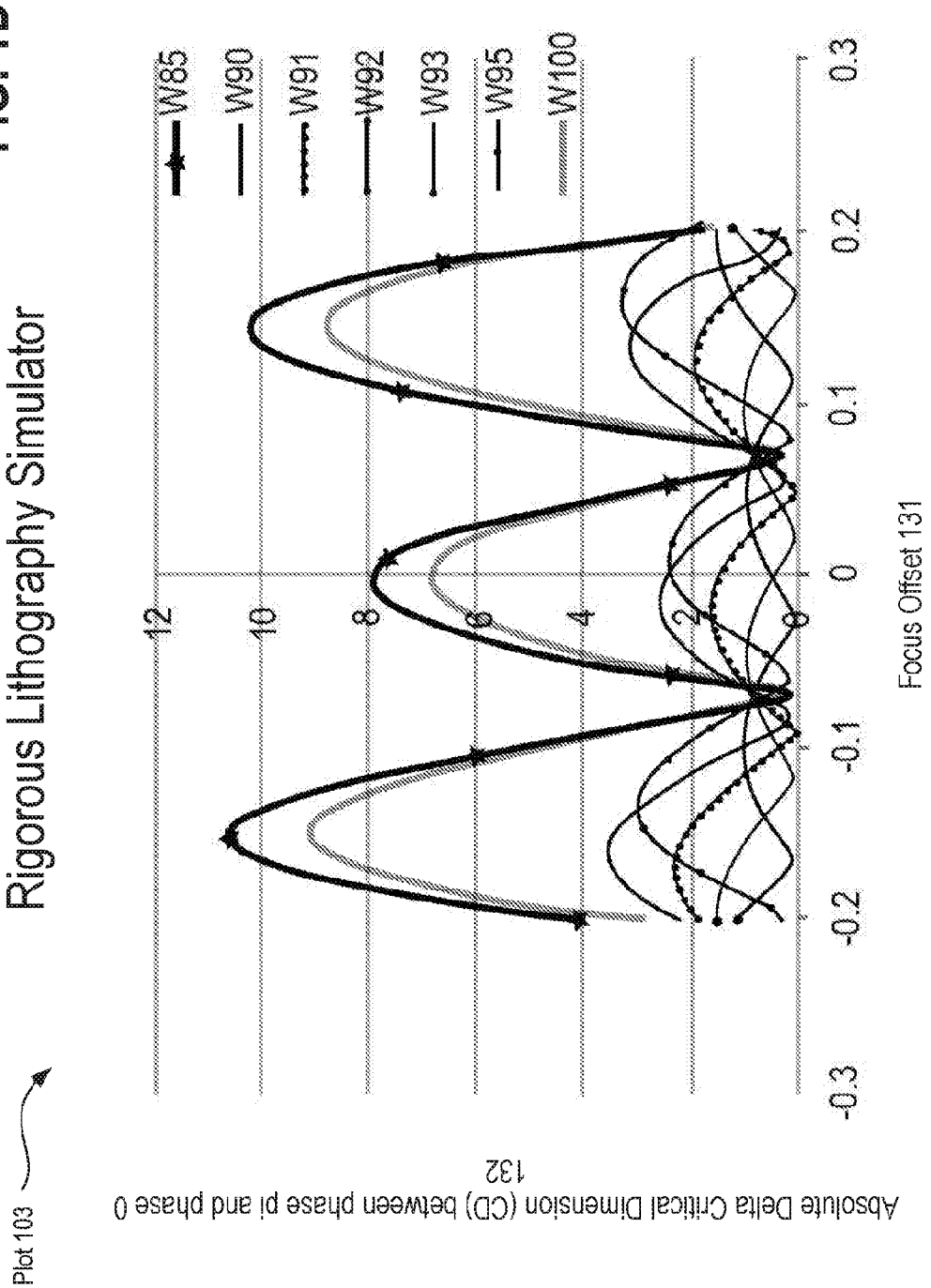

Equation 102
(to calculate three-beam interference)
x
z
$e^{-ik(-\alpha x+\beta z)}$
e^{-ikz}
$e^{-ik(\alpha x+\beta z)}$
(-α,β)
(0,1)
(α,β)
a1
a0
a1
$\alpha=\sin\theta=\frac{\lambda}{p},\beta=\cos\theta=\sqrt{1-\alpha^2}=\sqrt{1-\left(\frac{\lambda}{p}\right)^2}$

FIG. 1D


Rigorous Lithography Simulator
Plot 103
Absolute Delta Critical Dimension (CD) between phase pi and phase 0
132
W85
W90
W91
W92
W93
W95
W100
12
10
8
6
4
2
0
-0.3
-0.2
-0.1
0
0.1
0.2
0.3
Focus Offset 131

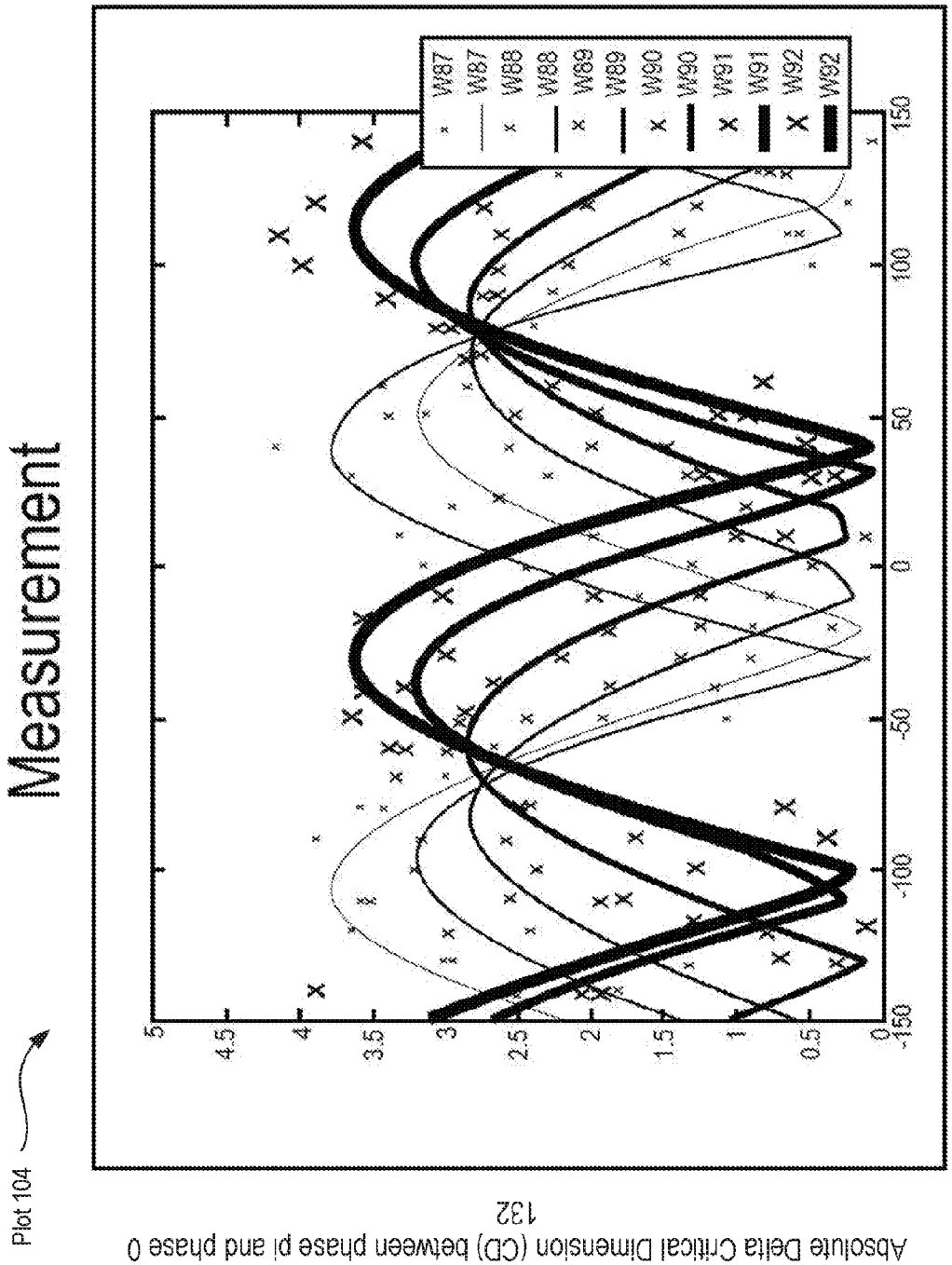

Measurement
Plot 104
Absolute Delta Critical Dimension (CD) between phase pi and phase 0
132
Focus Offset 131
W87
W87
W88
W88
W89
W89
W90
W90
W91
W91
W92
W92
5
4.5
4
3.5
3
2.5
2
1.5
1
0.5
0
-150
-100
-50
0
50
100
150

FIG. 1E

Fig. 1F

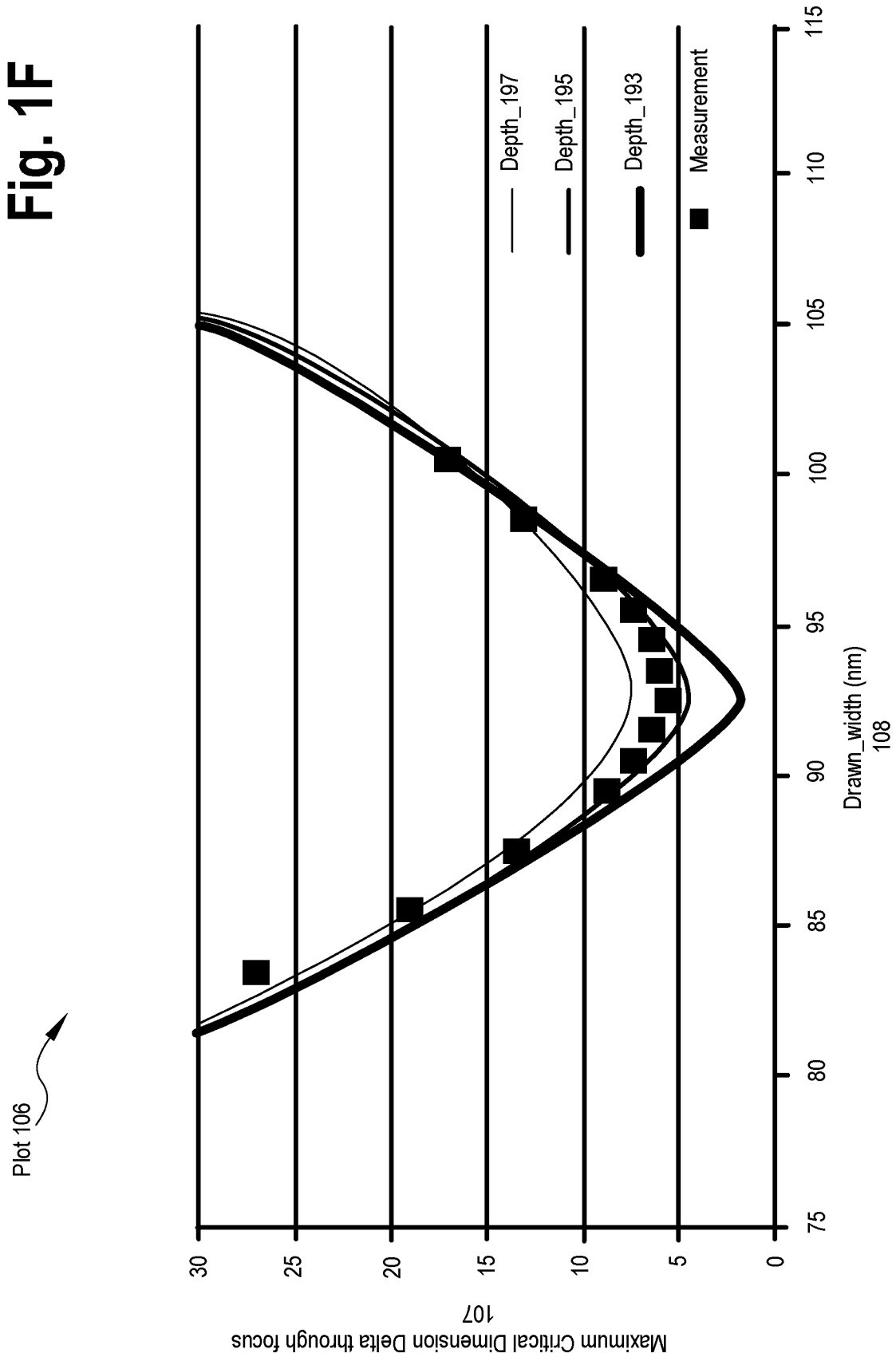

Plot 106
Maximum Critical Dimension Delta through focus
107
30
25
20
15
10
5
0
75
80
85
90
95
100
105
110
115
Drawn_width (nm)
108
Depth_197
Depth_195
Depth_193
Measurement

FIG. 1G

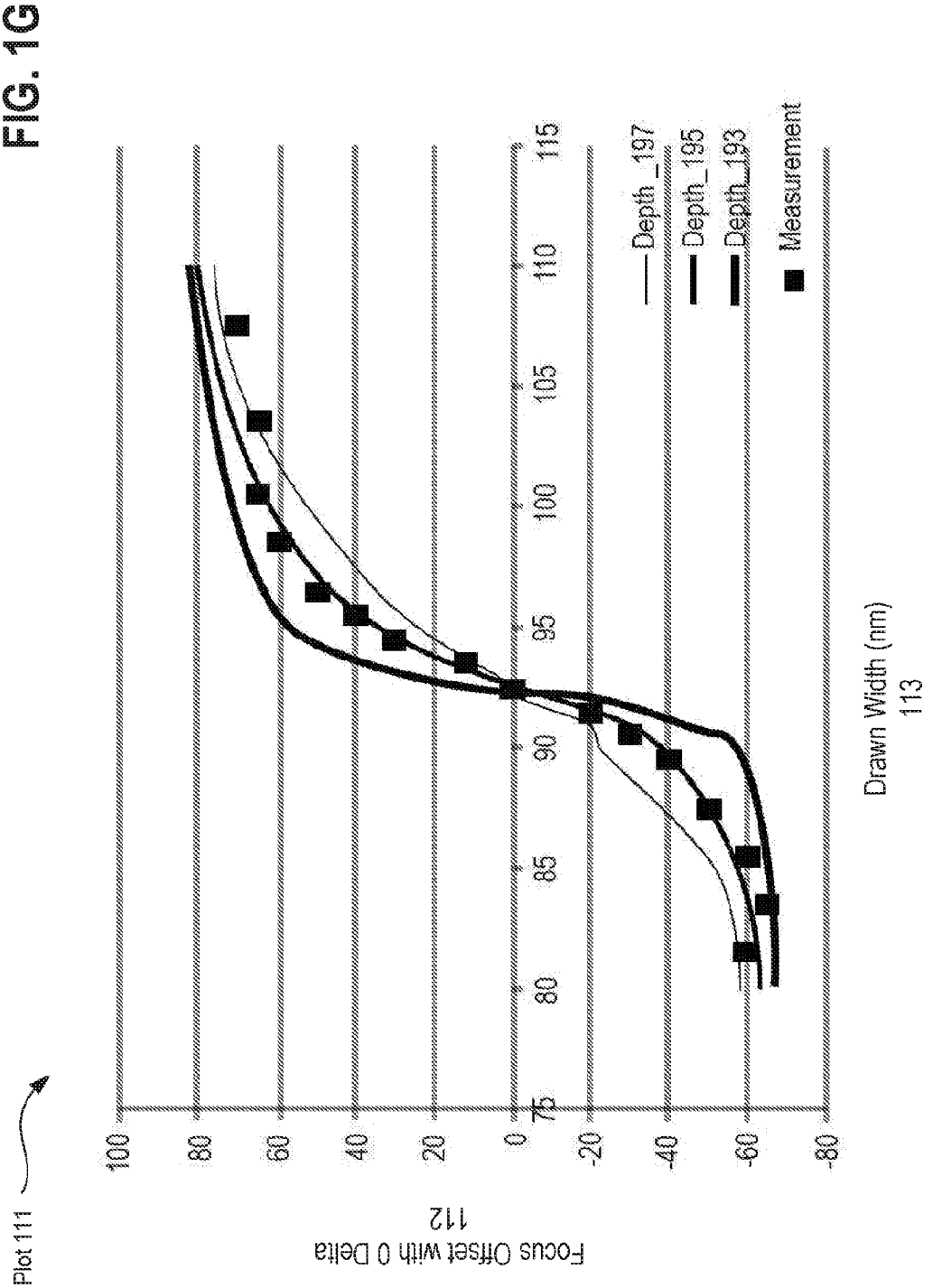
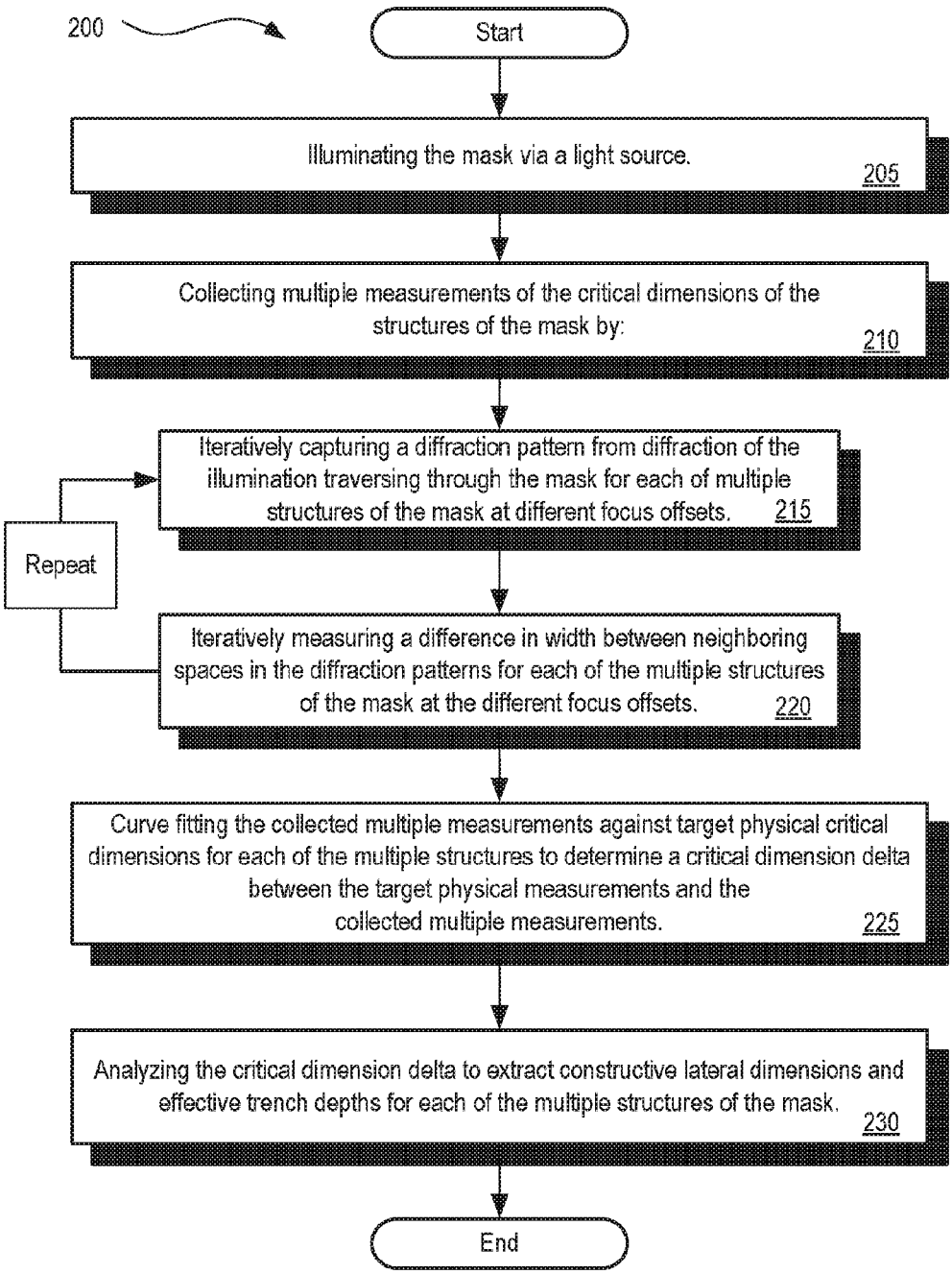

Plot 111
Focus Offset with 0 Delta
112
100
80
60
40
20
0
-20
-40
-60
-80
75
80
85
90
95
100
105
110
115
Drawn Width (nm)
113
Depth_197
Depth_195
Depth_193
Measurement

FIG. 2


200
Start
Illuminating the mask via a light source. 205
Collecting multiple measurements of the critical dimensions of the structures of the mask by: 210
Iteratively capturing a diffraction pattern from diffraction of the illumination traversing through the mask for each of multiple structures of the mask at different focus offsets. 215
Repeat
Iteratively measuring a difference in width between neighboring spaces in the diffraction patterns for each of the multiple structures of the mask at the different focus offsets. 220
Curve fitting the collected multiple measurements against target physical critical dimensions for each of the multiple structures to determine a critical dimension delta between the target physical measurements and the collected multiple measurements. 225
Analyzing the critical dimension delta to extract constructive lateral dimensions and effective trench depths for each of the multiple structures of the mask. 230
End

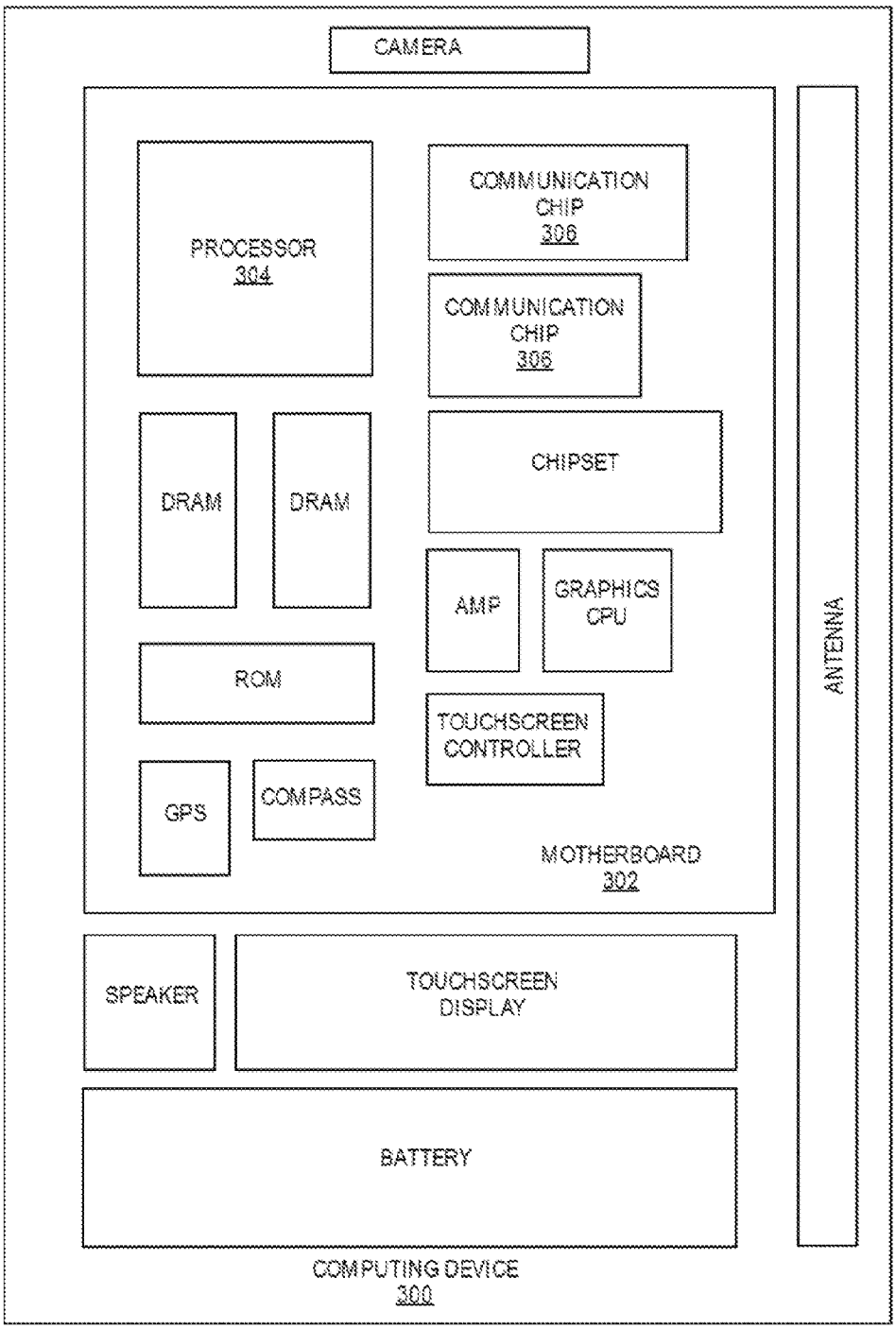

CAMERA
PROCESSOR
304
COMMUNICATION
CHIP
306
COMMUNICATION
CHIP
306
DRAM
DRAM
CHIPSET
AMP
GRAPHICS
CPU
ROM
TOUCHSCREEN
CONTROLLER
GPS
COMPASS
MOTHERBOARD
302
ANTENNA
SPEAKER
TOUCHSCREEN
DISPLAY
BATTERY
COMPUTING DEVICE
300

FIG. 3

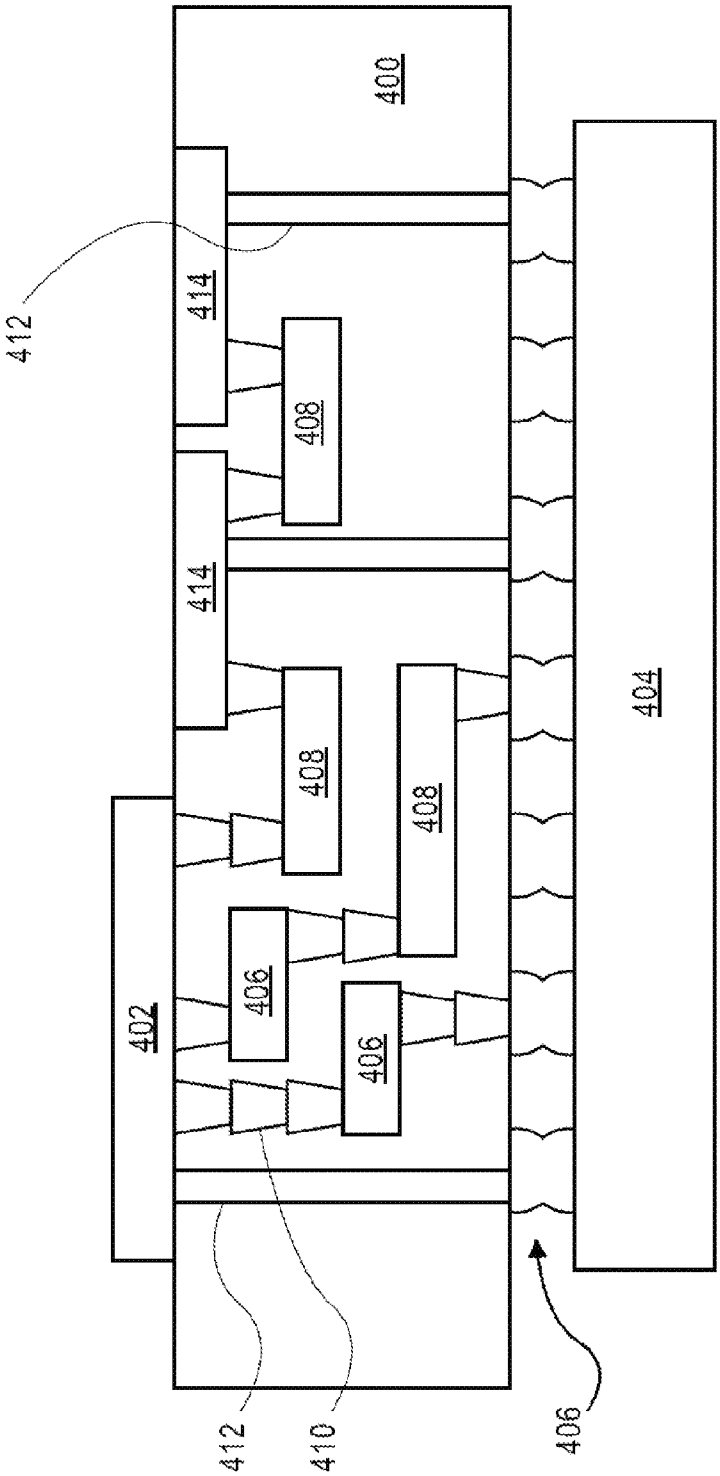


FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/025749

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/027(2006.01)i, G03F 7/20(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/027; G02B 21/00; G01B 11/24; G03C 5/00; G03F 7/20

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: critical dimension, measurement, pattern, focus offset, fitting, trench

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6917901 B2 (REGINALD R. BOWLEY, JR. et al.) 12 July 2005 See abstract, column 4, line 49 - column 6, line 5, claims 1, 16, 23 and figures 1-4.	1-28
A	JP 06-294625 A (ISHIKAWAJIMA HARIMA HEAVY IND. CO., LTD.) 21 October 1994 See paragraphs [0010]-[0021], claims 1, 2 and figures 1-4.	1-28
A	US 2015-0085267 A1 (ASML NETHERLANDS B.V.) 26 March 2015 See abstract, paragraphs [0061]-[0065], claims 1, 2 and figures 8, 9.	1-28
A	KR 10-2000-0026756 A (SAMSUNG ELECTRONICS CO., LTD.) 15 May 2000 See abstract, pages 2, 3, claims 1, 2 and figure 3.	1-28
A	US 2003-0048458 A1 (WALTER MIEHER et al.) 13 March 2003 See abstract, paragraphs [0031]-[0076], claim 1 and figure 1.	1-28

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
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"P" document published prior to the international filing date but later than the priority date claimed
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
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Date of the actual completion of the international search	Date of mailing of the international search report
20 December 2016 (20.12.2016)	**20 December 2016 (20.12.2016)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/025749

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6917901 B2	12/07/2005	US 2003-0158710 A1	21/08/2003
		US 2004-0267506 A1	30/12/2004
		US 6944578 B2	13/09/2005
JP 06-294625 A	21/10/1994	JP 3291825 B2	17/06/2002
US 2015-0085267 A1	26/03/2015	CN 103782238 A	07/05/2014
		CN 103782238 B	17/08/2016
		CN 105892238 A	24/08/2016
		JP 2014-529903 A	13/11/2014
		JP 5864752 B2	17/02/2016
		KR 10-2014-0068970 A	09/06/2014
		TW 201316135 A	16/04/2013
		TW I470374 B	21/01/2015
		US 2013-0050668 A1	28/02/2013
		US 9360769 B2	07/06/2016
		US 9360770 B2	07/06/2016
		WO 2013-029957 A2	07/03/2013
		WO 2013-029957 A3	25/04/2013
KR 10-2000-0026756 A	15/05/2000	None	
US 2003-0048458 A1	13/03/2003	JP 2005-513757 A	12/05/2005
		US 2008-0192221 A1	14/08/2008
		US 7382447 B2	03/06/2008
		US 7656512 B2	02/02/2010
		WO 03-001297 A2	03/01/2003
		WO 03-001297 A3	20/03/2003