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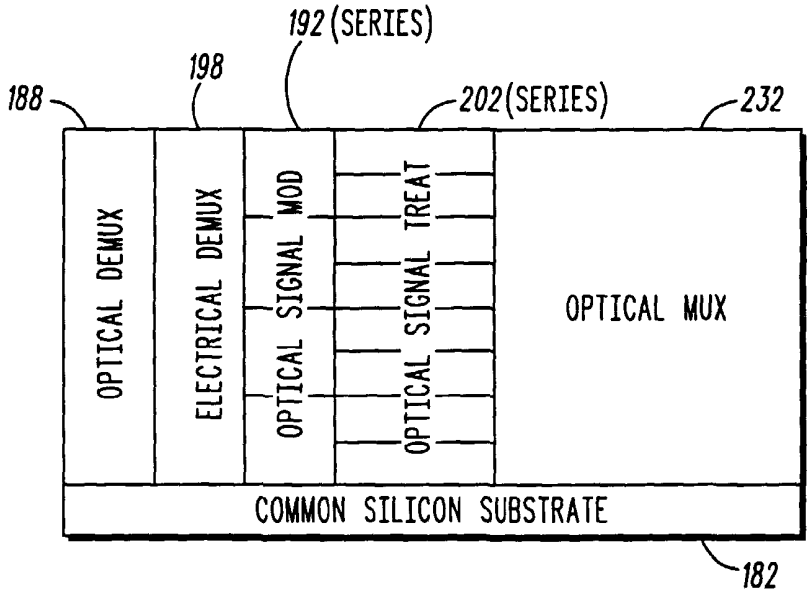
(54) **Title:** APPARATUS FOR HANDLING OPTICAL COMMUNICATION SIGNALS AND METHOD OF MANUFACTURE THEREFOR



(57) **Abstract:** An apparatus for effecting selected aspects of optically conveyed communications treats received incoming optical signals to produce treated outgoing optical signals. The apparatus comprises a plurality of optical signal handling devices (188, 192, 202, and 232) implemented in a monolithic integrated structure arranged on a single substrate (182). The apparatus may further comprise at least one electrically driven device (198) implemented in the monolithic integrated structure. Preferably, at least a first portion of the monolithic structure is implemented in silicon, and at least a second portion of the monolithic structure is implemented in at least one compound semiconductor material.

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APPARATUS FOR HANDLING OPTICAL COMMUNICATION SIGNALS AND METHOD OF MANUFACTURE THEREFOR

Field of the Invention

This invention relates generally to semiconductor structures and devices for optical communication signal handling apparatuses and to a method for their fabrication. This invention more specifically relates to compound semiconductor structures and devices and to the fabrication and use of semiconductor structures, devices, and integrated circuits that include a monocrystalline compound semiconductor material.

Background of the Invention

Optical communication systems, including telecommunication systems, data communication systems and other communication systems, are arranged in several configurations. Which configuration is employed for a particular communication system is dependent upon many varied factors. In whatever configuration a system is established, there are certain optical communication apparatuses that are employed in the system. That is, there are certain basic "building block" apparatuses that are employed to "build" an optical communication system, whatever its ultimate configuration may be. For example, there are optical amplifying apparatuses, optical multiplexing/demultiplexing apparatuses, optical encoding/decoding apparatuses, and other functionally-oriented apparatuses. Whether the particular optical communication system that is contemplated is to be configured as a wide area switching network involving packet switching or a local area network with a token ring configuration or a star configuration or a simple bus distribution arrangement, some of the apparatuses employed in constructing the communication system are common to many or all such configurations.

Optical communication apparatuses (of whatever configuration or for whatever function) are usually manufactured using technologies that are

advantageous for the particular components comprising the apparatus. Some components are best implemented in silicon technology. Other components are best implemented in technologies employing compound semiconductor materials, such as gallium arsenide. As a result, prior art semiconductor technology employs differing manufacturing technologies in fabricating, or implementing, the components that make up the apparatuses used in optical communication systems and this necessarily leads to the use of multiple discrete devices.

Cumbersome packaging and operating inefficiencies are occasioned by the need for employing discrete devices to make up an apparatus. Incorporation of differing technologies in fashioning an apparatus creates a requirement for I/O (input/output) interface devices for optical links or high speed RF (radio frequency) links, interconnecting wires, optic fibers, and other sundry parts to establish correct interface arrangements among components implemented in different technologies. For example, optical fibers carrying an optical signal from an optical device implemented in a first technology to another optical device implemented in a second technology may need to be converted (in a first I/O device) from an optical signal to an electronic signal. The converted electronic signal (representing the optical signal) is conveyed to the second optical device and is then converted (in a second I/O device) to an optical signal for handling by the second optical device. Each conversion is an opportunity for error, a possible source of noise or other signal aberrations, and an occasion for losses, as well as signal propagation delays. The losses may be manifested as heat or as some other bothersome parameter. These limitations are especially disadvantageous when the desired use for a communication apparatus is in a high speed communication system.

Integration of the several devices that comprise a product, or apparatus, into a unitary structure would reduce or eliminate the need for many of these interfaces required for signal hand off, buffering and other functions that must be accomplished in a multi-element, multi-technology product. Prior art fabrication techniques available for producing unitary structures involving various

semiconductor materials, however, have been prohibitively costly and space-inefficient to yield significant improvements by unifying structures.

A monolithic structure that achieves apparatus unitary structure at the fabrication level would reduce the need for individual I/O interfaces for each module transition, and thereby eliminate the need for on-chip "real estate" to accommodate such I/O interfaces. Other advantages realized by such a cost-efficient unitary fabrication structure include a significant reduction in size, an increase in operating speed, a reduction of electromagnetic noise and radiation emanations, an increase in performance reliability, a reduction in cost of manufacture and lower operating power requirements with an attendant lower cost of operation and lower levels of heat generation.

A capability for truly unitary fabrication employing a variety of semiconductor manufacturing technologies provides opportunities to produce multi-technology unitary structures that meet a wide variety of needs. For example, unitary structures may be fabricated to satisfy a wide variety of communication standards, such as cellular telephone standards, personal communication system (PCS) standards, "Bluetooth" communication standards, optical communication standards (e.g., SONET) and other industry-wide standards. Such construction capabilities permit manufacture of optical communication products that are easily adaptable for different system configurations, consume less power, generate less radiation and electromagnetic noise, and are lower in cost, among other benefits.

There is a need for an optical communication signal handling apparatus manifested in a cost-effective power-efficient integrated unitary structure.

The vast majority of semiconductor discrete devices and integrated circuits, including those employed for optical communication signal handling, are fabricated from silicon, at least in part because of the availability of inexpensive, high quality monocrystalline silicon substrates. Other semiconductor materials, such as the so called compound semiconductor materials, have physical attributes, including wider bandgap and/or higher mobility than silicon, or direct bandgaps that makes these materials advantageous for certain types of semiconductor

devices. Unfortunately, compound semiconductor materials are generally much more expensive than silicon and are not available in large wafers as is silicon. Gallium arsenide (GaAs), the most readily available compound semiconductor material, is industrially available in wafers only up to about 150 millimeters (mm) in diameter. In contrast, silicon wafers are available up to about 300 mm and are widely available at 200 mm. The 150 mm GaAs wafers are many times more expensive than are their silicon counterparts. Wafers of other compound semiconductor materials are even less available and are more expensive than GaAs.

Because of the desirable characteristics of compound semiconductor materials, and because of their present generally high cost and low availability in bulk form, for many years attempts have been made to grow thin films of the compound semiconductor materials on a foreign substrate. To achieve optimal characteristics of the compound semiconductor material, however, a monocrystalline film of high crystalline quality is desired. Attempts have been made, for example, to grow layers of a monocrystalline compound semiconductor material on germanium, silicon, and various insulators. These attempts have generally been unsuccessful because lattice mismatches between the host crystal and the grown crystal have caused the resulting thin film of compound semiconductor material to be of low crystalline quality.

If a large area thin film of high quality monocrystalline compound semiconductor material was available at low cost, a variety of semiconductor devices could advantageously be fabricated in that film at a low cost compared to the cost of fabricating such devices on a bulk wafer of compound semiconductor material or in an epitaxial film of such material on a bulk wafer of compound semiconductor material. In addition, if a thin film of high quality monocrystalline compound semiconductor material could be realized on a bulk wafer such as a silicon wafer, an integrated device structure could be achieved that took advantage of the best properties of both the silicon and the compound semiconductor material.

Accordingly, a need exists for a semiconductor structure that provides a high quality monocrystalline compound semiconductor film over another monocrystalline material and for a process for making such a structure.

Brief Description of the Drawings

The present invention is illustrated by way of example and not limitation in the accompanying figures, in which like references indicate similar elements, and in which:

FIGS. 1 - 3 illustrate schematically, in cross section, device structures in accordance with various embodiments of the invention.

FIG. 4 illustrates graphically the relationship between maximum attainable film thickness and lattice mismatch between a host crystal and a grown crystalline overlayer.

FIG. 5 illustrates a high resolution Transmission Electron Micrograph of a structure including a monocrystalline accommodating buffer layer.

FIG. 6 illustrates an x-ray diffraction spectrum of a structure including a monocrystalline accommodating buffer layer.

FIG. 7 illustrates a high resolution Transmission Electron Micrograph of a structure including an amorphous oxide layer.

FIG. 8 illustrates an x-ray diffraction spectrum of a structure including an amorphous oxide layer.

FIG. 9 is a schematic block diagram of a representative prior art optical communication apparatus implemented in discrete components.

FIG. 10 is a schematic block diagram in plan view of a representative optical communication apparatus constructed according to the teachings of the present invention.

FIG. 11 is a schematic block diagram in elevation view of the representative optical communication apparatus constructed according to the teachings of the present invention illustrated in FIG. 10.

FIG. 12 is a flow diagram illustrating the method of the present invention.

Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help to improve understanding of embodiments of the present invention.

Detailed Description of the Drawings

FIG. 1 illustrates schematically, in cross section, a portion of a semiconductor structure 20 in accordance with an embodiment of the invention. Semiconductor structure 20 includes a monocrystalline substrate 22, accommodating buffer layer 24 comprising a monocrystalline material, and a layer 26 of a monocrystalline compound semiconductor material. In this context, the term "monocrystalline" shall have the meaning commonly used within the semiconductor industry. The term shall refer to materials that are a single crystal or that are substantially a single crystal and shall include those materials having a relatively small number of defects such as dislocations and the like as are commonly found in substrates of silicon or germanium or mixtures of silicon and germanium and epitaxial layers of such materials commonly found in the semiconductor industry.

In accordance with one embodiment of the invention, structure 20 also includes an amorphous intermediate layer 28 positioned between substrate 22 and accommodating buffer layer 24. Structure 20 may also include a template layer 30 between the accommodating buffer layer and compound semiconductor layer 26. As will be explained more fully below, the template layer helps to initiate the growth of the compound semiconductor layer on the accommodating buffer layer. The amorphous intermediate layer helps to relieve the strain in the accommodating buffer layer and by doing so, aids in the growth of a high crystalline quality accommodating buffer layer.

Substrate 22, in accordance with an embodiment of the invention, is a monocrystalline semiconductor wafer, preferably of large diameter. The wafer can be of a material from Group IV of the periodic table, and preferably a material

from Group IVA. Examples of Group IV semiconductor materials include silicon, germanium, mixed silicon and germanium, mixed silicon and carbon, mixed silicon, germanium and carbon, and the like. Preferably substrate 22 is a wafer containing silicon or germanium, and most preferably is a high quality monocrystalline silicon wafer as used in the semiconductor industry. Accommodating buffer layer 24 is preferably a monocrystalline oxide or nitride material epitaxially grown on the underlying substrate. In accordance with one embodiment of the invention, amorphous intermediate layer 28 is grown on substrate 22 at the interface between substrate 22 and the growing accommodating buffer layer by the oxidation of substrate 22 during the growth of layer 24. The amorphous intermediate layer serves to relieve strain that might otherwise occur in the monocrystalline accommodating buffer layer as a result of differences in the lattice constants of the substrate and the buffer layer. As used herein, lattice constant refers to the distance between atoms of a cell measured in the plane of the surface. If such strain is not relieved by the amorphous intermediate layer, the strain may cause defects in the crystalline structure of the accommodating buffer layer. Defects in the crystalline structure of the accommodating buffer layer, in turn, would make it difficult to achieve a high quality crystalline structure in monocrystalline compound semiconductor layer 26.

Accommodating buffer layer 24 is preferably a monocrystalline oxide or nitride material selected for its crystalline compatibility with the underlying substrate and with the overlying compound semiconductor material. For example, the material could be an oxide or nitride having a lattice structure matched to the substrate and to the subsequently applied semiconductor material. Materials that are suitable for the accommodating buffer layer include metal oxides such as the alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafnates, alkaline earth metal tantalates, alkaline earth metal ruthenates, alkaline earth metal niobates, alkaline earth metal vanadates, perovskite oxides such as alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide. Additionally, various nitrides such as gallium nitride, aluminum nitride, and boron nitride may also be used for the

accommodating buffer layer. Most of these materials are insulators, although strontium ruthenate, for example, is a conductor. Generally, these materials are metal oxides or metal nitrides, and more particularly, these metal oxide or nitrides typically include at least two different metallic elements. In some specific applications, the metal oxides or nitride may include three or more different metallic elements.

Amorphous interface layer 28 is preferably an oxide formed by the oxidation of the surface of substrate 22, and more preferably is composed of a silicon oxide. The thickness of layer 28 is sufficient to relieve strain attributed to mismatches between the lattice constants of substrate 22 and accommodating buffer layer 24. Typically, layer 28 has a thickness in the range of approximately 0.5-5 nm.

The compound semiconductor material of layer 26 can be selected, as needed for a particular semiconductor structure, from any of the Group IIIA and VA elements (III-V semiconductor compounds), mixed III-V compounds, Group II (A or B) and VIA elements (II-VI semiconductor compounds), and mixed II-VI compounds. Examples include gallium arsenide (GaAs), gallium indium arsenide (GaInAs), gallium aluminum arsenide (GaAlAs), indium phosphide (InP), cadmium sulfide (CdS), cadmium mercury telluride (CdHgTe), zinc selenide (ZnSe), zinc sulfur selenide (ZnSSe), and the like. Suitable template materials chemically bond to the surface of the accommodating buffer layer 24 at selected sites and provide sites for the nucleation of the epitaxial growth of the subsequent compound semiconductor layer 26. Appropriate materials for template 30 are discussed below.

FIG. 2 illustrates, in cross section, a portion of a semiconductor structure 40 in accordance with a further embodiment of the invention. Structure 40 is similar to the previously described semiconductor structure 20, except that an additional buffer layer 32 is positioned between accommodating buffer layer 24 and layer of monocrystalline compound semiconductor material 26. Specifically, the additional buffer layer is positioned between template layer 30 and the overlying layer of compound semiconductor material. The additional buffer layer,

formed of a semiconductor or compound semiconductor material, serves to provide a lattice compensation when the lattice constant of the accommodating buffer layer cannot be adequately matched to the overlying monocrystalline compound semiconductor material layer.

FIG. 3 schematically illustrates, in cross section, a portion of a semiconductor structure 34 in accordance with another exemplary embodiment of the invention. Structure 34 is similar to structure 20, except that structure 34 includes an amorphous layer 36, rather than accommodating buffer layer 24 and amorphous interface layer 28, and an additional semiconductor layer 38.

As explained in greater detail below, amorphous layer 36 may be formed by first forming an accommodating buffer layer and an amorphous interface layer in a similar manner to that described above. Monocrystalline semiconductor layer 26 is then formed (by epitaxial growth) overlying the monocrystalline accommodating buffer layer. The accommodating buffer layer is then exposed to an anneal process to convert the monocrystalline accommodating buffer layer to an amorphous layer. Amorphous layer 36 formed in this manner comprises materials from both the accommodating buffer and interface layers, which amorphous layers may or may not amalgamate. Thus, layer 36 may comprise one or two amorphous layers. Formation of amorphous layer 36 between substrate 22 and semiconductor layer 38 (subsequent to layer 38 formation) relieves stresses between layers 22 and 38 and provides a true compliant substrate for subsequent processing--*e.g.*, compound semiconductor layer 26 formation.

The processes previously described above in connection with FIGS. 1 and 2 are adequate for growing monocrystalline compound semiconductor layers over a monocrystalline substrate. However, the process described in connection with FIG. 3, which includes transforming a monocrystalline accommodating buffer layer to an amorphous oxide layer, may be better for growing monocrystalline compound semiconductor layers because it allows any strain in layer 26 to relax.

Semiconductor layer 38 may include any of the materials described throughout this application in connection with either of compound semiconductor

material layer 26 or additional buffer layer 32. For example, layer 38 may include monocrystalline Group IV or monocrystalline compound semiconductor materials.

In accordance with one embodiment of the present invention, semiconductor layer 38 serves as an anneal cap during layer 36 formation and as a template for subsequent semiconductor layer 26 formation. Accordingly, layer 38 is preferably thick enough to provide a suitable template for layer 26 growth (at least one monolayer) and thin enough to allow layer 38 to form as a substantially defect free monocrystalline semiconductor compound.

In accordance with another embodiment of the invention, semiconductor layer 38 comprises compound semiconductor material (*e.g.*, a material discussed above in connection with compound semiconductor layer 26) that is thick enough to form devices within layer 38. In this case, a semiconductor structure in accordance with the present invention does not include compound semiconductor layer 26. In other words, the semiconductor structure in accordance with this embodiment only includes one compound semiconductor layer disposed above amorphous oxide layer 36.

The following non-limiting, illustrative examples illustrate various combinations of materials useful in structures 20, 40, and 34 in accordance with various alternative embodiments of the invention. These examples are merely illustrative, and it is not intended that the invention be limited to these illustrative examples.

Example 1

In accordance with one embodiment of the invention, monocrystalline substrate 22 is a silicon substrate oriented in the (100) direction. The silicon substrate can be, for example, a silicon substrate as is commonly used in making complementary metal oxide semiconductor (CMOS) integrated circuits having a diameter of about 200-300 mm. In accordance with this embodiment of the invention, accommodating buffer layer 24 is a monocrystalline layer of $Sr_zBa_{1-z}TiO_3$ where z ranges from 0 to 1 and the amorphous intermediate layer is a layer of silicon oxide (SiO_x) formed at the interface between the silicon substrate and the accommodating buffer layer. The value of z is selected to obtain one or more lattice constants closely matched to corresponding lattice constants of the subsequently formed layer 26. The accommodating buffer layer can have a thickness of about 2 to about 100 nanometers (nm) and preferably has a thickness of about 10 nm. In general, it is desired to have an accommodating buffer layer thick enough to isolate the compound semiconductor layer from the substrate to obtain the desired electrical and optical properties. Layers thicker than 100 nm usually provide little additional benefit while increasing cost unnecessarily; however, thicker layers may be fabricated if needed. The amorphous intermediate layer of silicon oxide can have a thickness of about 0.5-5 nm, and preferably a thickness of about 1.5-2.5 nm.

In accordance with this embodiment of the invention, compound semiconductor material layer 26 is a layer of gallium arsenide (GaAs) or aluminum gallium arsenide (AlGaAs) having a thickness of about 1 nm to about 100 micrometers (μm) and preferably a thickness of about 0.5 μm to 10 μm. The thickness generally depends on the application for which the layer is being prepared. To facilitate the epitaxial growth of the gallium arsenide or aluminum gallium arsenide on the monocrystalline oxide, a template layer is formed by capping the oxide layer. The template layer is preferably 1-10 monolayers of Ti-As, Sr-O-As, Sr-Ga-O, or Sr-Al-O. By way of a preferred example, 1-2 monolayers of Ti-As or Sr-Ga-O have been shown to successfully grow GaAs layers.

Example 2

In accordance with a further embodiment of the invention, monocrystalline substrate 22 is a silicon substrate as described above. The accommodating buffer layer is a monocrystalline oxide of strontium or barium zirconate or hafnate in a cubic or orthorhombic phase with an amorphous intermediate layer of silicon oxide formed at the interface between the silicon substrate and the accommodating buffer layer. The accommodating buffer layer can have a thickness of about 2-100 nm and preferably has a thickness of at least 5 nm to ensure adequate crystalline and surface quality and is formed of a monocrystalline $SrZrO_3$, $BaZrO_3$, $SrHfO_3$, $BaSnO_3$ or $BaHfO_3$. For example, a monocrystalline oxide layer of $BaZrO_3$ can grow at a temperature of about 700 degrees C. The lattice structure of the resulting crystalline oxide exhibits a 45 degree rotation with respect to the substrate silicon lattice structure.

An accommodating buffer layer formed of these zirconate or hafnate materials is suitable for the growth of compound semiconductor materials in the indium phosphide (InP) system. The compound semiconductor material can be, for example, indium phosphide (InP), indium gallium arsenide (InGaAs), aluminum indium arsenide, (AlInAs), or aluminum gallium indium arsenic phosphide (AlGaInAsP), having a thickness of about 1.0 nm to 10 μm. A suitable template for this structure is 1-10 monolayers of zirconium-arsenic (Zr-As), zirconium-phosphorus (Zr-P), hafnium-arsenic (Hf-As), hafnium-phosphorus (Hf-P), strontium-oxygen-arsenic (Sr-O-As), strontium-oxygen-phosphorus (Sr-O-P), barium-oxygen-arsenic (Ba-O-As), indium-strontium-oxygen (In-Sr-O), or barium-oxygen-phosphorus (Ba-O-P), and preferably 1-2 monolayers of one of these materials. By way of an example, for a barium zirconate accommodating buffer layer, the surface is terminated with 1-2 monolayers of zirconium followed by deposition of 1-2 monolayers of arsenic to form a Zr-As template. A monocrystalline layer of the compound semiconductor material from the indium phosphide system is then grown on the template layer. The resulting lattice structure of the compound semiconductor material exhibits a 45 degree rotation

with respect to the accommodating buffer layer lattice structure and a lattice mismatch to (100) InP of less than 2.5%, and preferably less than about 1.0%.

Example 3

In accordance with a further embodiment of the invention, a structure is provided that is suitable for the growth of an epitaxial film of a II-VI material overlying a silicon substrate. The substrate is preferably a silicon wafer as described above. A suitable accommodating buffer layer material is $Sr_xBa_{1-x}TiO_3$, where x ranges from 0 to 1, having a thickness of about 2-100 nm and preferably a thickness of about 5-15 nm. The II-VI compound semiconductor material can be, for example, zinc selenide (ZnSe) or zinc sulfur selenide (ZnSSe). A suitable template for this material system includes 1-10 monolayers of zinc-oxygen (Zn-O) followed by 1-2 monolayers of an excess of zinc followed by the selenidation of zinc on the surface. Alternatively, a template can be, for example, 1-10 monolayers of strontium-sulfur (Sr-S) followed by the ZnSeS.

Example 4

This embodiment of the invention is an example of structure 40 illustrated in FIG. 2. Substrate 22, monocrystalline oxide layer 24, and monocrystalline compound semiconductor material layer 26 can be similar to those described in example 1. In addition, an additional buffer layer 32 serves to alleviate any strains that might result from a mismatch of the crystal lattice of the accommodating buffer layer and the lattice of the monocrystalline semiconductor material. Buffer layer 32 can be a layer of germanium or a GaAs, an aluminum gallium arsenide (AlGaAs), an indium gallium phosphide (InGaP), an aluminum gallium phosphide (AlGaP), an indium gallium arsenide (InGaAs), an aluminum indium phosphide (AlInP), a gallium arsenide phosphide (GaAsP), or an indium gallium phosphide (InGaP) strain compensated superlattice. In accordance with one aspect of this embodiment, buffer layer 32 includes a $GaAs_xP_{1-x}$ superlattice, wherein the value

of x ranges from 0 to 1. In accordance with another aspect, buffer layer 32 includes an $In_yGa_{1-y}P$ superlattice, wherein the value of y ranges from 0 to 1. By varying the value of x or y, as the case may be, the lattice constant is varied from bottom to top across the superlattice to create a match between lattice constants of the underlying oxide and the overlying compound semiconductor material. The compositions of other materials, such as those listed above, may also be similarly varied to manipulate the lattice constant of layer 32 in a like manner. The superlattice can have a thickness of about 50-500 nm and preferably has a thickness of about 100-200 nm. The template for this structure can be the same of that described in example 1. Alternatively, buffer layer 32 can be a layer of monocrystalline germanium having a thickness of 1-50 nm and preferably having a thickness of about 2-20 nm. In using a germanium buffer layer, a template layer of either germanium-strontium (Ge-Sr) or germanium-titanium (Ge-Ti) having a thickness of about one monolayer can be used as a nucleating site for the subsequent growth of the monocrystalline compound semiconductor material layer. The formation of the oxide layer is capped with either a monolayer of strontium or a monolayer of titanium to act as a nucleating site for the subsequent deposition of the monocrystalline germanium. The monolayer of strontium or titanium provides a nucleating site to which the first monolayer of germanium can bond.

Example 5

This example also illustrates materials useful in a structure 40 as illustrated in FIG. 2. Substrate material 22, accommodating buffer layer 24, monocrystalline compound semiconductor material layer 26 and template layer 30 can be the same as those described above in example 2. In addition, a buffer layer 32 is inserted between the accommodating buffer layer and the overlying monocrystalline compound semiconductor material layer. The buffer layer, a further monocrystalline semiconductor material, can be, for example, a graded layer of indium gallium arsenide (InGaAs) or indium aluminum arsenide (InAlAs). In

accordance with one aspect of this embodiment, buffer layer 32 includes InGaAs, in which the indium composition varies from 0 to about 47%. The buffer layer preferably has a thickness of about 10-30 nm. Varying the composition of the buffer layer from GaAs to InGaAs serves to provide a lattice match between the underlying monocrystalline oxide material and the overlying layer of monocrystalline compound semiconductor material. Such a buffer layer is especially advantageous if there is a lattice mismatch between accommodating buffer layer 24 and monocrystalline compound semiconductor material layer 26.

Example 6

This example provides exemplary materials useful in structure 34, as illustrated in FIG. 3. Substrate material 22, template layer 30, and monocrystalline compound semiconductor material layer 26 may be the same as those described above in connection with example 1.

Amorphous layer 36 is an amorphous oxide layer which is suitably formed of a combination of amorphous intermediate layer materials (e.g., layer 28 materials as described above) and accommodating buffer layer materials (e.g., layer 24 materials as described above). For example, amorphous layer 36 may include a combination of SiO_x and $Sr_zBa_{1-z}TiO_3$ (where z ranges from 0 to 1), which combine or mix, at least partially, during an anneal process to form amorphous oxide layer 36.

The thickness of amorphous layer 36 may vary from application to application and may depend on such factors as desired insulating properties of layer 36, type of semiconductor material comprising layer 26, and the like. In accordance with one exemplary aspect of the present embodiment, layer 36 thickness is about 2 nm to about 100 nm, preferably about 2-10 nm, and more preferably about 5-6 nm.

Layer 38 comprises a monocrystalline compound semiconductor material that can be grown epitaxially over a monocrystalline oxide material such as material used to form accommodating buffer layer 24. In accordance with one

embodiment of the invention, layer 38 includes the same materials as those comprising layer 26. For example, if layer 26 includes GaAs, layer 38 also includes GaAs. However, in accordance with other embodiments of the present invention, layer 38 may include materials different from those used to form layer 26. In accordance with one exemplary embodiment of the invention, layer 38 is about 1 monolayer to about 100 nm thick.

Referring again to FIGS. 1 - 3, substrate 22 is a monocrystalline substrate such as a monocrystalline silicon substrate. The crystalline structure of the monocrystalline substrate is characterized by a lattice constant and by a lattice orientation. In similar manner, accommodating buffer layer 24 is also a monocrystalline material and the lattice of that monocrystalline material is characterized by a lattice constant and a crystal orientation. The lattice constants of the accommodating buffer layer and the monocrystalline substrate must be closely matched or, alternatively, must be such that upon rotation of one crystal orientation with respect to the other crystal orientation, a substantial match in lattice constants is achieved. In this context the terms "substantially equal" and "substantially matched" mean that there is sufficient similarity between the lattice constants to permit the growth of a high quality crystalline layer on the underlying layer.

FIG. 4 illustrates graphically the relationship of the achievable thickness of a grown crystal layer of high crystalline quality as a function of the mismatch between the lattice constants of the host crystal and the grown crystal. Curve 42 illustrates the boundary of high crystalline quality material. The area to the right of curve 42 represents layers that tend to be polycrystalline. With no lattice mismatch, it is theoretically possible to grow an infinitely thick, high quality epitaxial layer on the host crystal. As the mismatch in lattice constants increases, the thickness of achievable, high quality crystalline layer decreases rapidly. As a reference point, for example, if the lattice constants between the host crystal and the grown layer are mismatched by more than about 2%, monocrystalline epitaxial layers in excess of about 20 nm cannot be achieved.

In accordance with one embodiment of the invention, substrate 22 is a (100) or (111) oriented monocrystalline silicon wafer and accommodating buffer layer 24 is a layer of strontium barium titanate. Substantial matching of lattice constants between these two materials is achieved by rotating the crystal orientation of the titanate material by 45° with respect to the crystal orientation of the silicon substrate wafer. The inclusion in the structure of amorphous interface layer 28, a silicon oxide layer in this example, if it is of sufficient thickness, serves to reduce strain in the titanate monocrystalline layer that might result from any mismatch in the lattice constants of the host silicon wafer and the grown titanate layer. As a result, in accordance with an embodiment of the invention, a high quality, thick, monocrystalline titanate layer is achievable.

Still referring to FIGS. 1 - 3, layer 26 is a layer of epitaxially grown monocrystalline material and that crystalline material is also characterized by a crystal lattice constant and a crystal orientation. In accordance with one embodiment of the invention, the lattice constant of layer 26 differs from the lattice constant of substrate 22. To achieve high crystalline quality in this epitaxially grown monocrystalline layer, the accommodating buffer layer must be of high crystalline quality. In addition, in order to achieve high crystalline quality in layer 26, substantial matching between the crystal lattice constant of the host crystal, in this case, the monocrystalline accommodating buffer layer, and the grown crystal is desired. With properly selected materials this substantial matching of lattice constants is achieved as a result of rotation of the crystal orientation of the grown crystal with respect to the orientation of the host crystal. If the grown crystal is gallium arsenide, aluminum gallium arsenide, zinc selenide, or zinc sulfur selenide and the accommodating buffer layer is monocrystalline $Sr_xBa_{1-x}TiO_3$, substantial matching of crystal lattice constants of the two materials is achieved, wherein the crystal orientation of the grown layer is rotated by 45° with respect to the orientation of the host monocrystalline oxide. Similarly, if the host material is a strontium or barium zirconate or a strontium or barium hafnate or barium tin oxide and the compound semiconductor layer is indium phosphide or gallium indium arsenide or aluminum indium arsenide, substantial matching of

crystal lattice constants can be achieved by rotating the orientation of the grown crystal layer by 45° with respect to the host oxide crystal. In some instances, a crystalline semiconductor buffer layer between the host oxide and the grown compound semiconductor layer can be used to reduce strain in the grown monocrystalline compound semiconductor layer that might result from small differences in lattice constants. Better crystalline quality in the grown monocrystalline compound semiconductor layer can thereby be achieved.

The following example illustrates a process, in accordance with one embodiment of the invention, for fabricating a semiconductor structure such as the structures depicted in FIGS. 1 - 3. The process starts by providing a monocrystalline semiconductor substrate comprising silicon or germanium. In accordance with a preferred embodiment of the invention, the semiconductor substrate is a silicon wafer having a (100) orientation. The substrate is preferably oriented on axis or, at most, about 0.5° off axis. At least a portion of the semiconductor substrate has a bare surface, although other portions of the substrate, as described below, may encompass other structures. The term "bare" in this context means that the surface in the portion of the substrate has been cleaned to remove any oxides, contaminants, or other foreign material. As is well known, bare silicon is highly reactive and readily forms a native oxide. The term "bare" is intended to encompass such a native oxide. A thin silicon oxide may also be intentionally grown on the semiconductor substrate, although such a grown oxide is not essential to the process in accordance with the invention. In order to epitaxially grow a monocrystalline oxide layer overlying the monocrystalline substrate, the native oxide layer must first be removed to expose the crystalline structure of the underlying substrate. The following process is preferably carried out by molecular beam epitaxy (MBE), although other epitaxial processes may also be used in accordance with the present invention. The native oxide can be removed by first thermally depositing a thin layer of strontium, barium, a combination of strontium and barium, or other alkali earth metals or combinations of alkali earth metals in an MBE apparatus. In the case where strontium is used, the substrate is then heated to a temperature of about 750° C to cause the

strontium to react with the native silicon oxide layer. The strontium serves to reduce the silicon oxide to leave a silicon oxide-free surface. The resultant surface, which exhibits an ordered 2x1 structure, includes strontium, oxygen, and silicon. The ordered 2x1 structure forms a template for the ordered growth of an overlying layer of a monocrystalline oxide. The template provides the necessary chemical and physical properties to nucleate the crystalline growth of an overlying layer.

In accordance with an alternate embodiment of the invention, the native silicon oxide can be converted and the substrate surface can be prepared for the growth of a monocrystalline oxide layer by depositing an alkali earth metal oxide, such as strontium oxide, strontium barium oxide, or barium oxide, onto the substrate surface by MBE at a low temperature and by subsequently heating the structure to a temperature of about 750°C. At this temperature a solid state reaction takes place between the strontium oxide and the native silicon oxide causing the reduction of the native silicon oxide and leaving an ordered 2x1 structure with strontium, oxygen, and silicon remaining on the substrate surface. Again, this forms a template for the subsequent growth of an ordered monocrystalline oxide layer.

Following the removal of the silicon oxide from the surface of the substrate, in accordance with one embodiment of the invention, the substrate is cooled to a temperature in the range of about 200-800°C and a layer of strontium titanate is grown on the template layer by molecular beam epitaxy. The MBE process is initiated by opening shutters in the MBE apparatus to expose strontium, titanium and oxygen sources. The ratio of strontium and titanium is approximately 1:1. The partial pressure of oxygen is initially set at a minimum value to grow stochiometric strontium titanate at a growth rate of about 0.3-0.5 nm per minute. After initiating growth of the strontium titanate, the partial pressure of oxygen is increased above the initial minimum value. The overpressure of oxygen causes the growth of an amorphous silicon oxide layer at the interface between the underlying substrate and the growing strontium titanate layer. The growth of the silicon oxide layer results from the diffusion of oxygen through the growing

strontium titanate layer to the interface where the oxygen reacts with silicon at the surface of the underlying substrate. The strontium titanate grows as an ordered monocrystal with the crystalline orientation rotated by 45° with respect to the ordered 2x1 crystalline structure of the underlying substrate. Strain that otherwise might exist in the strontium titanate layer because of the small mismatch in lattice constant between the silicon substrate and the growing crystal is relieved in the amorphous silicon oxide intermediate layer.

After the strontium titanate layer has been grown to the desired thickness, the monocrystalline strontium titanate is capped by a template layer that is conducive to the subsequent growth of an epitaxial layer of a desired compound semiconductor material. For the subsequent growth of a layer of gallium arsenide, the MBE growth of the strontium titanate monocrystalline layer can be capped by terminating the growth with 1-2 monolayers of titanium, 1-2 monolayers of titanium-oxygen or with 1-2 monolayers of strontium-oxygen. Following the formation of this capping layer, arsenic is deposited to form a Ti-As bond, a Ti-O-As bond or a Sr-O-As. Any of these form an appropriate template for deposition and formation of a gallium arsenide monocrystalline layer. Following the formation of the template, gallium is subsequently introduced to the reaction with the arsenic and gallium arsenide forms. Alternatively, gallium can be deposited on the capping layer to form a Sr-O-Ga bond, and arsenic is subsequently introduced with the gallium to form the GaAs.

FIG. 5 is a high resolution Transmission Electron Micrograph (TEM) of semiconductor material manufactured in accordance with the present invention. Single crystal $SrTiO_3$ accommodating buffer layer 24 was grown epitaxially on silicon substrate 22. During this growth process, amorphous interfacial layer 28 is formed which relieves strain due to lattice mismatch. GaAs compound semiconductor layer 26 was then grown epitaxially using template layer 30.

FIG. 6 illustrates an x-ray diffraction spectrum taken on structure including GaAs compound semiconductor layer 26 grown on silicon substrate 22 using accommodating buffer layer 24. The peaks in the spectrum indicate that both the

accommodating buffer layer 24 and GaAs compound semiconductor layer 26 are single crystal and (100) orientated.

The structure illustrated in FIG. 2 can be formed by the process discussed above with the addition of an additional buffer layer deposition step. The buffer layer is formed overlying the template layer before the deposition of the monocrystalline compound semiconductor layer. If the buffer layer is a compound semiconductor superlattice, such a superlattice can be deposited, by MBE for example, on the template described above. If instead the buffer layer is a layer of germanium, the process above is modified to cap the strontium titanate monocrystalline layer with a final layer of either strontium or titanium and then by depositing germanium to react with the strontium or titanium. The germanium buffer layer can then be deposited directly on this template.

Structure 34, illustrated in FIG. 3, may be formed by growing an accommodating buffer layer, forming an amorphous oxide layer over substrate 22, and growing semiconductor layer 38 over the accommodating buffer layer, as described above. The accommodating buffer layer and the amorphous oxide layer are then exposed to an anneal process sufficient to change the crystalline structure of the accommodating buffer layer from monocrystalline to amorphous, thereby forming an amorphous layer such that the combination of the amorphous oxide layer and the now amorphous accommodating buffer layer form a single amorphous oxide layer 36. Layer 26 is then subsequently grown over layer 38. Alternatively, the anneal process may be carried out subsequent to growth of layer 26.

In accordance with one aspect of this embodiment, layer 36 is formed by exposing substrate 22, the accommodating buffer layer, the amorphous oxide layer, and semiconductor layer 38 to a rapid thermal anneal process with a peak temperature of about 700°C to about 1000°C and a process time of about 1 to about 10 minutes. However, other suitable anneal processes may be employed to convert the accommodating buffer layer to an amorphous layer in accordance with the present invention. For example, laser annealing or "conventional" thermal annealing processes (in the proper environment) may be used to form layer 36.

When conventional thermal annealing is employed to form layer 36, an overpressure of one or more constituents of layer 30 may be required to prevent degradation of layer 38 during the anneal process. For example, when layer 38 includes GaAs, the anneal environment preferably includes an overpressure of arsenic to mitigate degradation of layer 38.

As noted above, layer 38 of structure 34 may include any materials suitable for either of layers 32 or 26. Accordingly, any deposition or growth methods described in connection with either layer 32 or 26, may be employed to deposit layer 38.

FIG. 7 is a high resolution Transmission Electron Micrograph (TEM) of semiconductor material manufactured in accordance with the embodiment of the invention illustrated in FIG. 3. In Accordance with this embodiment, a single crystal $SrTiO_3$ accommodating buffer layer was grown epitaxially on silicon substrate 22. During this growth process, an amorphous interfacial layer forms as described above. Next, GaAs layer 38 is formed above the accommodating buffer layer and the accommodating buffer layer is exposed to an anneal process to form amorphous oxide layer 36.

FIG. 8 illustrates an x-ray diffraction spectrum taken on a structure including GaAs compound semiconductor layer 38 and amorphous oxide layer 36 formed on silicon substrate 22. The peaks in the spectrum indicate that GaAs compound semiconductor layer 38 is single crystal and (100) orientated and the lack of peaks around 40 to 50 degrees indicates that layer 36 is amorphous.

The process described above illustrates a process for forming a semiconductor structure including a silicon substrate, an overlying oxide layer, and a monocrystalline gallium arsenide compound semiconductor layer by the process of molecular beam epitaxy. The process can also be carried out by the process of chemical vapor deposition (CVD), metal organic chemical vapor deposition (MOCVD), migration enhanced epitaxy (MEE), atomic layer epitaxy (ALE), physical vapor deposition (PVD), chemical solution deposition (CSD), pulsed laser deposition (PLD), or the like. Further, by a similar process, other monocrystalline accommodating buffer layers such as alkaline earth metal

titanates, zirconates, hafnates, tantalates, vanadates, ruthenates, and niobates, peroskite oxides such as alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide can also be grown. Further, by a similar process such as MBE, other III-V and II-VI monocrystalline compound semiconductor layers can be deposited overlying the monocrystalline oxide accommodating buffer layer.

Each of the variations of compound semiconductor materials and monocrystalline oxide accommodating buffer layer uses an appropriate template for initiating the growth of the compound semiconductor layer. For example, if the accommodating buffer layer is an alkaline earth metal zirconate, the oxide can be capped by a thin layer of zirconium. The deposition of zirconium can be followed by the deposition of arsenic or phosphorus to react with the zirconium as a precursor to depositing indium gallium arsenide, indium aluminum arsenide, or indium phosphide respectively. Similarly, if the monocrystalline oxide accommodating buffer layer is an alkaline earth metal hafnate, the oxide layer can be capped by a thin layer of hafnium. The deposition of hafnium is followed by the deposition of arsenic or phosphorous to react with the hafnium as a precursor to the growth of an indium gallium arsenide, indium aluminum arsenide, or indium phosphide layer, respectively. In a similar manner, strontium titanate can be capped with a layer of strontium or strontium and oxygen and barium titanate can be capped with a layer of barium or barium and oxygen. Each of these depositions can be followed by the deposition of arsenic or phosphorus to react with the capping material to form a template for the deposition of a compound semiconductor material layer comprising indium gallium arsenide, indium aluminum arsenide, or indium phosphide.

FIG. 9 is a schematic block diagram of a representative prior art optical communication apparatus implemented in discrete components. FIG. 9 is not a representation of a particular optical communication apparatus. Rather, FIG. 9 illustrates shortcomings of prior art implementations of various generically described devices in optical communication apparatuses. In FIG. 9, an optical communication signal handling apparatus 110 receives incoming signals at an

optical input portal 112 and emits treated multiplexed output optical signals at an optical output portal 114. Signals traversing optical portals 112, 114 may be simplex signals (single channel signals) or may be complex signals (several signals at different frequencies or several signals, each encoded for identification). In the embodiment of the prior art apparatus illustrated in FIG. 9, it is presumed that incoming signals received at optical input portal 112 are complex signals.

Incoming signals received at optical incoming portal 112 are received at an I/O (input/output) unit 115 to appropriately configure received signals for handling by a demultiplexer unit 116. Demultiplexer unit 116 sorts out the various signals contained in the incoming signal received at optical input portal 112 into constituent signals and distributes resultant constituent signals to I/O units 118a, 118b, 118c, 118d. I/O unit 118a appropriately configures signals received from demultiplexer unit 116 for handling by a waveguide 120a to convey signals to an optical signal modification unit 124a via an I/O unit 122a. I/O unit 122a appropriately configures signals received via waveguide 120a for handling by optical signal modification unit 124a. I/O unit 118b appropriately configures signals received from demultiplexer unit 116 for handling by a waveguide 120b to convey signals to an optical signal modification unit 124b via an I/O unit 122b. I/O unit 122b appropriately configures signals received via waveguide 120b for handling by optical signal modification unit 124b. I/O unit 118c appropriately configures signals received from demultiplexer unit 116 for handling by a waveguide 120c to convey signals to an optical signal modification unit 124c via an I/O unit 122c. I/O unit 122c appropriately configures signals received via waveguide 120c for handling by optical signal modification unit 124c. I/O unit 118d appropriately configures signals received from demultiplexer unit 116 for handling by a waveguide 120d to convey signals to an optical signal modification unit 124d via an I/O unit 122d. I/O unit 122d appropriately configures signals received via waveguide 120d for handling by optical signal modification unit 124d. Waveguides 120a, 120b, 120c, 120d may be implemented as optical fiber transmission devices or as electrical conductors carrying electrical representations of optical signals.

An electrical input signal is received by apparatus 110 at an electrical input node 126. Electrical input signals are received from input node 126 at an I/O device 128 to appropriately configure electrical input signals for handling by an electrical demultiplexer unit 130.

Signals received at electrical input node 126 may be single channel signals or may be complex signals (several signals at different frequencies or several signals, each encoded for identification). In the embodiment of the representative prior art apparatus illustrated in FIG. 9, it is presumed that incoming signals received at electrical input node 126 are complex signals. Incoming electrical signals received at electrical input node 126 are received at an I/O (input/output) unit 128 to appropriately configure received signals for handling by an electrical demultiplexer unit 130. Electrical demultiplexer unit 130 sorts out the various signals contained in the incoming signal received at electrical input node 126 into constituent signals and distributes resultant constituent signals to an I/O unit 132. I/O unit 132 appropriately configures signals received from electrical demultiplexer unit 130 for handling by electrical conductors 134a, 134b, 134c, 134d to convey electrical signals to optical signal modification units 124a, 124b, 124c, 124d via respective I/O units 136a, 136b, 136c, 136d. I/O units 136a, 136b, 136c, 136d appropriately configure signals received via electrical conductors 134a, 134b, 134c, 134d for handling by optical signal modification units 124a, 124b, 124c, 124d.

By way of example, electrical signals conveyed via electrical conductors 134a, 134b, 134c, 134d may be modulation signals that are employed by optical signal modification units 124a, 124b, 124c, 124d to modulate optical signals received via waveguides 120a, 120b, 120c, 120d and I/O units 122a, 122b, 122c, 122d.

Optical signal modification units 124a, 124b, 124c, 124d produce modified optical signals to I/O units 138a, 138b, 138c, 138d. I/O units 138a, 138b, 138c, 138d appropriately configure signals received from optical signal modification units 124a, 124b, 124c, 124d for handling by waveguides 140, 146, 152, 158. Waveguide 140 branches to waveguides 142, 144. Waveguide 146 branches to

waveguides 148, 150. Waveguide 152 branches to waveguides 154, 156. Waveguide 158 branches to waveguides 160, 162. Waveguides 140, 142, 144, 146, 148, 150, 152, 154, 156, 158, 160, 162 convey modified optical signals to optical signal treating units 166a, 166b, 166c, 166d, 166e, 166f, 166g, 166h via I/O units 164a, 164b, 164c, 164d, 164e, 164f, 164g, 164h. Waveguides 140, 142, 144, 146, 148, 150, 152, 154, 156, 158, 160, 162 may be implemented as optical fiber transmission devices or as electrical conductors carrying electrical representations of optical signals. I /O units 164a, 164b, 164c, 164d, 164e, 164f, 164g, 164h appropriately configure signals received from waveguides 140, 142, 144, 146, 148, 150, 152, 154, 156, 158, 160, 162 for handling by optical signal treating units 166a, 166b, 166c, 166d, 166e, 166f, 166g, 166h (hereafter sometimes referred to as "166 (series)"). Optical signal treating units 166 (series) may be, for example, signal smoothing units, or timing synchronization units, or buffer units, or another unit that treats optical signals to modify an aspect of the signals.

Optical signal treating units 166 (series) produce treated optical signals to I/O units 168a, 168b, 168c, 168d, 168e, 168f, 168g, 168h (hereafter sometimes referred to as "168 (series)"). I/O units 168 (series) appropriately configure treated optical signals received from optical treating units 166 (series) for handling by waveguides 170a, 170b, 170c, 170d, 170e, 170f, 170g, 170h (hereafter sometimes referred to as "170 (series)") to convey treated optical signals to optical multiplexer 172 via I/O units 174a, 174b, 174c, 174d, 174e, 174f, 174g, 174h (hereafter sometimes referred to as "174 (series)"). Waveguides 170 (series) may be implemented as optical fiber transmission devices or as electrical conductors carrying electrical representations of optical signals. I /O units 174 (series) appropriately configure signals received from waveguides 170 (series) for multiplexing by optical multiplexer 172. Optical multiplexer 172 provides multiplexed treated optical signals to an I/O unit 176. I/O unit 176 appropriately configures signals received from optical multiplexer 172 for conveyance via optical output portal 114 to other parts of a communication network (not shown in FIG. 9) in which apparatus 110 is employed.

Each of the elements of optical communication signal handling apparatus 110 – including optical demultiplexer unit 116, electrical demultiplexer unit 130, optical modification units 124 (series), optical signal treating units 166 (series), and optical multiplexer 172 - are implemented in discrete components that are linked using wires, fiber optic cables or other connection structures.

The various elements of optical communication signal handling apparatus 110 may be gathered into a single package 111, but the discrete nature of the components and the interconnection structures necessitated by such discrete component construction (such as I/O devices 118, 122, 132, 136, 138, 164, 168, 174, extra buffer units or similar interface components; some not shown in FIG. 9) ensure that any such single package will be bulky and relatively inefficient compared with a similar communication signal handling apparatus implemented according to the present invention in a monolithically fabricated integrated unitary structure.

Thus, an important structural feature emphasized in connection with the representative prior art apparatus illustrated in FIG. 9 is that the various devices employed in that prior art apparatus are embodied in discrete "chips", or components. The various chips are implemented in various topologies and technologies that are cost effective or otherwise appropriate for their respective operational parameters.

Accordingly, one device may be implemented in silicon, and another device may be implemented in a compound semiconductor material, such as gallium arsenide. An important point in this regard is that there are significant limitations with prior art technology in fabricating devices of such various topologies within one unitary package. Because there is no opportunity with prior art techniques for fabricating the various topologies on a single common substrate, the most "unitary" construction that a collection of several such devices may achieve is to be contained within a single enclosure, in a "unified packaging" of a plurality of chips in an attempt at a unitary structure.

Substrates employed for such unified packaging, such as alumina substrates, are oriented in a generally planar configuration upon which the various elements

(i.e., devices) of the package are arrayed. Variances in the surface of such alumina substrates, measured substantially perpendicular to the plane of the substrate, are quite rough. Such roughness precludes alignment of devices to within micrometer tolerances of vertical displacement from a common plane. Such micrometer tolerances are required, for example, in crafting a unitary collection of optically communicating devices. The alternative available using rough-surfaced prior art substrates, such as alumina substrates, is to fabricate the various optical devices on separate substrates and employ fiber communications or electrical signal conveyances, with the attendant required I/O terminations at each end of each fiber connector or electrical conveyance. Fabricating semiconductor devices on a common substrate during the deposition or other processes used for creating the devices permits vertical placement tolerances on the order of micrometers. Such fine control of vertical placement allows ample latitude for direct optical alignment among devices on a common substrate.

Limitations in placement of devices adjacent each other are also problematic. That is, the spacing between adjacent devices, measured substantially parallel with the plane of the common substrate (e.g., alumina substrate), is limited by the accuracy of placement performed by pick-and-place machinery or similar tools used in manufacturing. As a result, the tolerance of such horizontal proximity placement is on the order of tenths of a millimeter (0.1 mm). Producing semiconductor devices on a common substrate during the deposition or other fabrication processes used for creating the devices involves horizontal placement tolerances on the order of micrometers – a difference by a factor of 100 over prior art production pick-and-place capabilities.

Being able to fabricate semiconductor devices on a common substrate during the deposition or etching or other processes used for creating the devices permits creation of very small, compact devices. Several benefits are realized by such integral manufacturing techniques, including: manufacturing costs are reduced; fewer I/O devices are needed; circuit paths are shorter resulting in lower power requirements, lower radiation levels and less electromagnetic noise generation; fewer circuit elements liable to fail means that reliability is increased.

Monolithic construction attainable with such unitary structures is more easily sealed against environmental influences. The benefits of such an improved semiconductor manufacturing capability at the fabrication (deposition or other process) level are especially significant in optical systems because various optical elements may be aligned within photolithographical tolerances – on the order of micrometers – to ensure alignment of optical elements such as waveguides, lasers, fibers and other elements. Connecting fibers and I/O terminations (e.g., I/O devices 118, 122, 132, 136, 138, 164, 168, 174 in FIG. 9) intermediate various optical elements, and their associated losses and other inefficiencies, may thereby be eliminated.

FIG. 10 is a schematic block diagram in plan view of a representative optical communication apparatus constructed according to the teachings of the present invention. FIG. 10 is not a representation of a particular optical communication apparatus. Rather, FIG. 10 illustrates advantages of using teachings of the present invention for implementations of various generically described devices in optical communication apparatuses. In FIG. 10, an optical communication signal handling apparatus 180 is monolithically fabricated in a unitary structure upon a common substrate 182. Preferably, common substrate 182 is a silicon substrate. In FIG. 10, optical communication signal handling apparatus 180 receives incoming signals at an optical input portal 184 and emits treated multiplexed output optical signals at an optical output portal 186. Signals traversing optical portals 184, 186 may be simplex signals (single channel signals) or may be complex signals (several signals at different frequencies or several signals, each encoded for identification). In the embodiment of apparatus 180 illustrated in FIG. 10, it is presumed that incoming signals received at optical input portal 184 are complex signals.

Incoming signals received at optical incoming portal 184 are received at an I/O (input/output) unit 185 to appropriately configure received signals for handling by an optical demultiplexer unit 188. I/O unit 185 is necessary because optical signals arriving at optical input portal 184 are first encountering apparatus 180. As will become apparent as FIG. 10 is described in further detail, signals handled

internally within apparatus 180 (i.e., within the monolithic integral structure of apparatus 180) do not generally require I/O units at each interface between devices. Demultiplexer unit 188 sorts out the various signals contained in the incoming signal received at optical input portal 184 into constituent signals and distributes resultant constituent signals to waveguides 190a, 190b, 190c, 190d (hereafter sometimes referred to as "190 (series)") to convey signals to optical signal modification units 192a, 192b, 192c, 192d (hereafter sometimes referred to as "192 (series)"). Waveguides 190 (series) may be implemented as optical fiber transmission devices. Alternatively, if optical demultiplexer 188 is appropriately aligned with optical signal modification units 192 (series), then waveguides 190 (series) may be omitted and optical signals may be directly transmitted between optical demultiplexer 188 and optical signal modification units 192 (series).

An electrical input signal is received by apparatus 180 at an electrical input node 194. Electrical input signals are received from input node 194 at an I/O device 196 to appropriately configure electrical input signals for handling by an electrical demultiplexer unit 198. Signals received at electrical input node 194 may be single channel signals or may be complex signals (several signals at different frequencies or several signals, each encoded for identification). In the embodiment of the optical communication signal handling apparatus 180 illustrated in FIG. 10, it is presumed that incoming signals received at electrical input node 194 are complex signals. Electrical demultiplexer unit 198 sorts out the various signals contained in the incoming signal received at electrical input node 194 into constituent signals and distributes resultant constituent signals to optical signal modification units 192 (series) via electrical conductors 200a, 200b, 200c, 200d (hereafter sometimes referred to as "200 (series)").

I/O device 196 is necessary because electrical signals arriving at electrical input node 194 are first encountering apparatus 180. As will become apparent as FIG. 10 is described in further detail, signals handled internally within apparatus 180 (i.e., within the monolithic integral structure of apparatus 180) do not generally require I/O units at each interface between devices.

By way of example, electrical signals conveyed via electrical conductors 200 (series) may be modulation signals that are employed by optical signal modification units 192 (series) to modulate optical signals received via waveguides 190 (series).

Optical signal modification units 192 (series) produce modified optical signals to waveguides 204, 210, 216, 222. Waveguide 204 branches to waveguides 206, 208. Waveguide 210 branches to waveguides 212, 214. Waveguide 216 branches to waveguides 218, 220. Waveguide 222 branches to waveguides 224, 226.

Waveguides 204, 206, 208, 210, 212, 214, 216, 218, 220, 222, 224, 226 convey modified optical signals to optical signal treating units 202a, 202b, 2026c, 202d, 202e, 202f, 202g, 202h (hereafter sometimes referred to as "202 (series)"). Waveguides 204, 206, 208, 210, 212, 214, 216, 218, 220, 222, 224, 226 may be implemented as optical fiber transmission devices. Alternatively, if optical signal modification units 192 (series) are appropriately aligned with respective optical signal treating units 202 (series), then waveguides 204, 206, 208, 210, 212, 214, 216, 218, 220, 222, 224, 226 may be omitted and optical signals may be directly transmitted between optical signal modification units 192 (series) and optical signal treating units 202 (series). Optical signal treating units 202 (series) may be, for example, signal smoothing units, or timing synchronization units, or buffer units, or another unit that treats optical signals to modify an aspect of the signals.

Optical signal treating units 202 (series) produce treated optical signals to waveguides 230a, 230b, 230c, 230d, 230e, 230f, 230g, 230h (hereafter sometimes referred to as "230 (series)") to convey treated optical signals to optical multiplexer 232. Waveguides 230 (series) may be implemented as optical fiber transmission devices. Alternatively, if optical signal treating units 202 (series) are appropriately aligned with optical multiplexer 232, then waveguides 230 (series) may be omitted and optical signals may be directly transmitted between optical signal treating units 202 (series) and optical multiplexer 232.

Optical multiplexer 232 provides multiplexed treated optical signals to an I/O unit 234. I/O unit 234 appropriately configures signals received from optical

multiplexer 232 for conveyance via optical output portal 186 to other parts of a communication network (not shown in FIG. 10) in which apparatus 180 is employed. I/O unit 234 is necessary because optical signals arriving at optical output portal 186 are first encountering the communication network in which apparatus 180 is employed.

A salient feature of apparatus 180 is the unitary construction employed in its fabrication. Respective elements of optical communication signal handling apparatus 180 are illustrated in FIG. 10 as physically displaced in order to facilitate understanding of the invention. In its preferred embodiment, respective elements of optical communication signal handling apparatus 180 are compactly arrayed upon substrate 182 according to the teachings of the present invention. Individual elements of optical communication signal handling apparatus 180 in FIG. 10 are substantially similar to selected elements of apparatus 110 (FIG. 9). For example, optical signal modification units 124 (FIG. 9) may be optical signal modification units 192 (FIG. 10). A significant difference between apparatus 110 (FIG. 9) and optical communication signal handling apparatus 180 (FIG. 10) is that the elements of apparatus 180 are monolithically fabricated upon a common substrate (preferably a silicon substrate). This feature of optical communication signal handling apparatus 180 is illustrated in FIG. 11.

FIG. 11 is a schematic block diagram in elevation view of the representative optical communication apparatus constructed according to the teachings of the present invention illustrated in FIG. 10. In FIG. 11, optical communication signal handling apparatus 180 is comprised of a plurality of elements arrayed upon a common silicon substrate 182. The elements are preferably monolithically fabricated as a unitary structure. Thus, optical demultiplexer 188, electrical demultiplexer 198, optical signal modification units 192 (series), optical signal treating units 202 (series) and optical multiplexer 232 are illustrated as being constructed in their preferred embodiment as a single integral structure substantially intimately situated and connected upon substrate 182.

FIG. 12 is a flow diagram illustrating the method of the present invention. In FIG. 12, the method for treating received optical communication signals to produce outgoing optical signals comprises the step of providing a plurality of optical signal handling devices implemented in a monolithic integrated structure arranged on a single substrate, as indicated by a block 250.

The method may include the further step of providing at least one electrically driven device for cooperating with selected optical signal handling devices of the plurality of optical signal handling devices to effect the treating, the at least one electrically driven device being implemented in the monolithic integrated structure, as indicated by a block 252.

The apparatus and method of the present invention provide many key attributes. For example, products may be manufactured more cheaply using the teachings of the present invention to photolithographically define apparatuses for implementation of a monolithic integration of components and functions in unitary products. The unitary products thus advantageously manufactured may embody entire functionality of an optical communication network node on a single chip. The embodiment on a chip may handle simple or complex functions, and may be employable in numerous varied applications in a network system.

The advantages of the present invention are achieved by the ability to grow thick layers (e.g., > 4000 Angstroms) layers of oxide on silicon with amorphous interface structures, that is, the ability to grow Group III – V or II – VI materials on silicon substrates. Employing such an ability with selective etching and re-growth techniques enables implementation of multi-functionality in products having unitary structure photolithographically defined on a single substrate. Among the advantages provided by such implementation are reduced numbers of interfaces between components, reduced losses and noise, reduced power consumption, simpler interface structures, lower cost of manufacture, smaller apparatus size, increased density of parts within apparatuses and other advantages. Among the other advantages is a capability to realize things not previously economically possible, such as monolithically integrated circuits employing both silicon technology and complex semiconductor material technology.

An example of an advantageous employment of the teachings of the present invention is implementing a Mach-Zehnder interferometer. A Mach-Zehnder interferometer is a common device for converting electronic signals to on-off keyed (modulated) optical signals in fiber networks. Using an electro-optic material (commonly Lithium Niobate), a square wave information signal may be employed to modulate the delay of an optical signal in an optical path sufficiently to effect cancellation by an undelayed version of the optical signal. This creates an interferometric, or interference, effect. When no voltage is applied to a Mach-Zehnder device whose path lengths are balanced, optical energy is constructively combined, and the light passed through at a maximum attainable power. When a particular voltage is applied to the device, the optical energy is destructively combined, and a minimal amount of optical power is transmitted. By applying an electrical voltage in such an alternating pattern, an on-off modulation effect is realized. The voltage level causing total destructive interference is called V-π, which is the voltage required to cause of phase shift of π radians. The modulating voltage signal is applied to the Mach-Zehnder interferometer by means of conductive metal electrodes deposited in some fashion on the surface of the lithium niobate. The power dissipation associated with driving these electrodes is proportional to required voltage. Further the associated capacitance of the electrodes will limit the data rate which may be effectively realized, and is a limiting factor when system speeds greater than 1 gigabit-per-second (Gbps) are used. Finally, the electrical losses associated with proper modulation levels of the lithium niobate modulators can be high enough to require the use of expensive line amplifiers. Integration of the required amplifiers would be beneficial, however the heat from such power dissipation prevents integration of more than a few light channels into a single device. This limitation of the number of light channels that can be integrated in to a single device has the effect of limiting the benefits of Dense Wavelength Division Multiplexing (DWDM); DWDM contemplates employment of 40 or more different wavelengths to facilitate 40 Gbps communication networks.

It would also be beneficial, for example in a DWDM system, to multiplex a 1 Gbps driver signal from several signal sources operating at speeds of 100 Megabits-per-second (Mbps) so that network distribution from several sources becomes practical. By using the advantages taught by the present invention, a silicon multiplexer may be used to advantage to form several 100 Mbps signals into one signal stream operating at 1 Gbps. By employing such a configuration, a 1 Gbps line driver of silicon or gallium arsenide can be configured to provide the electronic signal input for a Mach-Zehnder interferometer. Because such a line driver device is integrated on the same monolithic device as the multiplexer and the lithium niobate Mach-Zehnder, sub-picofarad line capacitances are realizable. As a result, a driver operating at a speed of 1-10 Gbps may be implemented that will dissipate less than 2 watts. Such a power-efficient implementation is useful for driving multiple DWDM modules.

Another example: the apparatus and method of the present invention may provide for fabricating a laser and a photodiode in proximity to each other. In such an embodiment VCSEL (vertical cavity surface emitting laser) technology may be grown on a silicon layer, and an adjacent photodiode may be fabricated on the same common silicon substrate in an appropriate material sensitive to the wavelength emitted by the laser. Horizontally (i.e., substantially parallel to the plane of the common substrate) emitting laser structures may be employed using the teachings of the present invention with equal advantage.

Optical communication signal handling apparatuses constructed in such a process-level unified construction as is taught by the present invention are better aligned, more compact, more reliable and robust, more readily protected against environmental influences (including electromagnetic noise), and generally more versatile and convenient in their employability for particular applications because of their lower power requirements and smaller size.

An important aspect of the present invention is the integration of functional process blocks in a subsuming multifunctional processing block (as is seen in FIGs. 9 and 10). The incoming signal or signals undergo some "treatment", such as to alter the signal itself (in the example of a modulator), alter the arrangement

of the information carried by the processing block (as in the example of multiplexing or demultiplexing wavelengths), or to groom the signal in some fashion so as to increase the usefulness in the overall communication system (as in the example of integration of electrical or optical gain).

In the case of multiple input signals, each of which is to undergo some individual treatment which may be a combination singly or in multiples of those described above, the method by which the integration can be effected is multi-dimensional.

In a simple one dimensional integration, the individual signals are acted upon (treated) by each of the several functional blocks in sequence as the signal propagates through the multifunctional processing block. A first alternative structure provides a one dimensional integration in which the several signals (either individually or in groups comprising subsets of the plurality of incoming signals) are acted upon by one or more functional process blocks in parallel. All signals in the set or subset may be acted upon (treated) simultaneously in a given functional block. The output of such parallel process functional blocks may be input to subsequent parallel process functional blocks or input to sequential individual process blocks, as described above. In such manner multiple processes may be integrated in an apparatus in a one dimensional fashion: either temporally as the signal progresses through the multifunctional processing block, or spatially in sets or subsets defined however a system designer requires for a particular application.

The extension of this integration into a multi-dimensional case follows by combinations of the spatial and temporal directions of integration described above. As an example, consider a subset of the incoming signals which are treated in a first functional process block which includes both aspects of parallel and serial processing. As a specific example, consider wavelength division multiplexed signals which are amalgamations of individual time division multiplexed streams. The wavelengths may be separated and the time slot information extracted for subsequent re-assembly in time (and then wavelength) on the basis of common destination, quality of service level guarantees, load balancing, or other

provisioning, such as packet labeling. This particular subset of signals may itself be treated in a serial or parallel fashion with other individual signals, sets of signals or subsets comprising groups of signals. The net result is a complex multifunctional process block, the individual single functional process blocks of which are combined in serial, parallel, or logical configuration whose purpose is the treatment of the input signals as previously described. The treatments may be electrical or optical in nature.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential features or elements of any or all the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.

CLAIMS

We claim:

1. An apparatus for effecting selected aspects of optically conveyed communications; the apparatus treating at least one incoming optical signal to produce at least one treated outgoing optical signal; the apparatus comprising a plurality of optical signal handling devices; said plurality of optical signal handling devices being implemented in a monolithic integrated structure arranged on a single substrate.

2. An apparatus for effecting selected aspects of optically conveyed communications as recited in Claim 1 wherein the apparatus further comprises at least one electrically driven device; said at least one electrically driven device cooperating with selected optical signal handling devices of said plurality of optical signal handling devices to effect said treating; said at least one electrically driven device being implemented in said monolithic integrated structure.

3. An apparatus for effecting selected aspects of optically conveyed communications as recited in Claim 2 wherein said plurality of optical signal handling devices includes at least one active optical signal handling device and at least one passive optical signal handling device.

4. An apparatus for effecting selected aspects of optically conveyed communications as recited in Claim 3 wherein said selected optical signal handling devices include said at least one active optical signal handling device.

5. An apparatus for effecting selected aspects of optically conveyed communications as recited in Claim 4 wherein said plurality of optical signal

handling devices and said at least one electrically driven device are integrally configured substantially in a monoplanar configuration.

6. An apparatus for effecting selected aspects of optically conveyed communications as recited in Claim 4 wherein said plurality of optical signal handling devices and said at least one electrically driven device are integrally configured among a plurality of planar configurations.

7. An apparatus for effecting selected aspects of optically conveyed communications as recited in Claim 1 wherein said plurality of optical signal handling devices includes at least one active optical signal handling device and at least one passive optical signal handling device.

8. An apparatus for effecting selected aspects of optically conveyed communications as recited in Claim 7 wherein said plurality of optical signal handling devices are integrally configured substantially in a monoplanar configuration.

9. An apparatus for effecting selected aspects of optically conveyed communications as recited in Claim 7 wherein said plurality of optical signal handling devices are integrally configured among a plurality of planar configurations.

10. An apparatus for effecting selected aspects of optically conveyed communications as recited in Claim 7 wherein said selected optical signal handling devices include said at least one active optical signal handling device.

11. An apparatus for effecting selected aspects of optically conveyed communications as recited in Claim 10 wherein said plurality of optical signal

handling devices are integrally configured among a plurality of planar configurations.

12. A method for manufacturing an apparatus for treating received optical communication signals to produce treated outgoing optical signals, the method comprising:

providing a monocrystalline silicon substrate;

depositing a monocrystalline perovskite oxide film overlying the monocrystalline silicon substrate, the film having a thickness less than a thickness of the material that would result in strain-induced defects;

forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline silicon substrate;

epitaxially forming a monocrystalline compound semiconductor layer overlying the monocrystalline perovskite oxide film;

forming, using at least part of the monocrystalline compound semiconductor layer, at least a first optical signal handling device capable of receiving an incoming optical signal and a second optical signal handling device capable of outputting a treated optical signal.

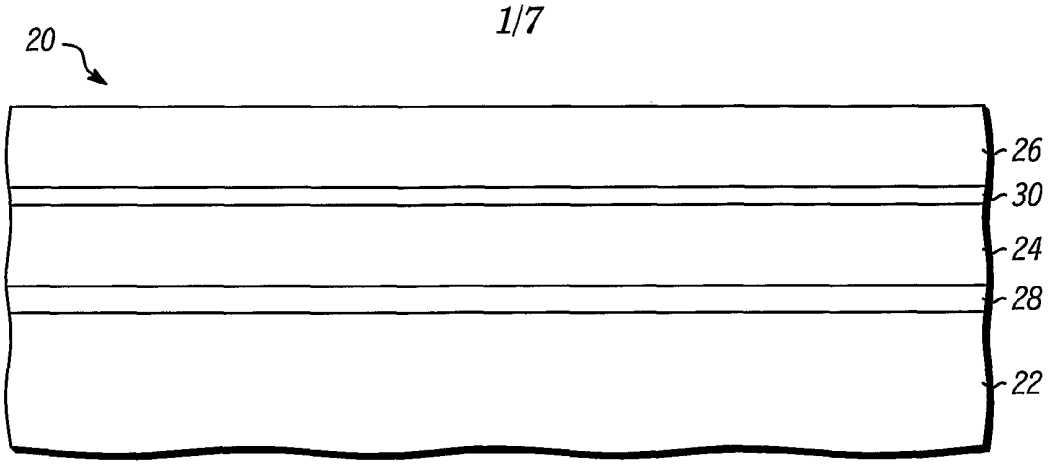


FIG. 1

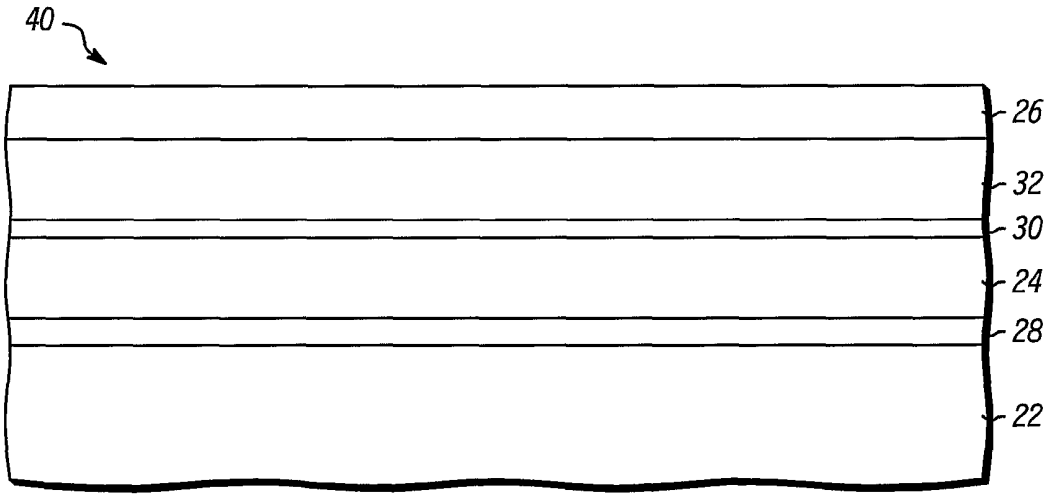


FIG. 2

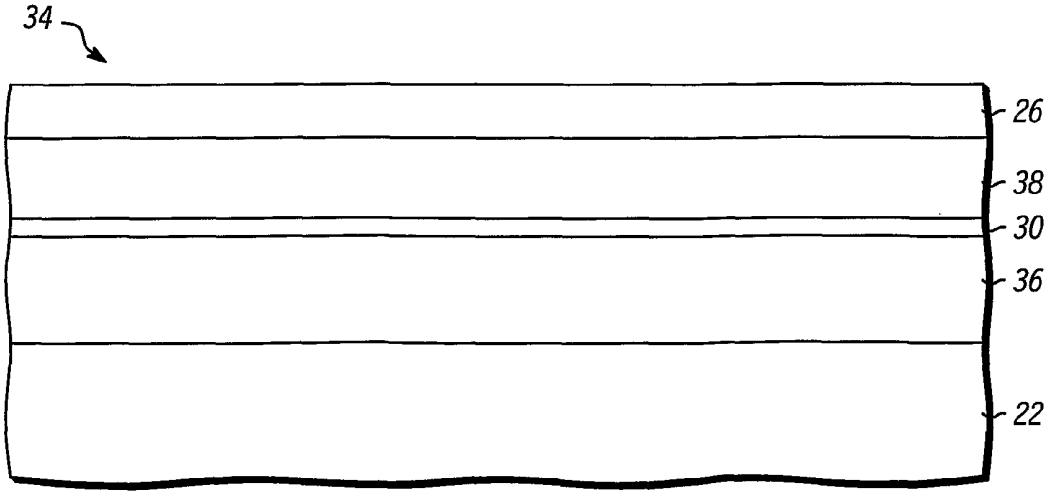


FIG. 3

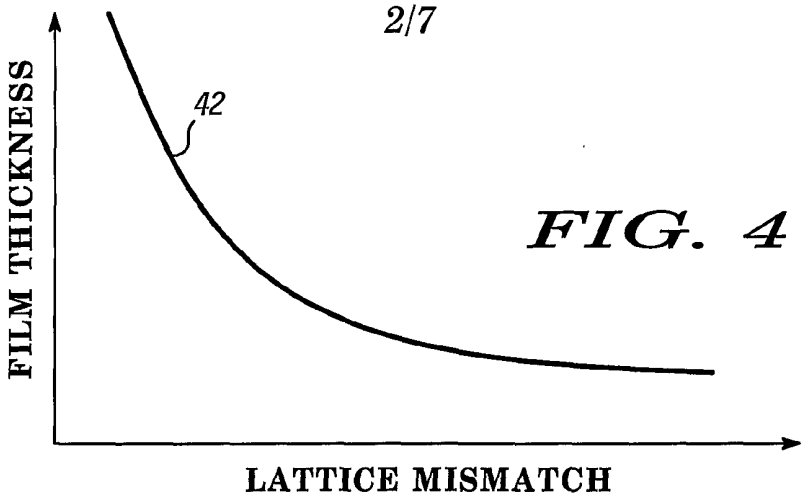


FIG. 4

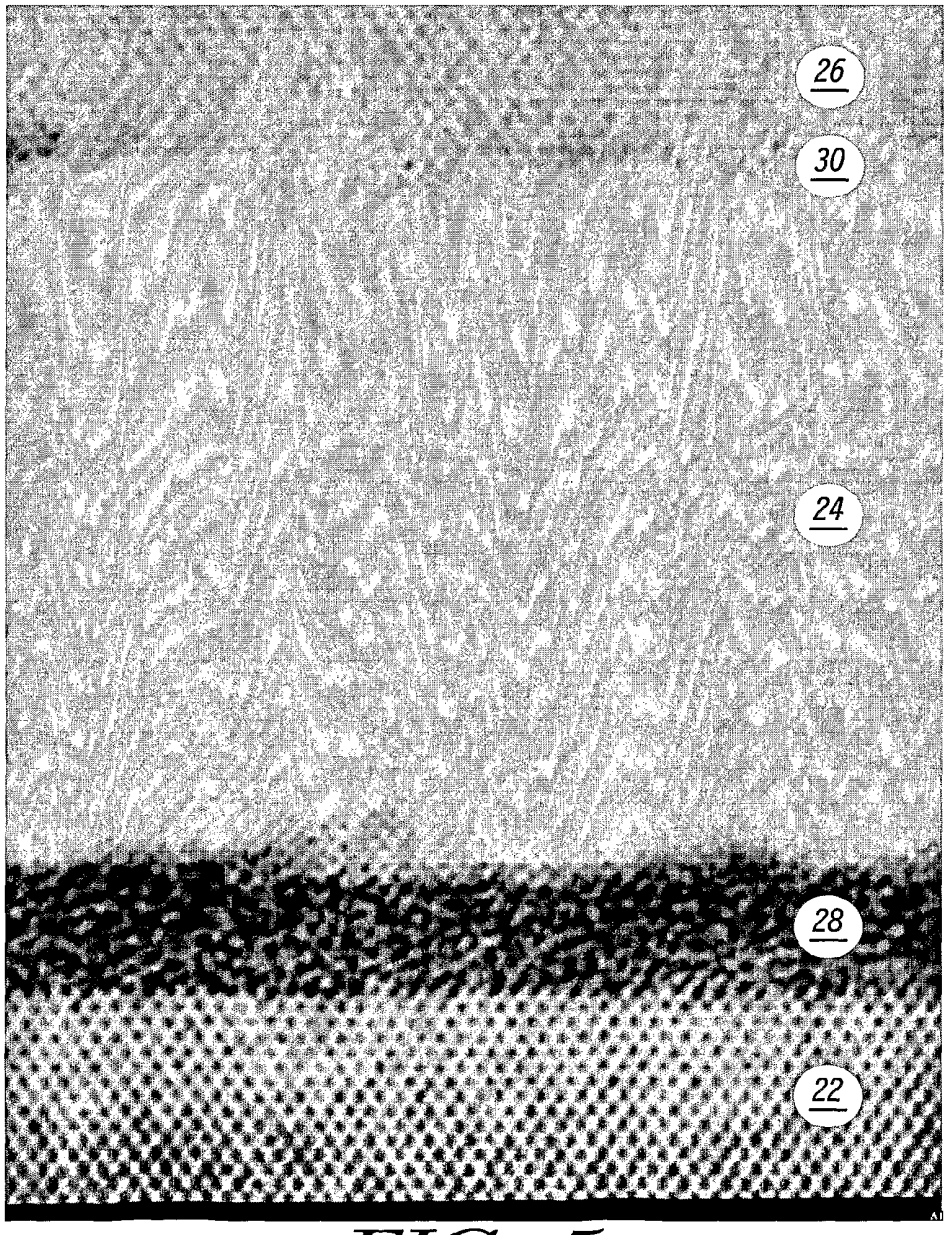
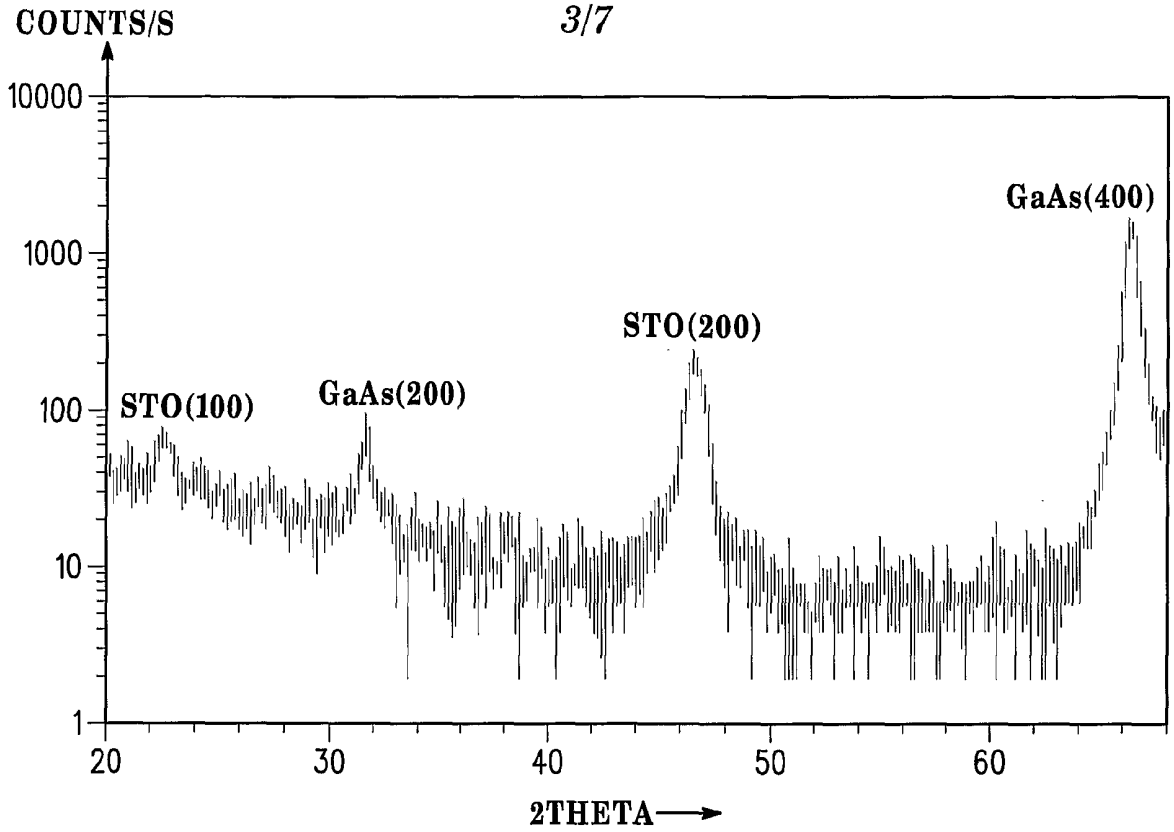


FIG. 5


COUNTS/S
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1000
100
10
1
20
30
40
50
60
2THETA
STO(100)
GaAs(200)
STO(200)
GaAs(400)

FIG. 6

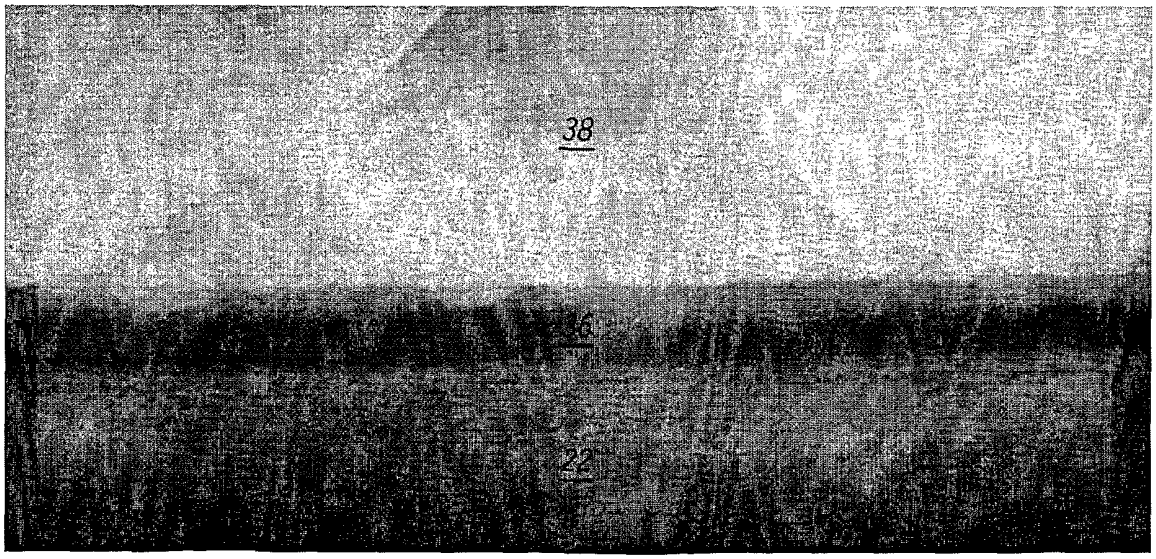
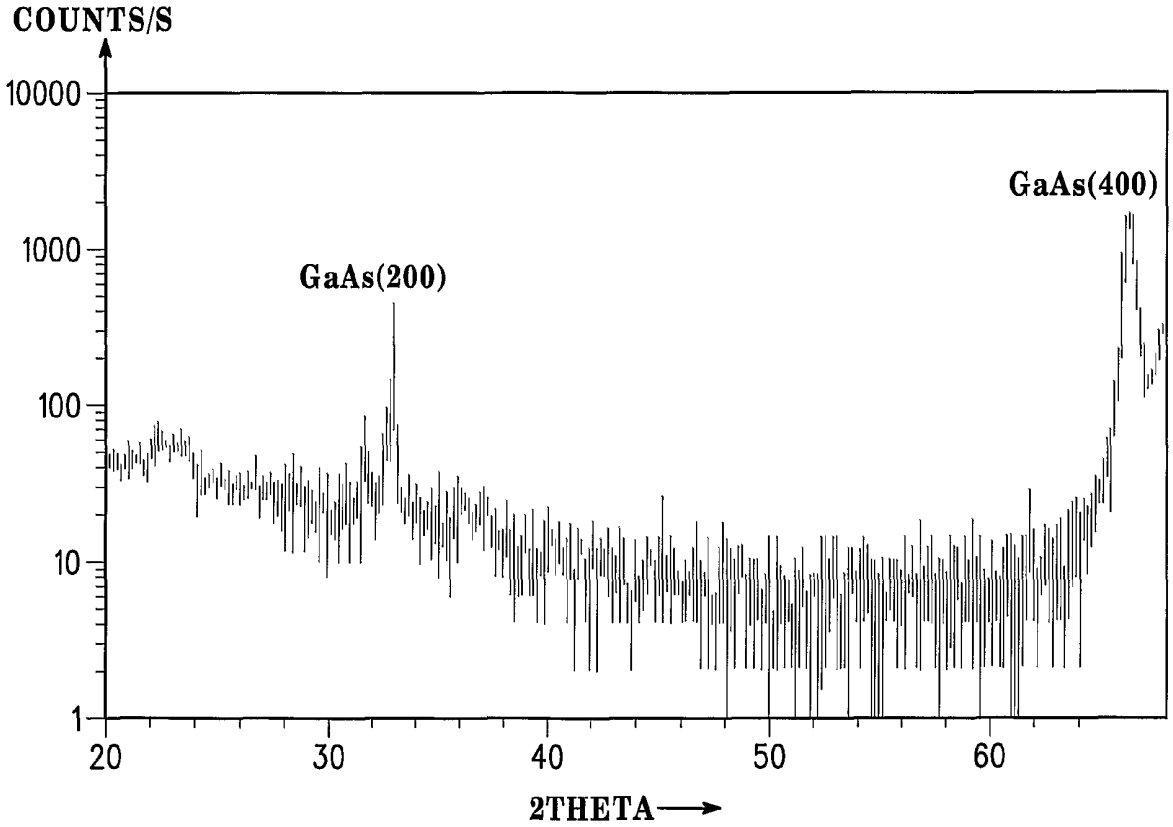

38
36
22

FIG. 7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GaAs(200)
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40
50
60
2THETA

FIG. 8

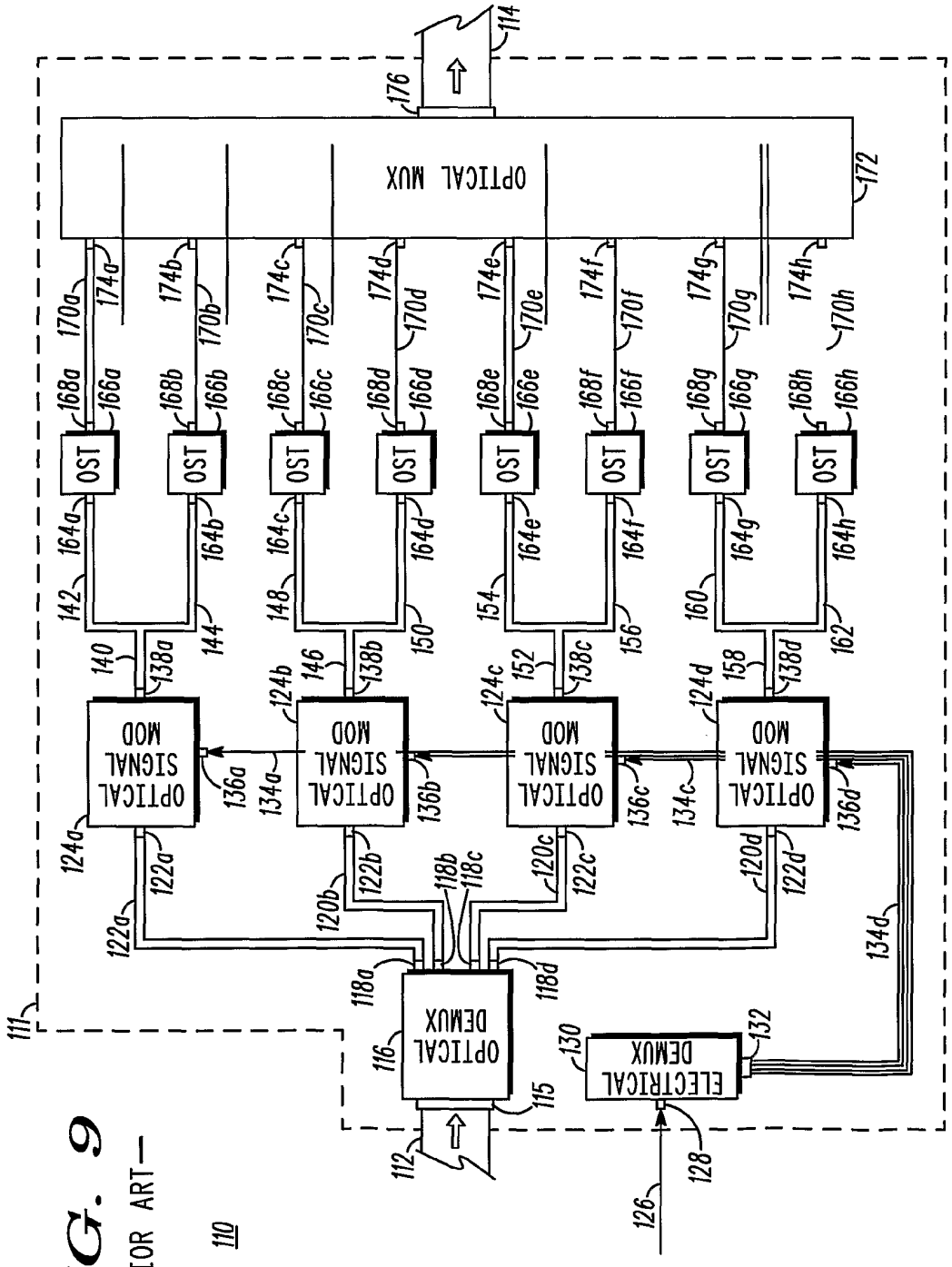

FIG. 9
—PRIOR ART—

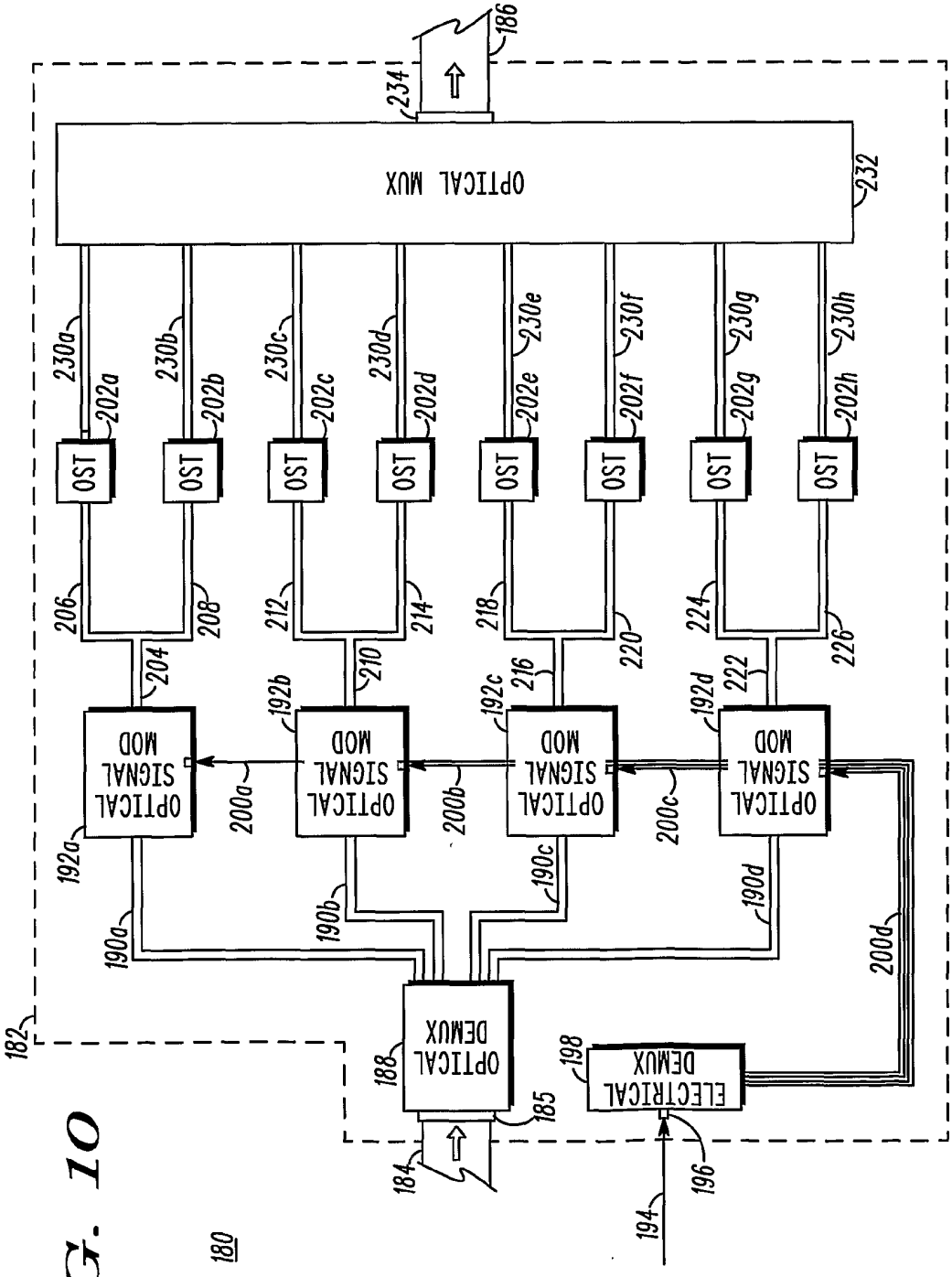
OPTICAL MUX
OST
OPTICAL SIGNAL MOD
OPTICAL DEMUX
ELECTRICAL DEMUX

FIG. 10

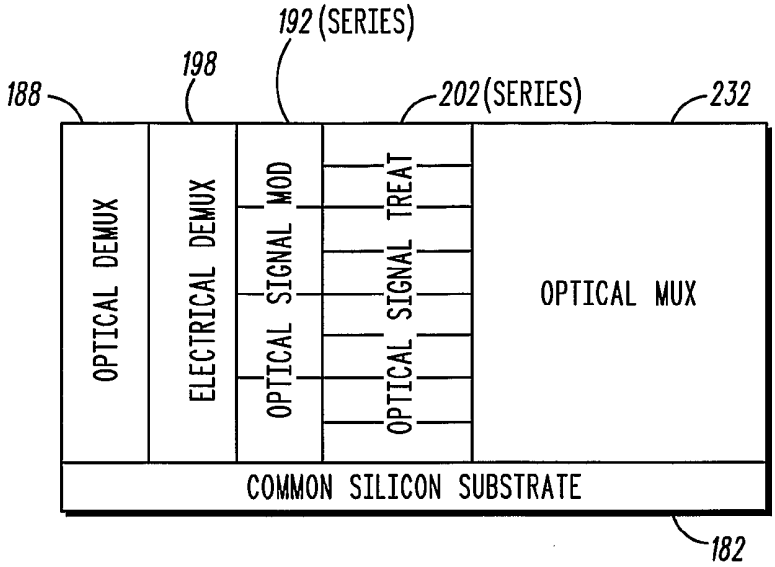
192 (SERIES)
198
188
202 (SERIES)
232
OPTICAL DEMUX
ELECTRICAL DEMUX
OPTICAL SIGNAL MOD
OPTICAL SIGNAL TREAT
OPTICAL MUX
COMMON SILICON SUBSTRATE
182

FIG. 11

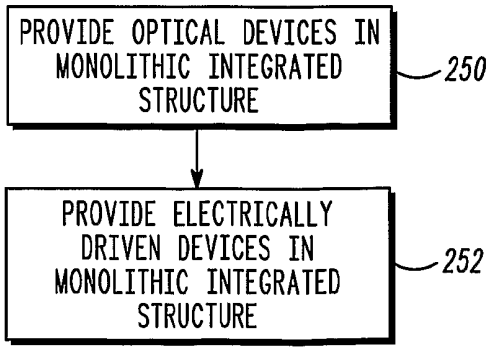
PROVIDE OPTICAL DEVICES IN MONOLITHIC INTEGRATED STRUCTURE
250
PROVIDE ELECTRICALLY DRIVEN DEVICES IN MONOLITHIC INTEGRATED STRUCTURE
252

FIG. 12