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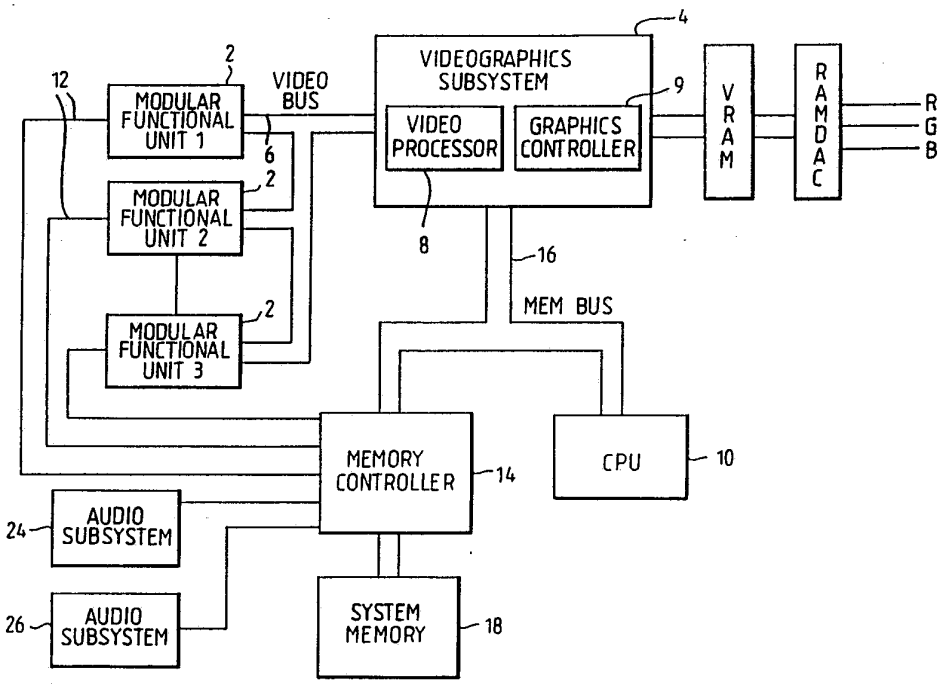

(57) Abstract

A computer which is capable of displaying both video and graphical data is provided with a central processing unit (10), a memory controller (14), and a display system (4). These units are all connected to a bus (16). Modular functional units (2), e.g. video codecs, TV outputs, audio subsystems, are used to provide optional additional functions for the display system. A coupling means (6, 12) is provided to link the modular functional units to the display system (4) and to the memory controller (14).

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MULTIMEDIA DISPLAY

FIELD OF THE INVENTION

This invention relates to computers and in particular to computers which can display both video and graphics data.

BACKGROUND OF THE INVENTION

Historically, computer systems have been designed and produced without careful considerations for video and to a lesser extent audio capabilities. Many systems have been produced that add video capability to the computer system by colour keying and analogue multiplexing of the computer's graphics output. For example US Patent No. 5,027,212. Such systems generally involve multiple frame buffers holding video and graphics data separately. More recently a unified approach based on a single frame buffer of the type described in our International Patent Application No. PCT GB9202164 has been adopted. This approach treats video and graphics in exactly the same way. The single frame buffers can be based on either triple port memories or time multiplexing of video and graphics data on a common bus using suitable rate buffering and arbitration as described in the above numbered International patent application.

These techniques can be or have been used to integrate video into a computer display system. However, to date, such integration has been carried out within the constraints of the available personal computers and workstations. This has meant that such systems are costly and bulky and have limited expandability.

SUMMARY OF THE INVENTION

In preferred embodiments of this invention a conventional graphics subsystem is closely coupled with a video processing subsystem capable of performing a number of essential functions described below. Both graphics and video processing subsystems have access

to the shared frame buffer via the techniques described in International patent application no. PCT GB9202164. The combination consistutues a "videographics" subsystem which caters for cost effective and modular multimedia enablement.

Preferred embodiments of this invention seek to remove these limitations by moving to a computer architecture which takes the multimedia requirements into account in the initial system architecture.

Four preferred embodiments provide architectural structures that allow compact and cost effective multimedia computer systems to be constructed and configured. The modularity is achieved by equipping the base computer system with the required expansion capabilities and basic services allowing easy and cost effective addition of special function modules for multimedia capability. In particular the proposed architecture caters for the inevitable trend towards very compact personal computers.

The proposed systems take into account the need to add efficiently special function modules, such as video codecs, (coder/decoders), still image compression, analogue video input, TV output and audio subsystems to a modern computer system. Four architectures are described. The first approach includes a videobus for moving high speed data between various functional modules and an integrated frame buffer. The integrated frame buffer combines the normal computer graphics with the video data. The functional modules are centrally controlled and fed with control signals and compressed data over a serial communications system. The second approach replaces the parallel videobus with a collection of additional point-to-point serial communications between the graphics subsystem and the functional modules. The third approach is a further extension of the first approach in that it combines the functionality of the high speed video bus with that of the serial connections carrying control/compressed data. In this aproach a single bus connects the various functional modules to the

graphics/video subsystem. This single bus carries both data and control tokens which can include uncompressed and compressed video/audio data, set up and configuration data as well as other control data.

The fourth approach further combines the multimedia bus described in the third approach with the main computer bus. In this approach the single system bus will require to have both the necessary bandwidth and the real time capabilities required in a multimedia environment. All approaches partition the architecture in such a way as to both maximise system performance and minimise system cost by proper exploitation of silicon integrated trends.

The invention is defined in the appended claims to which reference should now be made.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will now be described in more detail, by way of example, with reference to the accompanying drawings in which:

Figure 1 shows a first computer system embodying the invention;

Figure 2 shows a second computer system embodiying the invention;

Figure 3 shows a third computer system embodying the invention;

Figure 4 shows a computer system, which modifies the embodiment of Figure 1; and

Figure 5 shows a fourth embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Videobus Based Architectures

In this approach, as shown in Figure 1, a plurality of modular functional units 2 are directly coupled to and communicate with a computer's graphics subsystem 4 via a videobus 6. The base

graphics subsystem includes a video processing unit 8, for carrying out processes such as format conversions (e.g. YUV to RGB etc.) and scaling functions along with a graphics controller 9 and circuits for combining video and graphics data in a frame buffer. An important feature of the proposed architectures is the incorporation of a number of video functions performed by the video processing unit in the normal computer graphics subsystem. These additional capabilities include but are not limited to:

1. Video scaling which allows the incoming video to be enlarged or scaled down before it is written into the shared frame buffer. The scaling down can be carried out using techniques covered in US Patent No. 5027212. The scale up can use techniques such as bilinear interpolation.

2. Video format conversion which supports conversion between various YUV and RGB video streams before the video data is written to the frame buffer. The particular formats of interest are YUV 422, YUV 411, YUV 444, RGB 24, RGB 16 (5,5,5 and 5,6,5) and RGB 8. The format conversion allows a degree of data compression as YUV format is denser than the conventional RGB. Also direct support for YUV allows lowcost interfacing to video digitisers which generally rely on YUV format. Also software video codecs can benefit from hardware support for their format conversion and scaling requirements. The format conversion can be done using a general 3x3 matrix multiplier architecture and conventional interpolating and decimating functions.

3. Video windowing which allows certain video pixels to be written to specific areas within a shared frame buffer and certain video pixels to be masked so that they are not loaded into the frame buffer. This will allow complex video windows and graphics overlays to be displayed in the graphics buffer.

4. A possible capability of the video processing system which is

closely coupled to the graphics subsystem is the concept of pixel masking. This capability can be supported two ways. One is where a mask bit is supplied by a modular function unit along a pixel stream. This mask bit determines whether a pixel is displayed or thrown away as it enters the shared frame buffers. The alternative approach is based on the video subsystem accessing a mask plane in the graphics memory and depending on the state of the mask bit update the shared frame buffer with the pixel data or not.

5. The video processing unit can access the graphics data and colour key the video by choosing a graphics colour for deciding whether a pixel in the shared frame buffer is overwritten by the incoming pixel stream.

6. The video processing unit has a decompression capability whereby it can decompress streams that it receives over the video bus or from the host via the graphics subsystem. This is necessary where video data has been stored in compressed form and is known as software playback of data.

7. All the features in 1-6 above can be accessed in software as an extension to graphics capabilities.

8. The video processing subsystem and the graphics subsystem both have access to a shared frame buffer. The techniques used to achieve this are described in International patent aplication no. PCT GB9202164 where a small amount of buffer is provided for the video channel to deal with the real time needs and the shared memory is arbitrated between the packetised video and the graphics controller. The buffer on the video channel allows critical activities such as memory refresh and screen updates to be carried out while the video data is collected in the buffer. During non critical graphics activites the video buffer is emptied into the shared frame buffer while the graphics controller is kept in an inactive state.

9. The video processing unit has an address generation unit allowing it to address the shared frame buffer in the required manner.

10. The video processing unit can also output proportions of the shared frame buffer with optional processing such as scaling to the video bus. A video encoder can be used to convert such regions of interest to a TV signal.

There are two main reasons for including the video postprocessing unit 8 as a central resource in the graphics/video (videographics) subsystem. One reason is that functions such as scaling and format conversion often result in an increase in bandwidth. By including these functions as a postprocessing activity in the graphics/video subsystem, the actual required bandwidth between the modular functional units and the graphics/video subsystem is minimised. This results in a much less complex videobus specification and demands less performance from the videobus. The second reason for the inclusion of the video processing unit as a central resource in the graphics/video subsystem is that all the modular functional units 2 can share this resource which results in simplifications in these units, and hence cost reduction.

The scaling operation can compensate for aspect ratio differences between a computer display and the incoming video signal as well as up/down scaling of the video to fit users requirements.

The modular functional units communicate with a CPU 10 and are controlled via a collection of serial connections 12. These serial connections originate from a memory controller 14 and each connects to an individual modular functional unit 2. The CPU 10, the memory controller 14 and the graphics subsystem 4 are the three main elements of the base computer that are tightly coupled over a high performance bus 16 (Mem Bus). The memory controller 14 supports memory accesses to a system memory 18 originating from the CPU 10

and from the graphics subsystem 4 as well as providing direct memory access (DMA) channels via the serial connections 12 to the modular functional units 2. This arrangement effectively decouples the tightly coupled CPU/memory/graphics subsystems from the optional and the more loosely coupled multimedia functional units 2.

The independent DMA support, via the memory controller, for these modular functional units 2 ensures that the real time needs of these units are met without frequent intervention from the CPU 10.

This approach also reduces the complexity of the support software needed in the system. This is particularly so since the DMA capability and the intelligence level of the memory controller unit can be modified towards a balanced operation.

Each modular functional unit 2 can read from or write to a relevant region of interest in a display buffer within the video/graphics subsystem 4. Mask planes in the graphics subsystem are used to control active areas associated with each video window. The access of the functional units 2 to the shared videobus is time multiplexed. The protocol for this multiplexing can be sub-line, line or region oriented. The exact choice will vary the extent of the buffering needed in each functional unit and the degree of context required in the video processing unit.

Examples of the modular functional units include video Digitisers, TV Encoders H261 video conferencing module, MPEG decoder and JPEG still image coders/decoders.

An enhanced version of the system is shown in Figure 2, where the memory controller 14 incorporates an intelligent router 22 which allows functional units 2 to communicate with each other directly. In this system by simply adding headers to data packets travelling on the serial links, the router will be able to set up dynamic circuits between various modules without interfering with the CPU

or the system memory.

Alternatively, the point-to-point connections between the memory controller and the functional units 2 can be replaced with a single serial bus (not illustrated). Such a system will of course offer lower performance.

Also as shown in Figure 1, the architecture easily allows inclusion of an audio subsystem 24 (digital signal processor, DSP) via a serial connection. In fact the DMA driven serial connections originating from the memory controller offer an ideal mechanism for adding other key subsystems such as disk 26 (or disk arrays) as demonstrated in Figure 1.

Networking (LAN's, MAN's, WAN's) interfaces can also be added to the system in a similar manner. Again the impact of these options on the CPU will be minimal as any real time transaction can take place via the memory control with little CPU intervention.

Direct Architecture

In this second approach the videobus is replaced with multiple point-to-point serial connections 28 between the functional units 2 and graphics/video subsystem 4. This is shown in Figure 3. In this approach the video processing unit will sufficiently buffer the data arriving from or leaving on each serial connection. The video post processing (format conversion/scaling) is then carried out on a time multiplexing basis. Leaving the format conversion and scaling function to the graphics/video subsystem 4 (as compared to the operation being done by individual functional units) ensures minimisation of the data rate requirement for the serial connections 28.

The basic operation of this approach is very similar to that described for the videobus based architecture. The advantage of the Direct Architecture is in minimisation of parallel buses. This has three major benefits:

1. A very compact base machine can be provided.

2. Much better utilisation of space on optional functional units is possible by virtue of avoiding large connector areas; and

3. Real-time performance requirement can be addressed in a much easier way as various activities are highly decoupled.

It is proposed that the systems embodying the invention can be provided such that each block shown in the figures can be provided on a single chip thereby enabling a very compact computer to be produced. Thus all that is needed is a chip for the CPU, a chip for the graphics/video subsystem, and a chip for the memory controller/router. Alternatively all may be provided on a single chip or combinations of the various units may be provided on single chips.

MULTIMEDIA BUS APPROACH

In Figure 4 there is shown a further extension of the embodiment of Figure 1 in which the videobus 6 and serial connectors 12 of the system of Figure 1 are combined into a single multimedia bus 30 which carries both data (video, audio, compressed and uncompressed), and the control information previously transmitted by serial connectors 12 of Figure 1. This has all the advantages associated with a combined graphic and video subsystem, capable of video scaling and format conversion.

The multimedia bus 30 operates in a time sharing mode using a packetised data/control protocol. The exact nature of the protocol employed is not critical to the present invention and various options will be known to those skilled in the art. All that is

required is an arbitration and scheduling scheme which can allocate sufficient bandwidth to each device and guarantee a worst case latency in operation. Such an approach allows the real time need needs of the system to be met. For example, a round robin scheduler allocating different amounts of time to each device can both provide the bandwidth in a predetermined way and obtain a worst case system latency. Multiple priorities can be added to the scheduler to allow a reduced latency figure for those devices which are allocated a higher priority.

SINGLE BUS APPROACH

A fourth approach illustrated in Figure 5 combines the multimedia bus of Figure 4 with the main computer bus. This gives a system bus 32 coupling the videographics subsystem 4, CPU 10, and the modular functional units 2. The main requirement of this combined system bus is that it should be capable of real time operation. Thus it must be able to operate in such a way as to be able to allocate sufficient bandwidth to each device and to guarantee a worst case latency. Preferably it operates using the same type of packetised data/control protocol as that referred to with reference to Figure 4. Again the videographics subsystem is capable of video scaling and format conversion and thus possesses all the advantages described with reference to Figure 1.

In all of the above cases the integration of the video processing subsystem and the graphics subsystem into a single videographics subsystem capable of performing both graphics and video functions (scaling, format, conversion, windowing and masking) is an important part of the proprosed invention. The functionality of the graphics and the video processing, sharing the same frame buffer, can be implemented in any one of many VLSI devices.

CLAIMS

1. A computer for displaying both video and graphical data comprising a central processing unit (CPU), a memory controller and a display system all connected to a bus and means for coupling at least one modular functional unit to the memory controller and to the display system.

2. A computer according to claim 1 in which the display system incorporates a video processing means.

3. A computer according to claim 2 in which the modular functional units access the graphics system via the video processing means.

4. A computer according to claim 1, 2 or 3 in which the coupling means comprise bidirectional connections between the functional unit and the display system.

5. A computer according to claim 1, 2, 3 or 4 in which the modular functional units make time multiplexed accesses to the display system.

6. A computer according to any preceding claim in which the coupling means comprises a plurality of point to point connections for coupling the memory controller to modular functional units.

7. A computer according to any of claims 1 to 5 in which the coupling means comprises a second bus means for coupling the memory controller to modular functional units.

8. A computer according to any preceding claim in which the coupling means comprises a plurality of point to point connections for coupling the display system to modular functional units.

9. A computer according to any of claims 1 to 7 in which the

coupling means comprises a third bus means for coupling the display system to modular functional units.

10. A computer according to any preceding claim in which the memory controller is coupled to a fourth bus means for accessing a memory means.

11. A computer according to any preceding claim in which the memory controller provides memory accesses in response to signals from the CPU and from the display system.

12. A computer according to any preceding claim in which the memory controller includes routing means whereby modular functional units may communicate with each other.

13. A computer according to claim 1 in which the CPU, the memory controller, and the display system are each provided on a separate integrated circuit.

14. A computer according to claim 1 in which at least two of: the CPU; the memory controller; and the display system, are provided on a single chip.

15. A computer according to claims 1, 2 or 3 in which the coupling means comprise a multimedia bus linking the functional units to the display system and the first bus which links the display system to the memory controller.

16. A coputer according to claim 15 in which the multimedia bus operates in a time sharing mode for the transmission of data and control signals.

17. A computer according to claims 1, 2 or 3 in which the coupling means comprises the bus to which the functional units are also connected.

18. A computer according to claim 17 in which the bus is a multimedia bus.

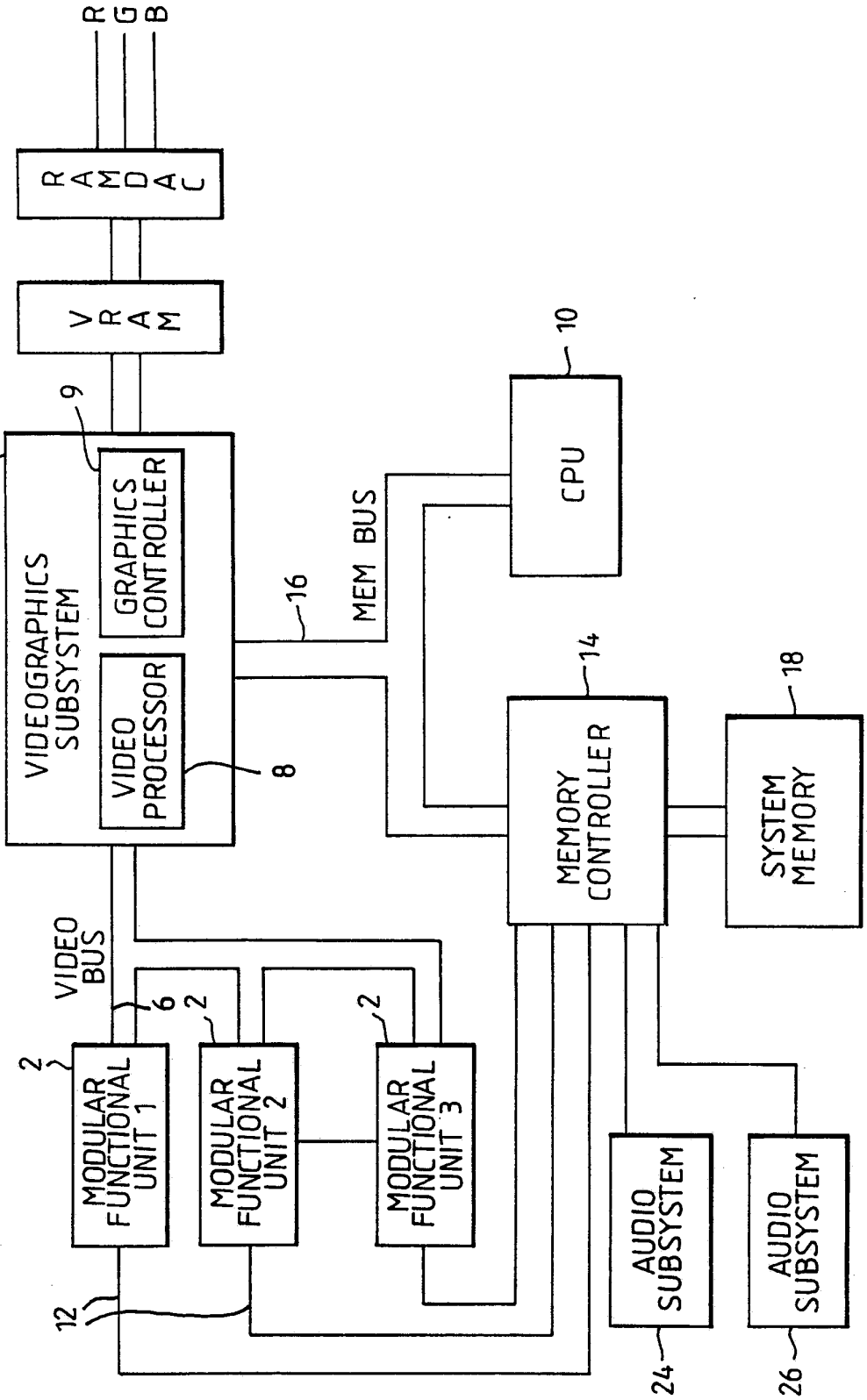
19. A computer according to claim 18 in which the bus operates in a time sharing mode for the transmission of data and control signals.

20. A computer according to claim 2 in which the video processing means comprise video scaling means.

21. A computer according to claims 2 or 20 in which the video processing means comprise video format conversion means.

22. A computer according to claims 2, 20 or 21 in which the video processing means comprise masking means to protect areas of a frame buffer associated with the display system.

23. A computer according to claim 2, 20, 21 or 22 in which the video processing means comprises decompression means for software playback of data.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VRAM
4
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GRAPHICS CONTROLLER
VIDEO PROCESSOR
8
16
MEM BUS
10
CPU
14
MEMORY CONTROLLER
18
SYSTEM MEMORY
VIDEO BUS
6
2
2
2
MODULAR FUNCTIONAL UNIT 1
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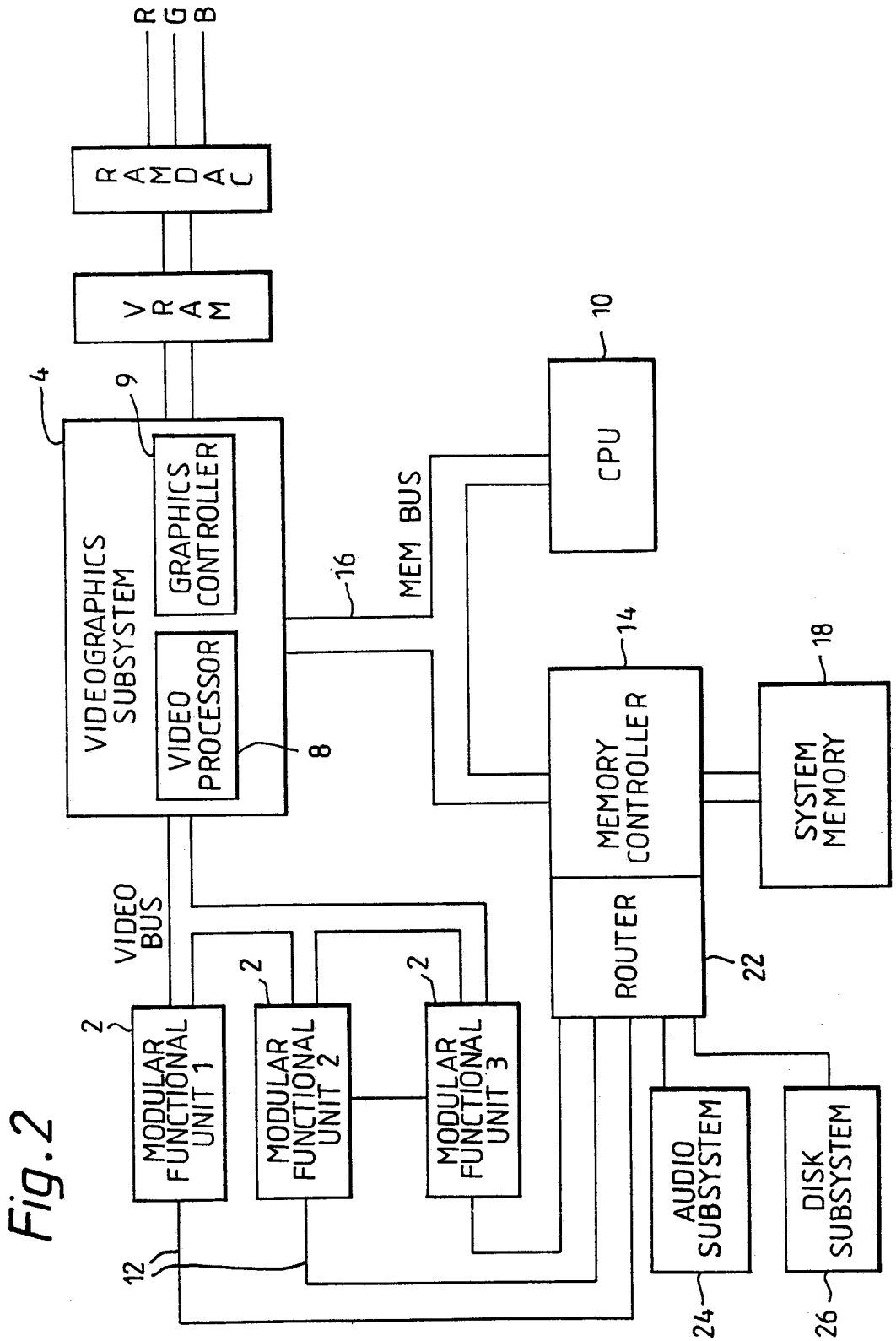
MODULAR FUNCTIONAL UNIT 3
12
AUDIO SUBSYSTEM
AUDIO SUBSYSTEM
24
26

Fig.1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VIDEO BUS
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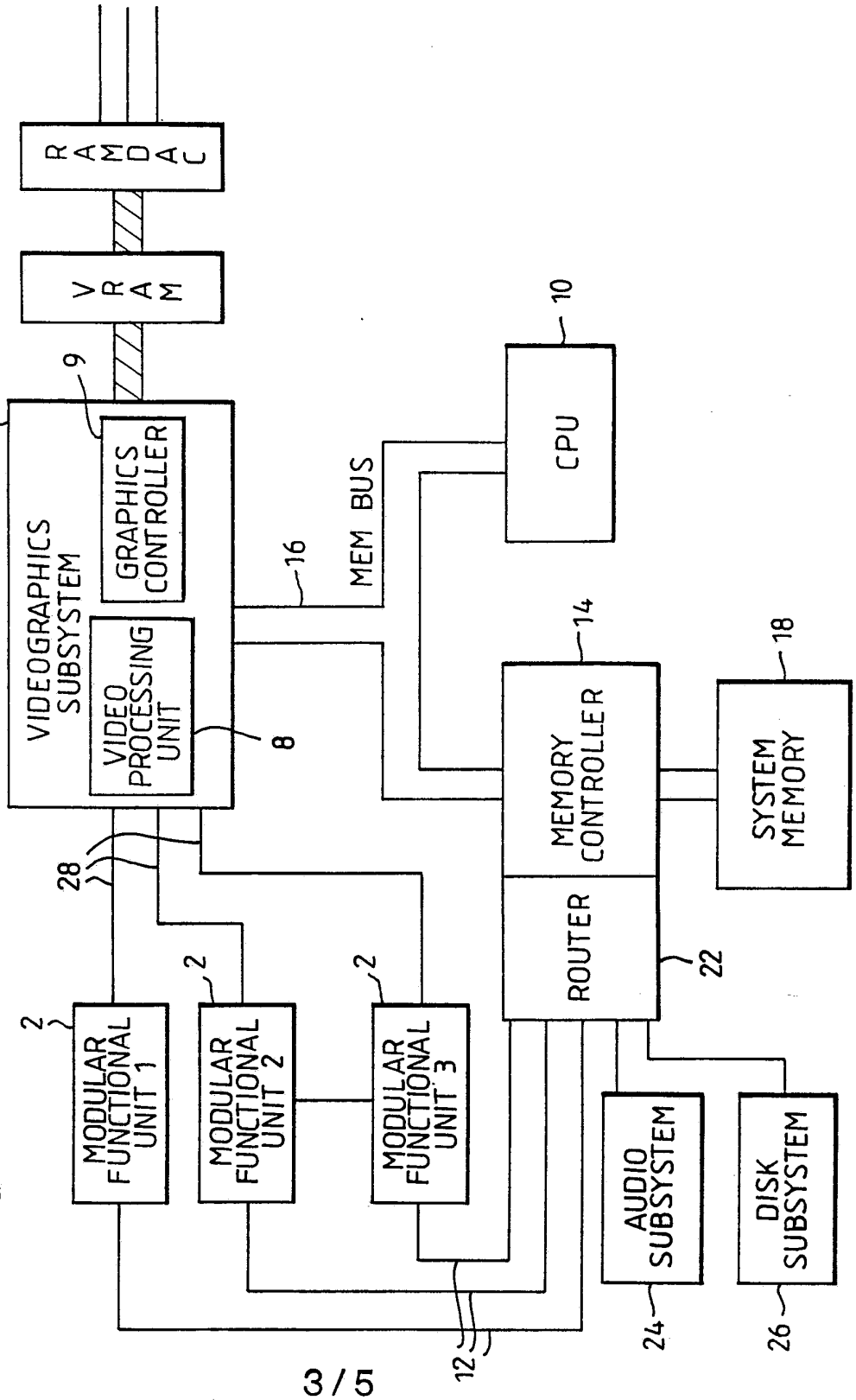
AUDIO SUBSYSTEM
24
DISK SUBSYSTEM
26

Fig.2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MODULAR FUNCTIONAL UNIT 3
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DISK SUBSYSTEM
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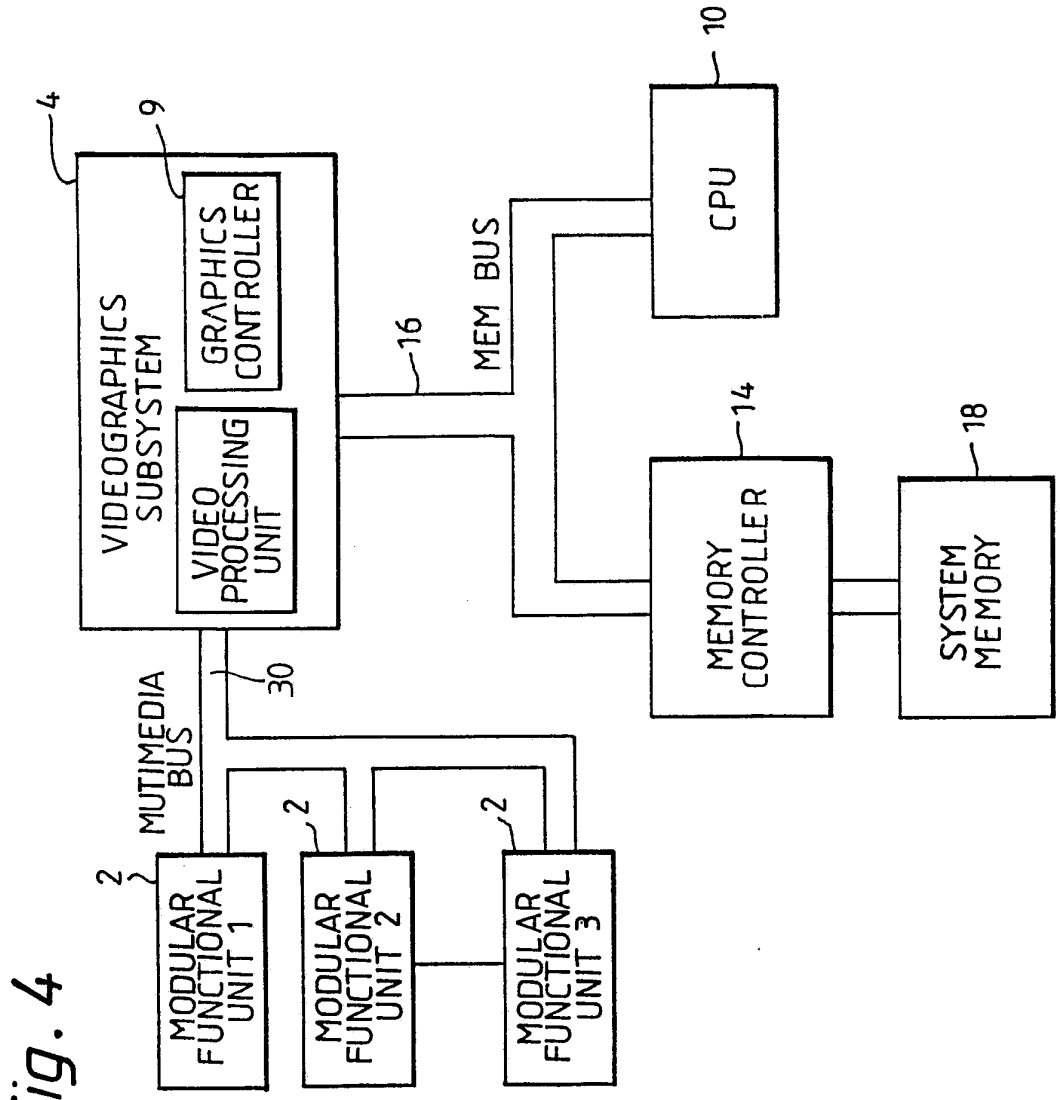
Fig. 3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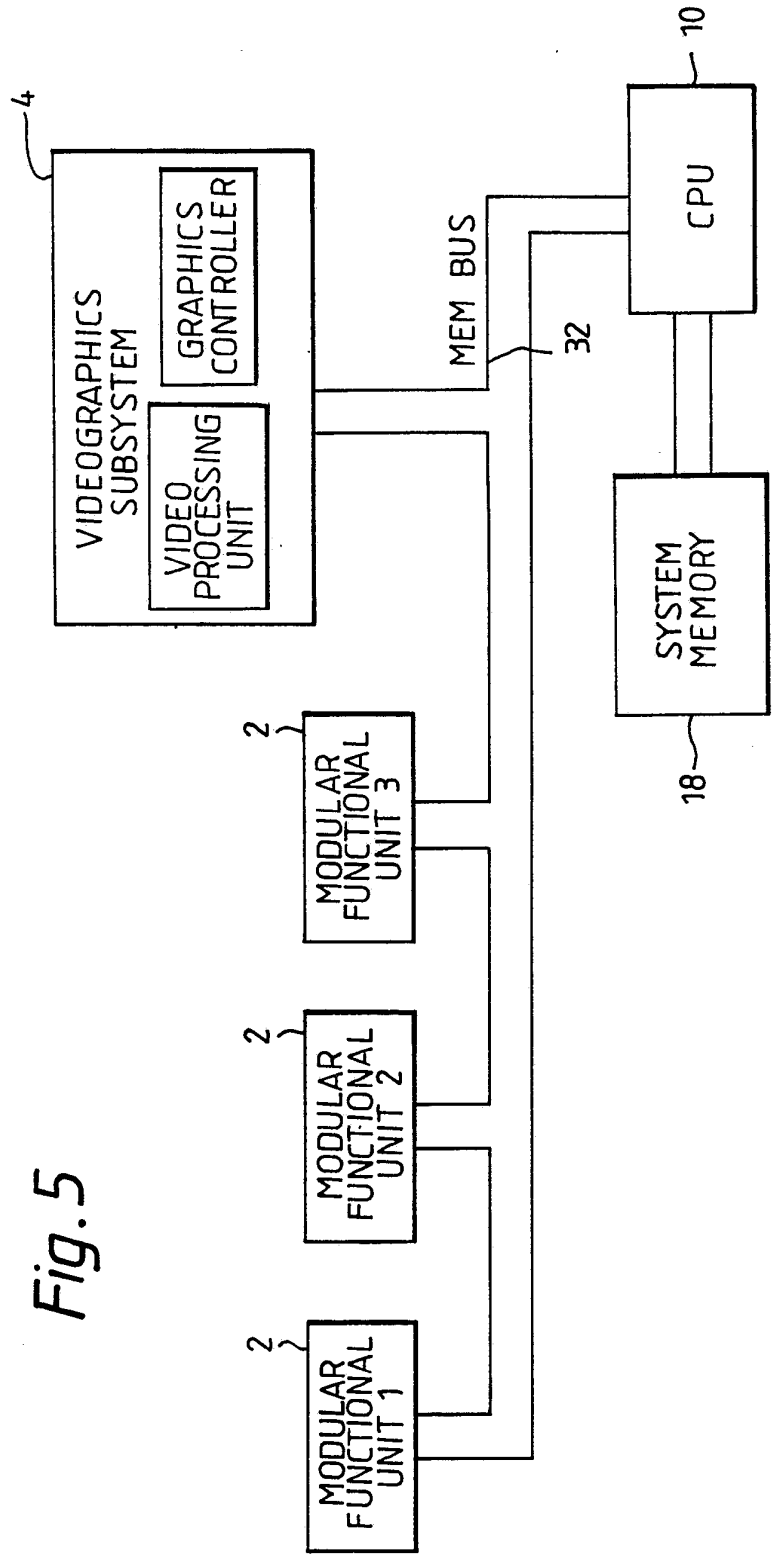
MODULAR FUNCTIONAL UNIT 3

Fig. 4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MODULAR FUNCTIONAL UNIT 2
2
MODULAR FUNCTIONAL UNIT 1

Fig. 5

INTERNATIONAL SEARCH REPORT

International Application No PCT/GB 93/00749

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 G06F3/14

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	G06F ; G09G ; H04N

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document,[11] with indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
P,X	EP,A,0 493 881 (INTERNATIONAL BUSINESS MACHINES CO.) 8 July 1992	1
P,A	see page 2, column 1, line 16 - page 3, column 4, line 25 see page 6, column 10, line 46 - page 7, column 11, line 46 see page 7, column 12, line 37 - page 8, column 13, line 43 see page 9, column 15, line 35 - line 39 see figures 1,3	2,7,9

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
22 JULY 1993	29. 07. 93
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	FARRICELLA L.

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category °	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
A	EP,A,0 454 414 (SONY CORPORATION OF AMERICA) 30 October 1991 see page 3, column 2, line 46 - page 4, column 3, line 11 see page 4, column 4, line 1 - line 10 see page 5, column 5, line 10 - page 6, column 7, line 1 see figure 2	1
A	FUNKSCHAU vol. 62, no. 26, 14 December 1990, MUNCHEN DE pages 60 - 75 KAMENZKY ET AL. 'Computer mit Fernseh-Ambitionen'	
A	COMPUTER TECHNOLOGY REVIEW vol. 12, no. 4, April 1992, LOS ANGELES US page 1 B. CAHILL 'Integrating Video/Graphics Neat Trick'	

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO.

GB 9300749
SA 72686

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
The members are as contained in the European Patent Office EDP file on
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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A-0493881	08-07-92	JP-A- 4351181	04-12-92
EP-A-0454414	30-10-91	None	