



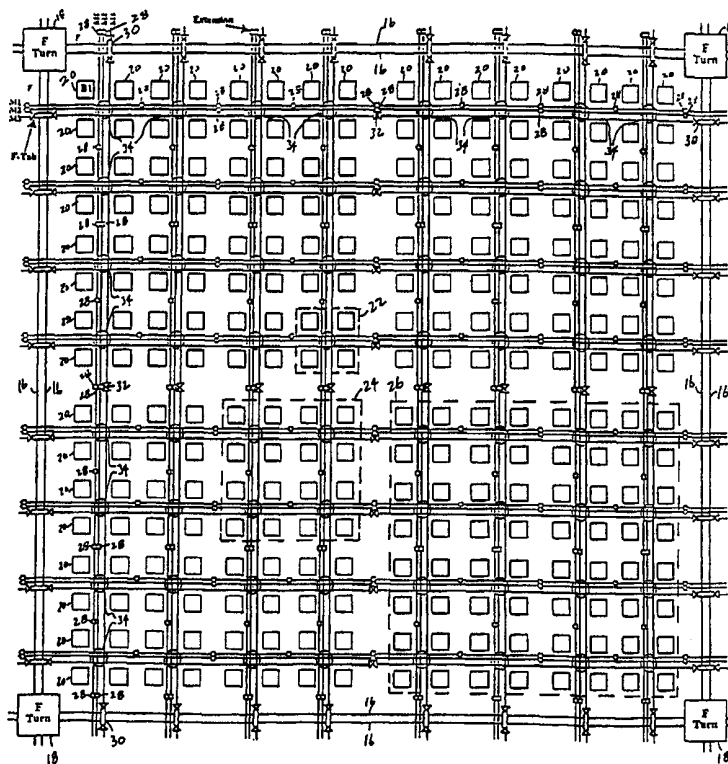
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(54) Title: A SEMI-HIERARCHICAL REPROGRAMMABLE FPGA ARCHITECTURE

(57) Abstract

A semi-hierarchical FPGA having a top level, a middle level and a low level. The top level having a plurality of first tiles (12), each of the plurality of first tiles having a freeway routing channel (16), and a plurality of first switch matrices (18) disposed at each corner of each of the first tiles and coupled to said freeway routing channels. The middle level having a plurality of second tiles (26), each of the plurality of second tiles having an associated horizontal and vertical expressway routing channels (M1, M2, M3). Each horizontal/vertical expressway routing channel having a tab (30) for coupling the horizontal/vertical expressway routing channel to the freeway routing channel and for coupling the horizontal/vertical expressway routing channel to the adjacent horizontal/vertical expressway routing channel. The low level (22) having a block (20), the block coupled by block connectors, and the expressway routing channels to other block connectors by a switching matrix.



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SPECIFICATION

A SEMI-HIERARCHICAL REPROGRAMMABLE FPGA ARCHITECTURE

BACKGROUND OF THE INVENTION

1. Field Of The Invention

The present invention relates to a reprogrammable field programmable gate array (FPGA) architecture. More particularly, the present invention relates to a semi-hierarchical reprogrammable FPGA architecture .

2. The Background Art

In the FPGA art both antifuse based programmable architectures and SRAM based reprogrammable architectures are well known. One of the differences between antifuse based programmable FPGA architectures and SRAM based reprogrammable FPGA architectures is the need for greater symmetry in a reprogrammable FPGA architecture.

This need arises from the fact that the reconfigurable memory bits take up a large area and cannot be provided for every possibly desired location. As a result, in a reprogrammable architecture the selection of the placement of the must be made with care. This termed "depopulation". Without a high degree of symmetry in the reprogrammable architecture, the reconfigurable memory bit depopulation makes the place and route of nets in the FPGA very difficult.

The symmetry in the architectural resources alleviates some of the difficulties faced in the place and route caused by the depopulation. With greater symmetry, the

depopulation of the can be increased and the cost in terms of routing resources in the place and route of a net can be lowered. One of the places this symmetry is obtained in the use of look-up tables (LUT) at the logic level, because a LUT has perfect symmetry among its inputs.

5 Strictly hierarchical reprogrammable FPGA architectures wherein the routing resources at a particular level may be couple to the routing resources at another level, but may not be extended to additional logic groupings at the same level are known. A strictly hierarchical architecture has an advantage in that commonly a low cost FPGA architecture to manufacture. However, the performance in a strictly hierarchical FPGA
10 architecture typically suffers. Because of the depopulation problem in reprogrammable FPGA architectures, there exists a need for an improvement from a strictly hierarchical FPGA architecture.

15 It is therefore an object of the present invention to provide a semi-hierarchical FPGA architecture that includes crossing interconnection within a single level of the hierarchy.

 It is a further object of the present invention to improve the performance of a strictly hierarchical FPGA architecture with the employment of crossing interconnections while maintaining some of the advantage of the lower cost of manufacture associated with a strictly hierarchical FPGA architecture.

20 BRIEF DESCRIPTION OF THE INVENTION

 The present invention is directed to a semi-hierarchical FPGA architecture having

top, middle and low levels. The semi-hierarchical nature of the FPGA architecture according to the present invention has crossing intersections between the levels in the hierarchy that significantly improve the place and route of nets or circuits in the lowest level of the architecture and in the connection of these nets to higher levels in the semi-hierarchical architecture.

The top level of the architecture is an array of the B16x16 tiles arranged in a rectangular array and enclosed by I/O blocks on the periphery. On each of the four sides of a B16x16 tile, and also associated with each of the I/O blocks is a freeway routing channel. The width freeway routing channel in the rectangular array can be changed to accommodate different numbers of B16x16 tiles without disturbing the internal structure of the B16x16 tiles. The freeway routing channels can be extended in any combination of directions at each end by a freeway turn matrix (F-turn).

A B16x16 tile in the middle level of hierarchy is a sixteen by sixteen array of B1 blocks. The B16x16 tile is a nesting of a B2x2 tile that includes a two by two array of four B1 blocks. The B2x2 tiles are stepped into a four by four array of sixteen B1 blocks in a B4x4 tile, and the B4x4 tiles are stepped into a eight by eight array of sixty-four B1 blocks in a B8x8 tile. A B16x16 tile includes four B8x8 tiles.

The routing resources in the middle level of hierarchy are expressway routing channels M1, M2, and M3 including groups of interconnect conductors. The expressway routing channels M1, M2, and M3 are segmented, and between each of the segments in the expressway routing channels M1, M2, and M3 are disposed extensions that can extend the expressway routing channel M1, M2, or M3 an identical distance

along the same direction. The extensions that couple the segments in the expressway routing channels M1 and M2 provide a one-to-one coupling between the interconnect conductors of the expressway routing channels M1 and M2 on either side of the extensions.

5 The segments of an M3 expressway routing channel is extended at the boundary of a B16x16 tile where an expressway routing channel M3 crosses a freeway routing channel by an F-tab, and otherwise by an M3 extension. An F-tab is an active device of tristatable buffers coupled to a matrix of reprogrammable switches wherein the interconnect conductors in the freeway routing channels and the expressway routing
10 channel M3 that are fed into an F-tab may be coupled or continue in the same direction through the F-tab, even through the interconnect conductors are coupled to other interconnect conductors by the reprogrammable switches. An M3 extension is an active device that includes tristatable buffers coupled to a matrix of reprogrammable switches wherein the interconnect conductors in the expressway routing channel M3 that are fed
15 into an M3 extension may be coupled by the reprogrammable switches to many of the other interconnect conductors in the expressway routing channel M3 that come into the M3 extension.

 At the intersections of each of the expressway routing channels M1, M2, and M3 in the horizontal direction with the expressway routing channels M1, M2 and M3 in the
20 vertical direction is an E-turn disposed at the center of each B2x2 tile. An E-turn is a passive device that includes and a matrix of reprogrammable switches wherein the interconnect conductors in the expressway routing channels M1, M2 and M3 that are fed into an E-turn may be coupled to many of the other interconnect conductors in the

expressway routing channels M1, M2 and M3 that come into the E-turn by the programmable switches, and also continue in the same direction through the E-turn even though the interconnect conductors are coupled to other interconnect conductors by the reprogrammable switches.

5 At the lowest level of the semi-hierarchical FPGA architecture, there are block connect (BC) routing channels, local mesh (LM) routing channels, and direct connect (DC) interconnect conductors. The BC routing channels through an E-tab couple B1 blocks together at the lowest level in the architecture, and also provide access to the expressway routing channels M1, M2, and M3 in the middle level of the architecture.

10 Each BC routing channel shares an E-tab with a BC routing channel in an adjacent B1 block that may be employed to couple a signal between adjacent B1 blocks in a first direction. Further, each BC routing channel shares a BC extension with a BC routing channel in an adjacent B1 block that may be employed to couple a signal between adjacent B1 blocks in a second direction.

15 An E-tab is an active device that includes tri-state buffers and a matrix of reprogrammable switches wherein the interconnect conductors in the BC routing channels and the expressway routing channels M1, M2, and M3 may be coupled to many of the other interconnect conductors in the BC routing channels and expressway routing channels M1, M2, and M3. The expressway routing channels M1, M2, and M3

20 also continue in the same direction through the E-tab.

Each LM routing channels in a B1 block shares an LM extension with an LM routing channel through in an adjacent B1 block in either the corresponding horizontal

or vertical direction that may be employed to couple a signal between adjacent B1 blocks in either the horizontal or vertical direction. The LM extensions provide a one-to-one coupling between the interconnect conductors of the LM routing channels on either side of the LM extensions.

5 The DC interconnect conductors form a high performance direct connection between the logic elements in adjacent B1 blocks to implement data path functions such as counters, comparators, adders and multipliers.

Each B1 block includes four clusters of devices. Each of the four clusters includes first and second LUT3s, a LUT2, and a DFF. Each of the LUT3s have first, 10 second, and third inputs indicated as "A", "B", and "C", and a single output indicated as "Y". Each of the LUT2s have first and second inputs indicated as "A" and "B", and a single output indicated as "Y". Each DFF has a data input indicated as "D" and a data output indicated as "Q". In each of the clusters, the outputs "Y" of the LUT3s are multiplexed to the input of DFF, and further multiplexed with the "Q" output of the DFF 15 to form first and second outputs of each of the clusters.

An extension is disposed in between the horizontal and vertical BC routing channels to enhance the routability of the horizontal and vertical BC routing channels to the inputs and outputs of the devices in the clusters.

The LM routing channels that pass through the B1 block are segmented in the B1 20 block by extensions that provide a one-to-one coupling between the interconnect

conductors of the LM routing channels on either side of the extension.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of the floor plan of an FPGA including the top level of a semi-hierarchical architecture according to the present invention.

5 FIG. 2 is a block diagram of a B16x16 tile in a an FPGA and the associated routing resources in the middle level of semi-hierarchical architecture according to the present invention.

10 FIG. 3 is a block diagram of a B2x2 tile in an FPGA and the connection of the routing resources in the lowest level to the middle level of a semi-hierarchical architecture according to the present invention.

FIG. 4 is a block diagram of a B2x2 tile in an FPGA and the routing resources in the lowest level of a semi-hierarchical architecture according to the present invention.

FIG. 5 is a block diagram of a B1 block in an FPGA and the routing resources in the lowest level of a semi-hierarchical architecture according to the present invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

15 Those of ordinary skill in the art will realize that the following description of the present invention is illustrative only and not in any way limiting. Other embodiments of the invention will readily suggest themselves to such skilled persons.

The present invention is directed to a semi-hierarchical architecture implemented in an FPGA. According to the present invention, there are top, middle and low levels in the semi-hierarchical architecture. The architecture is termed semi-hierarchical, because although the three levels of the architecture are coupled to one another as in a hierarchy, the three separate levels are not strictly hierarchical because the routing resources in each of the three levels may be extended to similar architectural groups in the same level of the architecture. The semi-hierarchical nature of the FPGA architecture according to the present invention significantly improves the place and route of nets or circuits in the lowest level of the architecture and in the connection of these nets to higher levels in the semi-hierarchical architecture. A description of the three levels of the semi-hierarchical architecture according to the present invention is made herein.

Turning now to FIG. 1 a block diagram of the floor plan of an FPGA 10 according to the present invention including the top level of the semi-hierarchical architecture is illustrated. The top level of the architecture is an array of the B16x16 tiles 12 arranged in a rectangular array and enclosed by I/O blocks 14 on the periphery and the associated routing resources. A B16x16 tile 12 is a sixteen by sixteen array of B1 blocks. As will be described in detail below, a B16x16 tile 12 and its associated routing resources represents the middle level in the semi-hierarchical architecture, and a B1 block and its associated routing resources represents the lowest level in the semi-hierarchical architecture.

On each of the four sides of a B16x16 tile 12, and also associated with each of the I/O blocks 14 is freeway routing channel 16. The coupling of a freeway routing channel

16 to the routing resources in the middle level of the semi-hierarchical architecture will be described in greater detail below. From FIG. 1, it should be appreciated that on each side of a B16x16 tile 12 there are two freeway routing channels 16, either as a result of the disposition of two freeway routing channels 16 between adjacent B16x16 tiles 12 or as a result of the disposition of two freeway routing channels between a B16x16 tile 12 and an adjacent I/O block 14.

It should be appreciated that the number of B16x16 tiles 12 in the rectangular array may be fewer or greater than the four shown in FIG. 1. According to the present invention, it is presently contemplated that the width of a freeway routing channel 16 in the rectangular array can be changed to accommodate different numbers of B16x16 tiles 12 without disturbing the internal structure of the B16x16 tiles 12. In this manner, the floorplan of the FPGA 10 can readily be custom sized by including the desired number of B16x16 tiles 12 in the design.

The freeway routing channels 16 can be extended in any combination of directions at each end by a freeway turn matrix (F-turn) 18. An F-turn 18 is an active device that includes tri-state buffers and a matrix of reprogrammable switches. The reprogrammable switches are preferably SRAM pass devices. The interconnect conductors in the freeway routing channels 16 that are fed into an F-turn 18 may be coupled to many of the other interconnect conductors in the freeway routing channels 16 that come into the F-turn 18 by the programmable switches. Further, the interconnect conductors in the freeway routing channels 16 that are fed into an F-turn 18 continue in the same direction through the F-turn 18, even though the interconnect conductors are coupled to other interconnect conductors by the reprogrammable switches. A

description of the implementation of an F-turn 18 is beyond the scope of this disclosure and will not be made herein to avoid overcomplicating the disclosure and thereby obscuring the present invention.

The freeway routing channels 16 along with the F-turns 18 form a course mesh. A freeway routing channel 16 will very rarely be utilized all by itself without any extension, since such distances are abundantly covered by the routing resources in the middle hierarchy to be described below. A freeway routing channel 16 is primarily intended to be used in conjunction with one or more other freeway routing channel 16 in any direction that together can span a distances of two or more B16x16 tiles 12.

In FIG. 2, a block diagram of a B16x16 tile 12 and the associated routing resources in the middle level of hierarchy is illustrated. The B16x16 tile 12 is a sixteen by sixteen array of B1 blocks 20. To avoid overcomplicating the drawing figure, only the B1 blocks 20 in a single row and a single column are indicated by the reference numeral 20. The B16x16 tile 12 is based on the repetition and nesting of smaller groupings (tiles) of B1 blocks 20. The smallest tile that is directly replicated and stepped is a B2x2 tile 22 that includes a two by two array of four B1 blocks 20. The B2x2 tiles 22 are stepped into a four by four array of sixteen B1 blocks 20 in a B4x4 tile 24, and the B4x4 tiles 24 are stepped into a eight by eight array of sixty-four B1 blocks 20 in a B8x8 tile 26. A B16x16 tile 12 includes four B8x8 tiles 26.

Though not depicted in FIG. 2, the B16x16 tile 12 further includes a block of user assignable static random access memory (SRAM) disposed between the two upper B8x8 tiles 26, and a block of SRAM disposed between the two lower B8x8 tiles 26.

The routing resources in the middle level of hierarchy are termed expressway routing channels. There are three types of expressway routing channels, namely M1, M2, and M3. In FIG. 2, only a single row and a single column of expressway routing channels M1, M2, and M3 are denominated to avoid overcomplicating the drawing figure. In a preferred embodiment of the present invention, there is a single group of nine interconnect conductors in an M1 expressway routing channel, two groups of nine interconnect conductors in an M2 expressway routing channel, and six groups of nine interconnect conductors in an M3 expressway routing channel.

The expressway routing channels M1, M2, and M3 are segmented so that each expressway routing channel M1, M2, and M3 spans a distance of a B2x2 tile 22, a B4x4 tile 24, and a B8x8 tile 26, respectively. Between each of the segments in the expressway routing channels M1, M2, and M3 are disposed extensions that can extend the expressway routing channel M1, M2, or M3 an identical distance along the same direction.

The extensions 28 that couple the segments in the expressway routing channels M1 and M2 are passive reprogrammable elements that are preferably an SRAM pass device. The extensions 28 provide a one-to-one coupling between the interconnect conductors of the expressway routing channels M1 and M2 on either side of the extensions 28. To avoid overcomplicating the drawing figure, only the extensions 28 in a single row and a single column are indicated by the reference numeral 28.

The segments of an M3 expressway routing channel is extended at the boundary

of a B16x16 tile 12 where an expressway routing channel M3 crosses a freeway routing channel 16 by a freeway tab (F-tab) 30, and otherwise by an M3 extension 32. To avoid overcomplicating the drawing figure, only the F-tabs 30, and M3 extensions 32 in a single row and a single column are indicated by the reference numeral 30 and 32, respectively.

An F-tab 30 is an active device that includes tri-state buffers and a matrix of reprogrammable switches. The reprogrammable switches are preferably an SRAM pass device. The interconnect conductors in the freeway routing channels 16 and the expressway routing channel M3 that are fed into an F-tab 30 may be coupled to many of the other interconnect conductors in the freeway routing channels 16 and the expressway routing channel M3 that come into the F-tab 30 by the programmable switches. Further, the interconnect conductors in the freeway routing channels 16 and the expressway routing channel M3 that are fed into an F-tab 30 continue in the same direction through the F-tab 30, even through the interconnect conductors are coupled to other interconnect conductors by the reprogrammable switches. A description of the implementation of the an F-tab 30 is beyond the scope of this disclosure and will not be made herein to avoid overcomplicating the disclosure and thereby obscuring the present invention.

Accordingly, an F-tab 30 implements the dual role of providing an extension of the middle level routing resources in a B16x16 tile 12 to the middle level routing resources in an adjacent B16x16 tile 12 and providing access between the middle level routing resources of B16x16 tile 12 and a freeway routing channel 16 in the highest level of the architecture. An F-tab 30 can combine the two roles of access and extension

simultaneously in the formation of a single net.

An M3 extension 32 is an active device that includes tristatable buffers coupled to a matrix of reprogrammable switches. The reprogrammable switches are preferably an SRAM pass device. The interconnect conductors in the expressway routing channel M3 that are fed into an M3 extension 32 may be coupled by the reprogrammable switches to many of the other interconnect conductors in the expressway routing channel M3 that come into the M3 extension 32. A description of the implementation of an M3 extension 32 is beyond the scope of this disclosure and will not be made herein to avoid overcomplicating the disclosure and thereby obscuring the present invention.

As depicted in FIG. 2, all of the expressway routing channels M1, M2, and M3 run both vertically through every column and horizontally through every row of B2x2 tiles 22. At the intersections of each of the expressway routing channels M1, M2, and M3 in the horizontal direction with the expressway routing channels M1, M2 and M3 in the vertical direction is an expressway turn (E-turn) 34 disposed at the center of each B2x2 tile 22. To avoid overcomplicating the drawing figure, only the E-turns 34 disposed in the B2x2 tiles 22 in a single row and a single column are indicated by the reference numeral 34.

An E-turn 34 is a passive device that includes and a matrix of reprogrammable switches. The reprogrammable switches are preferably an SRAM pass device. The interconnect conductors in the expressway routing channels M1, M2 and M3 that are fed into an E-turn 34 may be coupled to many of the other interconnect conductors in

the expressway routing channels M1, M2 and M3 that come into the E-turn 30 by the programmable switches. Further, the interconnect conductors in the expressway routing channels M1, M2 and M3 that are fed into an E-turn 34 continue in the same direction through the E-turn 34, even though the interconnect conductors are coupled to other interconnect conductors by the reprogrammable switches. A description of the implementation of an E-turn 34 is beyond the scope of this disclosure and will not be made herein to avoid overcomplicating the disclosure and thereby obscuring the present invention.

At the lowest level of the semi-hierarchical FPGA architecture, there are three types of routing resources, block connect (BC) routing channels, local mesh (LM) routing channels, and direct connect (DC) interconnect conductors. According to a preferred embodiment of the present invention, there are nine interconnect conductors in each BC routing channel and six interconnect conductors in each LM routing channel. Of these three, the BC routing channels serve the dual purpose of being able to both couple B1 blocks 20 together at the lowest level in the architecture, and also provide access to the expressway routing channels M1, M2, and M3 in the middle level of the architecture. In FIG. 3 aspects of the BC routing channels will be described, and in FIG. 4 aspects of the LM routing channels and the DC interconnect conductors will be described.

Turning now to FIG. 3, a B2x2 tile 22 including four B1 blocks 20 is illustrated. Associated with each of the B1 blocks 20 is a horizontal BC routing channel 50-1 and a vertical BC routing channel 50-2. Each horizontal BC routing channel 50-1 and vertical BC routing channel 50-2 is coupled to an expressway tabs (E-tab) 52 to provide access

for each B1 block 20 to the vertical and horizontal expressway routing channels M1, M2, and M3, respectively.

An E-tab 52 is an active device that includes tri-state buffers and a matrix of reprogrammable switches. The reprogrammable switches are preferably an SRAM pass device. The interconnect conductors in the BC routing channels 50 and the expressway routing channels M1, M2, and M3 that are fed into an E-tab 52 may be coupled by the programmable switches to many of the other interconnect conductors in the expressway routing channels M1, M2, and M3 that come into the E-tab 52. Further, the expressway routing channels M1, M2, and M3 that are fed into an E-tab 52 continue in the same direction through the E-tab 52, even through the interconnect conductors are coupled to other interconnect conductors by the reprogrammable switches. A description of the implementation of an E-tab 52 is beyond the scope of this disclosure and will not be made herein to avoid overcomplicating the disclosure and thereby obscuring the present invention.

At the E-tabs 52, the signals provided on the BC routing channels 50 can connect to any of the expressway routing channels M1, M2, or M3. Once a signal emanating from a B1 block 20 has been placed on an expressway routing channel M1, M2 or M3 and traversed a selected distance, an E-tab 52 is employed to direct that signal onto a horizontal or vertical BC routing channel 50-1 or 50-2 into a B1 block 20 at a selected distance from the B1 block 20 from which the signal originated. As the connection between the routing resources at the lowest level in the architecture and the routing resources in the middle level of the architecture, the E-tabs 52 provide that the place and route of signals both inside and outside the B1 blocks 20 may be implemented

independently from one another.

In FIG. 4, the expressway routing channels M1, M2, and M3 and the E-turn 34 have been omitted for clarity. As further depicted in FIG. 4, in addition to the horizontal and vertical BC routing channels 50-1 and 50-2 associated with each B1 block 20, there are also associated with each B1 block 20 four LM routing channels 54-1 through 54-4 and first and second DC interconnect conductors 56-1 and 56-2. The BC routing channels 50, the LM routing channels 54, and the DC interconnect conductors 56 provide significantly better performance than a strict hierarchy, and further help avoid congesting the expressway routing channels M1, M2, and M3. The BC routing channels 50 and the LM routing channels 54 combine to form two meshes. One is a mesh connection within a B1 block 20, and a second is a mesh connection between B1 blocks 20.

The BC routing channels 50 provide portions of the two meshes. The portion of the mesh connection within a B1 block 20 is described below. In the portion of the mesh providing connection between adjacent B1 blocks 20, each horizontal and vertical BC routing channel 50-1 and 50-2 share an E-tab 52 with a horizontal or vertical BC routing channel 50-1 and 50-2 in an adjacent B1 block 20 that may be employed to couple a signal between adjacent B1 blocks 20 in a first direction. Further, each horizontal and vertical BC routing channel 50-1 and 50-2 share a BC extension 58 with a horizontal or vertical BC routing channel 50-1 and 50-2 in an adjacent B1 block 20 that may be employed to couple a signal between adjacent B1 blocks 20 in a second direction. The BC extensions 58 provide a one-to-one coupling between the interconnect conductors of the BC routing channels 50 on either side of the BC

extensions 58. Accordingly, each BC routing channel 50, in the horizontal and vertical directions is coupled to the adjacent B1 blocks 20 in the corresponding horizontal and vertical directions by a E-tab 52 in a first direction along both the horizontal and vertical and in a second direction along both the horizontal and vertical by a BC extension 58.

5 From drawing FIG. 4, it should be appreciated that the LM routing channels 54-1 through 54-4 pass through the B1 block 20 as two vertical LM routing channels 51-1 and 54-4 and two horizontal LM routing channels 54-2 and 54-3, and that the intersections 60 of the vertical and horizontal LM routing channels 54 are hardwired along a diagonal.

10 The LM routing channels 54 also provide portions of the two meshes. The portion of the mesh connection formed along with the BC routing channels 50 within a B1 block 20 will be described below. In the portion of the mesh formed along with BC routing channels between B1 block 20, each of the four LM routing channels 54-1 through 54-4 in each B1 block 20 shares an LM extension 62 with an LM routing
15 channel 54-1 through 54-4 in an adjacent B1 block 20 in either the corresponding horizontal or vertical direction that may be employed to couple a signal between adjacent B1 blocks 20 in either the horizontal or vertical direction. The LM extensions 62 provide a one-to-one coupling between the interconnect conductors of the LM routing channels 54 on either side of the LM extensions 62. Accordingly, between
20 adjacent B1 blocks 20 there are two LM routing channels 54 from each of the adjacent B1 blocks coupled by a LM extension 62 on all sides of adjacent B1 blocks 20.

The DC interconnect conductors 56-1 and 56-2 form a high performance direct

connection between the logic elements in adjacent B1 blocks 20 to implement data path functions such as counters, comparators, adders and multipliers. As will be described below, each B1 block 20 includes four clusters of logic elements. Preferably, each of the four clusters includes two three input look-up tables (LUT3), a single two-input look-up table (LUT2), and a D-type flip-flop (DFF). In the DC interconnect conductor routing path, each of the DC interconnect conductors 56-1 and 56-2 is multiplexed to an input to a separate one of the two LUT3s in each of the four cluster of a B1 block 20. The DC interconnect conductors 56-1 and 56-2 are connected between vertically adjacent B1 blocks 20 as is illustrated in FIG. 4.

FIG. 5 illustrates a B1 block 20 according to the present invention in greater detail. As described above, each B1 block 20 includes four clusters 70-1 through 70-4 of devices. Each of the four clusters 70-1 through 70-4 includes first and second LUT3s 72-1 and 72-2, respectively, a LUT2 74, and a DFF 76. Each of the LUT3s 72 have first, second, and third inputs indicated as "A", "B", and "C", and a single output indicated as "Y". Each of the LUT2s 74 have first and second inputs indicated as "A" and "B", and a single output indicated as "Y". With a LUT3 72, any three input boolean logic function may be implemented, and with a LUT2 74 any two input boolean logic function may be implemented.

Each DFF 76 has a data input indicated as "D" and a data output indicated as "Q". In each of the clusters 70-1 through 70-4, the outputs "Y" of the LUT3s 72-1 and 72-2 are multiplexed to the input of DFF 76, and further multiplexed with the output of the DFF 76 to form first and second outputs of each of the clusters 70-1 through 70-4.

Each DFF 76 also has an enable (EN) input , a set/reset (S/R) input, and a clock (CLK) input. The EN, S/R, and CLK input are coupled to utility routing channels, a discussion of which is beyond the scope of this disclosure, but which is found in United States Patent Application No. XXXX, filed February 22, 1999 by inventors Arunangshu Kundu, Gregory W. Bakker, nd Wayne Wong, entitled "GLOBAL SIGNAL DISTRIBUTION ARCHITECTURE IN A FIELD PROGRAMMABLE GATE ARRAY", having attorney docket No. ACT-281, and hereby incorporated by reference.

Within the B1 block 20, the horizontal BC routing channel 50-1 is disposed between the upper clusters 70-1 and 70-2 and the lower clusters 70-3 and 70-4, and the vertical BC routing channel 50-2 is disposed between the two clusters 70-1 and 70-3 on the left side of the B1 block 20 and the two clusters 70-2 and 70-4 on the right side of the B1 block 20. It should be appreciated that due to the layout of the B1 block depicted in FIG. 4 wherein the input and outputs of the devices in the clusters 70-1 through 70-4 are all depicted horizontally, the horizontal BC routing channel 50-1 forms a diagonally hardwired connection at 78 with a routing channel that effectively sends the horizontal BC routing channel in a vertical direction.

An extension 80 is disposed between the diagonally hardwired connection 78 and a diagonally hardwired connection 82 between the horizontal BC routing channel 50-1 and the vertical BC channel 50-2 to enhance the routability of the horizontal and vertical BC routing channels to the inputs and outputs of the devices in the clusters 70-1 through 70-4. The extension 80 provides a one-to-one coupling between the interconnect conductors of the BC routing channels 50 on either side of the BC extension 80.

The LM routing channels 54-1 and 54-4 pass vertically through the B1 block 20 and the LM routing channels 54-2 and 54-3 pass horizontally through the B1 block 20. Each of the LM routing channels 54 is segmented in the B1 block 20 by extensions 84. The extensions 84 provides a one-to-one coupling between the interconnect
5 conductors of the LM routing channels 54 on either side of the extensions 84. Further, as described above, the intersections 60 of the vertical LM routing channels 54-1 and 54-4 and horizontal LM routing channels 54-2 and 54-3 are hardwired along a diagonal.

The horizontal and vertical BC routing channels 50-1 and 50-2, and the two
10 vertical LM routing channels 54-1 and 54-4 form intersections with the inputs and outputs of the LUT2s 74, the inputs of the LUT3s 72-1 and 72-2, and the multiplexed outputs of the LUT3s 72-1 and 72-2 and the DFF 76 in each of the clusters 70-1 through 70-4.

At some of the intersections formed between the horizontal and vertical BC
15 routing channels 50-1 and 50-2, and the two vertical LM routing channels 54-1 and 54-4 and the inputs of the LUT2s 74 and the inputs of the LUT3s 72-1 and 72-2 are disposed reprogrammable elements. For each separate LUT2s 74 and the LUT3s 72-1 and 72-2 input, the reprogrammable elements disposed at selected intersections are preferably controlled by SRAM bits that multiplex the horizontal and vertical BC
20 routing channels 50-1 and 50-2, and the two vertical LM routing channels 54-1 and 54-4 with the separate input. Accordingly, at a given time, each separate LUT2s 74 and the LUT3s 72-1 and 72-2 input may be coupled by a reprogrammable element to only

one of the interconnect conductors in the horizontal and vertical BC routing channels 50-1 and 50-2, and the two vertical LM routing channels 54-1 and 54-4.

At some of the intersections formed between the horizontal and vertical BC routing channels 50-1 and 50-2, and the two vertical LM routing channels 54-1 and 54-4 and the outputs of the LUT2s 74 and the multiplexed outputs of the LUT3s 72-1 and 72-2 and the DFF 76 are disposed reprogrammable elements, such as an SRAM pass device. For each separate LUT2 74 output and LUT3 72-1 and 72-2 and DFF 76 multiplexed output, each of the reprogrammable elements disposed at selected intersections are preferably controlled by a separate SRAM pass device.

These selected intersections, unlike the intersections formed between the horizontal and vertical BC routing channels 50-1 and 50-2, and the two vertical LM routing channels 54-1 and 54-4 and the inputs of the LUT2s 74 and the inputs of the LUT3s 72-1 and 72-2, are not multiplexed. Accordingly, at a given time, each separate LUT2 74 output and LUT3 72-1 and 72-2 and DFF 76 multiplexed output may be coupled to any of the interconnect conductors in the horizontal and vertical BC routing channels 50-1 and 50-2, and the two vertical LM routing channels 54-1 and 54-4 having an reprogrammable element disposed at an intersection. It should be appreciated, that no more than one LUT2 74 output and LUT3 72-1 and 72-2 and DFF 76 multiplexed output may be coupled simultaneously to the same interconnect conductor in the horizontal and vertical BC routing channels 50-1 and 50-2, and the two vertical LM routing channels 54-1 and 54-4.

As described above, each of the DC interconnect conductors 56-1 and 56-2 is

5 multiplexed in a serial fashion to an input of a separate one of the two LUT3s in each cluster 70-1 through 70-4 of a B1 block 20. For example, in the serial connection, the DC interconnect conductor 56-1 is multiplexed to the "A" input of the LUT3 72-1 of the cluster 70-1. Next, the "Y" output of the LUT3 72-1 in cluster 70-1 is multiplexed to the "A" input of the LUT3 72-1 in cluster 70-2. Next, the "Y" output of the LUT3 72-1 in cluster 70-2 is multiplexed to the "A" input of the LUT3 72-1 in cluster 70-3. Next, the "Y" output of the LUT3 72-1 in cluster 70-3 is multiplexed to the "A" input of the LUT3 72-1 in cluster 70-4. Finally, the "Y" output of the LUT3 72-1 in cluster 70-4 pass out of the B1 block 20, and is multiplexed to the "A" input of the LUT3 72-1 in cluster 70-2 of the B1 block 20 disposed vertically below. The DC interconnect conductors 56-2 is similarly connected, except that it is input and output from the LUT3 72-2 in each of the clusters 70-1 through 70-4.

15 While embodiments and applications of this invention have been shown and described, it would be apparent to those skilled in the art that many more modifications than mentioned above are possible without departing from the inventive concepts herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.

What is Claimed is:

1. A semi-hierarchical FPGA architecture comprising:

a top level in said semi-hierarchical FPGA architecture, said top level having a plurality of first tiles of logic entities, each of said plurality of first tiles having a freeway routing channel associated with each edge of said first tiles, and a plurality of first switch matrices, one of said plurality of first switch matrices disposed at each corner of each of said first tiles and coupled to said freeway routing channels;

a middle level in said semi-hierarchical FPGA architecture, said middle level having one of said plurality of first tiles including a plurality of second tiles of logic entities, each of said plurality of second tiles having an associated horizontal expressway routing channel and vertical expressway routing channel, each horizontal expressway routing channel having a tab for coupling said horizontal expressway to a freeway routing channel and for coupling said horizontal expressway to an adjacent horizontal expressway, each vertical expressway routing channel having a tab for coupling said vertical expressway to a freeway routing channel and for coupling said vertical expressway to an vertical horizontal expressway; and

a low level in said semi-hierarchical FPGA architecture, said low level having clusters of logic devices forming a block, said block couple by block connectors said expressway routing channels an to other block connectors by a switching matrix.

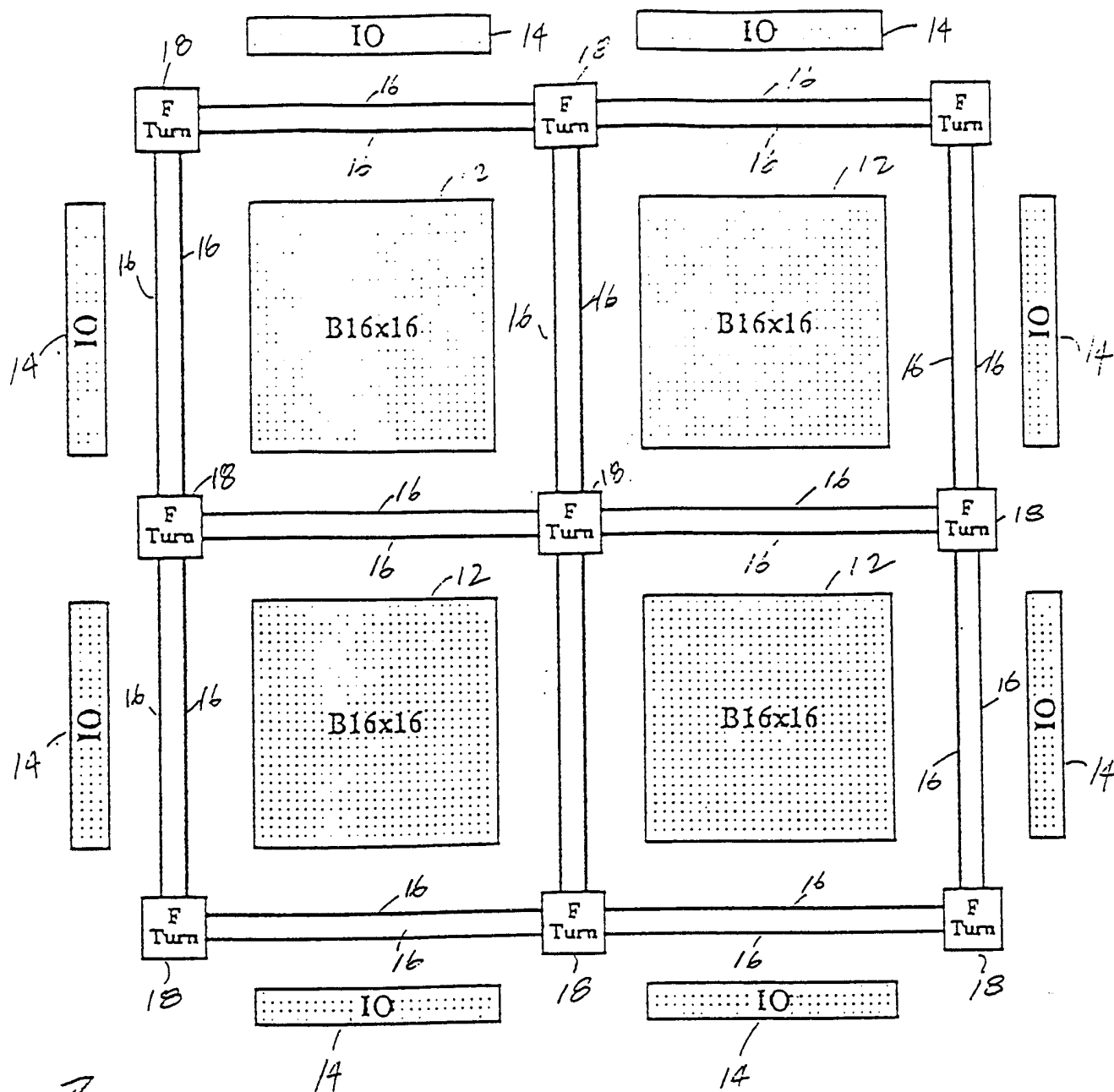


FIG. 1

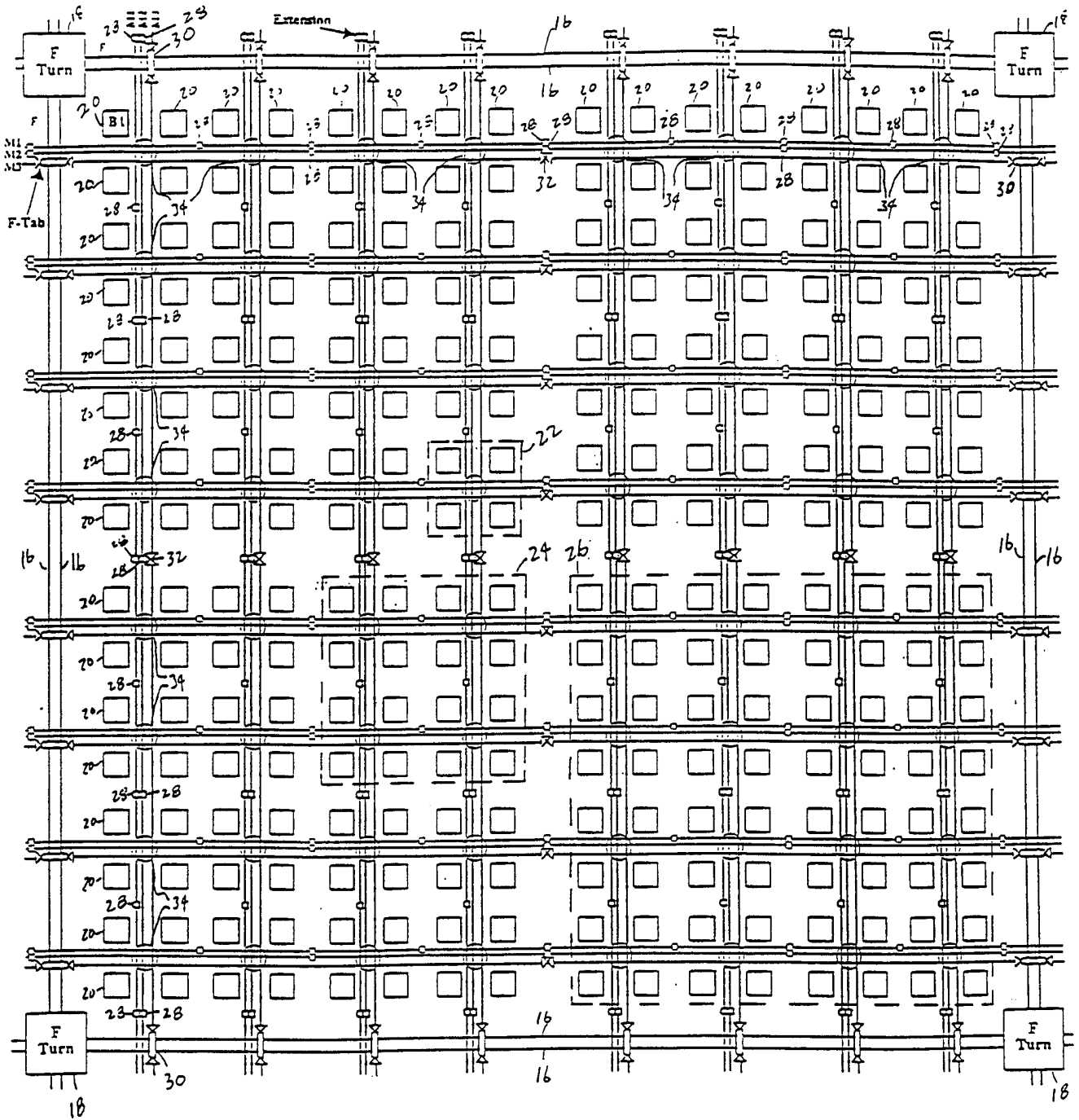


FIG. 2

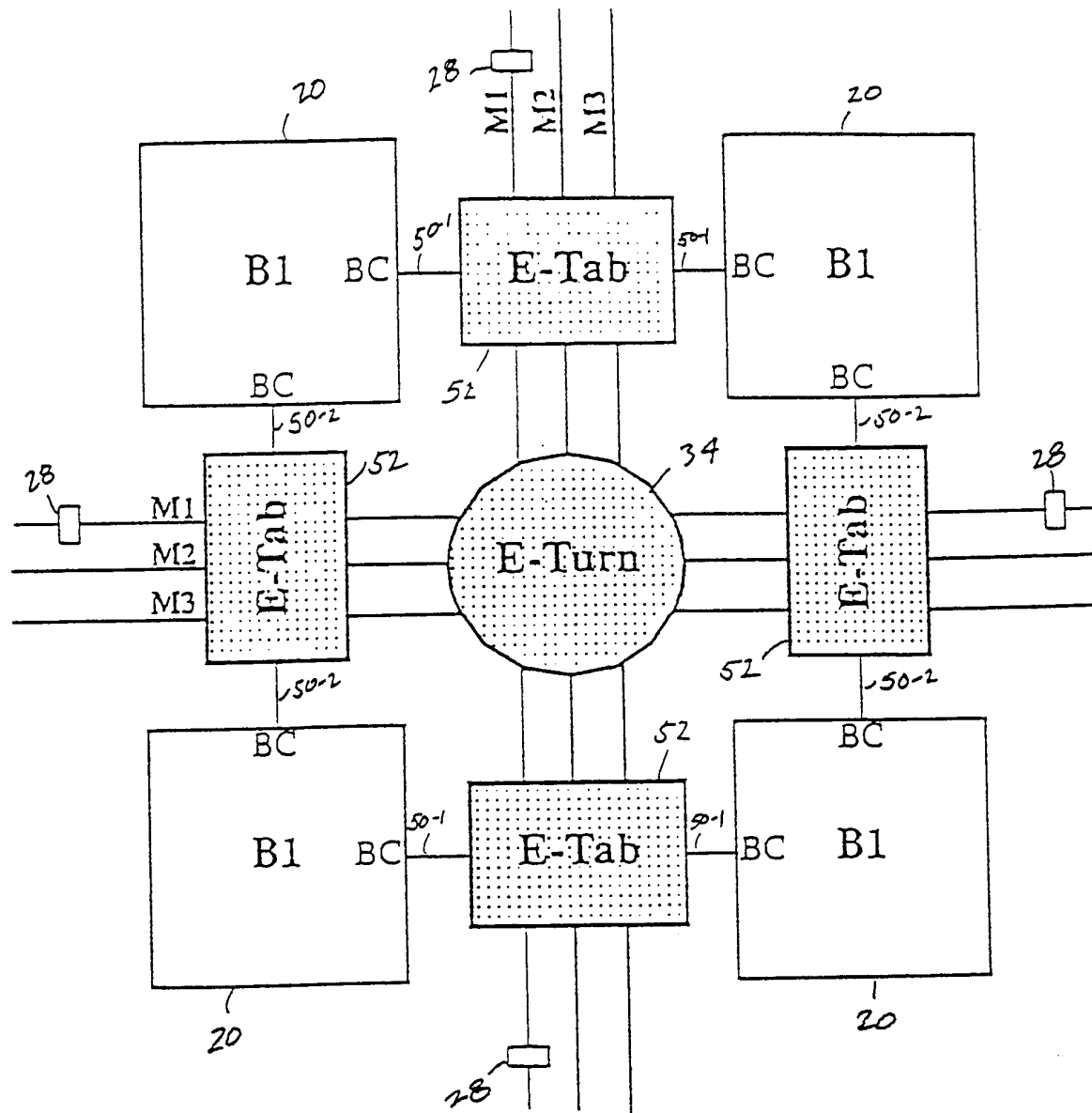


FIG. 3

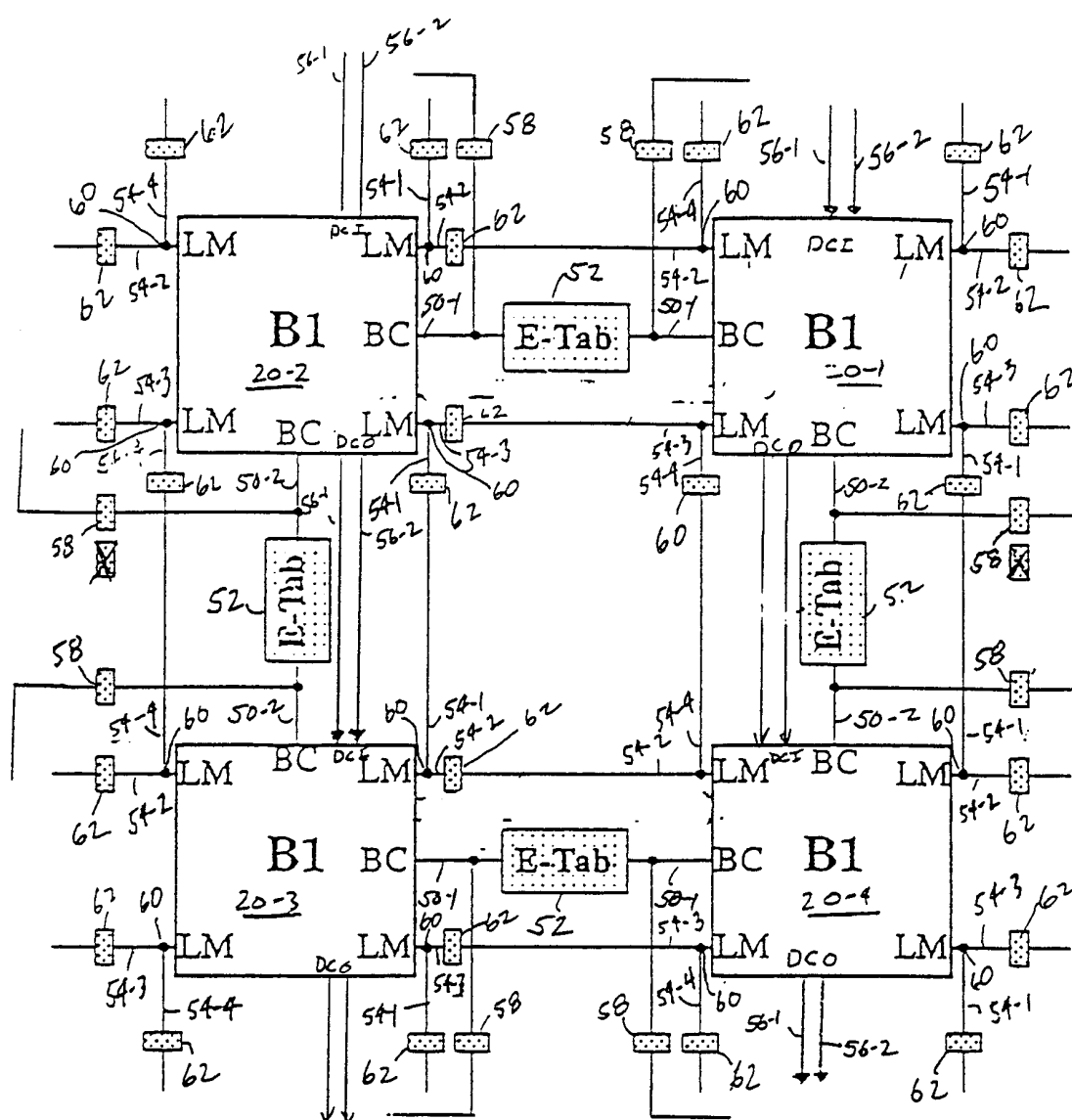


FIG. 4

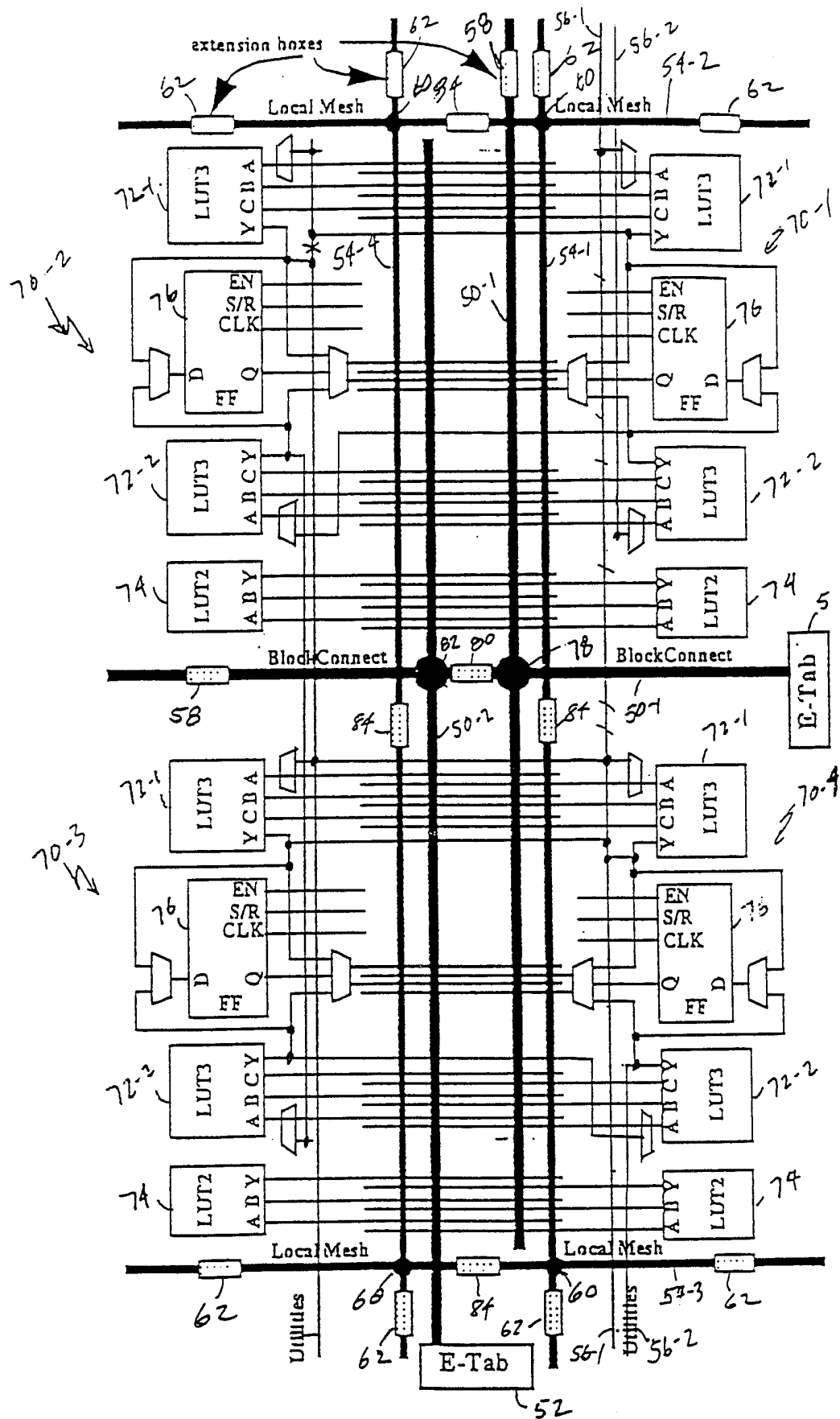


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US00/04460

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H01L 25/00; H03K 19/177

US CL : 326/39, 41

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 326/39, 41, 38, 40, 47

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

US EAST BRS

search terms: FPGA, hierarch\$4, horizontal, vertical, level, switch\$3

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,455,525 A (HO et al) 03 October 1995 (03.10.95), figures 1-6.	1
X	US 5,469,003 A (KEAN) 21 November 1995 (21.11.95), see entire document.	1
X	US 5,861,761 A (KEAN) 19 January 1999 (19.01.99), see entire document.	1

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

28 APRIL 2000

Date of mailing of the international search report

25 MAY 2000

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