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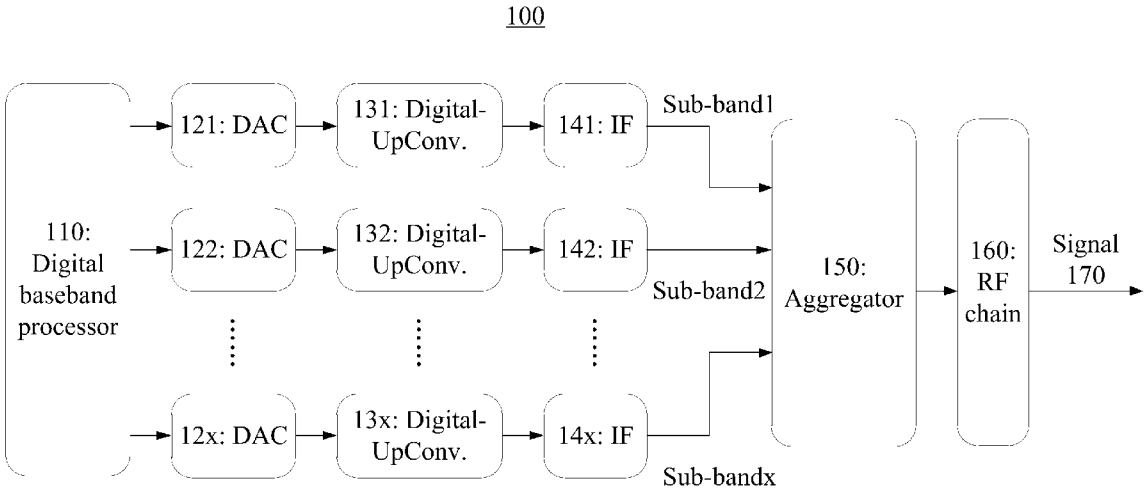


FIG. 1

(57) Abstract: Disclosed are apparatuses for communication. An example apparatus for transmitting may include a plurality of digital-to-analogue converters being configured for digital-to-analogue converting a plurality of digital baseband processed sub-band signals separated from a signal of the whole ultra-wide bandwidth, respectively; a plurality of digital up-converters being configured for up converting the plurality of digital-to-analogue converted sub-band signals, respectively; a plurality of intermediate frequency processors being configured for performing intermediate frequency processing on the plurality of up converted sub-band signals, respectively; an aggregator being configured for aggregating the plurality of intermediate frequency processed sub-band signals into an aggregated signal of the whole ultra-wide bandwidth; and a radio frequency chain being configured for processing the aggregated signal.

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APPARATUSES FOR COMMUNICATION

TECHNICAL FIELD

[0001] Various example embodiments relate to apparatuses for communication.

BACKGROUND

[0002] Terahertz (THz) or Sub-THz, for example 0.06-10 THz, band communication is one of the key enablers to fulfill high data rate requirements of the sixth generation mobile communication technology (6G). However, leveraging ultra-wide bandwidths, for example up to tens of GHz, brings many challenges in THz or Sub-THz transceiver design. One of the challenges is digital-to-analogue converter (DAC) and analogue-to-digital converter (ADC) capabilities. According to Nyquist-Shannon sampling theorem, the sampling rate of the DACs/ADCs shall be no less than the system bandwidth in order to avoid any information loss from a continuous-time signal. However, current on-shelf DACs/ADCs cannot support the efficient digital signal processing with such ultra-wide bandwidth in THz or Sub-THz communication. Further, power consumption of ultra-fast (e.g., of the order of 50 Gsps or faster), high-precise (e.g., from 8 to 16 bits) DACs/ADCs has a linear relationship with input signal bandwidth and grows exponentially with precision. Consequently, such DACs/ADCs are impractical for wireless communication devices. Moreover, THz or Sub-THz band radio frequency (RF) chain, for example a carrier frequency 220 GHz RF chain, mainly includes many expensive components/chipsets, which will lead to huge system cost and become unaffordable for such ultra-wide bandwidth deployment.

SUMMARY

[0003] A brief summary of exemplary embodiments is provided below to provide basic understanding of some aspects of various embodiments. It should be noted that this summary is not intended to identify key features of essential elements or define scopes of the embodiments, and its sole purpose is to introduce some concepts in a simplified form as a preamble for a more detailed description provided below.

[0004] In a first aspect, disclosed is an apparatus for transmitting. The apparatus may comprise:

a plurality of DACs being configured for digital-to-analogue converting a plurality of digital baseband processed sub-band signals separated from a signal of the whole ultra-wide bandwidth, respectively; a plurality of digital up-converters being configured for up converting the plurality of digital-to-analogue converted sub-band signals, respectively; a plurality of intermediate frequency processors being configured for performing intermediate frequency processing on the plurality of up converted sub-band signals, respectively; an aggregator being configured for aggregating the plurality of intermediate frequency processed sub-band signals into an aggregated signal of the whole ultra-wide bandwidth; and a RF chain being configured for processing the aggregated signal.

[0005] In a second aspect, disclosed is an apparatus for receiving. The apparatus may comprise: a radio frequency chain being configured for processing a signal of the whole ultra-wide bandwidth; a divider being configured for dividing the RF chain processed signal into a plurality of sub-band signals; a plurality of intermediate frequency processors being configured for performing intermediate frequency processing on the plurality of sub-band signals, respectively; a plurality of digital down-converters being configured for down converting the plurality of intermediate frequency processed sub-band signals, respectively; a plurality of ADCs being configured for analogue-to-digital converting the plurality of down converted sub-band signals, respectively, for digital baseband processing.

[0006] Other features and advantages of the example embodiments of the present disclosure will also be apparent from the following description of specific embodiments when read in conjunction with the accompanying drawings, which illustrate, by way of example, the principles of example embodiments of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Some example embodiments will now be described, by way of non-limiting examples, with reference to the accompanying drawings.

[0008] FIG. 1 shows an exemplary block diagram of an apparatus 100 for transmitting according to the example embodiments of the present disclosure.

[0009] FIG. 2 shows an exemplary block diagram of an apparatus 200 for receiving according to the example embodiments of the present disclosure.

[0010] Throughout the drawings, same or similar reference numbers indicate same or similar elements. A repetitive description on the same elements would be omitted.

DETAILED DESCRIPTION

[0011] Herein below, some example embodiments are described in detail with reference to the accompanying drawings. The following description includes specific details for the purpose of providing a thorough understanding of various concepts. However, it will be apparent to those skilled in the art that these concepts may be practiced without these specific details. In some instances, well known circuits, techniques and components are shown in block diagram form to avoid obscuring the described concepts and features.

[0012] Example embodiments of the present disclosure provide apparatuses for communication. The apparatuses for communication include apparatuses for transmitting and corresponding apparatuses for receiving, which can support ultra-wide bandwidths, for example up to tens of GHz, in THz or Sub-THz, for example 0.06-10 THz, frequency band with simplified architecture and significantly reduced overall system cost.

[0013] To well explore the tens of GHz bandwidth while avoiding immaturity challenge of high sampling rate DACs/ADCs, carrier aggregation (CA) solution may be applied in the architecture of the apparatus 100, where the ultra-wide bandwidth may be separated into multiple sub-bands with a narrow bandwidth, avoiding strong requirement on the DACs/ADCs sampling rate.

[0014] FIG. 1 shows an exemplary block diagram of an apparatus 100 for transmitting according to the example embodiments of the present disclosure. As an example, it may be assumed that the apparatus 100 for transmitting works in a Sub-THz communication system with carrier frequency 220 GHz and bandwidth 20 GHz.

[0015] Referring to the FIG. 1, the apparatus 100 may include a digital baseband processor 110, a plurality of DACs 121, 122,..., 12x, a plurality of digital up-converters 131, 132, ..., 13x, a plurality of intermediate frequency (IF) processors 141, 142, ..., 14x, an aggregator 150, and a RF chain 160. The modules in the downstream of the baseband processing may be deemed as a RF system.

[0016] The whole ultra-wide bandwidth may be separated into multiple continuous sub-bands. The digital baseband processor 110 may process the multiple sub-bands, respectively, and output

the multiple sub-band signals to the RF system for further processing.

[0017] In some embodiments, the digital baseband processor 110 may separate the signal of the whole ultra-wide bandwidth into a plurality of sub-band signals with a narrow bandwidth and then perform digital baseband processing on the plurality of sub-band signals.

[0018] Alternatively, in some embodiments, the signal of the whole ultra-wide bandwidth may be separated into a plurality of sub-band signals with a narrow bandwidth before being input into the digital baseband processor 110, and the digital baseband processor 110 may be replaced with a plurality of digital baseband processors (not shown). The number of the plurality of digital baseband processors may be identical to the number of the plurality of sub-band signals, and the plurality of digital baseband processors may perform digital baseband processing on the plurality of sub-band signals, respectively.

[0019] The digital baseband processor 110 or the plurality of digital baseband processors may output the plurality of digital baseband processed sub-band signals separated from the signal of the whole ultra-wide bandwidth into a plurality of processing chains of the RF system, respectively. The whole ultra-wide bandwidth may be an ultra-wide bandwidth, for example up to tens of GHz and may be separated into sub-bands with a narrow bandwidth of e.g. 1.25 GHz, and thus the plurality of processing chains may work at lower bandwidths.

[0020] As an example, the FIG. 1 shows x processing chains each including a DAC e.g. the DAC 12x, a digital up-converter e.g. the digital up-converter 13x, and an IF processor, e.g. the IF processor 14x, and it may be appreciated that x may be any integer larger than one. One processing chain may process one sub-band signal output from the digital baseband processor. For example, the DAC 12x, the digital up-converter 13x, and the IF processor 14x may process the signal of sub-bandx, and the processing chains may be independent to each other.

[0021] The plurality of DACs 121, 122, ..., 12x may perform digital-to-analogue conversion on the plurality of the signals of sub-band1, sub-band2, ..., sub-bandx, respectively. On-shelf mature DACs with low speed (sampling rate) and low cost may be employed as the DACs 121, 122, ..., 12x, and thus power-saving, feasibility, stability and reliability of the apparatus 100 may be ensured and the cost may be significantly reduced.

[0022] The plurality of digital up-converters 131, 132, ..., 13x may up convert the plurality of digital-to-analogue converted sub-band signals, respectively. For example, the digital up-

converter 13x may up convert the signal of sub-bandx to be with a carrier frequency of e.g. 3.11 GHz. Then, the plurality of IF processors 141, 142, ..., 14x may perform IF processing on the plurality of up converted sub-band signals, respectively.

[0023] In some embodiments, an IF processor in the apparatus 100, e.g. the IF processor 14x, may include an analog up-convertor, a filter, a power amplifier (PA), etc. The working frequency band of the plurality of IF processors 141, 142, ..., 14x may be higher than that of the plurality of digital up-converters 131, 132, ..., 13x and that of the plurality of DACs 121, 122, ..., 12x. By the IF processing, the carrier frequency of the signal of the sub-bandx may be up-converted to its own targeted frequency point, such as 12 GHz, 14 GHz, etc. The carrier frequency of the IF processing for each sub-band may be identical or different and may be continuous within the 20 GHz bandwidth.

[0024] Then, the aggregator 150 may aggregate the plurality of IF processed sub-band signals into an aggregated signal of the whole ultra-wide bandwidth, e.g. 20 GHz, and output the aggregated signal to the RF chain 160 of the RF system. The working frequency band of the RF chain 160 may be higher than that of the aggregator 150, for example, the RF chain 160 may work at Sub-THz or THz frequency band. The RF chain 160 may be an analog processing chain. In other words, the aggregator 150 may work as a bridge between the plurality of processing chains working at low frequency band and the RF chain working at Sub-THz or THz frequency band. In some embodiments, one aggregator 150 is sufficient for the apparatus 100.

[0025] In some embodiments, the RF chain 160 may be capable of working at a carrier frequency of e.g. Sub-THz band 220 GHz, and in this case the RF chain 160 may be termed as e.g. 220 GHz RF chain. In some embodiments, the RF chain 160 in the apparatus 100 may mainly include a multiplier, e.g. a local oscillator (LO) multiplier for mixer, a mixer for up converting the IF signal to 220 GHz RF for transmitting, a filter, e.g. a 220 GHz band pass filter with bandwidth of 20 GHz, and a PA, e.g. a 220 GHz PA for transmitting.

[0026] In some embodiments, one RF chain 160 is sufficient for the apparatus 100. The above-mentioned components/chipsets in the RF chain 160 are expensive, and thus compared with a solution without the aggregator 150 where the plurality of IF processors 141, 142, ..., 14x are followed by a plurality of RF chains, respectively, for processing the signals of the sub-band1, the sub-band2, ..., the sub-bandx, the apparatus 100 according to the example embodiments of

the present disclosure may significantly reduce the cost and simplify the architecture. Power-saving, feasibility, stability and reliability may also be achieved with the reduced number of modules in the apparatus 100

[0027] After the RF chain 160 processes the aggregated signal, the RF chain 160 processed signal 170 of the original whole ultra-wide bandwidth may be transmitted from an antenna array (not shown) over the air to receiving side.

[0028] FIG. 2 shows an exemplary block diagram of an apparatus 200 for receiving according to the example embodiments of the present disclosure. As an example, it may be assumed that the apparatus 200 for receiving works in a Sub-THz communication system with carrier frequency 220 GHz and bandwidth 20 GHz.

[0029] Referring to the FIG. 2, the apparatus 200 may include a digital baseband processor 210, a plurality of ADCs 221, 222,..., 22y, a plurality of digital down-converters 231, 232, ..., 23y, a plurality of IF processors 241, 242, ..., 24y, a divider 250, and a RF chain 260. The modules in the upstream of the baseband processing may be deemed as a RF system. And it may be appreciated that the processing performed by the apparatus 200 is an inverse of that performed by the apparatus 100.

[0030] Receiving the signal 170 of the whole ultra-wide bandwidth, e.g. 20 GHz, the RF chain 260 may process the signal 170. The RF chain 260 may be an analog processing chain. In some embodiments, the RF chain 260 may be capable of working at a carrier frequency of e.g. Sub-THz band 220 GHz, and in this case the RF chain 260 may be termed as e.g. 220 GHz RF chain. In some embodiments, the RF chain 260 in the apparatus 200 may mainly include a multiplier, e.g. a LO multiplier for mixer, a mixer for down converting the 220 GHz RF signal to IF signal for receiving, and a filter, e.g. a 220 GHz band pass filter with bandwidth of 20 GHz and in some examples further include a low noise amplifier (LNA) for receiving, e.g. a 220 GHz LNA.

[0031] In some embodiments, one RF chain 260 is sufficient for the apparatus 200. The above-mentioned components/chipsets in the RF chain 260 are expensive, and thus compared with a solution without the divider 250 where a plurality of RF chains process the signals of the sub-band1, the sub-band2, ..., the sub-bandy, respectively, the apparatus 200 according to the example embodiments of the present disclosure may significantly reduce the cost and simplify the architecture. Power-saving, feasibility, stability and reliability may also be achieved with the

reduced number of modules in the apparatus 200.

[0032] Then, the divider 250 may divide the RF chain 260 processed signal of the whole ultra-wide bandwidth, into a plurality of sub-band signals. In some examples, the whole ultra-wide bandwidth may be separated into multiple continuous sub-bands. The working frequency band of the RF chain 260 may be higher than that of the divider 250, for example, the RF chain 260 may work at Sub-THz or THz frequency band. In other words, the divider 250 separates the ultra-wide bandwidth signal into multiple narrow bandwidth signals for digital processing in multiple narrow bandwidth sub-band processing chains. In some embodiments, one divider 250 is sufficient for the apparatus 200.

[0033] The plurality of sub-band signals may be further processed by a plurality of processing chains of the RF system, respectively. The plurality of processing chains may work at bandwidth lower than the whole bandwidth.

[0034] As an example, the FIG. 2 shows y processing chains each including an IF processor e.g. the IF processor 24y, a digital down-converter e.g. the digital down-converter 23y, and a ADC e.g. the ADC 22y, and it may be appreciated that y may be any integer larger than one and may be the same as or different from the number x of processing chains in the apparatus 100. One processing chain may process one sub-band signal output from the divider 250. For example, the IF processor 24y, the digital down-converter 23y, and the ADC 22y may process the signal of sub-bandy, and the processing chains may be independent to each other.

[0035] The plurality of IF processors 241, 242, ..., 24y may perform IF processing on the plurality of sub-band signals, respectively. In some embodiments, an IF processor in the apparatus 200, e.g. the IF processor 24y, may include an analog down-convertor, a filter, a PA, etc. The working frequency band of the plurality of IF processors 241, 242, ..., 24y may be higher than that of the plurality of digital down-converters 231, 232, ..., 23y and that of the plurality of ADCs 221, 222, ..., 22y. By the IF processing, the signal of sub-bandy may be down converted to be with a carrier frequency of e.g. 3.11 GHz. The carrier frequency of the IF processing for each sub-band may be identical or different and may be continuous within the 20 GHz bandwidth.

[0036] Then, the plurality of digital down-converters 231, 232, ..., 23y may down convert the plurality of IF processed sub-band signals, respectively. For example, the digital down-converter

23y may down convert the signal of sub-bandy to be with a narrow bandwidth of e.g. 1.25 GHz.

[0037] Then, the plurality of ADCs 221, 222, ..., 22y may perform analogue-to-digital conversion on the plurality of the signals of sub-band1, sub-band2, ..., sub-bandy, respectively, for further digital baseband processing. On-shelf mature ADCs with low speed (sampling rate) and low cost may be employed as the ADCs 221, 222, ..., 22y, and thus power-saving feasibility, stability and reliability of the apparatus 200 may be ensured and the cost may be significantly reduced.

[0038] The digital baseband processor 210 may perform digital baseband processing on the analogue-to-digital converted signals of sub-band1, sub-band2, ..., sub-bandy, respectively.

[0039] Alternatively, in some embodiments, the digital baseband processor 210 may be replaced with a plurality of digital baseband processors (not shown). The number of the plurality of digital baseband processors may be identical to the number of the plurality of sub-band signals, and the plurality of digital baseband processors may perform digital baseband processing on the plurality of sub-band signals, respectively.

[0040] The CA concept based architecture requires many number of RF analog processing chains to process each sub-band signal dedicatedly, the apparatuses for communication according to the example embodiments of the present disclosure may save the number of RF analog processing chains. For example, only one RF analog processing chain, such as the RF chain 160 or RF chain 260 may be sufficient for the apparatus 100 or the apparatus 200.

[0041] In addition, the aggregator, e.g. the aggregator 150, and the divider, e.g. the divider 250, are not complicated for the low working frequency band, and thus the operations of the aggregator and the divider would not bring big extra complexity and cost.

[0042] Further, the apparatuses for communication according to the example embodiments of the present disclosure do not need high-speed DACs/ADCs to support ultra-wide bandwidth transmission. Low speed and low cost DACs/ADCs in digital communication systems can be migrated to THz or Sub-THz system directly. Thus, there is no need to design advanced hardware modules after/before the baseband signal process to adapt to THz or Sub-THz ultra-high frequency band. Further, other devices of the processing chains of the RF system can also be migrated from mature systems, which would help the THz or Sub-THz system co-existence with the mature systems.

[0043] The apparatus 100 for transmitting and the apparatus 200 for receiving according to the example embodiments of the present disclosure can leverage multiple on-shelf mature enough and low-cost DACs/DACs chipsets to support the ultra-wide bandwidth transmission, e.g. the tens of GHz bandwidth transmission over THz or Sub-THz band, and can use only one analog processing chain working at higher frequency band to conduct the analog processing, such that power-saving, feasibility, stability and reliability may be ensured and the overall system cost can be significantly reduced.

[0044] As used herein, "at least one of the following: <a list of two or more elements>" and "at least one of <a list of two or more elements>" and similar wording, where the list of two or more elements are joined by "and" or "or", mean at least any one of the elements, or at least any two or more of the elements, or at least all the elements.

[0045] While this disclosure includes references to illustrative embodiments, this specification is not intended to be construed in a limiting sense. Various modifications of the described embodiments, as well as other embodiments within the scope of the disclosure, which are apparent to persons skilled in the art to which the disclosure pertains are deemed to lie within the principle and scope of the disclosure, e.g., as expressed in the following claims. For example, while blocks are presented in a given arrangement, alternative embodiments may perform similar functionalities with different components and/or circuit topologies, and some blocks may be deleted, moved, added, subdivided, combined, and/or modified. At least one of these blocks may be implemented in a variety of different ways. The order of these blocks may also be changed. Any suitable combination of the elements and actions of the some embodiments described above can be combined to provide further embodiments. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the disclosure.

[0046] Some embodiments may be implemented as circuit-based processes, including possible implementation on a single integrated circuit.

[0047] Some embodiments can be embodied in the form of methods and apparatuses for practicing those methods. Some embodiments can also be embodied in the form of program code recorded in tangible media, such as magnetic recording media, optical recording media, solid state memory, floppy diskettes, CD-ROMs, hard drives, or any other non-transitory machine-

readable storage medium, wherein, when the program code is loaded into and executed by a machine, such as a computer or a DSP-based device, the machine becomes an apparatus for practicing the present disclosure. Some embodiments can also be embodied in the form of program code, for example, stored in a non-transitory machine-readable storage medium including being loaded into and/or executed by a machine, wherein, when the program code is loaded into and executed by a machine, such as a computer or a processor, the machine becomes an apparatus for practicing the present disclosure. When implemented on a general-purpose processor, the program code segments combine with the processor to provide a unique device that operates analogously to specific logic circuits.

[0048] Unless explicitly stated otherwise, each numerical value and range should be interpreted as being approximate as if the word "about" or "approximately" preceded the value or range.

[0049] It will be further understood that various changes in the details, materials, and arrangements of the parts which have been described and illustrated in order to explain the nature of this disclosure may be made by those skilled in the art without departing from the scope of the disclosure, e.g., as expressed in the following claims.

[0050] The use of figure numbers and/or figure reference labels in the claims is intended to identify one or more possible embodiments of the claimed subject matter in order to facilitate the interpretation of the claims. Such use is not to be construed as necessarily limiting the scope of those claims to the embodiments shown in the corresponding figures.

[0051] Although the elements in the following method claims, if any, are recited in a particular sequence with corresponding labeling, unless the claim recitations otherwise imply a particular sequence for implementing some or all of those elements, those elements are not necessarily intended to be limited to being implemented in that particular sequence.

[0052] Reference herein to "embodiments," "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment can be included in at least one embodiment of the disclosure. The appearances of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment, nor are separate or alternative embodiments necessarily mutually exclusive of other embodiments. The same applies to the term "implementation."

[0053] Unless otherwise specified herein, the use of the ordinal adjectives "first," "second,"

"third," etc., to refer to an object of a plurality of like objects merely indicates that different instances of such like objects are being referred to, and is not intended to imply that the like objects so referred-to have to be in a corresponding order or sequence, either temporally, spatially, in ranking, or in any other manner.

[0054] Unless otherwise specified herein, in addition to its plain meaning, the conjunction "if" may also or alternatively be construed to mean "when" or "upon" or "in response to determining" or "in response to detecting," which construal may depend on the corresponding specific context. For example, the phrase "if it is determined" or "if [a stated condition] is detected" may be construed to mean "upon determining" or "in response to determining" or "upon detecting [the stated condition or event]" or "in response to detecting [the stated condition or event]."

[0055] Unless the context clearly requires otherwise, throughout the description and the claims, the words "comprise," "comprising," and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of "including, but not limited to." Additionally, the words "herein," "above," "below," and words of similar import, when used in this application, shall refer to this application as a whole and not to any particular portions of this application. Where the context permits, words in the description using the singular or plural number may also include the plural or singular number respectively. The word "or" in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

[0056] Moreover, conditional language used herein, such as, among others, "can," "could," "might," "may," "e.g.," "for example," "such as" and the like, unless specifically stated otherwise, or otherwise understood within the context as used, is generally intended to convey that certain embodiments include, while other embodiments do not include, certain features, elements and/or states. Thus, such conditional language is not generally intended to imply that features, elements and/or states are in any way required for one or more embodiments or that one or more embodiments necessarily include logic for deciding, with or without author input or prompting, whether these features, elements and/or states are included or are to be performed in any particular embodiment.

[0057] Also for purposes of this description, the terms "couple," "coupling," "coupled,"

"connect," "connecting," or "connected" refer to any manner known in the art or later developed in which energy is allowed to be transferred between two or more elements, and the interposition of one or more additional elements is contemplated, although not required. Conversely, the terms "directly coupled," "directly connected," etc., imply the absence of such additional elements.

[0058] The same type of distinction applies to the use of terms "attached" and "directly attached," as applied to a description of a physical structure. For example, a relatively thin layer of adhesive or other suitable binder can be used to implement such "direct attachment" of the two corresponding components in such physical structure.

[0059] The described embodiments are to be considered in all respects as only illustrative and not restrictive. In particular, the scope of the disclosure is indicated by the appended claims rather than by the description and figures herein. All changes that come within the meaning and range of equivalency of the claims are to be embraced within their scope.

[0060] The description and drawings merely illustrate the principles of the disclosure. It will thus be appreciated that those of ordinary skill in the art will be able to devise various arrangements that, although not explicitly described or shown herein, embody the principles of the disclosure and are included within its scope. Furthermore, all examples recited herein are principally intended expressly to be only for pedagogical purposes to aid the reader in understanding the principles of the disclosure and the concepts contributed by the inventor(s) to furthering the art, and are to be construed as being without limitation to such specifically recited examples and conditions. Moreover, all statements herein reciting principles, aspects, and embodiments of the disclosure, as well as specific examples thereof, are intended to encompass equivalents thereof.

[0061] The functions of the various elements shown in the figures, including any functional blocks labeled as "processors" and/or "controllers," may be provided through the use of dedicated hardware as well as hardware capable of executing software in association with appropriate software. When provided by a processor, the functions may be provided by a single dedicated processor, by a single shared processor, or by a plurality of individual processors, some of which may be shared. Moreover, explicit use of the term "processor" or "controller" should not be construed to refer exclusively to hardware capable of executing software, and may implicitly include, without limitation, digital signal processor (DSP) hardware, network

processor, application specific integrated circuit (ASIC), field programmable gate array (FPGA), read only memory (ROM) for storing software, random access memory (RAM), and non volatile storage. Other hardware, conventional and/or custom, may also be included. Similarly, any switches shown in the figures are conceptual only. Their function may be carried out through the operation of program logic, through dedicated logic, through the interaction of program control and dedicated logic, or even manually, the particular technique being selectable by the implementer as more specifically understood from the context.

[0062] As used in this application, the term "circuitry" may refer to one or more or all of the following: (a) hardware-only circuit implementations (such as implementations in only analog and/or digital circuitry); (b) combinations of hardware circuits and software, such as (as applicable): (i) a combination of analog and/or digital hardware circuit(s) with software/firmware and (ii) any portions of hardware processor(s) with software (including digital signal processor(s)), software, and memory(ies) that work together to cause an apparatus, such as a mobile phone or server, to perform various functions); and (c) hardware circuit(s) and or processor(s), such as a microprocessor(s) or a portion of a microprocessor(s), that requires software (e.g., firmware) for operation, but the software may not be present when it is not needed for operation." This definition of circuitry applies to all uses of this term in this application, including in any claims. As a further example, as used in this application, the term circuitry also covers an implementation of merely a hardware circuit or processor (or multiple processors) or portion of a hardware circuit or processor and its (or their) accompanying software and/or firmware. The term circuitry also covers, for example and if applicable to the particular claim element, a baseband integrated circuit or processor integrated circuit for a mobile device or a similar integrated circuit in server, a cellular network device, or other computing or network device.

[0063] It should be appreciated by those of ordinary skill in the art that any block diagrams herein represent conceptual views of illustrative circuitry embodying the principles of the disclosure. Similarly, it will be appreciated that any flow charts, flow diagrams, state transition diagrams, pseudo code, and the like represent various processes which may be substantially represented in computer readable medium and so executed by a computer or processor, whether or not such computer or processor is explicitly shown.

[0064] "SUMMARY" in this specification is intended to introduce some example embodiments, with additional embodiments being described in "DETAILED DESCRIPTION" and/or in reference to one or more drawings. "SUMMARY" is not intended to identify essential elements or features of the claimed subject matter, nor is it intended to limit the scope of the claimed subject matter.

[0065] Abbreviations used in the description and/or in the figures are defined as follows:

6G	the sixth generation mobile communication technology
ADC	analogue-to-digital converter
CA	carrier aggregation
DAC	digital-to-analogue converter
IF	intermediate frequency
LNA	low noise amplifier
LO	local oscillator
PA	power amplifier
RF	radio frequency
GHz	Gigahertz
Gsps	Giga-samples per second
THz	Terahertz

WHAT IS CLAIMED IS:

1. An apparatus for transmitting, comprising:

a plurality of digital-to-analogue converters being configured for digital-to-analogue converting a plurality of digital baseband processed sub-band signals separated from a signal of a whole bandwidth, respectively;

a plurality of digital up-converters being configured for up converting the plurality of digital-to-analogue converted sub-band signals, respectively;

a plurality of intermediate frequency processors being configured for performing intermediate frequency processing on the plurality of up converted sub-band signals, respectively;

an aggregator being configured for aggregating the plurality of intermediate frequency processed sub-band signals into an aggregated signal of the whole bandwidth; and

a radio frequency chain being configured for processing the aggregated signal.

2. The apparatus of claim 1, wherein the number of the radio frequency chain is one.

3. The apparatus of claim 1 or 2, wherein working frequency band of the radio frequency chain is higher than that of the aggregator.

4. The apparatus of any of claims 1 to 3, wherein working frequency band of the plurality of intermediate frequency processors is higher than that of the plurality of digital up-converters and that of the plurality of digital-to-analogue converters.

5. An apparatus for receiving, comprising:

a radio frequency chain being configured for processing a signal of a whole bandwidth;

a divider being configured for dividing the radio frequency chain processed signal into a plurality of sub-band signals;

a plurality of intermediate frequency processors being configured for performing intermediate frequency processing on the plurality of sub-band signals, respectively;

a plurality of digital down-converters being configured for down converting the plurality of

intermediate frequency processed sub-band signals, respectively;

a plurality of analogue-to-digital converters being configured for analogue-to-digital converting the plurality of down converted sub-band signals, respectively, for digital baseband processing.

6. The apparatus of claim 5, wherein the number of the radio frequency chain is one.

7. The apparatus of claim 5 or 6, wherein working frequency band of the radio frequency chain is higher than that of the divider.

8. The apparatus of any of claims 5 to 7, wherein working frequency band of the plurality of intermediate frequency processors is higher than that of the plurality of digital down-converters and that of the plurality of analogue-to-digital converters.

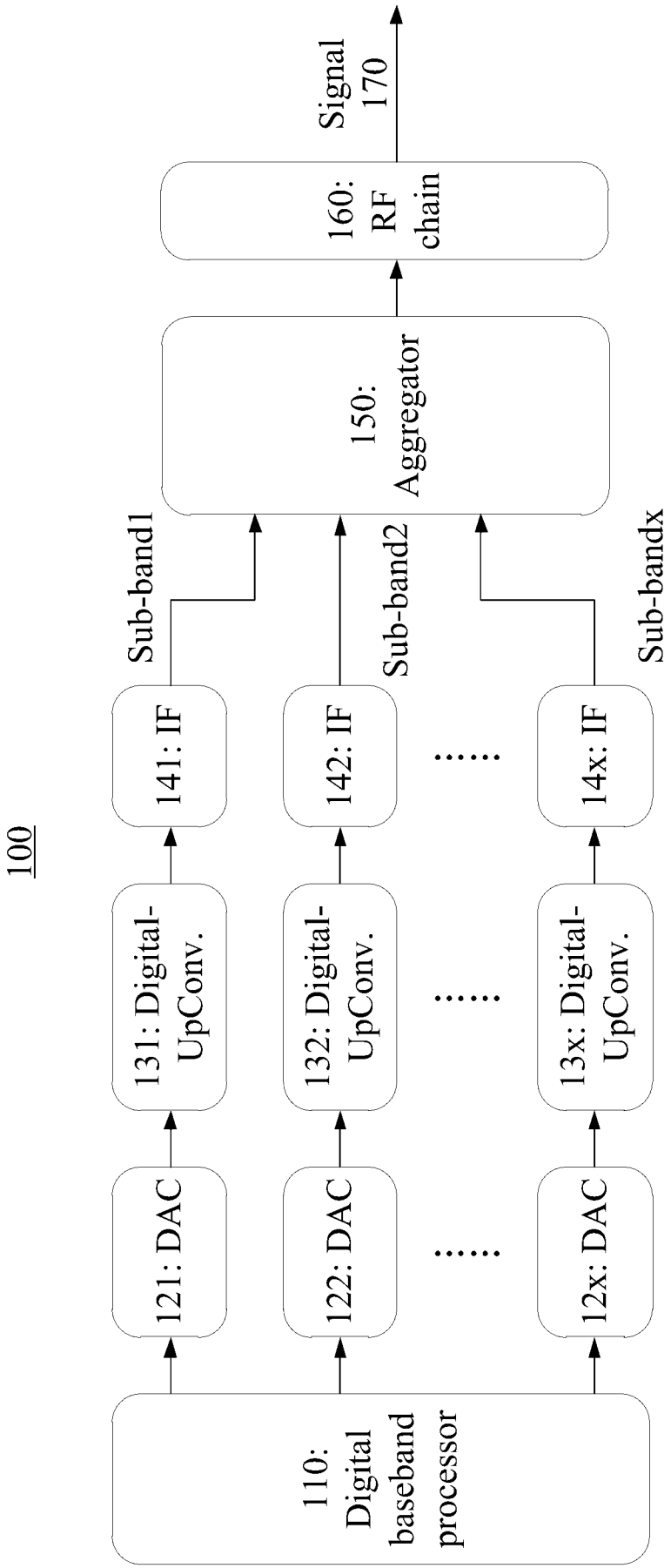

100
110: Digital baseband processor
121: DAC
122: DAC
12x: DAC
131: Digital-UpConv.
132: Digital-UpConv.
13x: Digital-UpConv.
141: IF
142: IF
14x: IF
Sub-band1
Sub-band2
Sub-bandx
150: Aggregator
160: RF chain
Signal 170

FIG. 1

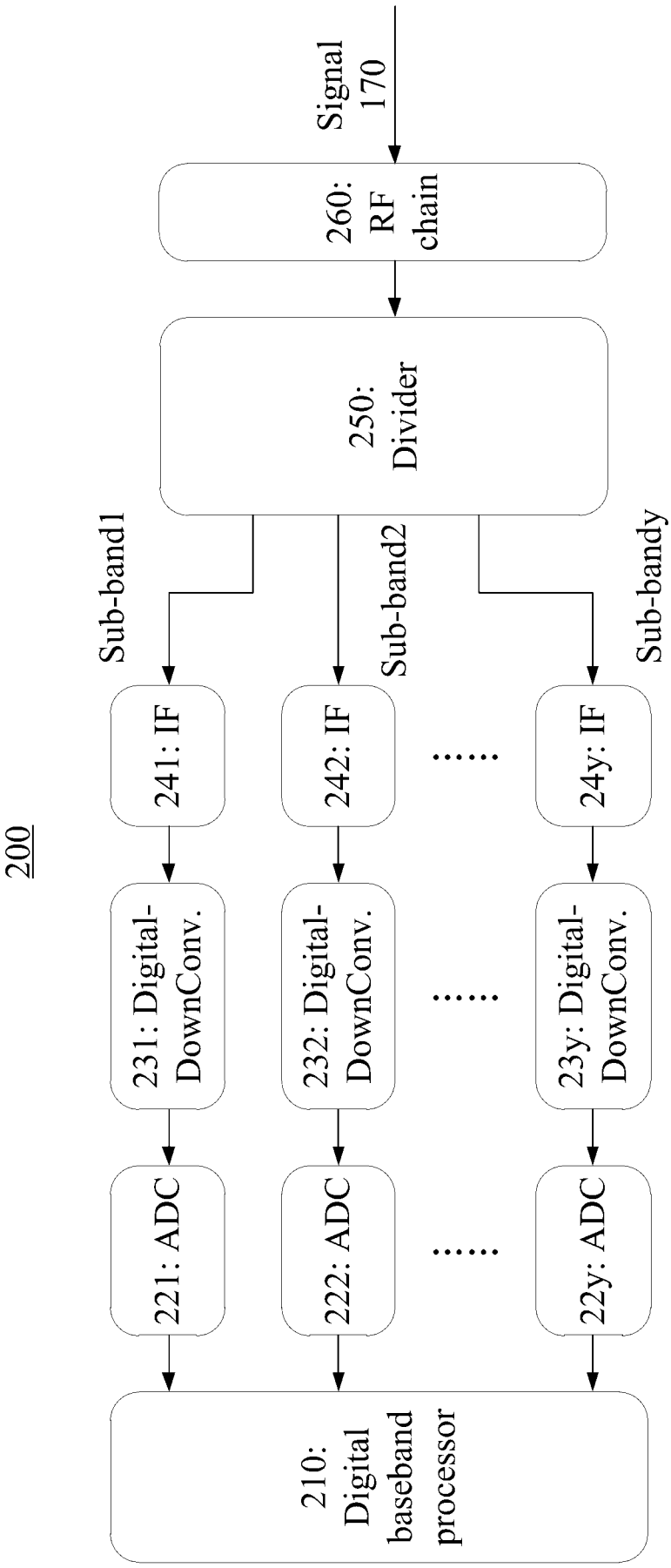

200
Signal 170
260: RF chain
250: Divider
Sub-band1
Sub-band2
Sub-bandy
241: IF
242: IF
24y: IF
231: Digital-DownConv.
232: Digital-DownConv.
23y: Digital-DownConv.
221: ADC
222: ADC
22y: ADC
210: Digital baseband processor

FIG. 2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2023/095695

A. CLASSIFICATION OF SUBJECT MATTER

H04L5/00(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNTXT,ENTXT,DWPI: digital baseband, AD, digital down converter, digital up converter, combine, aggregator, split, divide, sub-band, IF

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2018262218 A1 (THE BOEING COMPANY) 13 September 2018 (2018-09-13) description, paragraphs[0027]-[0040], figures 3-4	1-8
A	CN 101557375 A (SPREADTRUM COMMUNICATIONS(SHANGHAI) INC.) 14 October 2009 (2009-10-14) the whole document	1-8
A	US 2001054974 A1 (WRIGHT,Andrew S.) 27 December 2001 (2001-12-27) the whole document	1-8
A	US 2012269234 A1 (ZHANG,Zaichen et al.) 25 October 2012 (2012-10-25) the whole document	1-8

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 November 2023	**29 November 2023**
Name and mailing address of the ISA/CN **CHINA NATIONAL INTELLECTUAL PROPERTY ADMINISTRATION** **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088, China**	Authorized officer **YAN,Sai** Telephone No. **(+86) 010-53961605**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2023/095695

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