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(54) Title: INTERLEAVED MODULATOR

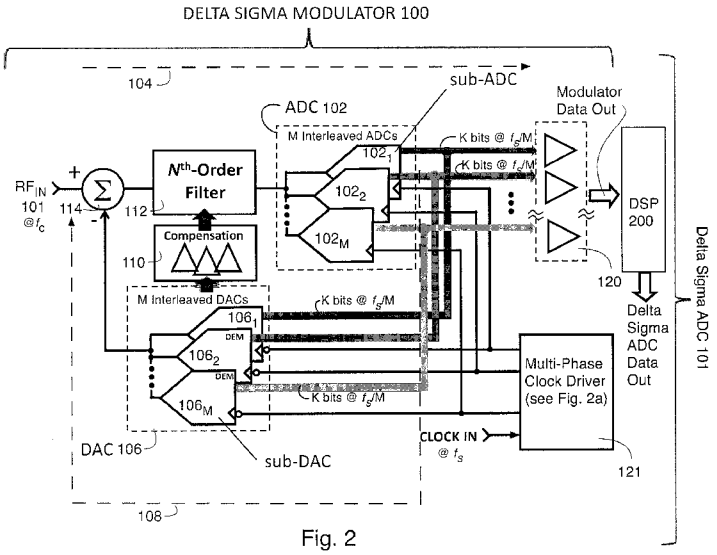

Fig. 2

(57) Abstract: A delta sigma modulator which has improved dynamic range. The ΔΣ modulator has a plurality of ADCs and a plurality of DACs, the plurality of ADCs and DACs are connected in a loop. The plurality of ADCs are coupled with an incoming analog signal. A clock generator provides a plurality of clock signals which control the plurality of ADCs and the plurality of DACs, the clock signals being offset relative to each other in the time domain thereby enabling each ADC in the plurality of ADCs one at a time and each DAC in the plurality of DACs one at a time so that the ΔΣ modulator processes data in the incoming analog signal in an interleaved fashion.

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Interleaved Modulator

Cross Reference to Related Applications

[0001] This application claims the benefit of US Provisional Patent Application Serial Number 62/015,021 filed 06/20/2014 and entitled "Interleaved Delta-Sigma Modulator", the disclosure of which is hereby incorporated herein by reference.

Statement Regarding Federally Sponsored Research or Development

[0002] None.

Technical Field

[0003] This invention relates to an interleaved Delta-Sigma ($\Delta\Sigma$) modulator with improved characteristics. The inventor also relates to a Delta-Sigma ($\Delta\Sigma$) Analog to Digital Convertor (ADC) which utilizes the aforementioned interleaved Delta-Sigma ($\Delta\Sigma$) modulator.

Background

[0004] A Delta-Sigma ($\Delta\Sigma$) modulator removes noise in a signal band of interest so that when the desired signal is received, the dynamic range within the signal band is improved. The dynamic range is measured as the difference between the received signal and noise floor as given in dBm. Removing the noise, or more specifically re-shaping the noise, out of the signal band increases the notch depth which is the same as lowering the noise floor. It is easier to remove the noise for deeper notch characteristics in narrow band applications (~1MHz) so a very high dynamic range (100dB) can then be achieved. Conversely for wider signal bandwidths (~200MHz), more shallow notches are obtained which result in less dynamic range (60dB).

[0005] A Delta-Sigma ($\Delta\Sigma$) is often used as an important part of a Analog to Digital Converter to lower the noise floor for a analog signal of interest. Such an Analog to Digital Converter is commonly called a Delta-Sigma Analog to Digital Converter.

[0006] Performance of a Delta-Sigma ($\Delta\Sigma$) modulator is strongly tied to the clock rate because (i) increasing the ratio of clock rate to signal bandwidth improves dynamic range, and (ii) faster sampling is necessary for bandpass operation at high signal frequencies. Increasing the clock rate, however, imposes even harder design challenges on the quantizers within the modulator. The architecture of the disclosed $\Delta\Sigma$ modulator leverages interleaving concepts to relax the quantizer clock rate (of the internal ADCs and DACs) without changing the effective oversampling ratio, thus, making it easier to reach aggressive dynamic range goals across wider bandwidths at higher frequencies than has been done in the prior art.

[0007] Traditional software-based (or software-defined) receiver architectures have extra conversion stages to reduce the Radio Frequencies (RF) down to a frequency that can be supported by a high-resolution ADC. These solutions have added complexity, size, power, and cost to the software-based receiver. Furthermore, traditional hardware based receivers have limited cross-functionality and can only be modified through physical intervention. Thus, the evolution in receiver design has been towards software-based receiver architectures due to their programmability and design efficiency but preferably without sacrificing performance of traditional hardware based receivers. The $\Delta\Sigma$ modulator has emerged as a preferred candidate for the front-end ADC in these software-based receiver architectures. However, attaining a high dynamic range (for example, a dynamic range of 80+ dB) at input signal frequencies (for example, frequencies above 1 GHz) has not yet been achieved.

[0008] The $\Delta\Sigma$ modulator architecture disclosed herein interleaves the multi-bit quantizers to maintain a fast effective sampling rate – thus supporting higher frequencies of operation – but the sampling rate of each quantizer is reduced by the interleaving factor thus enabling higher dynamic range performance.

[0009] Time-interleaving of two delta-sigma modulators has been published most recently by Chun-Yao Lu, "A High-Resoluion Time-Interleaved Delta-Sigma Modulator with Low Oversampling", *Proc. of the International Symposium on Integrated Circuits*, (ISIC), Dec. 2009 for use in audio applications. The two modulators are coupled together with additional analog paths for compensation similar to what is shown in Fig. 1(a) which is a simplified representation of the teachings of this prior art. The architecture presented can theoretically reduce the sampling rate by a factor of four and increase the dynamic range when compared to a conventional modulator. However, the prior art approach of this paper is effectively limited to low frequency operation because, in practice, a slight mismatch between the even and odd paths depicted in Fig. 1(a) (and in fig. 4 of that paper) could dramatically degrade the dynamic range of that modulator.

[0010] Another bandpass $\Delta\Sigma$ modulator architecture with partial interleaving has been designed for high-IF operation as taught by Julien Ryckaert et al., "A 6.1 GS/s 52.8 mW 43 dB DR 80 MHz Bandwidth 2.4 GHz RF Bandpass $\Delta\Sigma$ ADC in 40 nm CMOS" *IEEE Radio Frequency Integrated Circuits Symposium* (RFIC), May 2010. See Fig. 1(b). The ADC in the forward path of the modulator has been interleaved to relax the speed of the clock. The output quantized data is then multiplexed back up to the system data rate for conversion to the analog error signal by a single DAC. The ADC and DAC are not multi-bit quantizers, but rather single bit quantizers, and are limiting the achievable dynamic range for the chosen order of the modulator. An extension of the published architecture to multi-bit levels would not necessarily achieve a commensurate increase in dynamic range since the DAC – non-interleaved and still operating at full clock rate – would limit the overall modulator performance. A pictorial view of the architecture is shown in Fig. 1(b) for comparison with other prior art and with the approach presented herein.

[0011] A 1-bit ADC is just a single comparator which drives a 1-bit DAC which is a single switchable current source. A 1-bit DAC is inherently linear and does not introduce non-linearity to the system. Theory shows that every additional bit in the ADC and DAC increases the dynamic range (DR) by 6 dB, however, at some point the non-linearity of a multi-bit DAC becomes an issue so adding more bits does not further increase dynamic range. The basic theory

of delta-sigma demonstrates that the RMS noise goes as 2^{-K} where K is the number of quantizer bits. An example of a work covering this basic theory is "Oversampling Methods for A/D and D/A Conversion" by James C. Candy and Gabor C. Temes.

[0012] Interleaving both the multi-bit ADC and DAC, as proposed herein, is a substantially more difficult problem than that addressed in prior art. Meeting dynamic range goals requires matching among the interleaved DACs in addition to managing mismatch within an individual DAC. Also, interleaving increases the excess phase delay in the loop and therefor compensation is utilized to maintain stability. These challenges are difficult and may make the proposed solution appear infeasible to others but we have identified technical solutions that enable the new architecture.

Brief description

[0013] In one aspect the present invention provides a modulator having a forward path coupling an input summing block with a data out block, the forward path including at least a Nth order filter coupled to said input summing block and a plurality of interleaved multi-bit Analog to Digital Converters (ADCs), the interleaved multi-bit ADCs having inputs which are coupled to the Nth order filter and outputs which are coupled to the data out block, and a feedback path including a plurality of interleaved multi-bit Digital to Analog Converters (DACs), the interleaved multi-bit DACs having inputs which are coupled to respective outputs of the interleaved multi-bit ADCs, the interleaved multi-bit DACs having outputs which are summed together and applied to the input summing block. The concept of interleaving both ADCs and DACs allows a higher clock rate which enables higher input signal frequencies since the clock frequency has to be above the input frequency.

[0014] In another aspect the present invention provides a method increasing the dynamic range of a $\Delta\Sigma$ modulator, the method comprising; providing a plurality of ADCs and a plurality of DACs, the plurality of ADCs and DACs being connected in a loop; coupling the plurality of ADCs with an incoming analog signal; controlling said plurality of ADCs and plurality of DACs with a plurality of clock signals, the clock signals in said plurality of clock signals being offset

relative to each other in the time domain thereby enabling each ADC in said plurality of ADCs one at a time and enabling each DAC in said plurality of DACs one at a time such that the $\Delta\Sigma$ modulator processes data in said incoming analog signal in an interleaved fashion.

Brief Description of the Drawings

[0015] Fig. 1(a) depicts a simplified representation of a prior art $\Delta\Sigma$ modulator.

[0016] Fig. 1(b) depicts another $\Delta\Sigma$ modulator.

[0017] Fig. 2 is a block diagram of an embodiment of a $\Delta\Sigma$ modulator and a $\Delta\Sigma$ ADC incorporating the present invention.

[0018] Fig. 2a is a timing diagram for a multi-phase clock driver of Fig. 2.

[0019] Fig. 3(a) illustrates that the feedback DAC will have to be clocked at a time τ_D delayed from the sampling instant of the ADC.

[0020] Fig. 3(b) illustrates that since the ADCs in the proposed interleaved designs have a sampled clock period that is multiplied by the interleaving order, the excess phase delay increases proportionally.

[0021] Fig. 3(c) is a block diagram for a low-pass continuous time 2^{nd} order delta-sigma modulator while Fig. 3(d) is a block diagram for a band-pass continuous time 2^{nd} order delta-sigma modulator.

[0022] Fig. 4 is a block diagram of a $\Delta\Sigma$ modulator in accordance with a more specific embodiment the present invention where K=3, M=2 and N=6.

[0023] Figs. 4(a) and 4(b) include a timing diagram of the interleaved clocks and signals (Fig. 4(b)) and corresponds to the embodiment of Fig. 4 with Fig. 4(a) showing the signal correspondence therewith.

[0024] Fig. 5 depicts an embodiment of the 6th order filter utilized in the embodiment of Fig. 4 and also depicts an embodiment of the compensation network.

[0025] Fig. 5a depicts an embodiment of the 6th order filter utilized in the embodiment of Fig. 4 (which would preferably include, but does not show the compensation compensation network of Fig. 5), but shows control signals from the DSP for controlling the frequencies of the depicted LC networks and gains of the depicted transconductance amplifiers.

[0026] Fig. 5a-1 depicts a low speed DAC array used with the embodiment of Fig. 5a.

[0027] Figs. 6a-1, 6a-2, 6b-1 and 6b-2 depict two schemes for subtracting the feedback signal for the input signal (Figs. 6a-1 and 6b-1) and include more detailed corresponding possible circuit implementations (Figs. 6a-2 and 6b-2).

[0028] Fig. 7 is a block diagram showing the interleaving of two sub-ADCs.

[0029] Fig. 8 illustrates the fact that the interleaving of the DACs will preferably utilize an algorithm to interleave the separate Dynamic Element Matching (DEM) blocks.

[0030] Fig. 9 illustrates the a precision clock should be used with the disclosed $\Delta\Sigma$ modulator.

[0031] Fig. 9(a) is a jitter plot showing the effect of clock jitter from a 5-GHz and 10-GHz clock source on the SNR of an ideal 3-bit DAC driven by a delta-sigma modulated signal.

Detailed Description

[0032] A block diagram of the ΔΣ modulator 100 architecture of the present invention is illustrated by Fig. 2. The block diagram is shown for the most generic case: an N^{th} Order filter, an M time-wise interleaving factor, and K-bits in the quantizers of the depicted ADCs 102_1 - 102_M and the depicted DACs 106_1 - 106_M with a modulator clock rate of f_s. The architecture presented is different from a conventional continuous time ΔΣ modulator in that there is a bank 102 of interleaved Analog to Digital Converters (ADCs) 102_1 - 102_M in a forward path 104 and a bank 106 having an equal number of interleaved Digital to Analog Converters (DACs) 106_1 - 106_M in a feedback path 108. The input signal RF_{IN} is applied to a summing block 114 with the feedback path being subtracted at that summing block 116. The analog input characteristics (amplitude, frequency) of the RF_{IN} signal are encoded into a digital pulse stream which is applied to a DSP 200 which decimates the pulse string and when connected to the ΔΣ modulator 100 forms a ΔΣ ADC 101.

[0033] It should be noted that while Fig. 2 shows the input signal as being denominated as a RF or Radio Frequency signal, Fig. 2 and this invention may be used with an Intermediate Frequency (IF) signal instead. IF signals are produced, for example, by traditional superheterodyne receivers after one or more down conversions. As such, the input to summing block 114 may be an IF signal instead of an RF signal in certain embodiments, depending upon how the ΔΣ modulator 100 of Fig. 2 is utilized in practice. The disclosed modulator is capable of modulating the input signal 101 (RF or IF) having a carrier frequency f_c of 1 GHz or more and a bandwidth of 20 MHz and doing so with a dynamic range of 60 dB. These values are not limits on the invention, rather what is attainable today using commercially available components. As technology improves, an even better interleaved Delta-Sigma (ΔΣ) modulator capable of modulating even higher frequencies with even higher dynamic ranges will doubtlessly be possible following the teachings herein. Also, while the disclosed Delta-Sigma (ΔΣ) modulator is described herein as being useful with RF and IF signals (found in the radio art, for example), disclosed the Delta-Sigma (ΔΣ) modulator may be used in other applications outside of the radio arts if desired.

[0034] Bank 102 of $\Delta\Sigma$ modulator 100 of Fig. 2 may be referred to as an ADC herein while the individual ADCs 102_1 - 102_M may be referred to as either a plurality of ADCs or a plurality of sub-ADCs herein. Likewise bank 106 may be referred to as a DAC herein while the individual DACs 106_1 - 106_M may be referred to as either a plurality of DACs or a plurality of sub-DACs herein. All sub-ADCs 102_1 - 102_M are sampled at a reduced sampling rate of f_s/M and likewise the sub-DACs are sampled at the same reduced sampling rate of f_s/M. The number M should be the same for both the sub-ADCs 102_1 - 102_M and sub-DACs 106_1 - 106_M and the number M reflects the extent of interleaving that is occurring here (which also correspond to the numbers of sub-ADCs 102_1 - 102_M and sub-DACs 106_1 - 106_M which are utilized in the embodiment of Fig. 2). Typical values of M are binary values, for example 2, 4, 8 etc. Interleaving the ADC has the same effect as demultiplexing in the time domain (in the case of sub-ADCs 102_1 - 102_M) and interleaving the DAC has the same effect as multiplexing in the time domain (in the case of sub-DACs 106_1 - 106_M). A lowered output data rate of f_s/M eases the interface between the modulator of Fig. 2 and post-processing filter (a Digital Signal Processor or DSP 200) connected downstream of the modulator 100 shown in Fig. 2 thereby forming the Delta Sigma ADC 101. For example, if M=8 then the DSP 200 should be able to handle a clock rate of $f_s/8$ if the data rate is, for example 10 Gsps. If M=1 (and, hence no interleaving), then a hardware demultiplexer (demux) would likely be needed since a 10 Gsps data rate is probably too fast for current design DSPs. A track-and-hold circuit which commonly precedes interleaved ADCs is unnecessary because errors created in the forward path of the modulator are shaped by the feedback loop and have less consequence to the overall performance. Conversely, errors introduced in the feedback path from the sub-DACs 106_1 - 106_M should be addressed. There is no constraint on the filter order or type (e.g. bandpass or lowpass) of filter 112, however, the compensation network 110 for excess phase delay may become undesirably complex with higher order filters.

[0035] Interleaving occurs by controlling the clock inputs of the sub-ADCs 102_1 - 102_M and sub-DACs 106_1 - 106_M by means of a Multi-Phase Clock Driver 121. Exemplary clocks produced by the Multi-Phase Clock Driver 121 are exemplified in Fig. 2a which is a timing diagram of those clocks. Fig. 2a is a generalized illustration, and in the embodiment of the Multi-PhaseClock Driver 121 represented thereby, the clock phases are derived from the falling edge of

the master clock (fs). There will be pairs of clock signals that are 180 degrees out of phase with respect to one another, for example, $f_{\Phi 1}$ and $f_{\Phi M-1}$.

[0036] The filter 112 provides noise-shaping of the analog input signal RF_{IN} by placing the zeroes of the filter noise transfer function around the input signal carrier frequency (f_C) thus suppressing the quantization noise around it. The filtered signal is then sampled and quantized by the ADC 102. The digital output signal is converted back to an analog signal by a DAC 106 and fed back to the input for subtraction at block 114 to form a closed-loop operation. Post-filtering of the digital output signal is preferably performed in the DSP 200 to remove the out-of-band portion of the quantization error. Sampling the filtered signal at a rate much higher than the input signal bandwidth, a technique known as oversampling, in conjunction with post-process filter functions results in an effectively high-precision modulator 100 despite the use of relatively coarse sub-ADCs 102_1 - 102_M and sub-DACs 106_1 - 106_M. Coarse, in this context, means a few number of bits, such as, one to three. Preferably sub-ADCs 102_1 - 102_M and sub-DACs 106_1 - 106_M are each three bit devices. In comparison, a typical prior art ADC architecture would require 13 bits to achieve a dynamic range of 80dB. With the disclosed circuits, a dynamic range of 80dB can be achieved with sub-ADCs 102_1 - 102_M and sub-DACs 106_1 - 106_M implemented as three bit devices using a clock at f_s with a suitably small jitter.

[0037] The Nth order filter 112 is also coupled to the inputs (or outputs) of the sub-DACs 106_1 - 106_M preferably via a compensation network 110, which will be described in greater detail with respect to the embodiment of Fig. 4 which shows a particular embodiment of filter 112 (which embodiment utilized an Nth order filter with N=6) in greater detail. Whether the Nth order filter 112 is coupled to the inputs or outputs of the sub-DACs 106_1 - 106_M is discussed later herein.

[0038] Between the sub-ADCs sub-ADCs 102_1 - 102_M and the DSP 200 is a block 120 labeled "Data Out". This block 120, as will be seen, will include a decoder, a demultiplexer and possibly also output buffers, which are not depicted here for ease of illustration. See, for example the embodiments of Figs. 4 and 7 which depict such elements.

[0039] Interleaving alleviates many problems but complicates two aspects of the modulator design. The first problem is mismatch among the interleaved sub-DACs 106_1 - 106_M. These sub-DACs 106_1 - 106_M are each a K-bit (multi-bit) DAC. And as noted above, errors in the feedback path 108 directly influence overall modulator 100 performance. Specifically, the dynamic range of the DACs 106_1 - 106_M must meet the requirements of the full modulator 100. A power-efficient Dynamic Element Matching (DEM) network for the interleaved DACs 106 may be utilized if desired. See Fig. 7.

[0040] Fig. 2(a) is a timing diagram for a multi-phase clock driver 115 of Fig. 2. In this generalized illustration, the clock phases are derived from the falling edge of the master clock f_s. There will be pairs of clock signals that are 180 degrees out of phase with respect to one another, for example, as in the case of $f_{\Phi 1}$ and $f_{\Phi M-1}$. For an interleaving of M=2, the clock phases ($f_{\Phi 1}$ and $f_{\Phi 2}$) are half of the master clock frequency (f_s) and are 180 degrees out of phase with one another.

[0041] Fig. 4(b) is a timing diagram the interleaved clocks and signals and corresponds to the embodiment of Fig. 4. The signals shown on Fig. 4(b) are related back to the embodiment of Fig. 4 by Fig. 4(a) which is similar to Fig. 4, but the signals are labeled thereon to correspond with the timing diagram of Fig. 4(b). The exemplary timing diagram of Fig. 4(b)uses return-to-zero (RTZ) DACs which null the output current when the sample is not being evaluated. When RTZ sub-DACs are used, the output currents can be summed to produce the feedback current $I_{F/B}$. The use of non-return-to-zero (NRZ) DACs instead of RTZ sub-DACs would add complexity to the design.

[0042] The second problem introduced by interleaving is the effective increase in phase delay through the loop. Figs. 3(a) and 3(b) illustrate the increased challenge of excess loop delay in an interleaved architecture. The delay can degrade the performance of the loop and too much delay can result in an unstable modulator. Any practical ADC takes time to make a decision. Thus, the feedback DAC will have to be clocked at a time τD delayed from the sampling instant of the ADC as illustrated by Fig. 3(a). Since the ADCs in the proposed interleaved designs have a sampled clock period (which is the inverse of the frequency) that is multiplied by the

interleaving order (yielding f_s/M), the excess phase delay increases proportionally, since as is mentioned on Fig. 3(b), the reduced sampling rate in an interleaved design causes a multiplicative effect on excess loop delay. The compensation network employs techniques for mitigating the effects of the increased loop delay to restore the ideal noise transfer function. Such techniques as adding a direct path around the 1-bit feedback paths to interstage summation nodes in the filter and tuning the filter coefficients of filter 112 may be employed.

[0043] Figs. 3(c) and 3(d) show that interleaving the sub-ADCs and sub-DACs in a delta-sigma modulator 100 is not restricted to utilizing a band-pass filter 112 (see the band pass embodiment of filter 112 in Fig. 3(d)). The interleaving with a low-pass filter 112 embodiment (see the filter 112 of Fig. 3(c)) can offer a higher oversampling ratio to thereby obtain a further increase in dynamic range.

[0044] The proposed architecture is currently being reduced to practice for applications up to the cellular frequency band of 2.2 to 2.6 GHz. See Fig. 4 which is a block diagram of a $\Delta\Sigma$ modulator in accordance with a more specific embodiment the present invention where K=3, M=2 and N=6. Modulator design parameters are being chosen as a compromise between aggressive dynamic range goals (> 100dB), low power dissipation (< 500 mW), and practical technology limits. A summary of the modulator being reduced to practice is provided in in Table I below and a simplified block diagram is shown in Fig 4.

[0045] Table I: Modular Design Parameters for the embodiment of Fig. 4

Parameter		Reasoning
Filter Order of Filter 112	N = 6	Passive resonator approach must have even order and N=4 is insufficient to reach our dynamic range goals
Interleave Factor	M = 2	Optimum trade-off between power and the reduced clock rate fs/M
Quantizer Bits of the ADCs 102 and DACs 106	K = 3	Compromise between DAC performance and achievable modulator dynamic range.

[0046] A first embodiment of the 6th order filter 112 of the embodiment of Fig. 4 is shown in greater detail by Fig. 5. The filter 112 of the embodiment of Fig. 5 has three passive resonators L1-L3, multiple transconductance amplifiers T1-T8, and three integrators I1-I3. The configuration of the filter 112 in this embodiment is a feed-forward architecture – signals are being fed from earlier resonator stages into the final summing node FSN. Though a feedback architecture may offer more out-of-band noise shaping, a feed-forward architecture gives more flexibility in designing a stable modulator. This embodiment utilizes passive resonators L1-L3 because they have lower noise figures, higher linearity, require less power, and can operate at higher carrier frequencies than active resonators. Of course, some may elect to use active filters and/or a feedback architecture for the filter 112 if they wish. The quality factor, or Q, of each resonator L1-L3 is primarily set by the (inherent) series resistance of the inductor in each resonator. The tank values, amplifier transconductances, and integrator parameters of the filter can be determined by defining the desired noise transfer function, extracting the coefficients from the expression, then translating the coefficients into circuit parameters. Exemplary values for the inductors and capacitors making up resonators L1-L3 for a filter 112 having a passband from 2.0 to 2.4 GHz are given in Table II below

[0047] Table II: Exemplary Inductor and Capacitor Values for L1 - L3

L1	L2	L3
2.5 nH	2.5 nH	2.5 nH
3.62 pF	3.70 pF	3.74 pF

[0048] The compensation network 110 (two identical networks 110-1 and 110-2 are depicted for the embodiment of Fig. 5, one for each of the two 3-bit busses since M=2 in the embodiment of Fig. 4) is a generalized diagram showing three DACs 122 being driven by encoded digital data (from the inputs of DACs 106_1 and 106_2 - see Fig. 4) and feeding back to internal filter nodes of the filter 112. In the simplest form, each compensation network 110-1 and 110-2 might comprise a plurality of single 1-bit DACs 122 each driven by the most significant bit from one of sub-ADCs 102_1 and 102_2 and feeding back to the final summation node FSN of the filter 112. The depiction of Fig. 5 is more generalized in that there is a separate 1-bit DAC for

each of the 3 bits of each of the two 3-bits busses in the depicted embodiment of the compensation network 110. Also, the depicted 1-bit DACs could be connected to the outputs of sub-DACs 106_1 and 106_2 instead of their inputs. However, the 1-bit DACs are preferably connected to the inputs of sub-DACs 106_1 and 106_2 since, at the inputs of sub-DACs 106_1 and 106_2, the digital codes are voltage values while while at the outputs the data there is expressed in values of current.

[0049] The embodiment of filter 112 shown in Fig. 5 has fixed resonators L1-L3 and the gains of the transconductance amplifiers T1-T8 are also fixed. However more design flexibility results if the frequencies of the tank circuits (resonators) L1-L3 can be varied and if the gain of the transconductance amplifiers T1-T8 can likewise be varied. Such an embodiment of the filter is depicted by Fig. 5a. Turning to Fig. 5a, this figure depicts an embodiment of the filter 112 for tuning across a band of carrier frequencies (fc). Frequency notch control data, preferably the form of bits from DSP 200, are sent to control variable capacitors in the L1-L3 resonators to change the values of capacitance and thereby affect a change in the filter's notch frequency. To keep the modulator stable, coefficients, which are applied to the transconductance amplifiers T1-T8, modify their gains which gains are preferably varied as the notch changes location within the bandpass filter. The embodiment of Fig. 5a preferably continues to utilize compensation networks 110-1 and 110-2 shown in Fig. 5, but which they not depicted on Fig. 5a simply for ease of illustration.

[0050] In the embodiment of Fig. 5a frequency notch control bits preferably provided by DSP 200 control the resonant frequencies of resonators L1-L3 by varying the depicted variable capacitors. To do that, each depicted variable capacitor preferably comprises a bank of capacitors which are switched in or out of each resonator according to a multi-bit digital code from DSP 200. Alternatively, or in addition, the depicted inductor in each resonator L1-L3 may effectively be made variable by providing a bank of inductors which are switched in or or of the resonator by a multi-bit digital code from DSP.

[0051] The bank of capacitors (or inductors) may comprises, for example, a bank of 32 capacitors (or inductors) which can be be switched in and out of the resonator by a five bit code

from the DSP 200. If 32 capacitors and 32 inductors are utilized in each resonator, then both capacitors and inductors can be switched in and out, and the frequency notch control data should then be a ten bit code for each resonator.

[0052] The gains of the transconductance amplifiers T1-T8 are preferably also controlled from the DSP 200 in the embodiment of Fig. 5a as the notch and the desired carrier frequency changes. Fig. 5a includes a block 125 labeled Low Speed DAC Array. The Low Speed DAC Array 125 is shown in greater detail by Fig. 5a-1. In Fig. 5a-1 a single-bit digital data stream from DSP 200 is applied to a serial to parallel converter 126 along with a clock (which may a relatively slow speed in the kHz to low MHz range). The parallel outputs of the serial to parallel converter 126 are applied to a number of multi-bit DACs 128, one for each of the transconductance amplifiers T1-T8. The number of bits converted by each DAC 128 need not be the same. Some DACs may convert more bits that other DACs 128, so one is labeled a p-bit DAC while another one is labeled a n-bit DAC. The number of bits converted by each DAC 128 will depend on the amount of coarseness tolerated in applying the the aforementioned coefficients to the transconductance amplifiers T1-T8.

[0053] In the embodiment of Fig. 4 the Low-Noise Transconductance Amplifier (LNTA) is depicted as occurring prior to the summing block 116. This summing block 116 LNTA combination is shown schematically again by Fig. 6a-1 and Fig. 6a-2 depicts in greater detail how those summing block 116 might be implemented. The LNTA can occur after the summing block 116 as is schematically shown by Fig. 6b-1 while Fig. 6b-2 depicts in greater detail how the summing block 116 in that embodiment might be implemented.

[0054] These two approaches (see Figs. 6a-1 and 6b-1) for subtracting the feedback signal coming from the DACs 106 from the input signal RF_{IN}. "Subtraction" is really the summation of the inverted feedback value with the input signal RF_{IN}. The summation can be done as a current summation or voltage summation. Current summation is a broadband operation – the junction does not introduce delay and will not limit bandwidth. The disadvantage is that a higher signal amplitude is presented to the LNTA making it a more difficult component to design. When the subtraction precedes the LNTA as shown in he embodiment of Figs. 6b-1 and 6b-2, only the error

signal is presented to the LNTA so higher dynamic range operation is possible. Additionally the coupler can have a dual-use when RF cancellations are needed. The disadvantage of this approach is that the coupler adds delay and may cause the modulator 100 to be unstable. The first resonator L1 of the filter 112 is depicted in Figs. 6a-2 and 6b-2 for clarity of understanding. So the outputs of these circuits of Figs. 6a-2 and 6b-2 are applied at junction J of Fig. 5 since there is no need to repeat the first resonator L1.

[0055] Fig. 7 is a block diagram showing the interleaving of two sub-ADCs using preferably using flash architectures devices. Each sub-ADC 102_1 and 102_2 has a ladder and comparator bank to generate a thermometer code for the downstream sub-DACs 106_1 and 106_2. The decoders convert the thermometer code to binary to reduce the I/O count from 8 to 3 and the demultipexer (DEMUX) reduces the output data rate so that the DSP 200 can process the modulator 100 data. The sub-ADCs 102_1 and 102_2 are clocked 180 degrees out of phase with respect to each other and thus alternately sample the input analog data (from Filter 112). Sample-and-hold amplifiers (SHA) are commonly used at the front-end of an interleaved ADC to minimize timing errors but are challenging designs since they must operate at the full clock rate of 10.4 GHz in this embodiment. Errors introduced in the feedback path of the modulator, such as non-linearities from a multi-bit DAC, directly affect the performance of the modulator whereas errors in the forward path of the modulator are shaped by the closed loop feedback configuration. Since the errors of the sub-ADCs 102_1 and 102_2 are shaped by the modulator, the SHAs may be omitted when the interleaved ADCs are used in the disclosed modulator 100. Each sub-ADC is clocked at 5.2 GHz in this embodiment and produce a thermometer code at 5.2 Gigasamples per second (5.2 Gsps).

[0056] Fig. 8 illustrates the fact that the interleaving of the DAC will preferably utilize an algorithm to interleave the separate Dynamic Element Matching (DEM) blocks. The randomized outputs of the DEM block will drive the depicted unary current source switches. Only the output summation block need support 10.4 Gsps operation assuming a M=2 interleave with a 5.2 Gsps thermometer code going into the DAC. Dynamic element matching has been well studied in literature. See, for example, the article by Ian Galton, "Why Dynamic-Element-Matching DACs Work", *IEEE Transactions on Circuits and Systems – II:Express Briefs, Vol. 57, No. 2, Feb.*

2010, pp. 69-74 incorporated herein by reference. The idea is to "randomly" assign the connection between a latch and a unary current source. By doing this, any errors from process mismatch in making the DACs get distributed so spurious signals start to look like flat white noise and the dynamic range improves. DEM is well known in the art of DAC design and therefore it is not further discussed here.

[0057] Fig. 9 depicts the clock source f_s which needs to have ultra low jitter or ultimately the clock source will establish the noise floor and the noise from clock source is not shaped by the modulator. Fig. 9(a) is a plot showing the effect of clock jitter from a 5-GHz and 10-GHz clock source on SNR of an ideal 3-Bit DAC driven by a delta-sigma modulated signal. The trend shows a degradation in SNR of about 6dB for every doubling of the clock jitter. To attain 80dB of dynamic range, the clock generating f_s should have less than 30 fsec of RMS clock jitter based on the phase noise of the clock beyond 100 KHz. Such clocks are commercially available from Crystek of Fort Myers, Florida, and a high quality clock with low jitter clock with relatively low jitter should be utilized if a high dynamic range of, say, 80 dB is desired.

[0058] Having now described the invention in accordance with the requirements of the patent statutes, those skilled in this art will understand how to make changes and modifications to the present invention to meet their specific requirements or conditions. Such changes and modifications may be made without departing from the scope and spirit of the invention as disclosed herein.

[0059] This concludes the description of embodiments of the present invention. The foregoing description of these embodiments and the methods of making same has been presented for the purposes of illustration and description and it should now be apparent that the present invention has the following features and/or concepts:

[0060] Concept 1: A modulator comprising: a forward path coupling a input summing block with an data out block, the forward path including at least a Nth order filter coupled to said input summing block and a plurality of interleaved multi-bit Analog to Digital Converters (ADCs), the interleaved multi-bit ADCs the having inputs which are coupled to said Nth order filter and

outputs which are coupled to said data out block; and a feedback path including a plurality of interleaved multi-bit Digital to Analog Converters (DACs), the interleaved multi-bit DACs having inputs which are coupled to respective outputs of the interleaved multi-bit ADCs, the interleaved multi-bit DACs having outputs which are summed together and applied to said input summing block, with connections from the interleaved multi-bit DACs to the the Nth order filter.

[0061] Concept 2: The modulator of concept 1 wherein the data out block includes at least a decoder and a demultiplexer coupled in series between the outputs of the interleaved multi-bit ADCs and an output of the modulator.

[0062] Concept 3: The modulator of concepts 1 or 2 wherein the interleaved multi-bit ADCs output digital data in a thermometer code and the decoder translates thermometer coded data from the interleaved multi-bit ADCs into a gray or binary code.

[0063] Concept 4: The modulator of any one of more of the preceding concepts wherein the input summing block combines an input RF stream of analog data to the modulator with the outputs of the interleaved multi-bit DACs, so that, in use, analog data at the outputs of the interleaved multi-bit DACs is subtracted from the input RF stream of analog data.

[0064] Concept 5: The modulator of concept 4 wherein the input summing block includes a Low Noise Transconductance Amplifier (LNTA) which has an input thereof coupled to the input RF stream of analog data and an output connected to the outputs of the interleaved multi-bit DACs and to an input of the Nth order filter.

[0065] Concept 6: The modulator of concept 4 wherein the input summing block includes a coupler having inputs coupled to he input RF stream of analog data and to the outputs of the interleaved multi-bit DACs and at least one output, the input summing block further including a Low Noise Transconductance Amplifier (LNTA) which has an input thereof coupled the at least one output of said coupler and having an output coupled to an input of the Nth order filter.

[0066] Concept 7: The modulator of any one of more of the preceding concepts wherein the connections from the interleaved multi-bit DACs to the Nth order filter include at least one stability compensation circuit.

[0067] Concept 8: The modulator of concept 7 wherein the stability compensation circuit has inputs coupled at the inputs of the interleaved multi-bit DACs and at least one output coupled to a final summing node in said Nth order filter.

[0068] Concept 9: The modulator of concept 8 wherein said final summing node in said Nth order filter receives the most significant bits available at the inputs of the interleaved multi-bit DACs via a plurality of one-bit DACs.

[0069] Concept 10: The modulator of any one of more of concepts 7 - 9 wherein the stability compensation circuit has a plurality one-bit DACs coupling data available at the inputs of the interleaved multi-bit DACs to summing nodes within said Nth order filter.

[0070] Concept 11: The modulator of any one of more of concepts 7 - 9 wherein the stability compensation circuit has a plurality one-bit DACs coupling data available at the outputs of the interleaved multi-bit DACs to summing nodes within said Nth order filter.

[0071] Concept 12: The modulator of any one of more of the preceding concepts wherein the Nth order filter is a bandpass filter.

[0072] Concept 13: The modulator of any one of more of the concepts 1-11 wherein the Nth order filter is a lowpass filter.

[0073] Concept 14: The modulator of any one of more of the concepts 1-11 wherein the Nth order filter is a 6th order filter having three resonant circuits therein.

[0074] Concept 15: The modulator of any one of more of the preceding concepts wherein the plurality of interleaved multi-bit ADCs comprise a pair of interleaved three-bit ADCs, wherein the plurality of interleaved multi-bit DACs comprise a pair of interleaved three-bit DACs.

[0075] Concept 16: The modulator of any one of more of the preceding concepts wherein the plurality of interleaved multi-bit ADCs comprise a plurality of ladder circuits each coupled in series with a comparator circuit for generating a digital thermometer code corresponding to analog data provided to said ladder circuits.

[0076] Concept 17: The modulator of any one of any one of more of the preceding concepts wherein the Nth order filter has a plurality, and preferably N/2. resonators coupled in series between a filter input and a filter output.

[0077] Concept 18: The modulator of concept 17 wherein the resonators have fixed resonate frequencies.

[0078] Concept 19: The modulator of concept 17 wherein the resonators have variable resonate frequencies set by digitally controlled filter values.

[0079] Concept 20: The modulator of concept 19 wherein the digitally controlled filter values are derived from a digital signal processor coupled to said data out block.

[0080] Concept 21: The modulator of concept 18 further including a plurality of multi-bit DACs having inputs controlled by said digital signal processor and having outputs coupled to a plurality of transconductance amplifiers in said Nth for filter for controlling the gains thereof.

[0081] Concept 22: A analog to digital converter comprising the modulator of claim 2 and a decimator coupled to the output of the modulator of claim 2.

[0082] Concept 23: A method increasing the dynamic range of a $\Delta\Sigma$ modulator comprising: providing a plurality of ADCs and a plurality of DACs, the plurality of ADCs and DCAs being connected in a loop; coupling the plurality of ADCs with an incoming analog signal; controlling said plurality of ADCs and plurality of DACs with a plurality of clock signals, the clock signals in said plurality of clock signals being offset relative to each other in the time domain thereby enabling each ADC in said plurality of ADCs one at a time and enabling each DAC in said plurality of DACs one at a time such that the $\Delta\Sigma$ modulator processes data in said incoming analog signal in an interleaved fashion.

[0083] Concept 24: The method of concept 23 further including increasing a number of bits processed in parallel by each ADC in said plurality of ADCs and each DAC in said plurality of DACs such that each each ADC in said plurality of ADCs is a multibit ADC and each DAC in said plurality of DACs is a multibit DAC.

[0084] Concept 25: The method of concept 23 wherein the number of ADCs in said plurality of ADCs is equal to M and the number of bits processed a one time by each of said ADCs is equal to K, with M preferably being equal to 2 and K preferably being equal to 3.

[0085] Concept 26: The method of any one of concepts 23-25 further including applying the incoming analog signal to a summing junction along with outputs from the plurality of DACs and filtering data output from the summing junction by an Nth order filter and applying an output of the Nth order filter to the plurality of ADCs in said interleaved fashion.

[0086] This list and the disclosed embodiments are not intended to be exhaustive or to limit the invention to the precise embodiments, forms and/or methods disclosed. Many modifications and variations are possible in light of the above teachings. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

[0087] The foregoing Detailed Description of exemplary embodiments is presented for purposes of illustration and disclosure in accordance with the requirements of the law. It is not

intended to be exhaustive nor to limit the invention to the precise form(s) described, but only to enable others skilled in the art to understand how the invention may be suited for a particular use or implementation. The possibility of modifications and variations will be apparent to practitioners skilled in the art. No limitation is intended by the description of exemplary embodiments which may have included tolerances, feature dimensions, specific operating conditions, engineering specifications, or the like, and which may vary between implementations or with changes to the state of the art, and no limitation should be implied therefrom. Applicant has made this disclosure with respect to the current state of the art, but also contemplates advancements and that adaptations in the future may take into consideration of those advancements, namely in accordance with the then current state of the art. It is intended that the scope of the invention be defined by the Claims as written and equivalents as applicable. Reference to a claim element in the singular is not intended to mean "one and only one" unless explicitly so stated. Moreover, no element, component, nor method or process step in this disclosure is intended to be dedicated to the public regardless of whether the element, component, or step is explicitly recited in the Claims. No claim element herein is to be construed under the provisions of 35 U.S.C. Sec. 112, sixth paragraph, unless the element is expressly recited using the phrase "means for ..." and no method or process step herein is to be construed under those provisions unless the step, or steps, are expressly recited using the phrase "comprising the step(s) of ...".

[0082] All elements, parts and steps described herein are preferably included. It is to be understood that any of these elements, parts and steps may be replaced by other elements, parts and steps or deleted altogether as will be obvious to those skilled in the art.

[0083] Broadly, this writing discloses at least the following:

A delta sigma modulator which has improved the dynamic range. The ΔΣ modulator has a plurality of ADCs and a plurality of DACs, the plurality of ADCs and DACs are connected in a loop. The plurality of ADCs are coupled with an incoming analog signal. A clock generator provides a plurality of clock signals which control the plurality of ADCs and the plurality of DACs, the clock signals being offset relative to each other in the time domain thereby enabling each ADC in the plurality of ADCs one at a time and each DAC in the plurality of DACs one at a time so that the ΔΣ modulator processes data in the incoming analog signal in an interleaved fashion. The delta sigma modulator has an Nth order filter in a forward path of the loop.

What is claimed is:

1. A modulator comprising:
   a. a forward path coupling a input summing block with an data out block, the forward path including at least a Nth order filter coupled to said input summing block and a plurality of interleaved multi-bit Analog to Digital Converters (ADCs), the interleaved multi-bit ADCs the having inputs which are coupled to said Nth order filter and outputs which are coupled to said data out block; and
   b. a feedback path including a plurality of interleaved multi-bit Digital to Analog Converters (DACs), the interleaved multi-bit DACs having inputs which are coupled to respective outputs of the interleaved multi-bit ADCs, the interleaved multi-bit DACs having outputs which are summed together and applied to said input summing block, with connections between the interleaved multi-bit DACs and the Nth order filter.

2. The modulator of claim 1 wherein the data out block includes at least a decoder and a demultiplexer coupled in series between the outputs of the interleaved multi-bit ADCs and an output of the modulator.

3. The modulator of claim 2 wherein the interleaved multi-bit ADCs output digital data in a thermometer code and the decoder translates thermometer coded data from the interleaved multi-bit ADCs into a gray or binary code.

4. The modulator of any one of claims 1-3 wherein the input summing block combines an input RF stream of analog data to the modulator with the outputs of the interleaved multi-bit DACs, so that, in use, analog data at the outputs of the interleaved multi-bit DACs is subtracted from the input RF stream of analog data.

5. The modulator of claim 4 wherein the input summing block includes a Low Noise Transconductance Amplifier (LNTA) which has an input thereof coupled to the input RF stream of analog data and an output connected to the outputs of the interleaved multi-bit DACs and to an input of the Nth order filter.

6. The modulator of claim 4 wherein the input summing block includes a coupler having inputs coupled to he input RF stream of analog data and to the outputs of the interleaved multi-bit DACs and at least one output, the input summing block further including a Low Noise Transconductance Amplifier (LNTA) which has an input thereof coupled the at least one output of said coupler and having an output coupled to an input of the Nth order filter.

7. The modulator of claims 1-3 wherein the connections from the interleaved multi-bit DACs to the Nth order filter include at least one stability compensation circuit.

8. The modulator of claim 7 wherein the stability compensation circuit has inputs coupled at the inputs of the interleaved multi-bit DACs and at least one output coupled to a final summing node in said Nth order filter.

9. The modulator of claim 8 wherein said final summing node in said Nth order filter receives the most significant bits available at the inputs of the interleaved multi-bit DACs via a plurality of one-bit DACs.

10. The modulator of claim 7 wherein the stability compensation circuit has a plurality one-bit DACs coupling data available at the inputs of the interleaved multi-bit DACs to summing nodes within said Nth order filter.

11. The modulator of claim 7 wherein the stability compensation circuit has a plurality one-bit DACs coupling data available at the outputs of the interleaved multi-bit DACs to summing nodes within said Nth order filter.

12. The modulator of any one of claims 1-3 wherein the Nth order filter is a bandpass filter.

13. The modulator of any one of claims 1-3 wherein the Nth order filter is a lowpass filter.

14. The modulator of of any one of claims 1-3 wherein the Nth order filter is a 6th order filter having three resonant circuits therein.

15. The modulator of claim 12 wherein the plurality of interleaved multi-bit ADCs comprise a pair of interleaved three-bit ADCs, wherein the plurality of interleaved multi-bit DACs comprise a pair of interleaved three-bit DACs.

16. The modulator of any one of claims 1-3 wherein the plurality of interleaved multi-bit ADCs comprise a plurality of ladder circuits each coupled in series with a comparator circuit for generating a digital thermometer code corresponding to analog data provided to said ladder circuits.

17. The modulator of any one of claims 1-3 wherein the Nth order filter has a plurality, and preferably N/2, resonators coupled in series between a filter input and a filter output.

18. The modulator of claim 17 wherein the resonators have fixed resonate frequencies.

19. The modulator of claim 17 wherein the resonators have variable resonate frequencies set by digitally controlled filter values.

20. The modulator of claim 18 wherein the digitally controlled filter values are derived from a digital signal processor coupled to said data out block.

21. The modulator of claim 18 further including a plurality of multi-bit DACs having inputs controlled by said digital signal processor and having outputs coupled to a plurality of transconductance amplifiers in said Nth for filter for controlling the gains thereof.

22. A analog to digital converter comprising the modulator of claim 2 and a decimator coupled to the output of the modulator of claim 2.

23. A method increasing the dynamic range of a $\Delta\Sigma$ modulator comprising;

providing a plurality of ADCs and a plurality of DACs, the plurality of ADCs and DCAs being connected in a loop;

coupling the plurality of ADCs with an incoming analog signal;

controlling said plurality of ADCs and plurality of DACs with a plurality of clock signals, the clock signals in said plurality of clock signals being offset relative to each other in the time domain thereby enabling each ADC in said plurality of ADCs one at a time and enabling each DAC in said plurality of DACs one at a time such that the $\Delta\Sigma$ modulator processes data in said incoming analog signal in an interleaved fashion.

24. The method of claim 23 further including increasing a number of bits processed in parallel by each ADC in said plurality of ADCs and each DAC in said plurality of DACs such that each each ADC in said plurality of ADCs is a multibit ADC and each DAC in said plurality of DACs is a multibit DAC.

25. The method of claim 24 wherein the number of ADCs in said plurality of ADCs is equal to M and the number of bits processed a one time by each of said ADCs is equal to K, with M preferably being equal to 2 and K preferably being equal to 3.

26. The method of any one of claims 23 - 25 further including applying the incoming analog signal to a summing junction along with outputs from the plurality of DACs and filtering data output from the summing junction by an Nth order filter and applying an output of the Nth order filter to the plurality of ADCs in said interleaved fashion.

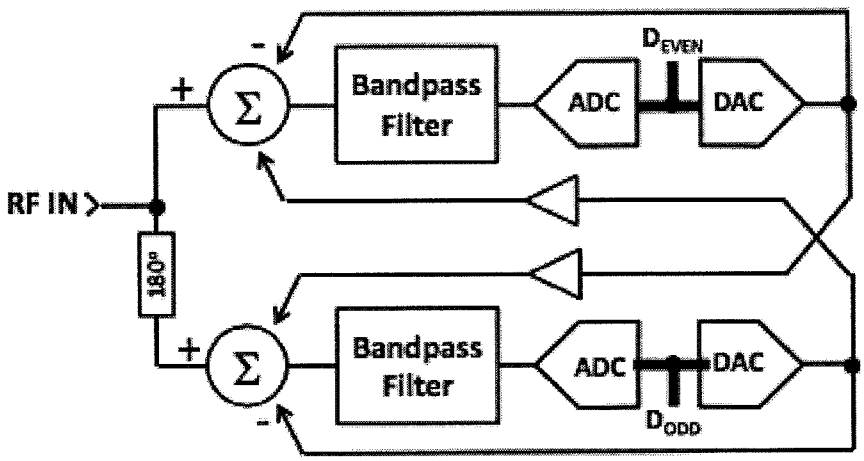
RF IN
180°
Σ
Σ
+
-
+
-
Bandpass Filter
Bandpass Filter
ADC
ADC
DAC
DAC
D_{EVEN}
D_{ODD}

Fig.1 (a)

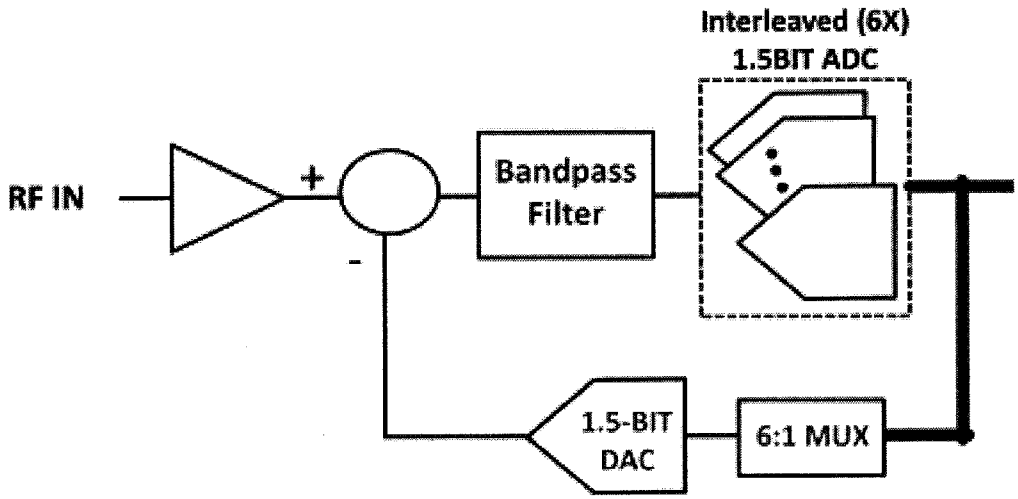
Interleaved (6X)
1.5BIT ADC
RF IN
+
-
Bandpass Filter
1.5-BIT DAC
6:1 MUX

Fig.1 (**b**)

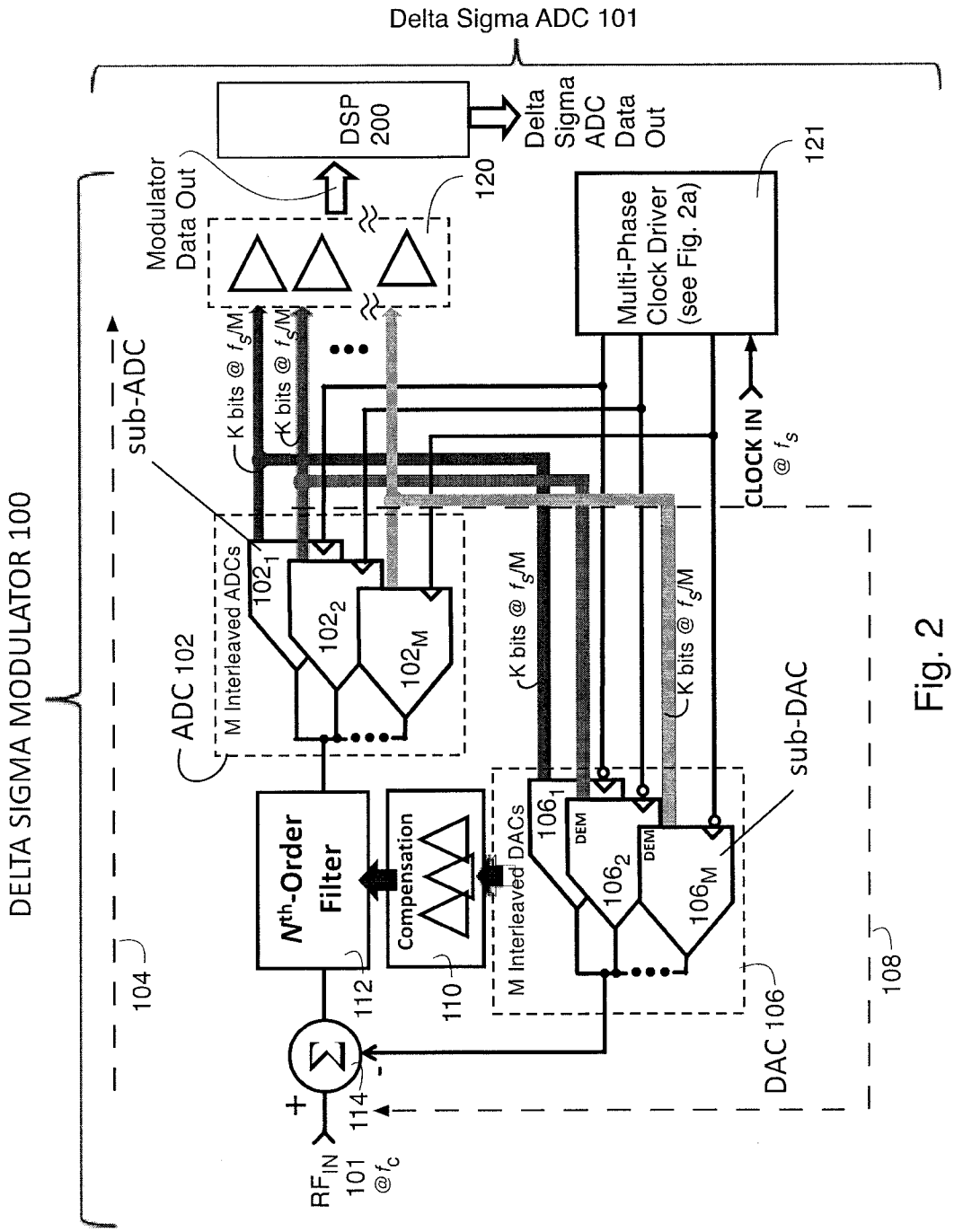
Delta Sigma ADC 101
DSP 200
Delta Sigma ADC Data Out
120
121
Modulator Data Out
Multi-Phase Clock Driver (see Fig. 2a)
CLOCK IN @ f_s
DELTA SIGMA MODULATOR 100
sub-ADC
K bits @ f_s/M
ADC 102
M Interleaved ADCs
102_1
102_2
102_M
sub-DAC
106_1
106_2
106_M
DEM
M Interleaved DACs
N^{th}-Order Filter
Compensation
104
110
112
114
108
DAC 106
RF_{IN} 101 @ f_c

Fig. 2

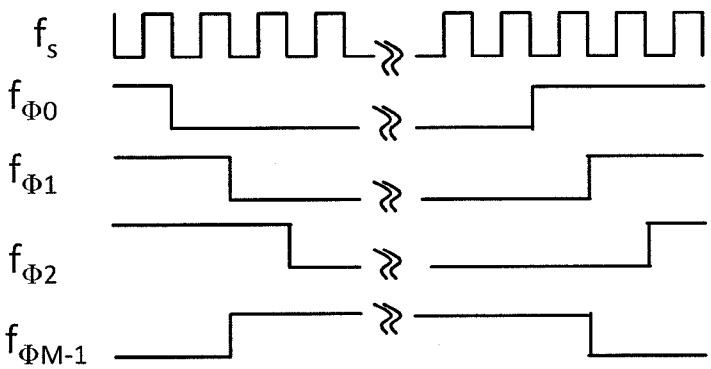

Fig. 2a

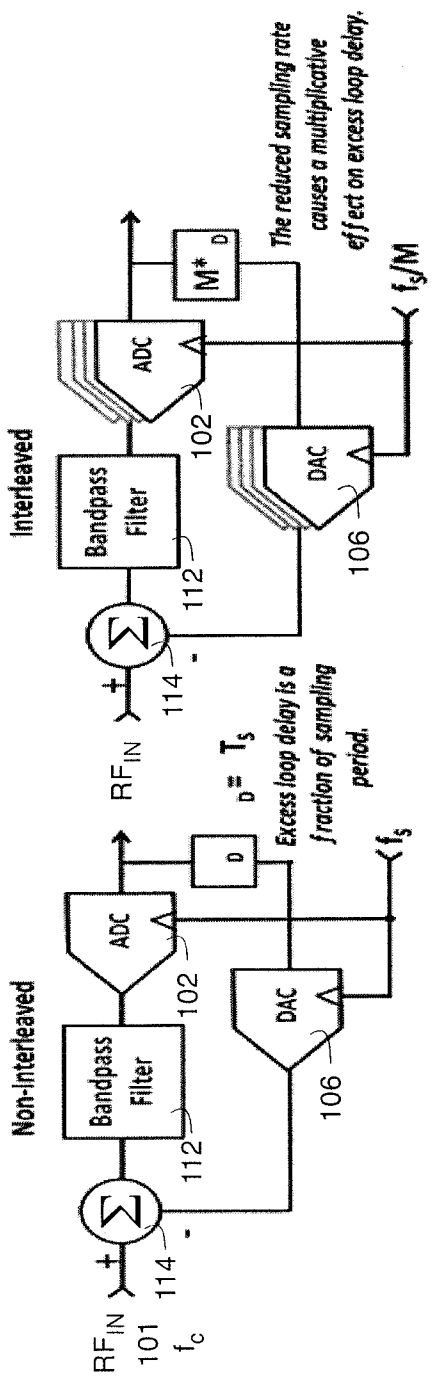
Non-Interleaved
RF_IN
101
f_c
114
112
Bandpass Filter
ADC
102
D
D = T_s
Excess loop delay is a fraction of sampling period.
f_s
DAC
106
RF_IN
Interleaved
114
112
Bandpass Filter
ADC
102
M* D
The reduced sampling rate causes a multiplicative effect on excess loop delay.
f_s/M
DAC
106

Fig. 3(a)

Fig. 3(b)

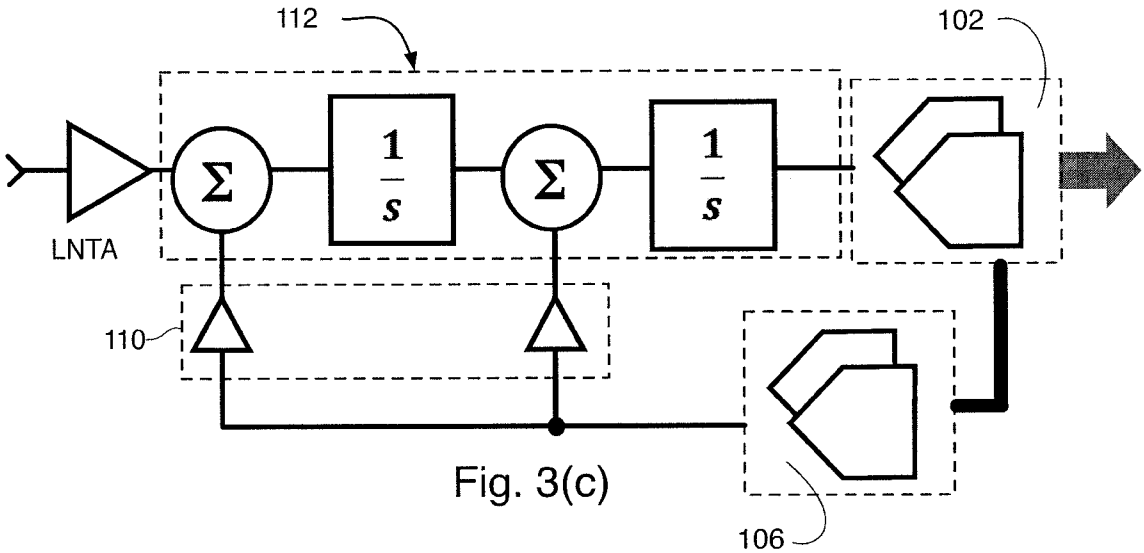
112
102
LNTA
Σ
1/s
Σ
1/s
110
106

Fig. 3(c)

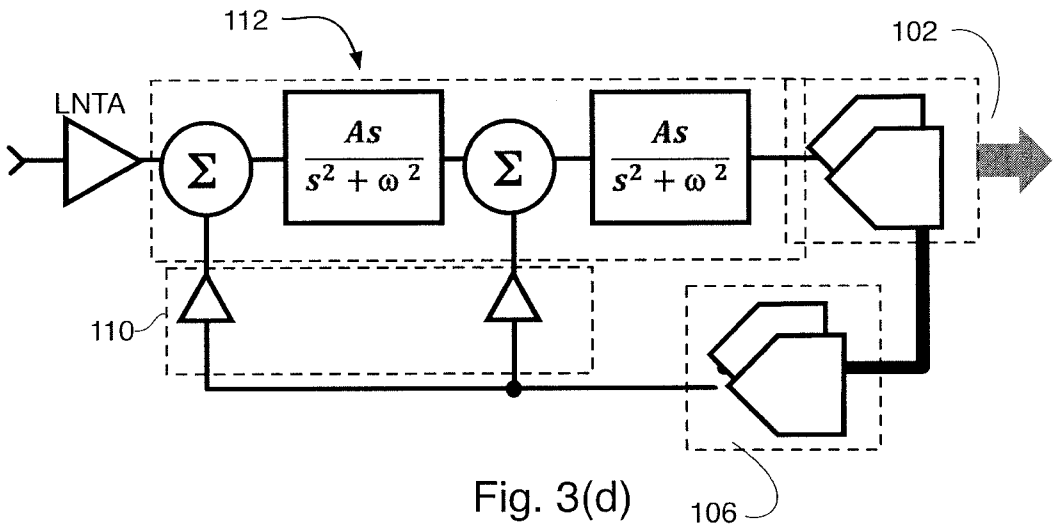
112
102
LNTA
Σ
As/(s² + ω²)
Σ
As/(s² + ω²)
110
106

Fig. 3(d)

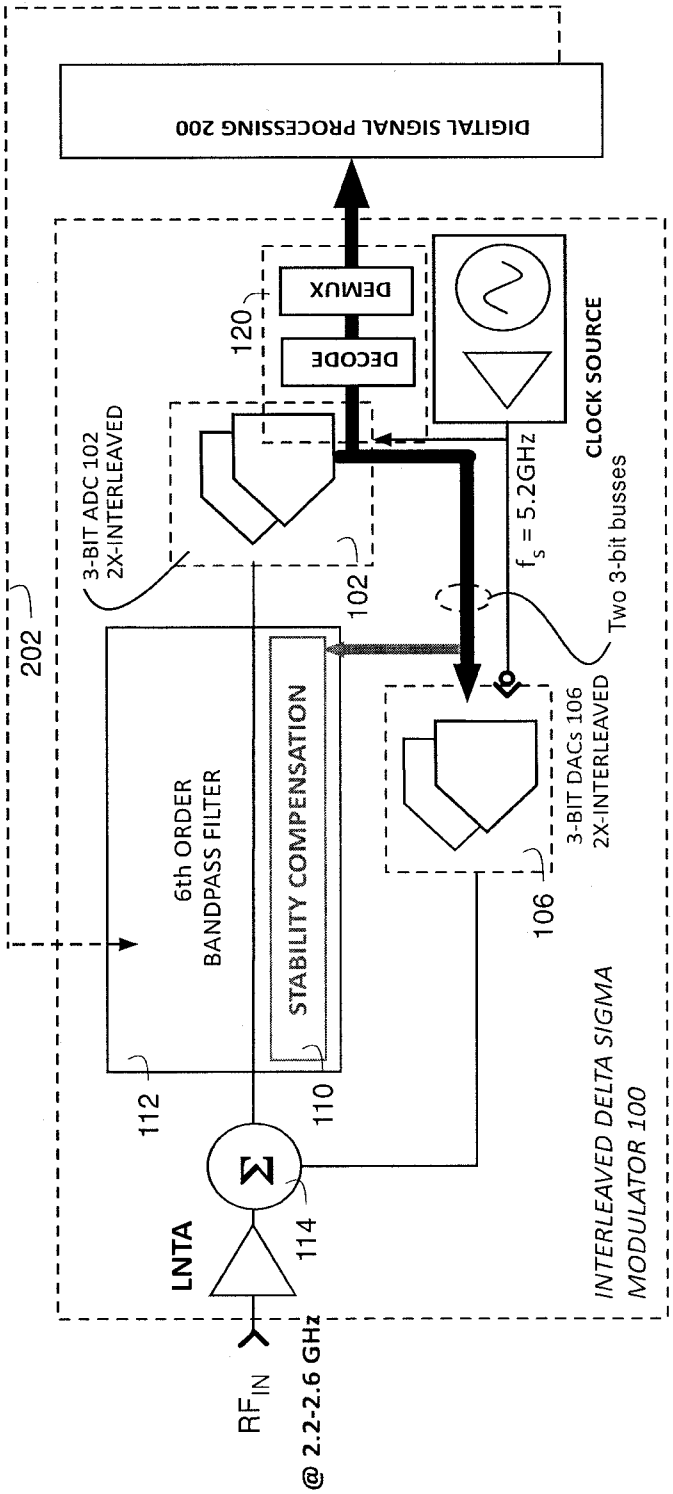
DIGITAL SIGNAL PROCESSING 200
DEMUX
DECODE
120
CLOCK SOURCE
f_s = 5.2GHz
Two 3-bit busses
3-BIT ADC 102
2X-INTERLEAVED
102
202
6th ORDER
BANDPASS FILTER
STABILITY COMPENSATION
3-BIT DACs 106
2X-INTERLEAVED
106
112
110
LNTA
114
RF_{IN}
@ 2.2-2.6 GHz
INTERLEAVED DELTA SIGMA
MODULATOR 100

Fig. 4

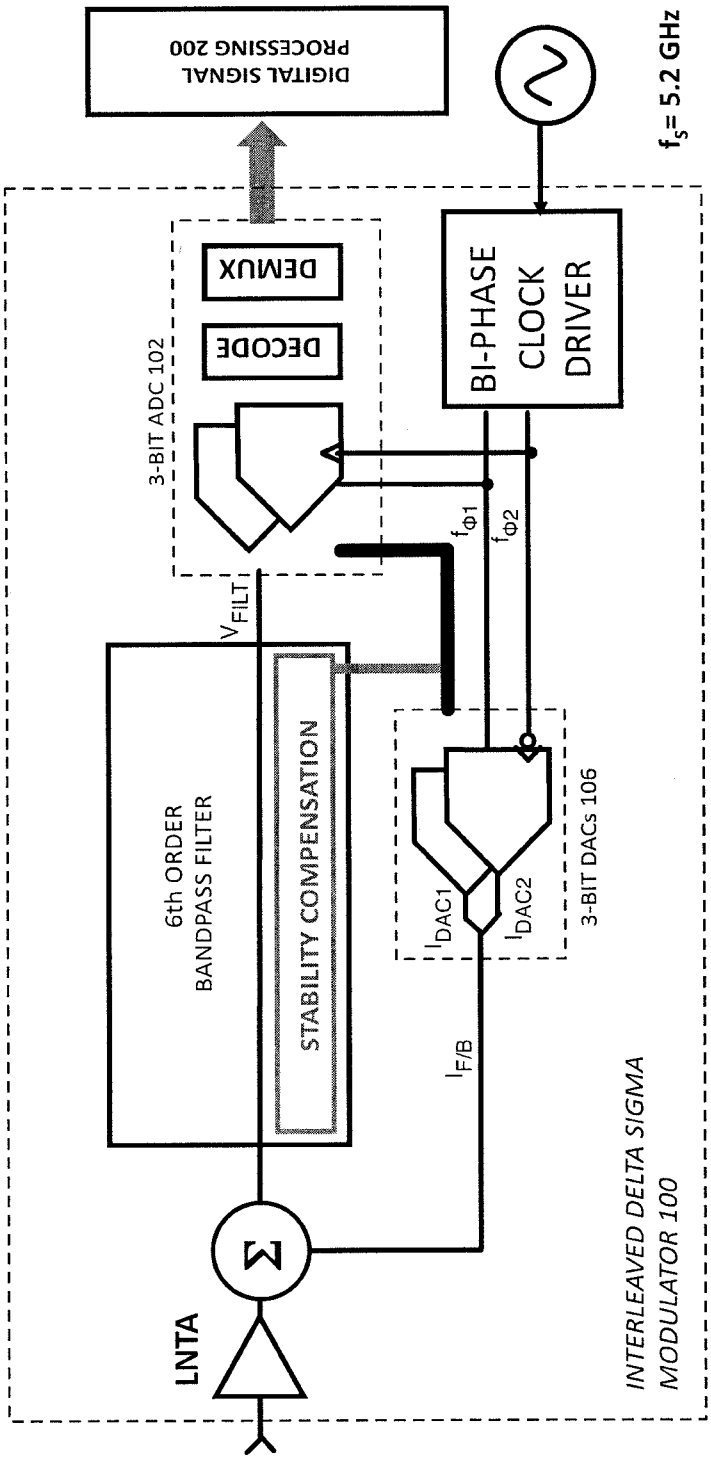
DIGITAL SIGNAL PROCESSING 200
f_S= 5.2 GHz
BI-PHASE CLOCK DRIVER
DEMUX
DECODE
3-BIT ADC 102
$f_{\Phi 1}$
$f_{\Phi 2}$
V_{FILT}
6th ORDER BANDPASS FILTER
STABILITY COMPENSATION
I_{DAC1}
I_{DAC2}
3-BIT DACs 106
$I_{F/B}$
Σ
LNTA
INTERLEAVED DELTA SIGMA MODULATOR 100

Fig. 4(a)

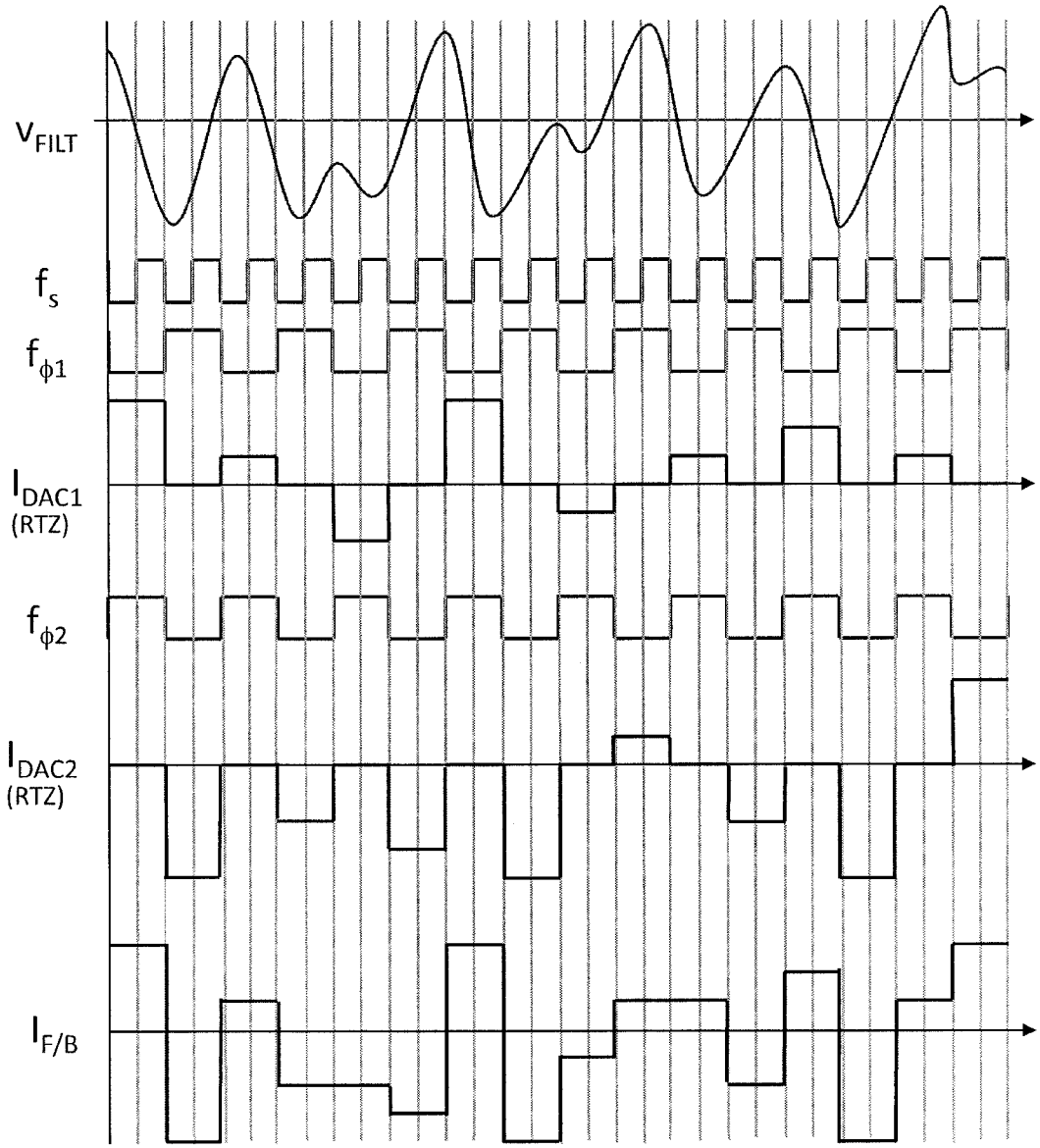

Fig. 4(b)

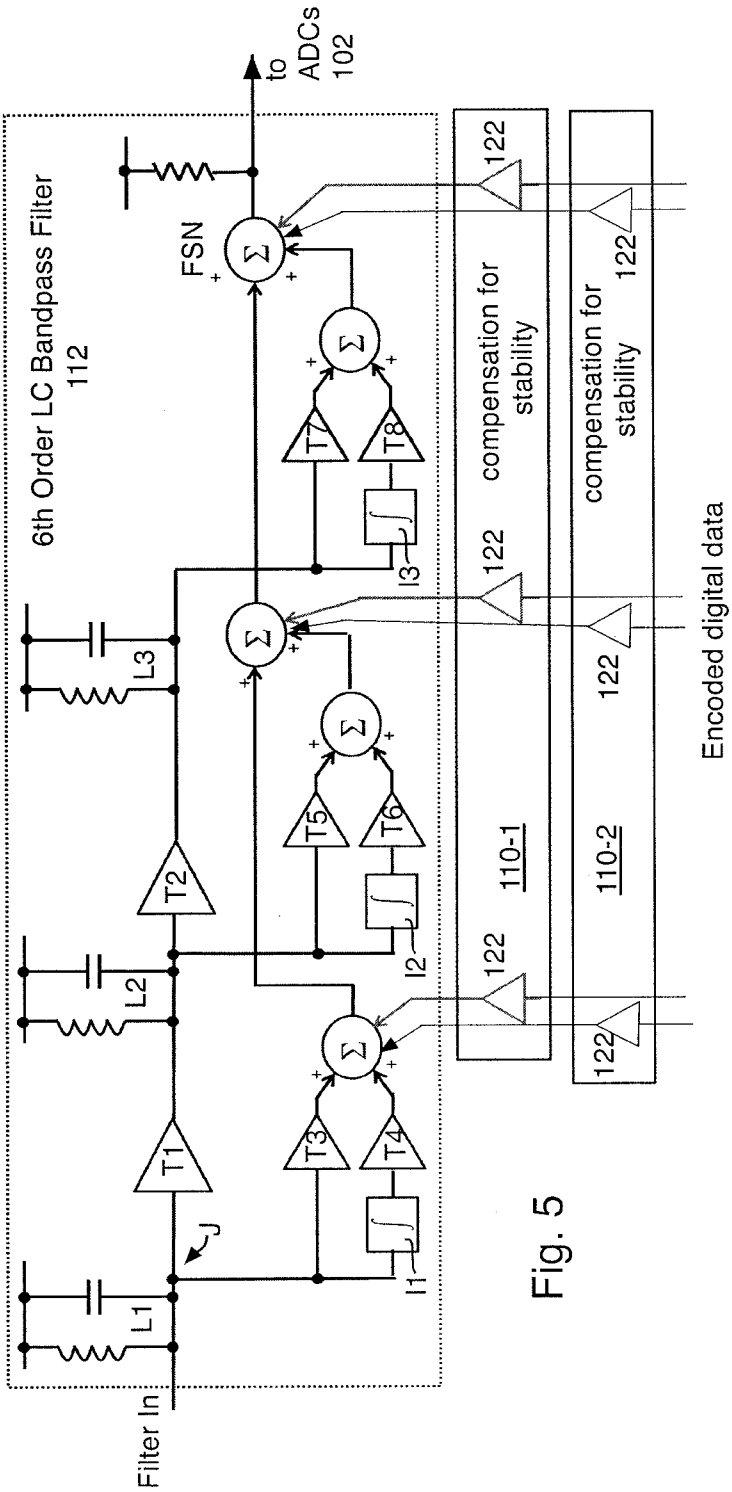
to ADCs 102
6th Order LC Bandpass Filter 112
FSN
Filter In
L1
L2
L3
T1
T2
T3
T4
T5
T6
T7
T8
I1
I2
I3
J
compensation for stability
compensation for stability
110-1
110-2
122
Encoded digital data

Fig. 5

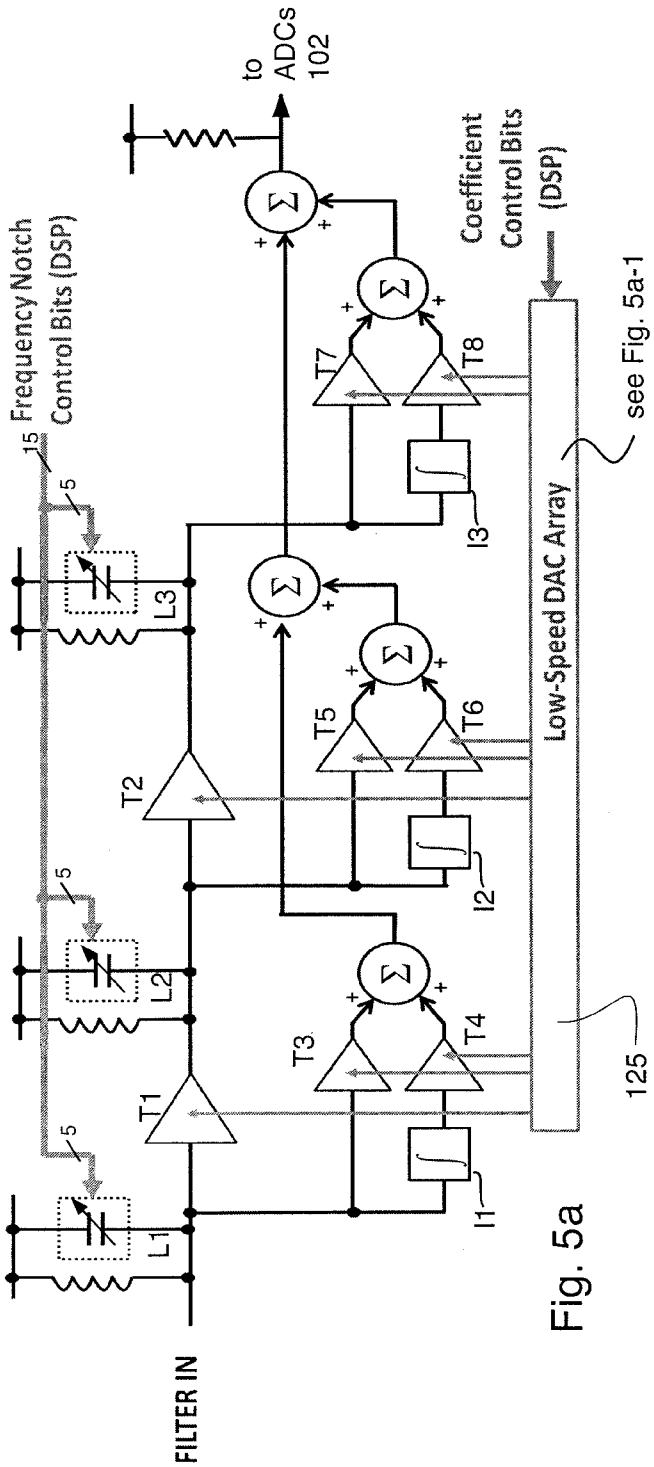
to ADCs 102
Coefficient Control Bits (DSP)
Frequency Notch Control Bits (DSP)
15
5
L1
L2
L3
T1
T2
T3
T4
T5
T6
T7
T8
I1
I2
I3
Low-Speed DAC Array
see Fig. 5a-1
125
FILTER IN

Fig. 5a

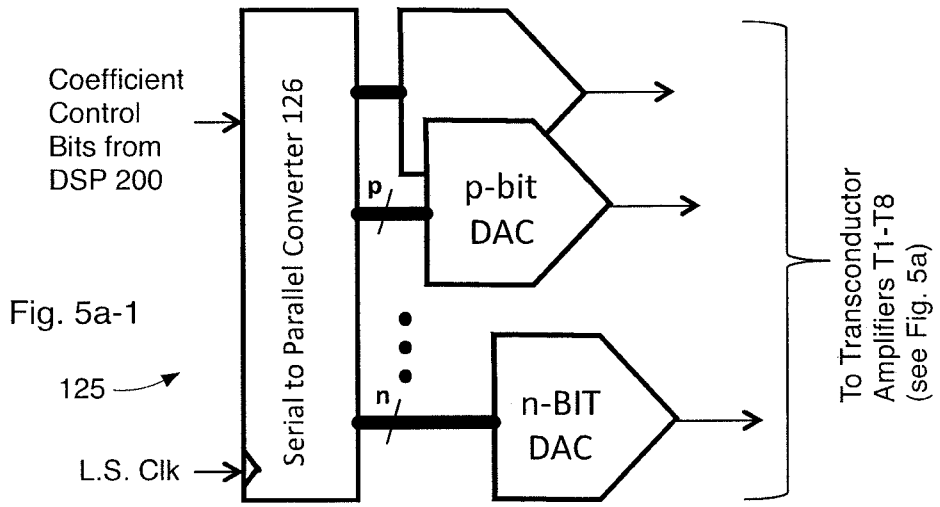

Fig. 5a-1

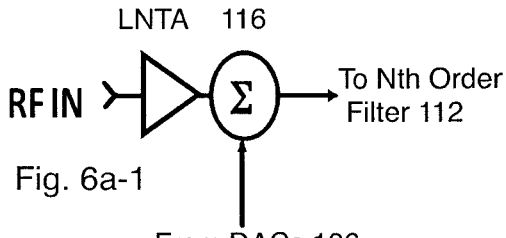

Fig. 6a-1

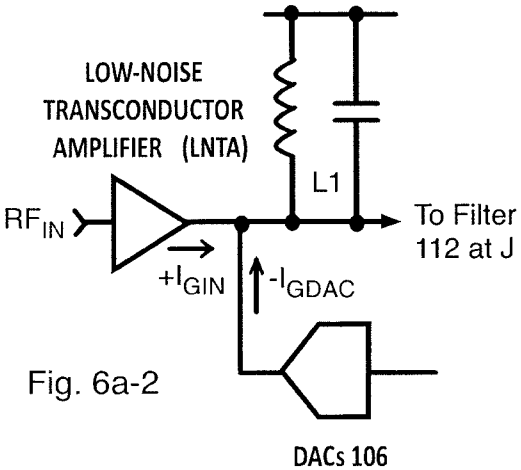

Fig. 6a-2

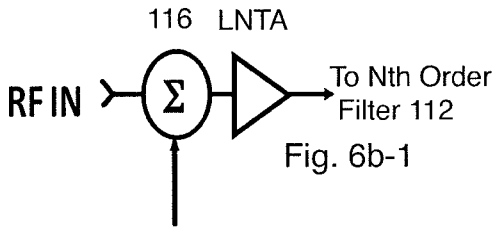

Fig. 6b-1

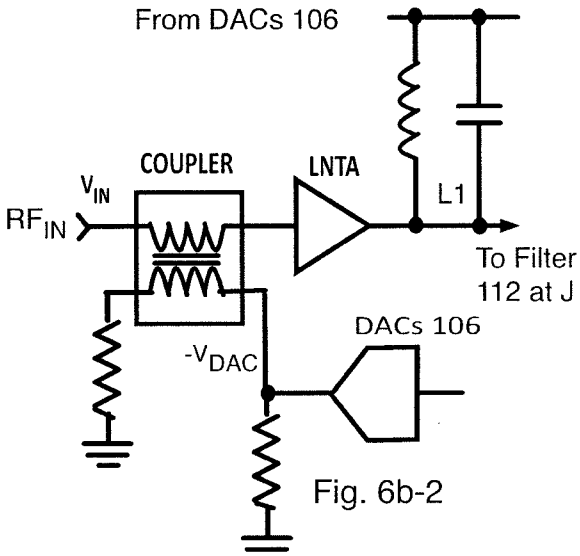

Fig. 6b-2

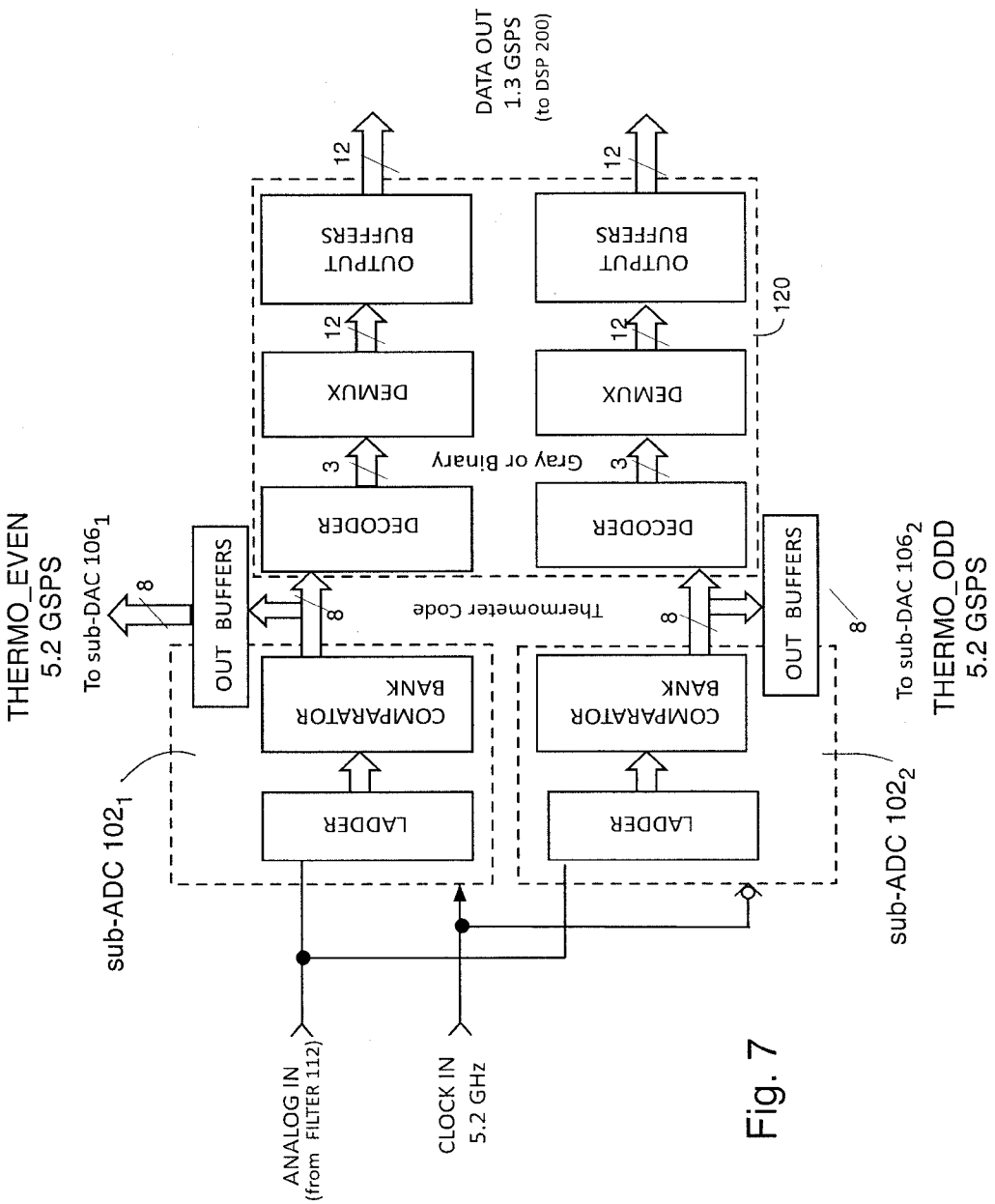
DATA OUT
1.3 GSPS
(to DSP 200)
12
12
OUTPUT BUFFERS
OUTPUT BUFFERS
120
12
12
DEMUX
DEMUX
3
3
Gray or Binary
DECODER
DECODER
Thermometer Code
8
8
8
8
OUT BUFFERS
OUT BUFFERS
THERMO_EVEN
5.2 GSPS
To sub-DAC 106$_1$
COMPARATOR BANK
COMPARATOR BANK
LADDER
LADDER
sub-ADC 102$_1$
sub-ADC 102$_2$
To sub-DAC 106$_2$
THERMO_ODD
5.2 GSPS
ANALOG IN
(from FILTER 112)
CLOCK IN
5.2 GHz

Fig. 7

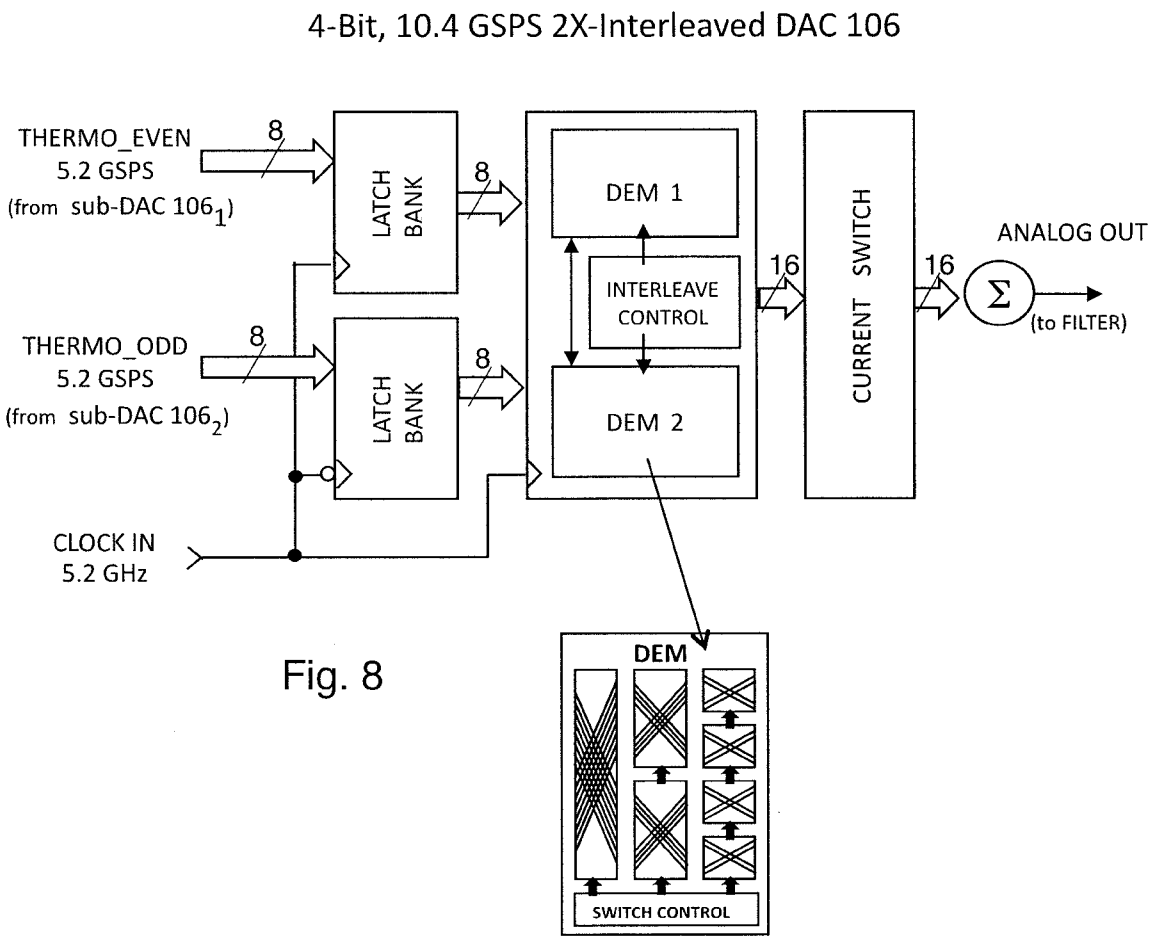
4-Bit, 10.4 GSPS 2X-Interleaved DAC 106
THERMO_EVEN
5.2 GSPS
(from sub-DAC 106$_1$)
8
LATCH BANK
8
THERMO_ODD
5.2 GSPS
(from sub-DAC 106$_2$)
8
LATCH BANK
8
CLOCK IN
5.2 GHz
DEM 1
INTERLEAVE CONTROL
DEM 2
16
CURRENT SWITCH
16
Σ
ANALOG OUT
(to FILTER)
DEM
SWITCH CONTROL

Fig. 8

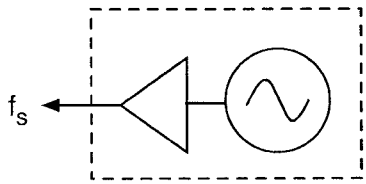
f_s

Fig. 9

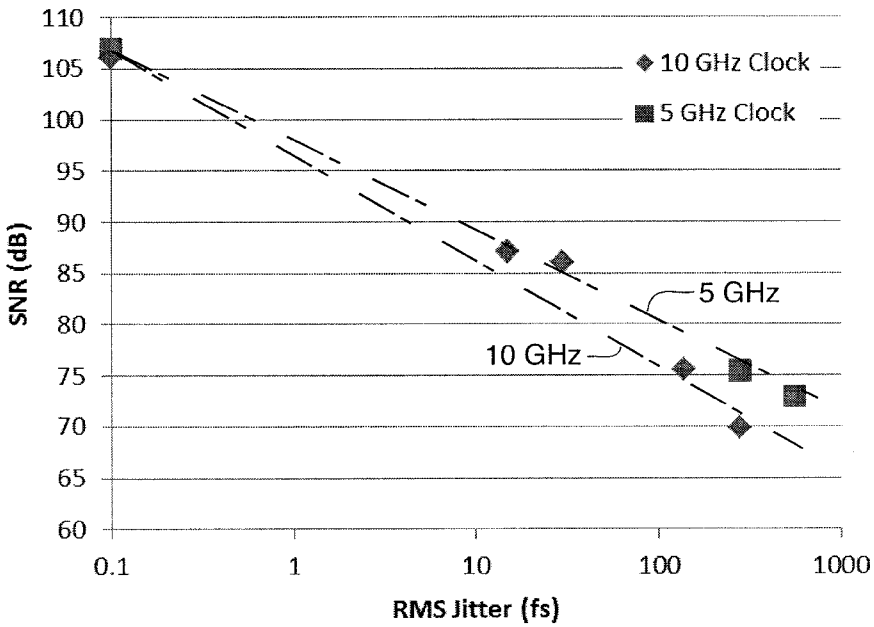
110
105
100
95
90
85
80
75
70
65
60
SNR (dB)
0.1
1
10
100
1000
RMS Jitter (fs)
10 GHz Clock
5 GHz Clock
5 GHz
10 GHz

Fig. 9(a)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/036833

A. CLASSIFICATION OF SUBJECT MATTER

H03M 3/02(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03M 3/02; H03M 1/10; H03M 3/00; H03M 1/40; H03M 1/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: modulator, delta sigma, interleaved, ADC (Analog to Digital Converter)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2013-0021180 A1 (AYMAN SHABRA et al.) 24 January 2013 See paragraphs [0017]-[0027]; and figures 1-3.	1-26
A	US 2012-0133536 A1 (FANG-SHI JORDAN LAI et al.) 31 May 2012 See paragraphs [0011]-[0044]; claim 1; and figures 1-3.	1-26
A	US 2008-0272946 A1 (JOHN L. MELANSON) 06 November 2008 See paragraphs [0033]-[0042]; and figures 3-5.	1-26
A	US 2005-0190091 A1 (UT-VA KOC et al.) 01 September 2005 See paragraphs [0020]-[0030]; and figures 2, 3.	1-26
A	US 2002-0093441 A1 (ANDREAS WIESBAUER et al.) 18 July 2002 See paragraphs [0022]-[0025]; and figure 1.	1-26

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
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"O" document referring to an oral disclosure, use, exhibition or other means
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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 October 2015 (12.10.2015)	**13 October 2015 (13.10.2015)**

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PCT/US2015/036833

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