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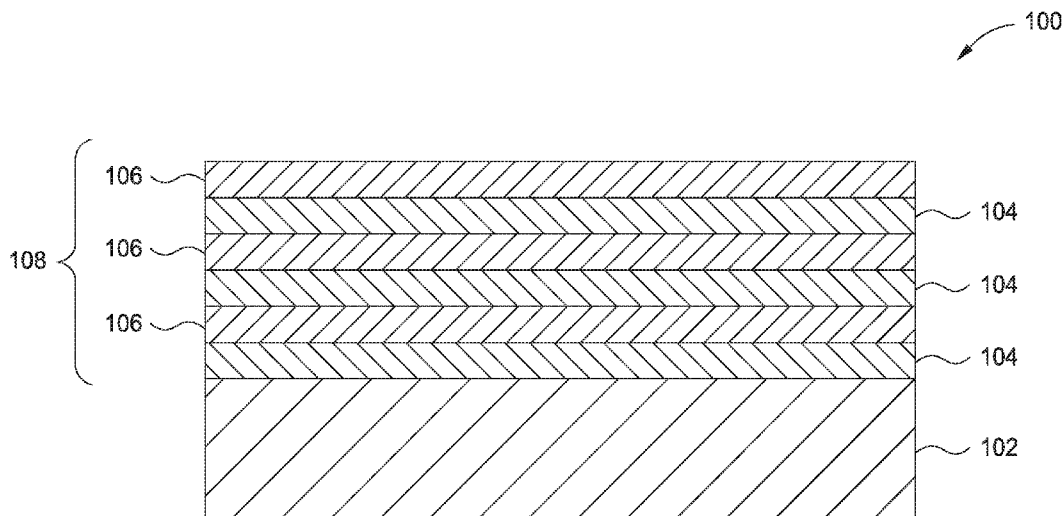


FIG. 1

(57) Abstract: Embodiments described herein generally relate to methods of manufacturing an oxide/polysilicon (OP) stack of a 3D memory cell for memory devices, such as NAND devices. The methods generally include treatment of the oxide and/or polysilicon materials with precursors during PECVD processes to lower the dielectric constant of the oxide and reduce the resistivity of the polysilicon. In one embodiment, the oxide material is treated with octamethylcyclotetrasiloxane (OMCTS) precursor. In another embodiment, germane (GeH₄) is introduced to a PECVD process to form SixGe(1-x) films with dopant. In yet another embodiment, a plasma treatment process is used to nitridate the interface between layers of the OP stack. The precursors and plasma treatment may be used alone or in any combination to produce OP stacks with low dielectric constant oxide and low resistivity polysilicon.



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LOW DIELECTRIC CONSTANT OXIDE AND LOW RESISTANCE OP STACK FOR 3D NAND APPLICATION

BACKGROUND

Field

[0001] Embodiments of the present disclosure generally relate to memory manufacturing processes, and more particularly, to methods of manufacturing 3D memory cells having a low dielectric constant and reduced resistivity.

Description of the Related Art

[0002] Growing demands continue to drive the need for high-capacity, high-performance computer memory devices with smaller geometries at lower costs. To this end, components of memory cells are stacked on top of each other to create three-dimensional (3D) memory cells, such as vertical gate 3D memory cells. One such technology is NAND flash memory, which is generally found in memory cards, USB flash drives, solid-state drives, and other similar devices for data storage and transfer. In NAND flash memory, memory cells made from transistors are connected in series and stacked in vertical layers to create densely-packed, high-capacity memory devices. Flash drives generally use less power and are more durable than ordinary hard drives because they do not contain moving parts. As such, there is great interest in increasing the capacity of flash drives, while reducing their size and cost.

[0003] As flash technology has progressed, limitations have continued to exist in how to create high-capacity devices on a small scale. For example, different materials that are combined on a microscopic scale have different physical properties that lead to non-uniformities in the flash memory device. Many vertical 3D memory cells include oxide/polysilicon (OP) stacks and/or oxide/nitride (ON) stacks due to their integration properties. Problematically, however, the oxide

material generally has a high dielectric constant and resistive-capacitive (RC) delay, and the polysilicon material has a high resistivity.

[0004] Therefore, there is a need for improved methods of manufacturing memory structures, such as 3D memory cells, having a low dielectric constant and reduced resistivity.

SUMMARY

[0005] Embodiments described herein generally relate to methods of manufacturing an oxide/polysilicon (OP) stack of a 3D memory cell for memory devices, such as NAND devices. The methods generally include treatment of the oxide and/or polysilicon materials with precursors during PECVD processes to lower the dielectric constant of the oxide and reduce the resistivity of the polysilicon. In one embodiment, the oxide material is treated with octamethylcyclotetrasiloxane (OMCTS) precursor. In another embodiment, germane (GeH_4) is introduced to a PECVD process to form doped $\text{Si}_x\text{Ge}_{(1-x)}$ films. In yet another embodiment, a plasma treatment process is used to nitridate the interface between layers of the OP stack. The precursors and plasma treatment may be used alone or in any combination to produce OP stacks with low dielectric constant oxide and low resistivity polysilicon.

[0006] In one embodiment, a memory cell manufacturing method is described. The method includes positioning a substrate in a PECVD chamber, introducing octamethylcyclotetrasiloxane precursor to the PECVD chamber to deposit a silicon oxide layer over the substrate, and depositing a polysilicon layer over the silicon oxide layer.

[0007] In another embodiment, a memory cell manufacturing method is described. The method includes positioning a substrate in a PECVD chamber, depositing a silicon oxide layer over the substrate, and introducing a silicon precursor and germane to the PECVD chamber to form a $\text{Si}_x\text{Ge}_{(1-x)}$ film over the silicon oxide layer.

[0008] In yet another embodiment, a memory device is described. The memory device includes a substrate, a silicon oxide layer disposed over the substrate, the silicon oxide layer having a dielectric constant between about 2.5 and about 3.2, and a polysilicon layer disposed over the silicon oxide layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] So that the manner in which the above recited features of the present disclosure can be understood in detail, a more particular description of the disclosure, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this disclosure and are therefore not to be considered limiting of scope, for the disclosure may admit to other equally effective embodiments.

[0010] Figure 1 is a cross-sectional view of a memory device according to embodiments of the present disclosure.

[0011] Figure 2 is a flow diagram summarizing a method according to embodiments of the present disclosure.

[0012] Figure 3 is a flow diagram summarizing a method according to embodiments of the present disclosure.

[0013] To facilitate understanding, identical reference numerals have been used, wherever possible, to designate identical elements that are common to the Figures. Additionally, elements of one embodiment may be advantageously adapted for utilization in other embodiments described herein.

DETAILED DESCRIPTION

[0014] Embodiments described herein generally relate to methods of manufacturing an oxide/polysilicon (OP) stack of a 3D memory cell for memory devices, such as NAND devices. The methods generally include treatment of the oxide and/or polysilicon materials with precursors during PECVD processes to

lower the dielectric constant of the oxide and reduce the resistivity of the polysilicon. In one embodiment, the oxide material is treated with octamethylcyclotetrasiloxane (OMCTS) precursor. In another embodiment, germane (GeH_4) is introduced to a PECVD process to form doped $\text{Si}_x\text{Ge}_{(1-x)}$ films. In yet another embodiment, a plasma treatment process is used to nitridate the interface between layers of the OP stack. The precursors and plasma treatment may be used alone or in any combination to produce OP stacks with low dielectric constant oxide and low resistivity polysilicon. The present disclosure contemplates an OP stack memory device as an example; however, other memory stacks also benefit from methods described herein.

[0015] Figure 1 is a memory device 100 according to embodiments of the present disclosure. The memory device 100 includes a substrate 102 with a plurality of first material layers 104 and a plurality of second material layers 106 thereon. The plurality of first material layers 104 and the plurality of second material layers 106 make up a memory stack 108. In the embodiment of an OP stack memory device, each of the first material layers 104 is generally a silicon oxide layer (O layer) and each of the second material layers 106 is generally an amorphous silicon layer, which becomes a polysilicon layer (P layer) after an annealing process. While Figure 1 depicts the second material layer 106 deposited over the first material layer 104, the deposition order may be reversed such that the first material layer 104 (O layer) is deposited over the second material layer 106 (P layer).

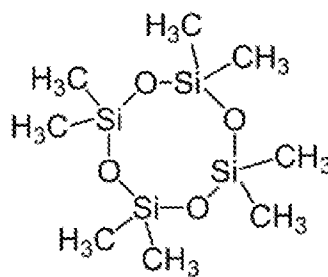
[0016] While memory device 100, as shown, includes three first material layers 104 and three second material layers 106, the number of first material layers 104 and second material layers 106 is generally any suitable number of layers depending upon the memory device being manufactured. For example, memory devices often include 8x, 16x, 24x, and even higher stack numbers.

[0017] In an embodiment in which the memory device 100 is a NAND flash memory cell, the memory device 100 further includes a source and a drain

disposed on opposite ends of a first surface of the substrate 102. For use as flash memory, multiple NAND flash cells are generally connected in series with the adjacent cells sharing a source or drain, and each cell is connected to a bitline and a wordline. In operation, each cell can store data, such as a "0" or "1," therein.

[0018] The methods of manufacturing memory devices, such as memory device 100, that follow are generally part of plasma-enhanced chemical vapor deposition (PECVD) process, which can be used to form silicon films at relatively low temperatures. The methods can be performed in any suitable PECVD chamber, such as PECVD chambers available from Applied Materials, Inc. of Santa Clara, California.

[0019] Figure 2 depicts a flow diagram summarizing a method 200 of manufacturing a memory device, such as the memory device 100. The method 200 begins at operation 210 by positioning the substrate 102 in a PECVD chamber. At operation 220, a first material layer 104, or silicon oxide layer, is deposited over the substrate 102 by introducing OMCTS precursor to the PECVD chamber. The chemical structure of OMCTS precursor is shown below as Structure 1. In one embodiment, the first material layer 104 is deposited on and in contact with the substrate 102.



(Structure 1)

[0020] As shown in Structure 1, an OMCTS molecule is a chemical structure having silicon oxide (Si—O) ring-like bonding, in addition to methyl (CH₃) groups.

Conventionally deposited silicon oxide layers have a dielectric constant of about 3.9. According to embodiments of the present disclosure, the carbon (C) from the above-described introduction of OMCTS precursor generally reduces the dielectric constant of the silicon oxide layer from its current value of about 3.9 to between about 2.5 and about 3.2, for example, to between about 2.8 and about 3.0. Additionally, the deposited silicon oxide layer has increased oxide quality through the Si—O ring-like structure.

[0021] Adjusting the processing conditions of the PECVD process will break C—H bonds of the OMCTS precursor. For example, increasing a plasma density during introduction of the OMCTS precursor to the PECVD chamber from about 25.56 megahertz (MHz) to about 27 MHz breaks the C—H bonds of the precursor. Additionally, or alternatively, the method 300 further includes bombarding the silicon oxide layer with a radiofrequency (RF frequency) of between about 300 kHz and about 400 kHz, such as about 350 kHz, to break the C—H bonds of the OMCTS precursor.

[0022] At operation 230, a second material layer 106, or polysilicon layer is deposited over the first material layer 104, or silicon oxide layer. The second material layer 106 may be deposited by any suitable deposition means. Generally, amorphous silicon is deposited by the introduction of precursors, including but not limited to, silane (SiH_4), argon (Ar), and helium (He), in addition to dopant precursors, including but not limited to, phosphane (PH_3) and diborane (B_2H_6). The amorphous silicon becomes polysilicon after an annealing process, such as a thermal anneal. In one embodiment, the second material layer 106 is deposited on and in contact with the first material layer 104.

[0023] Operations 220 and 230 are optionally repeated to form an OP stack having any number of first material layers 104 and any number of second material layers 106.

[0024] Figure 3 depicts a flow diagram summarizing a method 300 of manufacturing the memory device 100. The method 300 begins at operation 310 by positioning the substrate 102 in a PECVD chamber. At operation 320, a first material layer 104, or silicon oxide layer, is deposited over the substrate 102. The silicon oxide layer is generally deposited by any suitable deposition process, such as the process described at operation 220 of method 200. In one embodiment, the first material layer 104 is deposited on and in contact with the substrate 102.

[0025] At operation 330, a second material layer 106, or polysilicon layer, is deposited over the first material layer 104. More specifically, the polysilicon layer is deposited by introducing at least one silicon precursor, including but not limited to, silane (SiH_4), and germane (GeH_4) precursor to form a $\text{Si}_x\text{Ge}_{(1-x)}$ film having dopant therein, which has high mobility and low resistivity. An example of a suitable dopant is phosphine (PH_3). The GeH_4 precursor may be introduced at any suitable time during the PECVD process. In one embodiment, GeH_4 is introduced before plasma is generated in the PECVD chamber.

[0026] The deposited polysilicon has high mobility and reduced resistivity with the same, or a substantially similar, carrier concentration. Conventionally deposited n-type polysilicon (with phosphorous (P) doping) has a resistivity of about 1×10^{-3} ohm*cm, and conventionally deposited p-type polysilicon has a resistivity of about 3×10^{-3} ohm*cm. The introduction of GeH_4 precursor reduces the resistivity of the n-type polysilicon film to about 0.5×10^{-3} ohm*cm, and the resistivity of the p-type polysilicon film to about 1.5×10^{-3} ohm*cm.

[0027] Operations 320 and 330 are optionally repeated to form an OP stack having any number of first material layers 104 and any number of second material layers 106.

[0028] Additionally or alternatively, methods described herein may include plasma treatment at an interface between the first material layer 104, or silicon

oxide layer, and the second material layer 106, or polysilicon layer. More specifically, the interface between each of the silicon oxide layers and polysilicon layers may undergo plasma treatment to nitride and improve adhesion between the layers of the OP stack. For example, ammonia (NH₃)/nitrogen gas (N₂) plasma may be generated in the PECVD chamber to nitride and improve adhesion at the interface between the silicon oxide and polysilicon layers.

[0029] The operations of method 200 and method 300 can be used in any combination. In one further embodiment, a first material layer 104, or silicon oxide layer, is deposited over the substrate 102 by introducing OMCTS precursor, and a second material layer 106 is deposited by introducing at least one silicon precursor, including but not limited to, SiH₄, and germane (GeH₄) precursor to form Si_xGe_(1-x) film with dopant. These operations are repeated to form a memory device having any suitable number of layers.

[0030] Methods described herein provide improved memory devices having low dielectric constant oxide and low resistivity polysilicon with reduced thickness, which improves overall device extendibility while maintaining continued shrinking of overall memory device geometries.

[0031] While the foregoing is directed to embodiments of the present disclosure, other and further embodiments of the disclosure may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

What is claimed is:

1. A method of manufacturing a memory device stack comprising:
positioning a substrate in a PECVD chamber;
introducing octamethylcyclotetrasiloxane precursor to the PECVD chamber to deposit a silicon oxide layer over the substrate; and
depositing a polysilicon layer over the silicon oxide layer.
2. The method of claim 1, wherein the depositing a polysilicon layer over the silicon oxide layer comprises:
introducing silane and germane to the PECVD chamber to deposit the polysilicon layer.
3. The method of claim 1, wherein the introducing octamethylcyclotetrasiloxane precursor to the PECVD chamber to deposit the silicon oxide layer over the substrate occurs at a plasma density of about 27 megahertz.
4. The method of claim 1, further comprising:
bombarding the silicon oxide layer with an RF frequency of between about 300 kHz and about 400 kHz.
5. The method of claim 1, further comprising:
plasma treating an interface between the silicon oxide layer and the polysilicon layer, wherein the plasma treatment comprises introducing NH_3/N_2 to the PECVD chamber.
6. The method of claim 1, wherein depositing the polysilicon layer over the silicon oxide layer comprises:

introducing one or more precursors selected from the group consisting of silane, argon, and helium, and one or more dopant precursors selected from the group consisting of phosphane and diborane, to the PECVD chamber to deposit an amorphous silicon layer over the silicon oxide layer; and
annealing the amorphous silicon layer to form the polysilicon layer.

7. The method of claim 1, wherein depositing the polysilicon layer over the silicon oxide layer comprises:

introducing at least one silicon precursor selected from the group consisting of silane and germane to the PECVD chamber to form an $\text{Si}_x\text{Ge}_{(1-x)}$ film.

8. A method of manufacturing a memory device stack, comprising:

positioning a substrate in a PECVD chamber;

depositing a silicon oxide layer over the substrate; and

introducing a silicon precursor and germane to the PECVD chamber to deposit a polysilicon layer over the silicon oxide layer.

9. The method of claim 8, wherein the depositing a silicon oxide layer over the substrate comprises:

introducing OMCTS precursor to the PECVD chamber to deposit the silicon oxide layer.

10. The method of claim 8, further comprising:

plasma treating an interface between the silicon oxide layer and the polysilicon layer, wherein the plasma treatment comprises introducing NH_3/N_2 to the PECVD chamber.

11. A memory device, comprising:

a substrate;

a silicon oxide layer disposed over the substrate, the silicon oxide layer having a dielectric constant between about 2.5 and about 3.2; and

a polysilicon layer disposed over the silicon oxide layer.

12. The memory device of claim 11, wherein the dielectric constant of the silicon oxide layer is between about 2.8 and about 3.0.

13. The memory device of claim 11, wherein the silicon oxide layer is deposited on and in contact with the substrate and wherein the polysilicon layer is deposited on and in contact with the silicon oxide layer.

14. The memory device of claim 11, wherein the polysilicon layer is an n-type polysilicon layer, and wherein the n-type polysilicon layer has a resistivity of less than about 0.5×10^{-3} ohm*cm.

15. The memory device of claim 11, wherein the polysilicon layer is a p-type polysilicon layer, and wherein the p-type polysilicon layer has a resistivity of less than about 1.5×10^{-3} ohm*cm.

100

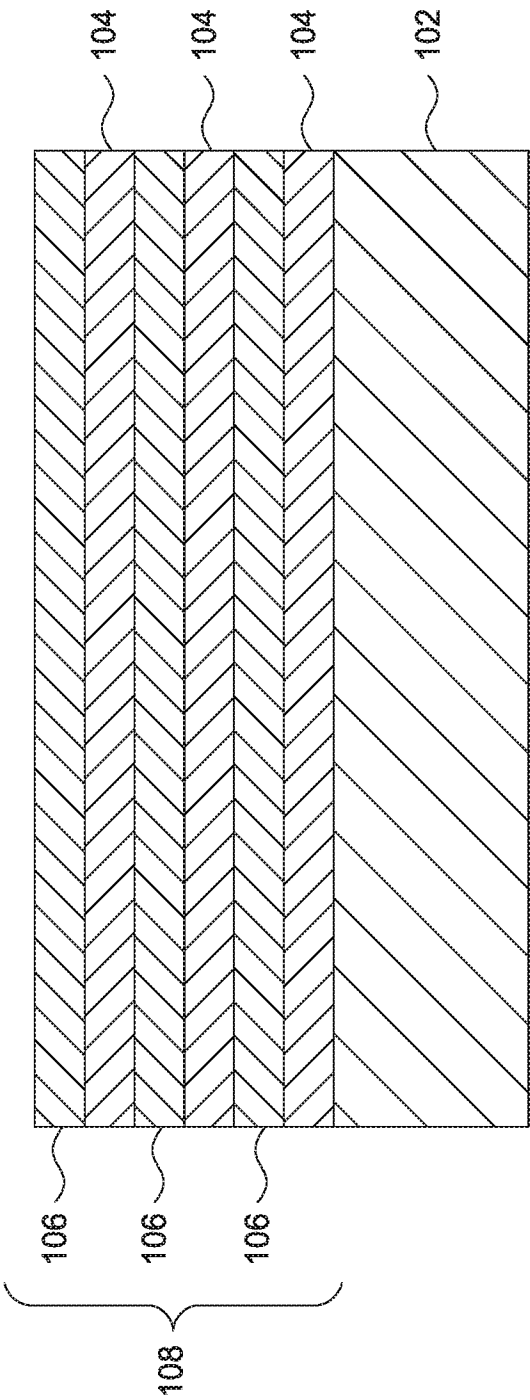


FIG. 1

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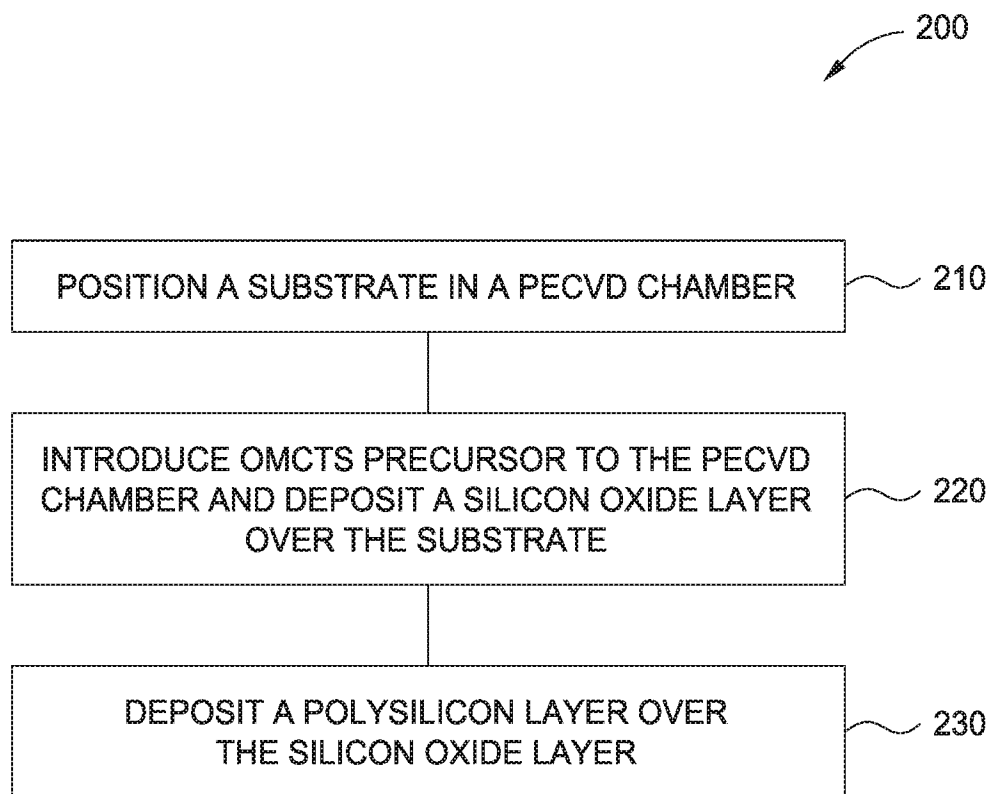


FIG. 2

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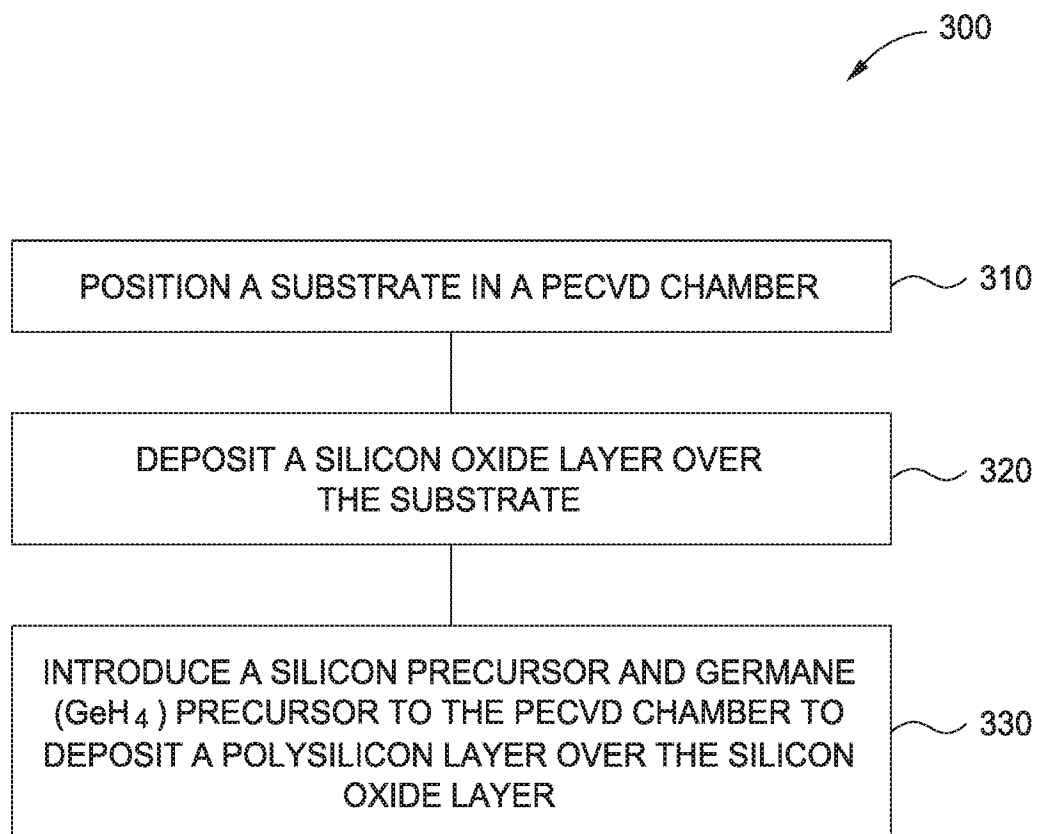


FIG. 3

A. CLASSIFICATION OF SUBJECT MATTER**H01L 27/11556(2017.01)i, H01L 27/11524(2017.01)i, H01L 27/11529(2017.01)i, H01L 25/065(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 27/11556; C23C 16/52; H01L 21/20; H01L 21/469; H01L 29/94; H01L 21/31; H01L 27/11524; H01L 27/11529; H01L 25/065

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: PECVD, octamethylcyclotetrasiloxane, OMCTS, silicon oxide, polysilicon, memory

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y	See paragraphs 7, 33-36, 43, 83; claim 8; and figures 1, 7.	1-7, 9-15
Y	US 2008-0026597 A1 (JEFFREY C. MUNRO et al.) 31 January 2008	1-7, 9, 11-15
	See paragraphs 23, 29, 37; and figure 1.	
Y	US 2006-0097305 A1 (KEE-JEUNG LEE) 11 May 2006	5, 10
	See paragraph 41; and figure 2.	
A	US 2013-0316518 A1 (ALICE HOLLISTER et al.) 28 November 2013	1-15
	See paragraphs 34-53; and figures 1-3.	
A	L.ZAJICKOVA et al., 'Characterization of silicon oxide thin films deposited by plasma enhanced chemical vapour deposition from octamethylcyclotetrasiloxane-oxygen feeds', Thin Solid Films, Volume 338, Issues 1-2, Pages 49-59, 18 October 1999 (https://doi.org/10.1016/S0040-6090(98)00976-6) See pages 49-58.	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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Information on patent family members

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