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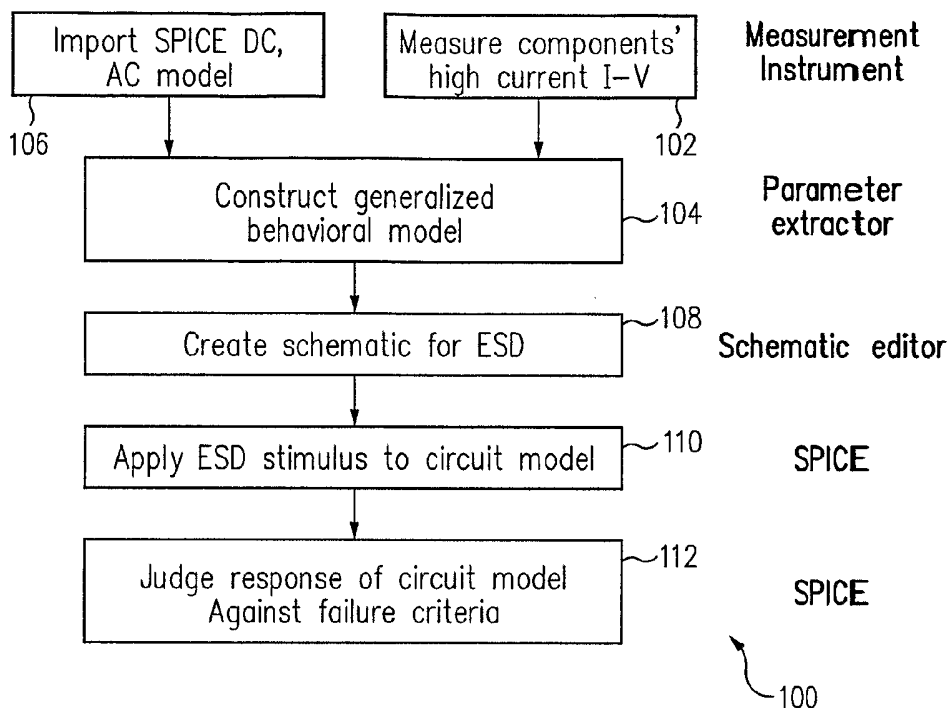
(54) Title: ELECTROSTATIC DISCHARGE SIMULATION



(57) Abstract: Systems and methods provide electrostatic discharge simulation techniques. For example, a method in accordance with an embodiment of the present invention provides a simulation of electrostatic discharge in integrated circuits. The method may allow for the design of protection circuits and simulating electrostatic discharge events concurrently with the design of the associated electrical circuit.

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ELECTROSTATIC DISCHARGE SIMULATION

5 The present invention relates generally to electrical circuits and, more particularly, to the simulation of electrostatic discharge.

BACKGROUND

A modern integrated circuit may communicate by utilizing a 10 number of different input and output signal standards. For example, an integrated circuit may transmit and receive information via one or more input/output circuits, which may be within the same input/output bank, at high speeds (e.g., 1 Gbps). The input/output circuit typically must also be designed 15 to be protected from (e.g., have a certain immunity to damage from) electrostatic discharge.

In general, an input/output circuit design may be very complex and involve difficult compromises between performance (e.g., speed or data rate) and electrostatic discharge (ESD) 20 protection. For example, a typical input/output circuit design process may involve adding standard, pre-approved ESD protection devices to the input/output circuit. The ESD protection device and the input/output circuit, for example, would then be implemented in silicon and tested to determine if the circuit 25 meets design specifications.

After testing, it may be determined that the selected ESD protection device was not optimum for the desired application, such as for example being too large or in an incorrect configuration, and the process would have to be repeated, such 30 as by selecting another ESD protection device or reconfiguring

the current design for further testing. In general, this approach is time consuming and expensive with results that are often difficult to predict. As a result, there is a need for improved ESD design techniques.

5

SUMMARY

Systems and methods are disclosed herein to provide electrostatic discharge design and simulation techniques. For example, in accordance with an embodiment of the present
10 invention, a method is disclosed for simulating electrostatic discharge in integrated circuits. The method may allow for the design of electrostatic discharge protection and simulating electrostatic discharge events concurrently with the design and simulation of the associated electrical circuit (e.g.,
15 input/output circuit). Consequently, a circuit designer may optimize a circuit design for electrostatic discharge protection and performance (e.g., speed) simultaneously or in a parallel fashion.

More specifically, in accordance with one embodiment of the
20 present invention, a method of determining electrostatic discharge protection for a circuit includes entering the circuit into a circuit simulation program; representing a circuit element of the circuit in the circuit simulation program by its behavior under electrostatic discharge conditions; running the
25 circuit simulation program to obtain simulation results, wherein the circuit simulation program provides an electrostatic discharge stimulus to the circuit; and comparing the simulation results to failure criteria for the circuit.

In accordance with another embodiment of the present
30 invention, a computer readable medium storing a circuit simulation program includes symbols for representing a behavior

of corresponding circuit elements under normal operating conditions; and symbols for representing a behavior of the corresponding circuit elements under electrostatic discharge conditions.

5 In accordance with another embodiment of the present invention, a method of testing a circuit for electrostatic discharge protection includes providing a circuit simulation program to simulate the circuit; and providing macros within the circuit simulation program which represent a behavior of 10 corresponding circuit elements under electrostatic discharge conditions.

In accordance with another embodiment of the present invention, a method of generating circuit element macros for simulating electrostatic discharge behavior includes testing a 15 physical circuit element to determine its behavior and failure criteria under electrostatic discharge conditions; and creating an associated macro for the physical circuit element representing the determined electrostatic discharge behavior, the macro suitable for use in a circuit simulation program.

20 The scope of the invention is defined by the claims, which are incorporated into this section by reference. A more complete understanding of embodiments of the present invention will be afforded to those skilled in the art, as well as a realization of additional advantages thereof, by a consideration 25 of the following detailed description of one or more embodiments. Reference will be made to the appended sheets of drawings that will first be described briefly.

30

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a flowchart illustrating operations performed to simulate electrostatic discharge for a circuit in accordance with an embodiment of the present invention.

5 Fig. 2 shows a block diagram illustrating a representative circuit for simulating electrostatic discharge in accordance with an embodiment of the present invention.

Fig. 3 shows a block diagram illustrating a representative circuit for simulating electrostatic discharge in accordance 10 with an embodiment of the present invention.

Fig. 4 shows an exemplary circuit implementation for a portion of Fig. 3 in accordance with an embodiment of the present invention.

Fig. 5 shows an exemplary circuit implementation for a 15 portion of Fig. 3 in accordance with an embodiment of the present invention.

Fig. 6 shows an exemplary circuit implementation for a portion of Fig. 3 in accordance with an embodiment of the present invention.

20 Fig. 7 shows an exemplary graph illustrating a simulation result for the circuit of Fig. 3 in accordance with an embodiment of the present invention.

Fig. 8 shows an exemplary graph illustrating a simulation result for the circuit of Fig. 3 in accordance with an 25 embodiment of the present invention.

Fig. 9 shows an exemplary graph illustrating a simulation result for the circuit of Fig. 3 in accordance with an embodiment of the present invention.

Fig. 10 shows an exemplary circuit for providing an electrostatic discharge stimulus in accordance with an embodiment of the present invention.

Fig. 11 shows an exemplary circuit for providing an electrostatic discharge stimulus in accordance with an embodiment of the present invention.

Fig. 12 shows an exemplary plot of current versus voltage for an electrical component in accordance with an embodiment of the present invention.

Fig. 13 shows an exemplary simulation plot of current versus voltage for an electrical component in accordance with an embodiment of the present invention.

Embodiments of the present invention and their advantages are best understood by referring to the detailed description that follows. It should be appreciated that like reference numerals are used to identify like elements illustrated in one or more of the figures.

DETAILED DESCRIPTION

Fig. 1 shows a flowchart 100 illustrating operations performed to simulate electrostatic discharge (ESD) for a circuit in accordance with an embodiment of the present invention. In step 102, one or more physical electrical components are tested to measure and characterize their behavior in response to high voltages and currents. Various parameters associated with an electrical component being tested may be varied to allow the construction of a generalized behavioral model in step 104 of the electrical component. For example, various parameters of a particular type of transistor, such as

its channel width or length may be varied over a desired range, to extract generalized parameters representing its behavior.

The generalized behavior model may be utilized to generate an associated macro for the electrical component to represent 5 its behavior under high voltage and/or high current conditions and the macro incorporated into a circuit simulation program, such as for example SPICE (step 106). A circuit having electrostatic discharge protection circuitry may then be designed which utilizes one or more of the electrical components 10 having associated macros and then entered into the circuit simulation program (step 108).

Various ESD stimuli may then be applied to the circuit being simulated within the circuit simulation program (step 110) and the circuit's response (based at least in part on the 15 macros) compared to failure criteria (step 112) for electrical components within the circuit and/or to the circuit as a whole. A user may compare the circuit's response to the failure criteria or the failure criteria may be provided to the circuit simulation program to automatically compare the circuit's 20 response to the failure criteria. The circuit simulation program may then run a large number of simulations under varying conditions and, for example, indicate any circuit failures to a user based on the provided failure criteria for the circuit.

Consequently, by varying the level of ESD stimulus and 25 checking for destructive failure of the simulated circuit based on the failure criteria, the circuit's level of ESD protection may be determined. Furthermore, the circuit's performance of its intended function may also be determined by the circuit simulation program so that ESD protection and circuit 30 performance are evaluated in a concurrent fashion through simulation.

One or more of the techniques disclosed herein may provide an improved approach to ESD protection design as compared to conventional approaches. For example, conventional approaches typically are experimental and iterative and require layout, mask generation, and silicon fabrication to test a design or implement a design change, which is generally a time-consuming and an expensive procedure. In contrast, one or more techniques disclosed herein employ simulation and synthesis to model ESD protection and circuit performance, which may provide a less expensive alternative and provide feedback quickly regarding ESD behavior and/or circuit performance.

Fig. 2 shows a block diagram illustrating an exemplary circuit 200 for simulating electrostatic discharge in accordance with an embodiment of the present invention. Circuit 200 includes an ESD protection circuit 204 and a load 206. ESD protection circuit 204 may represent any type of circuit or circuit element (e.g., a diode, a transistor, or a ballast resistor) for providing ESD protection for load 206. Load 206 represents a circuit or circuit element (e.g., a transistor, a resistor, a capacitor, an inductor, or wires) which is designed to perform the function desired for circuit 200 and which may require ESD protection.

Circuit 200 may be simulated in a circuit simulation program (e.g., SPICE) and one or more various types of ESD stimuli 202 applied to ESD protection circuit 204 and load 206 to measure simulated current and voltage levels. ESD stimuli 202 may represent, for example, a charge device model (CDM) or a human body model (HBM) ESD standard.

The current and voltage levels may be checked at various points (nodes) within circuit 200 to determine the maximum current and voltage levels. For example, the current through ESD protection circuit 204 (labeled I_1) and load 206 (labeled I_2)

may be checked along with the voltage (V) across ESD protection circuit 204 and load 206 against maximum allowable currents and voltages. Consequently, ESD protection for a circuit may be determined through simulation in a similar fashion as circuit performance is determined through simulation.

By testing physical circuit elements to measure their behavior under ESD conditions and creating macros to represent their behavior in a circuit simulation program, the circuit simulation program, such as SPICE, can provide an ESD simulation model for high currents and/or voltages (i.e., an ESD event) in addition to its existing direct current (DC) and alternating current (AC) simulation models. In general, one circuit element may be simulated or some portion of a circuit up to an entire integrated circuit may be simulated.

For example, when entering a portion of an integrated circuit into the SPICE circuit simulation program (although the SPICE simulation program is referenced herein, it should be understood that the techniques disclosed herein are generally applicable to other types of circuit simulation programs), the simulated circuit may include a pad (e.g., one or more input/output pads), devices (e.g., circuit elements) connected to the pad, and devices located one level of circuitry downstream from the devices connected to the pad. The simulated circuit would also include any ESD protection devices and supply clamps associated with the simulated circuit. Various other circuitry or expected parasitic circuit elements (e.g., estimated power supply capacitances) associated with the circuit may also be included as part of the simulated circuit.

The simulated circuit elements of the simulated circuit would be identified by the standard SPICE symbols. During ESD simulation, additional sub-circuits (corresponding to the macros incorporated into SPICE to represent the general behavior of the

corresponding circuit elements based on testing under ESD conditions and developed as discussed in reference to Fig. 1) are automatically added in parallel with each device in the netlist. Alternatively, the simulated circuit elements of the simulated circuit would be identified by the standard SPICE symbols and also identified in parallel by the ESD model symbols (or high current symbols) corresponding to the macros developed as discussed in reference to Fig. 1 (i.e., the macros incorporated into SPICE to represent the general behavior of the corresponding circuit elements based on testing under ESD conditions). For example, a MOS transistor in the SPICE simulation would be identified with a conventional MOS symbol along with an ESD symbol to represent its low current and high current behavior, respectively.

The simulated circuit may then be evaluated under various ESD conditions. For example, ESD stimulus may be applied to the simulated circuit and one or more points of interest of the simulated circuit, such as node voltages and/or branch currents, may be monitored and compared to maximum allowable peak voltages and currents. The maximum allowable peak voltages and currents for a circuit element may be determined through testing (e.g., step 102 of Fig. 1) and/or based on manufacturer specifications for the circuit element (e.g., to determine the failure criteria as discussed in step 112 of Fig. 1).

Fig. 3 shows a block diagram illustrating an exemplary circuit 300 for simulating electrostatic discharge in accordance with an embodiment of the present invention. Circuit 300 includes a protection circuit 302, a high voltage stage circuit 304, and a low voltage stage circuit 306. Protection circuit 302 may correspond to ESD protection circuit 204 (Fig. 2) and high voltage stage circuit 304 and low voltage stage circuit 306 may correspond to load 206 (Fig. 2).

Fig. 4 shows a circuit 400, which is an exemplary circuit implementation for protection circuit 302 of Fig. 3 in accordance with an embodiment of the present invention. Circuit 400 includes a transistor 402 and a resistor 404. As an example, transistor 402 may be represented in the SPICE circuit simulation program by its standard MOS transistor symbol and also by its ESD model symbol so that SPICE may simulate its low current and/or high current behavior, respectively.

Fig. 5 shows a circuit 500, which is an exemplary circuit implementation for high voltage stage circuit 304 of Fig. 3, and Fig. 6 shows a circuit 600, which is an exemplary circuit implementation for low voltage stage circuit 306 of Fig. 3, in accordance with an embodiment of the present invention. Circuits 500 and 600 include a number of circuit elements (e.g., transistors), which may be represented by their standard SPICE symbols and also, if desired, by their ESD model symbols to provide standard simulation results as well as ESD simulation results, respectively.

Figs. 7-9 show graphs illustrating exemplary simulation results for circuit 300 of Fig. 3 in accordance with an embodiment of the present invention. Fig. 7 shows input current versus time plots for waveforms 702 through 712 resulting from the application of a CDM-type of ESD stimulus at 200, 500, and 1000 volts. Waveforms 702, 704, and 706 represent the simulation results for circuit 300 and waveforms 708, 710, and 712 represent the corresponding measured test results of the physical embodiment of circuit 300. Waveforms 702 and 708, 704 and 710, and 706 and 712 correspond to ESD stimulus of 1000, 500, and 200 volts, respectively. As illustrated in Fig. 7, the simulated results compare favorably with the actual measured results.

Fig. 8 shows simulated results of voltage versus time based on a CDM ESD stimulus of 1000 volts. Waveforms are plotted corresponding to simulation voltage measurements at an input pad (labeled Pad), high voltage stage circuit 304 (labeled 1st
5 stage), and low voltage stage circuit 306 (labeled 2nd stage) of circuit 300.

Fig. 9 shows simulated results of current versus time for the CDM ESD stimulus of 1000 volts. Waveforms are plotted corresponding to simulation current measurements at an input pad
10 (labeled Pad), protection circuit 302 (labeled Clamp), high voltage stage circuit 304 (labeled High V), and low voltage stage circuit 306 (labeled Low V) of circuit 300.

Fig. 10 shows an exemplary circuit 1000 for providing a CDM ESD stimulus in accordance with an embodiment of the present
15 invention. Circuit 1000 includes a capacitor (C), an inductor (L), and a resistor (R), with exemplary values of 23.45 pF, 10.44 nH, and 34.98 ohms, respectively. The values for C, L, and R may be package and tester dependent. A square wave may be applied at an input node (labeled NESD) ranging in duration, for
20 example, from 1 picosecond to 10 nanoseconds (e.g., in SPICE set TRAN 1p 10n). The ESD testing may be performed in accordance with the desired standard, such as for example the CDM standard using a two-node method with one node at the stress voltage and all other nodes at zero volts (e.g., set NESD at stress voltage
25 and all other nodes at zero volts), although the polarities may be reversed as known by one skilled in the art.

Fig. 11 shows an exemplary circuit 1100 for providing a HBM ESD stimulus in accordance with an embodiment of the present invention. Exemplary values for the capacitor (C), the inductor
30 (L), and the resistor (R) are 100 pF, 7.5 μH, and 1500 ohms, respectively. The node (labeled NESD) receives the stress voltage, which may range in duration, for example, from 10

picoseconds to 200 nanoseconds (e.g., in SPICE set TRAN 10p 200n).

As discussed above (e.g., in reference to step 102 of Fig. 1), physical electrical components are tested to measure and 5 characterize their behavior in response to high voltages and currents (e.g., to ESD-like events). In accordance with an embodiment of the present invention, the testing of the electrical components may be performed via transmission line pulse techniques. For example, a transmission line pulse test 10 method may include charging a coaxial cable and then discharging the coaxial cable into a test device (i.e., an electrical component under test) via a relay. The current and voltage levels of the test device are monitored, for example, via probes of a fast scope, which allows measurement of the high currents 15 and voltages while possibly avoiding sample destruction (i.e., destruction of the test device due to the testing). Furthermore, the test techniques are applicable to two terminal devices (e.g., a diode) and also applicable to devices having, for example, three terminals or more (e.g., a transistor).

20 The amount of charge applied to the test device may be varied (e.g., gradually increased) and, for example, a current versus voltage plot generated for the test device based on test measurements. For example, Fig. 12 shows an exemplary plot of current versus voltage for an electrical component in accordance 25 with an embodiment of the present invention. The plot may, for example, represent transmission line pulse test results for an N-channel metal oxide semiconductor (MOS) transistor from drain-to-source terminal with its gate terminal grounded and coupled to the source terminal.

30 A point on the plot labeled V break indicates a failure point of the electrical component, while the plot between V break and a point labeled V hold represents the general

behavior (e.g., resistance) of the electrical component under ESD conditions. By utilizing test data, such as plotted in Fig. 12, generalized parameters may be developed regarding the electrical component to develop an associated macro representing 5 its behavior, which is incorporated into a circuit simulation program (as described in reference to Fig. 1).

As an example, Table 1 illustrates a table of failure criteria for various types of exemplary devices (e.g., various types of transistors and diodes). The values for IT2/W and 10 ITR/W represent exemplary failure currents, normalized and based on width, for these devices, with ITR/W representing the failure current in the direction opposite that of IT2/W. The value for Vtrig is the initial voltage measurement (e.g., as illustrated in Fig. 12), while HBM and CDM provide the maximum allowable 15 voltages (e.g., corresponding approximately to V break illustrated in Fig. 12) when the HBM or CDM ESD stimulus is applied, respectively.

The results of the circuit simulation program may be compared to failure criteria listed, for example, in Table 1 as 20 described for steps 110 and 112 of Fig. 1 to determine if the simulated circuit provides the desired ESD protection. For example, by varying the level of ESD stimulus and checking for destructive failure of the simulated circuit based on the failure criteria, the circuit's level of ESD protection may be 25 determined.

Table 1

DEVICE	IT2/W (mA/μm)	ITR/W (mA/μm)	Vtrig (V)	HBM |Vgmax|	CDM |Vgmax|
NMOS transistor (NO std spacing)	6.67	-6.67	8.9	13.5	18.9
NMOS transistor	8.47	-6.67	8.9	13.5	18.9

(NO 0.5)					
NMOS transistor (NIX) 2.5V	8.47	-5.28	8.9	13.5	18.9
PMOS transistor (PI) 2.5V	-3.2	3.7	8.2	13.5	18.9
NMOS transistor (NI) 2.5V	6.1	-13.2	8.5	13.5	18.9
PMOS transistor (PT) 2.5V	-9	13.5	8.0	13.5	18.9
NMOS transistor (NT) 2.5V	17.8	-47.5	8.5	13.5	18.9
PMOS transistor (PS) 1.2V	-10.5	10	5.9	6	8.4
NMOS transistor (NS) 1.2V	47	-48	4.4	6	8.4
PMOS transistor (PE) 1.2V	-14	21	4.3	6	8.4
NMOS transistor (NE) 1.2V	19.8	-38.5	3.7	6	8.4
Trench isolated diode p+/n-	46.2	-3.56			
Trench isolated diode n+/p-	47.0	-3.26			
Polybound diode p+/n-	43.4	-4.1			
Polybound diode n+/p-	43.4	-4.1			
Back-to-back Stack diode	43.4 46.0	-44.4 -45.5			

As an example, in accordance with an embodiment of the present invention, Table 2 illustrates an exemplary SPICE macro for an NMOS transistor, which provides the SPICE simulation with

the NMOS transistor's behavior under high current/voltage conditions (i.e., behavior under ESD conditions). SPICE macros, such as illustrated by the exemplary SPICE macro in Table 2, may be implemented for various circuit elements whose ESD behavior
5 is desired, as discussed above, to simulate circuit element or circuit behavior under ESD conditions.

Fig. 13 shows an exemplary SPICE simulation plot of current versus voltage for an NMOS transistor in accordance with an embodiment of the present invention. In the SPICE simulation
10 plot, a drain terminal voltage and current are plotted along an x-axis and a y-axis, respectively. The four plotted curves (labeled dc1 through dc4) correspond to a gate terminal bias voltage which varies from 0 to 1.5 volts, respectively, in 0.5 volt steps.

15 Table 2

```
.macro no5esd d g s b w=20 l=0.34 m=36
        .param
        +       sabl=0.8
        +       sabo=0.5
        +       sabg=0.56
        +       dcsb=0.56
        +       scg=1
        +       ct='0.12/2'
*       +       wintf2en=1.3e-7
        +       dw='2*wintf2en*1e6'
        .param
        +       rshsd=6
        +       drsab=0
        +       rshsab='400+drsab'
        +       nrd='sabg/(w-dw)+(dcsb+ct)/(w-dw-2*sabo)'
        +       nrs='(scg+ct)/(w-dw)'
        +       rsab1='rshsab*sabl/(w-dw-2*sabo)'
        +       rsab2='rshsab*(sabl+sabg+ct)/(2*sabo)'
        +       rsab='1/(1/rsab1+1/rsab2)'
        +       rcont='0.3*w*m/20'
        +       resd='rshsd*nrd+rsab+rcont'
        +       ress='rshsd*nrs+rcont'
        rd d ndx resd
        rs s nsx ress
        ddesd1 bb ndx desdu w='w-dw' l='sabl'
        ddesd2 bb ndx desdu w='2*sabo' l='dcsb+ct'
        ddesd3 bb ndx desds w='w-dw-2*sabo' l='dcsb+ct'
        mx1 dd g ss bb nicore w=w l=l geo=3
        + ad='sabg*(w-dw)'
        + as='(scg+ct)*(w-dw)'
```

```
        + pd='2*sabg+2*sabl+2*(dcsb+ct)'
        + ps='2*(dcsb+ct)+(w-dw)'

        rsub bb b '5*pwr(720*0.34/(m*w*l),2)'
        rbase bb nbx '600*pwr(720*0.34/(m*w*l),2)'
        .param CJSW     =1.53e-10
        .param CJB      ='CJSW*w*1e-6'
        .param BETA     ='3*pwr((0.34/l),0)'
        .param TRST     ='3.2*l*l/4*1e-9'
        .model npnb npn geom=-1
                +       area='w*0.1'
                +       areac='w*0.1'
                +       areab='w*l'
                +       tf=TRST tr=TRST cje=CJB cjc=CJB
                +       bf=BETA br=BETA
        qbase ncx nbx nex npnb
        vmd ndx dd
        vmc ndx ncx
        vms nsx ss
        vme nsx nex
        .param LEc      ='l*1'
        .param k1       =0.04
        .param k2       ='4*pwr((0.34/l),1.8)'
        .param d1       ='5.6*pwr((w*m/720),0.23)'
        .param d2       ='5.9*pwr((l/0.34),0.5)'
        .param vt       =0.5

        avdsatc ac 0 v  =IF (v(g)-v(ss)) LE vt THEN 0.0
                + ELSE  (v(g)-v(ss)-vt)/(1+(v(g)-v(ss)-vt)/LEc)
        avdsate ae 0 v  =IF (v(g)-v(dd)) LE vt THEN 0.0
                + ELSE  (v(g)-v(dd)-vt)/(1+(v(g)-v(dd)-vt)/LEc)

        amvds ad 0 v    =v(dd)-v(ss)

***** Igen(C) *****

        amvdp a1 0 v    =IF v(ad) LE v(ac) THEN 0.0
                + ELSE  v(ad)-v(ac)
        amcx amc 0 v    =IF v(a1) LE d1 THEN 1+exp(k2*(v(a1)-d2))
                + ELSE  exp(k1*(v(a1)-d1)) + exp(k2*(v(a1)-d2))

        Eamc1 jc 0 vol='-(v(amc)-1)/m'
        Ramc1 jc 0 1
        FIgc ndx nbx poly(3) Eamc1 vmd vmc 0 0 0 0 0 1 1


***** Igen(E) *****

        amvsp a2 0 v    =IF -v(ad) LE v(ae) THEN 0.0
                + ELSE  -v(ad)-v(ae)
        amex ame 0 v    =IF v(a2) LE d1 THEN 1+exp(k2*(v(a2)-d2))
                + ELSE  exp(k1*(v(a2)-d1)) + exp(k2*(v(a2)-d2))

        Eame1 je 0 vol='-(v(ame)-1)/m'
        Rame1 je 0 1
        FIge nsx nbx poly(3) Eame1 vms vme 0 0 0 0 0 1 1
.eom
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In accordance with one or more embodiments of the present invention, techniques are disclosed which provide for the measurement and characterization of physical electrical components (e.g., transistors and diodes) at high voltages and currents over a very short time domain to extract generalized parameters representing their behavior. The desired electrical components are then incorporated into a circuit schematic and the circuit schematic read into a circuit simulator, such as for example SPICE, along with their generalized parameters (e.g., in the form of associated macros that define the behavior of the electrical components under ESD conditions). A stimulus corresponding to an ESD event is applied to the simulated circuit and resultant voltages and currents are monitored and compared against failure criteria (e.g., a table of failure criteria determined for the electrical components). By varying the level of ESD input stimulus and checking for destructive failure of the simulated circuit based on the failure criteria, a value of ESD immunity (i.e., ESD protection) is obtained for the circuit.

Embodiments described above illustrate but do not limit the invention. It should also be understood that numerous modifications and variations are possible in accordance with the principles of the present invention. Accordingly, the scope of the invention is defined only by the following claims.

CLAIMS

We claim:

1 1. A method of determining electrostatic discharge
2 protection for a circuit, the method comprising:

3 entering the circuit into a circuit simulation program;

4 representing a circuit element of the circuit in the
5 circuit simulation program by its behavior under electrostatic
6 discharge conditions;

7 running the circuit simulation program to obtain simulation
8 results, wherein the circuit simulation program provides an
9 electrostatic discharge stimulus to the circuit; and

10 comparing the simulation results to failure criteria for
11 the circuit.

1

1 2. The method of Claim 1, further comprising testing a
2 physical form of the circuit element to determine its behavior
3 and failure criteria under electrostatic discharge conditions.

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1 3. The method of Claim 2, wherein the testing comprises
2 applying transmission line pulses to the physical circuit
3 element to determine current and voltage behavior of the circuit
4 element.

1

1 4. The method of Claim 2, wherein various parameters of
2 the physical circuit element are varied during the testing to
3 form a generalized behavior model of the circuit element.

1

1 5. The method of Claim 2, wherein various parameters of
2 the physical circuit element are varied during the testing to
3 form a macro for the representing of the circuit element.

1

1 6. The method of Claim 1, wherein the circuit simulation
2 program comprises a SPICE circuit simulation program.

1

1 7. The method of Claim 1, wherein the electrostatic
2 discharge stimulus comprises a charge device model or a human
3 body model.

1

1 8. The method of Claim 1, further comprising determining
2 a performance of the circuit for its intended function based on
3 results of the circuit simulation program.

1 9. A computer readable medium storing a circuit
2 simulation program comprising:

3 symbols for representing a behavior of corresponding
4 circuit elements under normal operating conditions; and

5 symbols for representing a behavior of the corresponding
6 circuit elements under electrostatic discharge conditions.

1

1 10. The computer readable medium of Claim 9, wherein the
2 circuit simulation program further comprises a circuit model for
3 providing electrostatic discharge input signals to a simulated
4 circuit.

1

1 11. The computer readable medium of Claim 10, wherein the
2 circuit model comprises a charge device circuit model and/or a
3 human body circuit model.

1

1 12. The computer readable medium of Claim 9, wherein the
2 symbols for representing a behavior of the corresponding circuit
3 elements under electrostatic discharge conditions correspond to
4 macros which provide a general behavior of the corresponding
5 circuit elements based on electrostatic discharge testing of the
6 circuit elements.

1

1 13. A method of testing a circuit for electrostatic
2 discharge protection, the method comprising:

3 providing a circuit simulation program to simulate the
4 circuit; and

5 providing macros within the circuit simulation program
6 which represent a behavior of corresponding circuit elements
7 under electrostatic discharge conditions.

1

1 14. The method of Claim 13, further comprising providing
2 an electrostatic discharge circuit model within the circuit
3 simulation program to simulate an electrostatic discharge
4 applied to the circuit.

1

1 15. The method of Claim 14, wherein the electrostatic
2 discharge circuit model comprises a charge device circuit model
3 or a human body circuit model.

1

1 16. The method of Claim 13, wherein the circuit simulation
2 program is operable to simulate the circuit under electrostatic
3 discharge conditions.

1

1 17. The method of Claim 13, wherein the circuit simulation
2 program is operable to simulate the circuit under electrostatic
3 discharge conditions and compare simulation results to failure
4 criteria.

1

1 18. The method of Claim 13, wherein the circuit simulation
2 program is operable to simulate the circuit under electrostatic
3 discharge conditions to generate simulation results for
4 comparison to failure criteria.

1

1 19. The method of Claim 13, wherein the macros are based
2 on test results of the corresponding circuit elements under
3 electrostatic discharge conditions.

1

1 20. The method of Claim 13, wherein the circuit simulation
2 program comprises a SPICE circuit simulation program.

1

1 21. A method of generating circuit element macros for
2 simulating electrostatic discharge behavior, the method
3 comprising:

4 testing a physical circuit element to determine its
5 behavior and failure criteria under electrostatic discharge
6 conditions; and

7 creating an associated macro for the physical circuit
8 element representing the determined electrostatic discharge
9 behavior, the macro suitable for use in a circuit simulation
10 program.

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1 22. The method of Claim 21, wherein the testing operation
2 further comprises varying parameters of the physical circuit
3 element to generalize the determined electrostatic discharge
4 behavior for the physical circuit element.

1

1 23. The method of Claim 21, wherein the circuit simulation
2 program comprises a SPICE circuit simulation program.

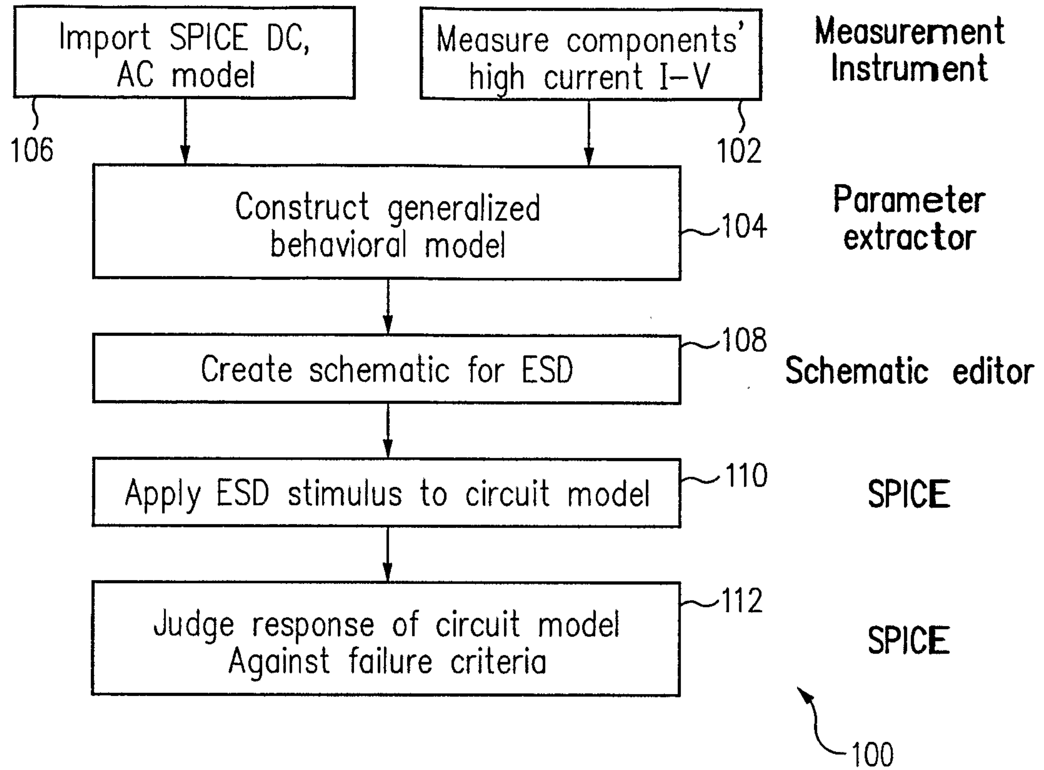

FIG. 1

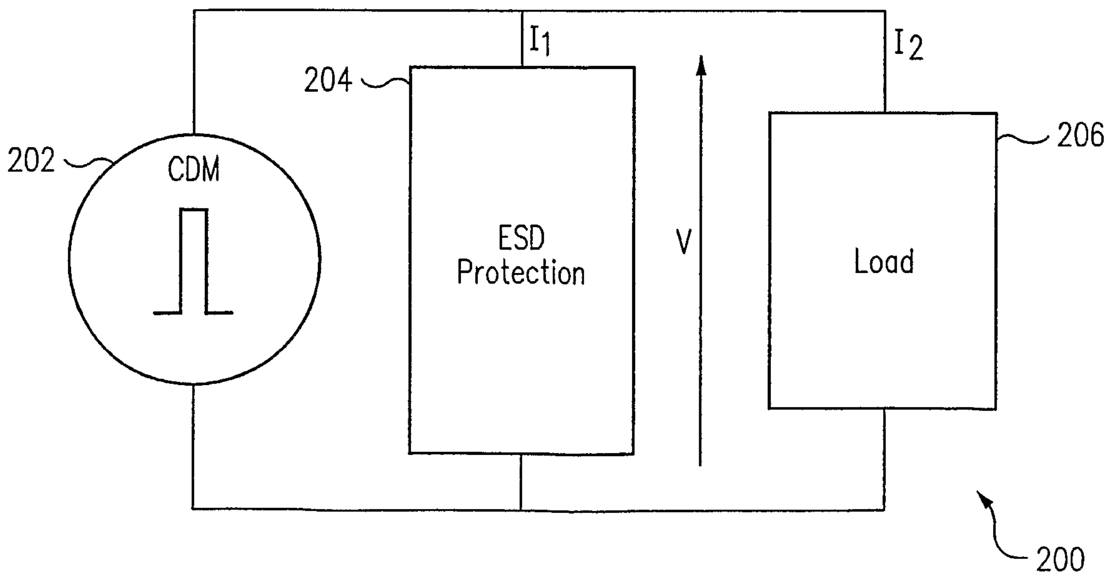

FIG. 2

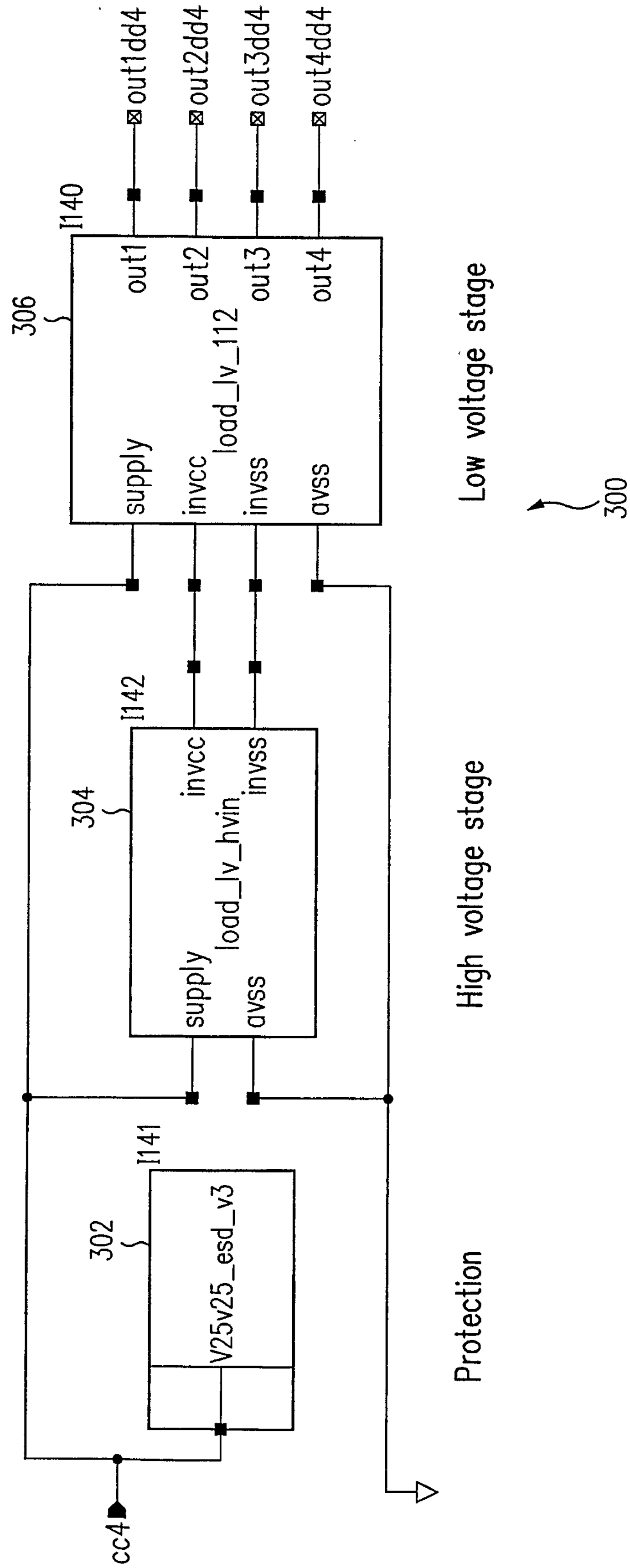

FIG. 3

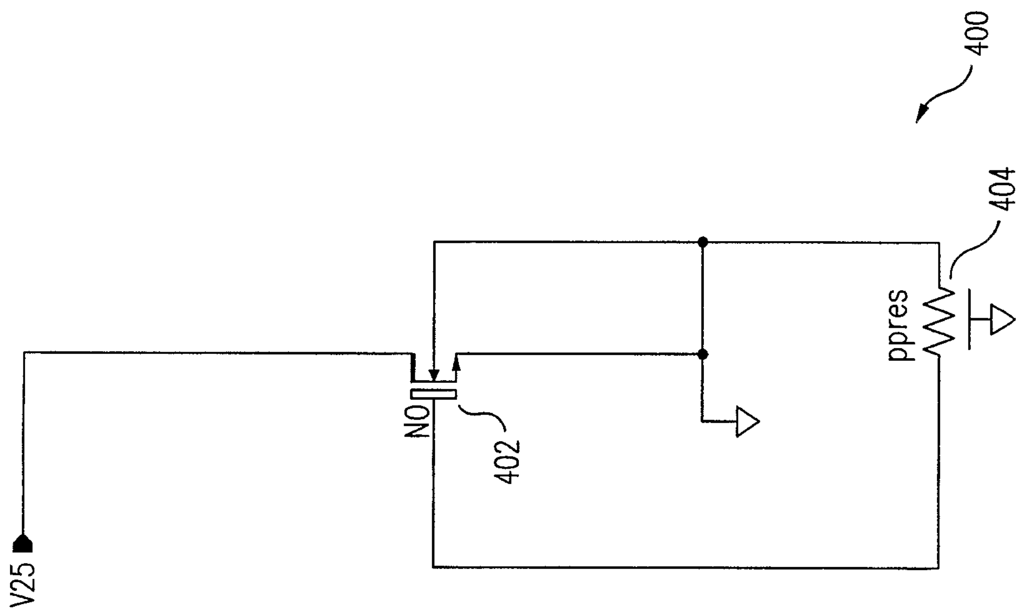

FIG. 4

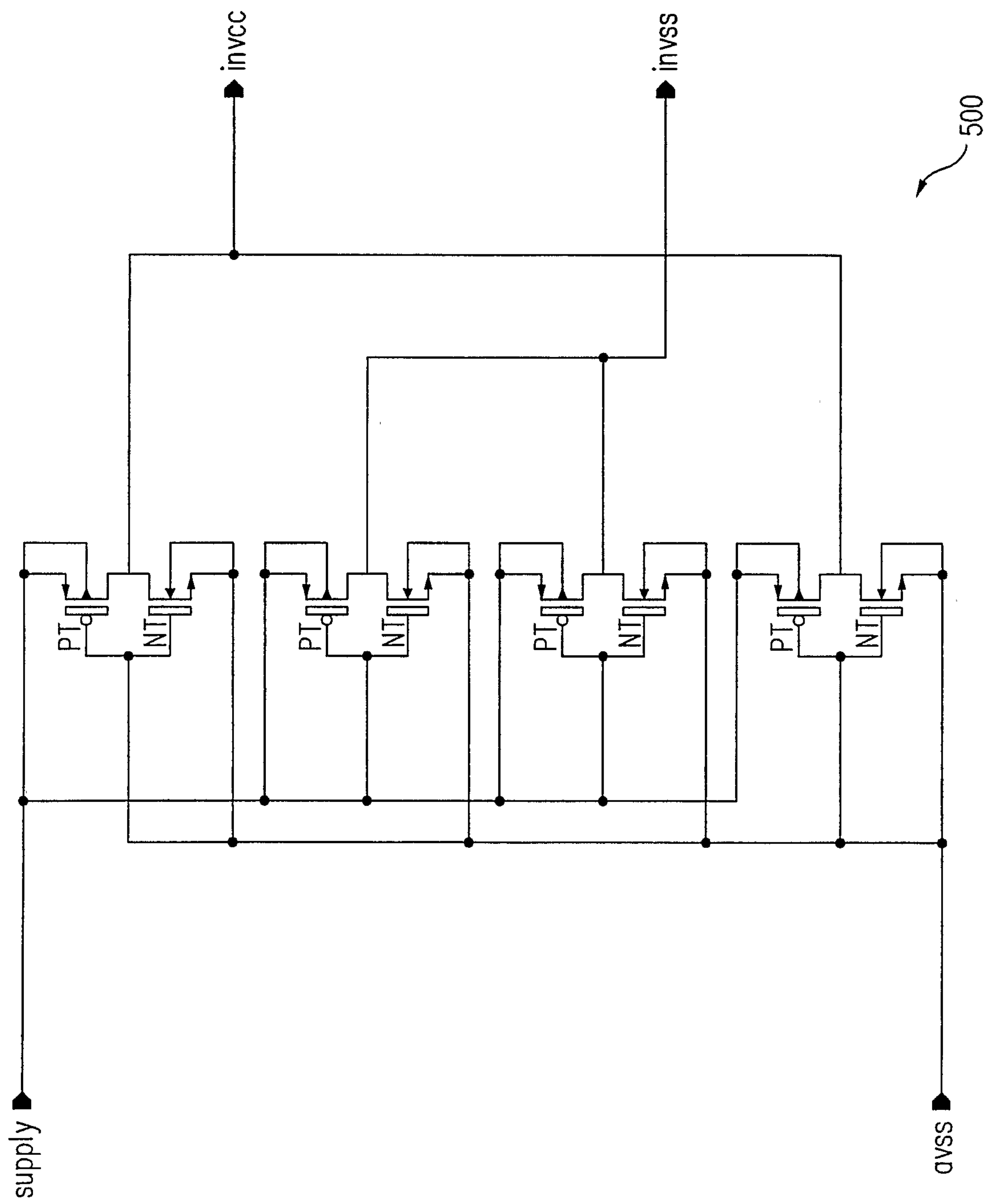

FIG. 5

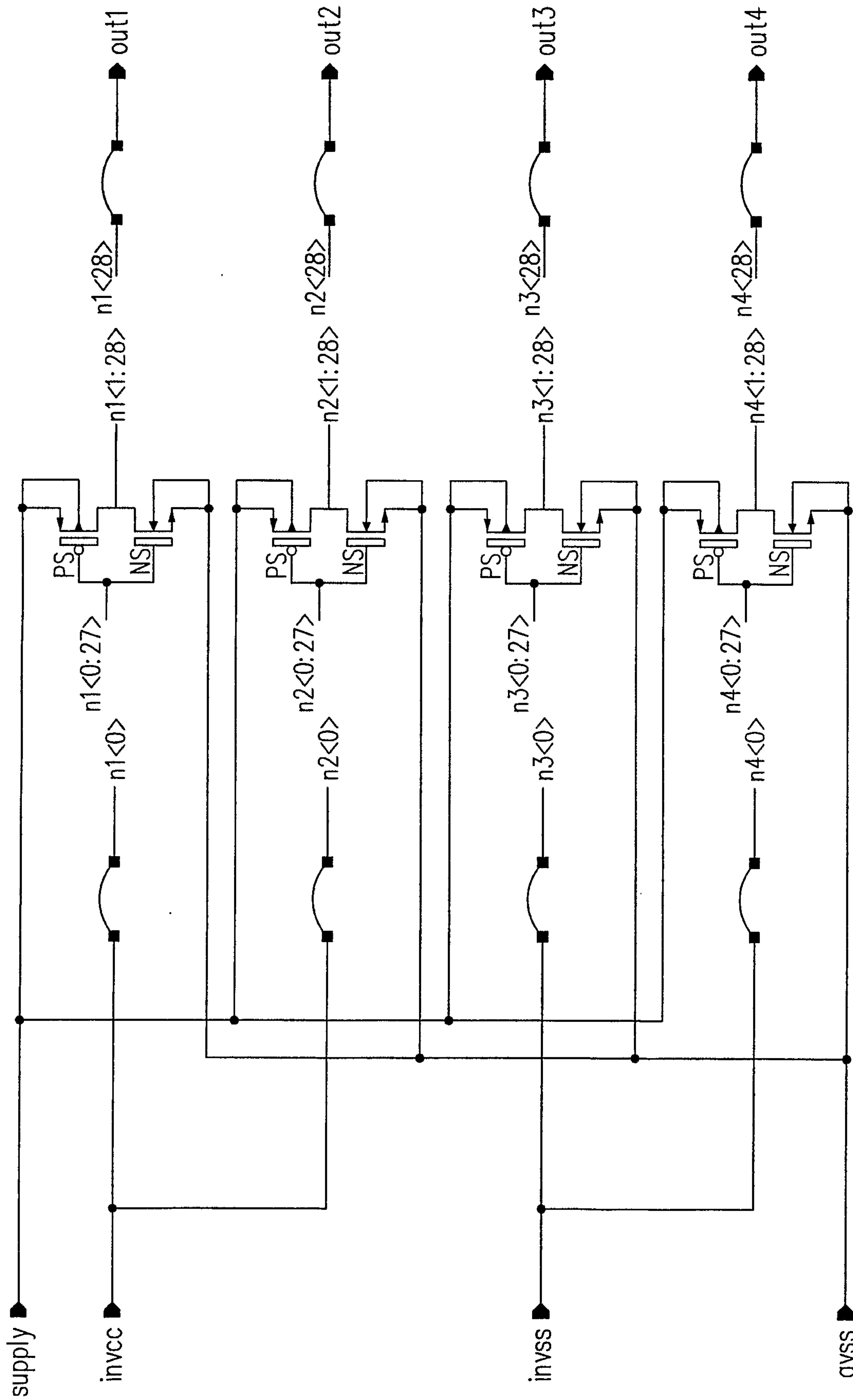

FIG. 6

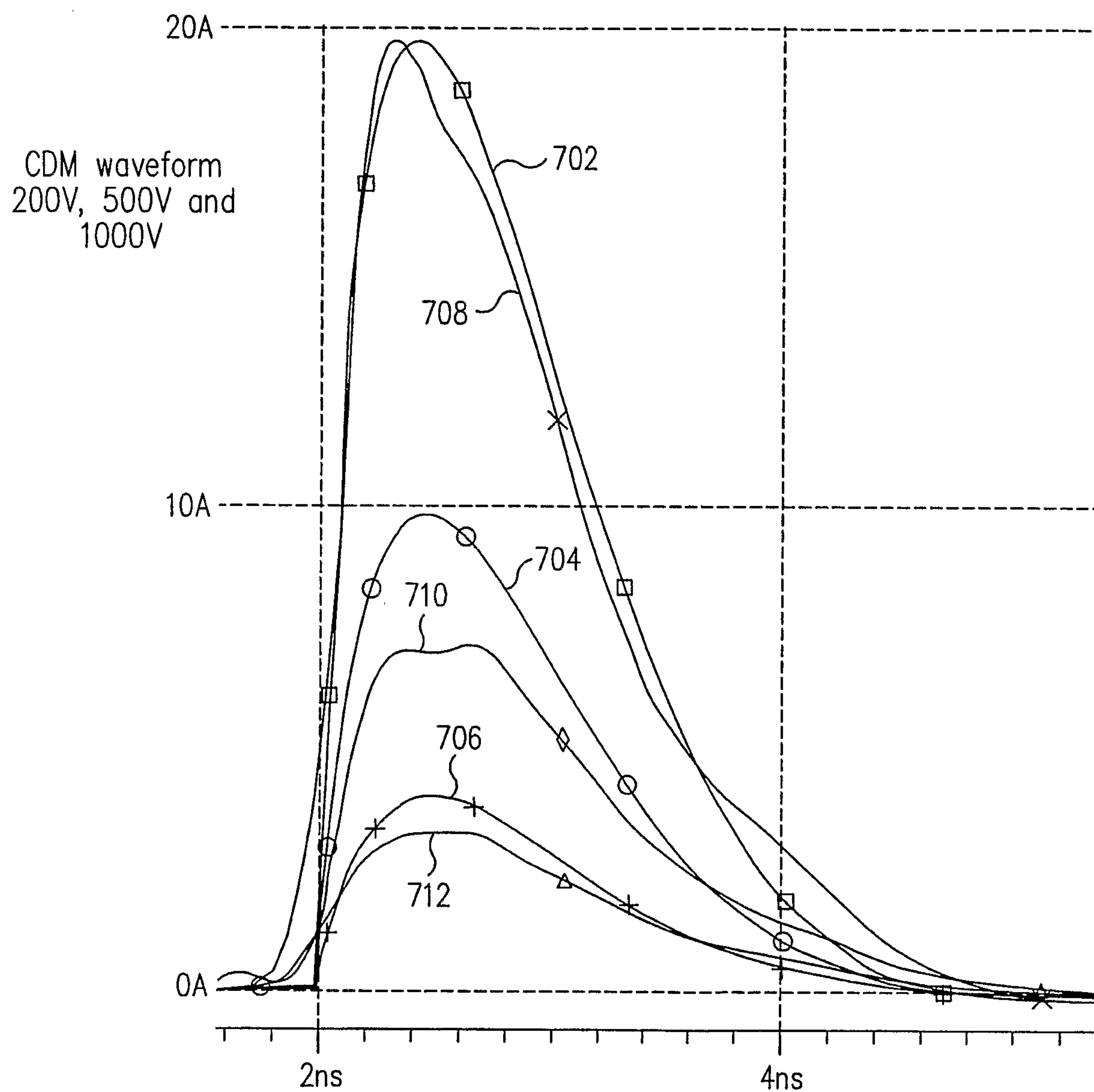

FIG. 7

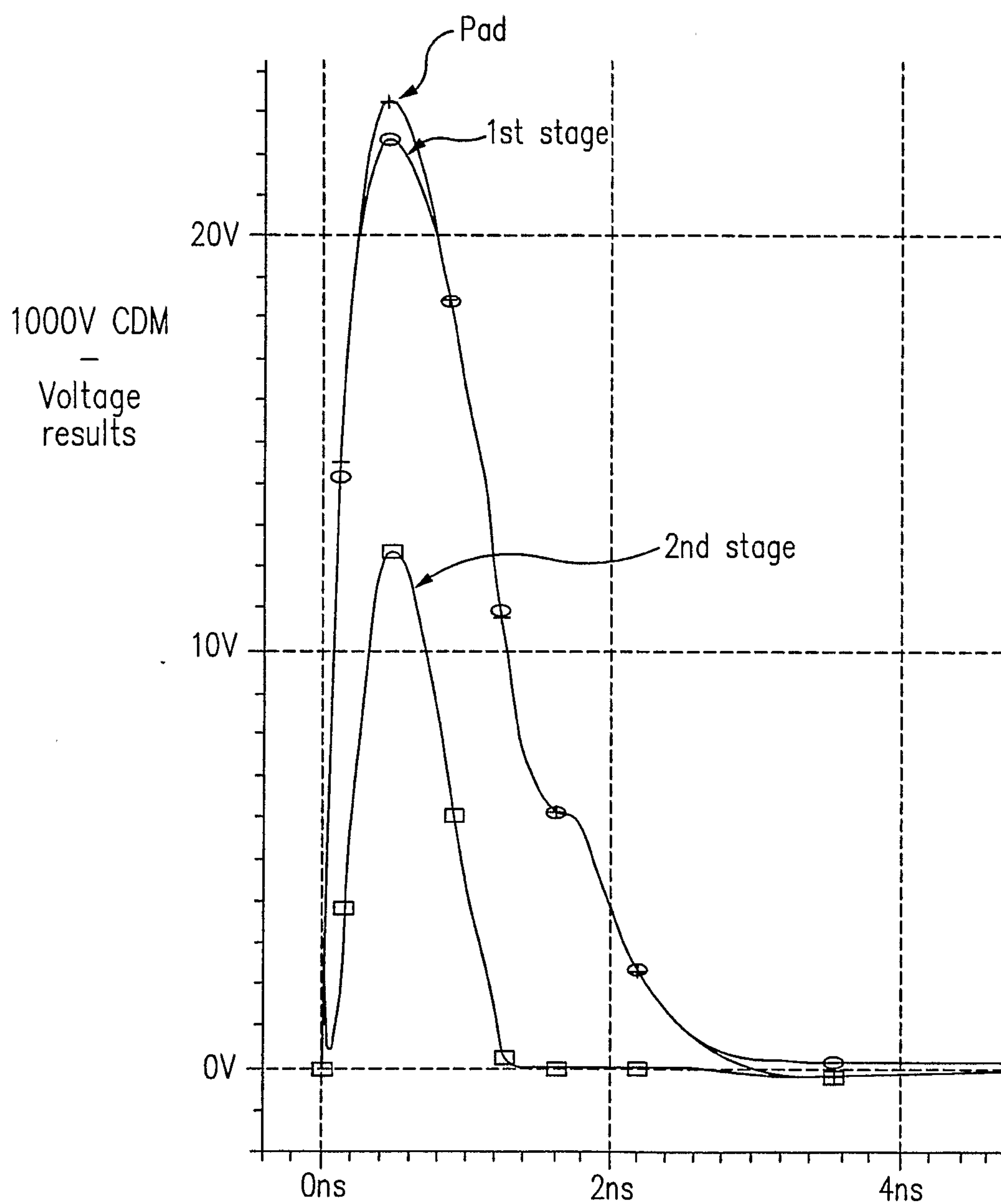

FIG. 8

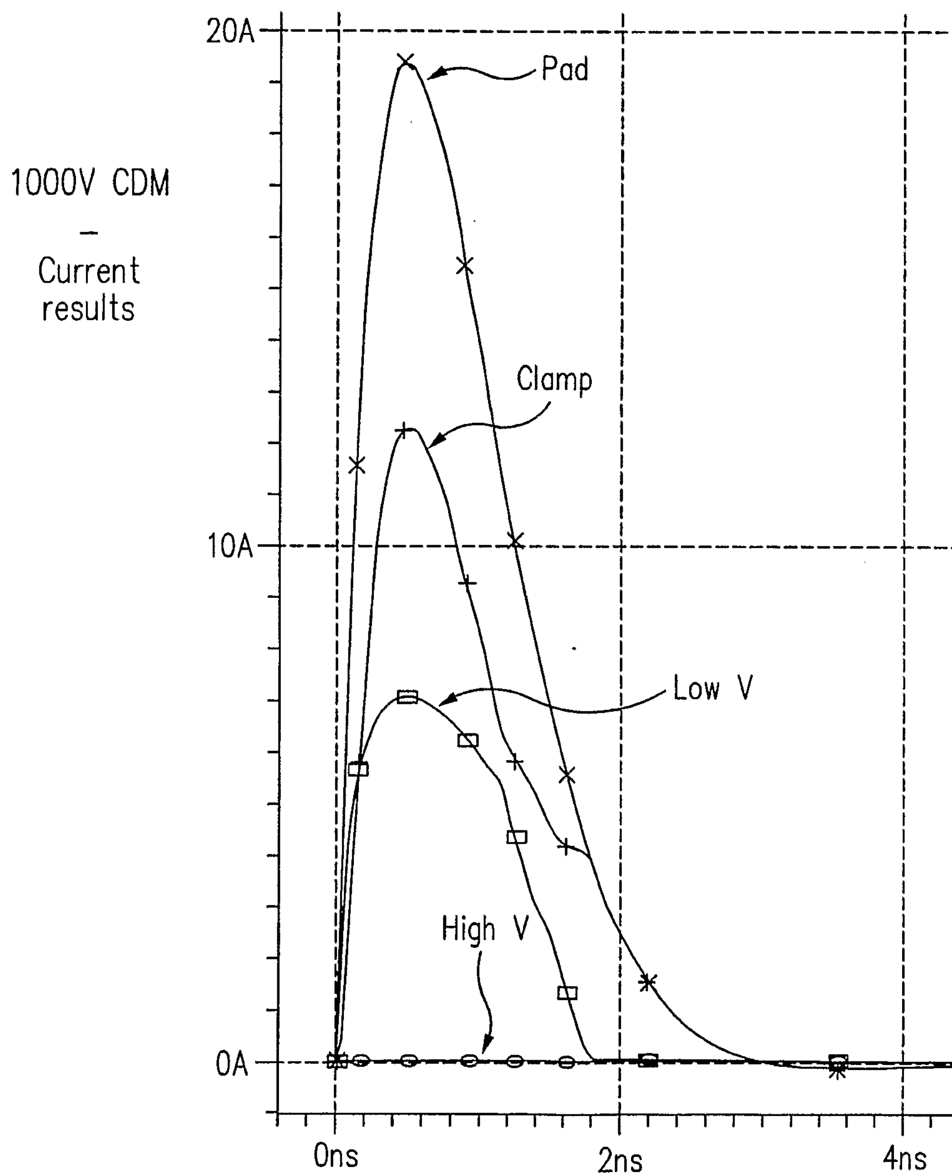

FIG. 9

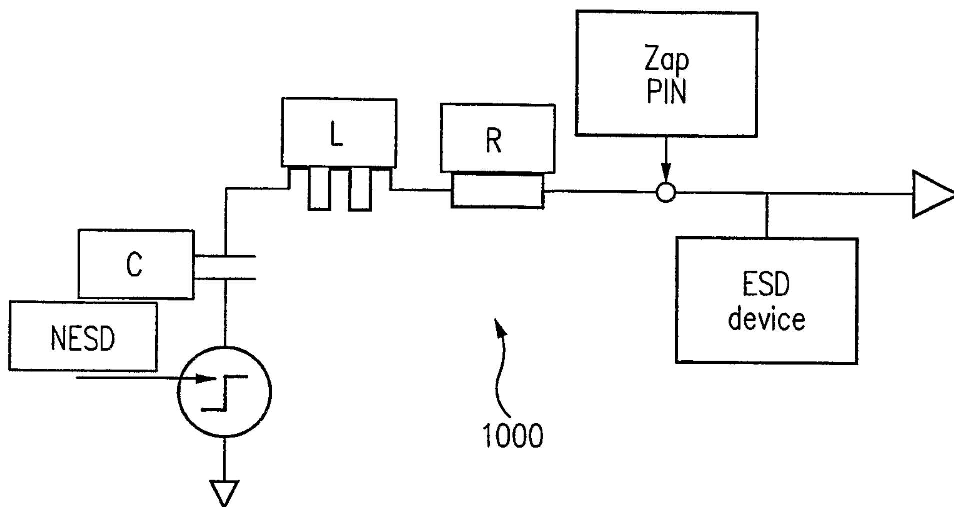

FIG. 10

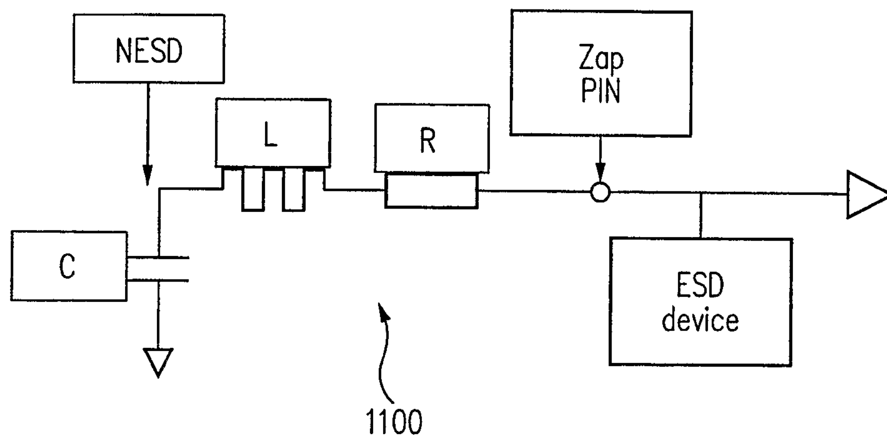

FIG. 11

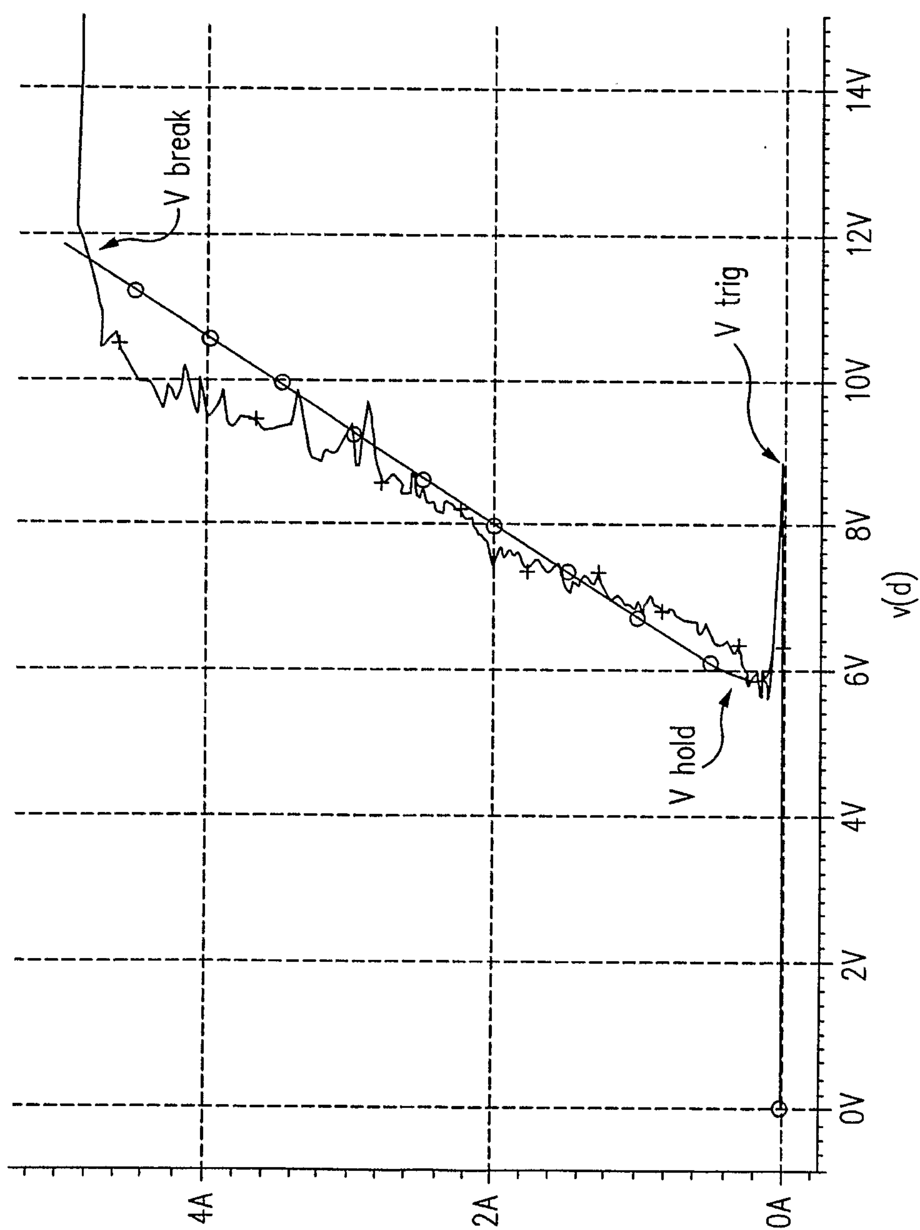

FIG. 12

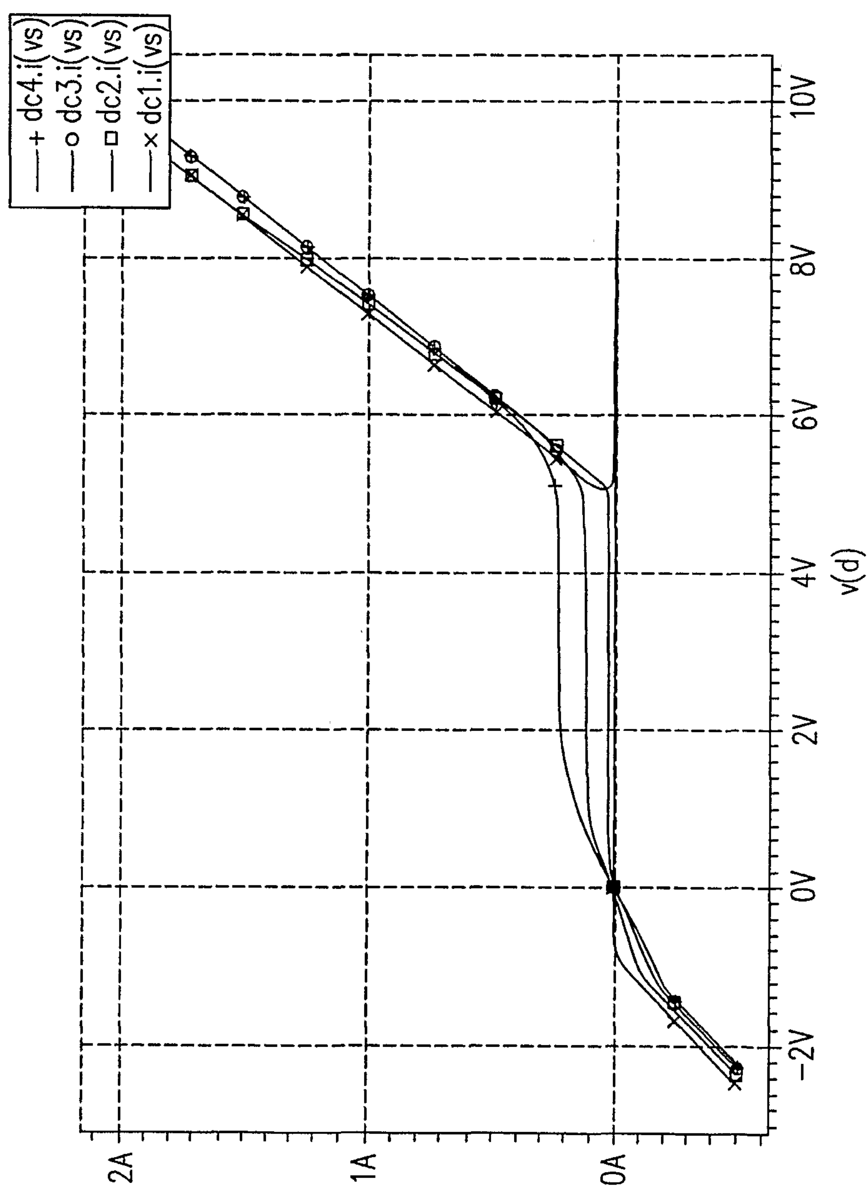

FIG. 13