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(71) Applicant: **SOLAR JUNCTION CORPORATION** [US/US]; 401 Charcot Avenue, San Jose, California 95131 (US).

(72) Inventors: **FIDANER, Onur**; 373 River Oaks Circle, Apt 803, San Jose, California 95134 (US). **WIEMER, Michael West**; 21 Heritage Court, Campbell, California 95008 (US).

(74) Agents: **LAMBERT, William R.** et al.; Kilpatrick Townsend & Stockton LLP, Two Embarcadero Center, 8th Floor, San Francisco, California 94111 (US).

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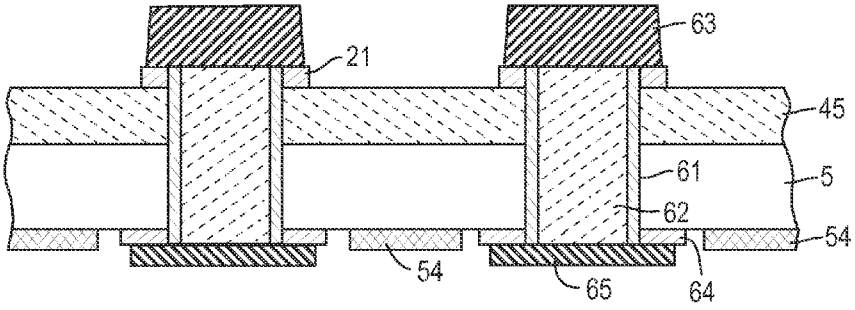



FIG. 5A

(57) Abstract: Multi-junction solar cells and methods for making multi-junction solar cells are disclosed. Back-contact-only multi-junction solar cells wherein the side facing the sun, is capable of withstanding environments for use in space are disclosed.

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# MULTI-JUNCTION SOLAR CELLS WITH THROUGH-SUBSTRATE VIAS

[0001] This application is a continuation-in-part of U.S. Application No. 13/856,573 filed on April 4, 2013, which claims the benefit under 35 U.S.C. § 119 (e) of U.S. Provisional Application No. 61/621,277 filed on April 6, 2012; and this application claims the benefit under 35 U.S.C. § 119 (e) of U.S. Provisional Application No. 61/794,293 filed on March 15, 2013, each of which is incorporated by reference in its entirety.

## FIELD

[0002] This disclosure relates to multi-junction solar cells and methods for making multi-junction solar cells. More particularly, the disclosure relates to back-contact-only multi-junction solar cells and the process flows for making such solar cells wherein the side facing the sun, is capable of withstanding environments for both terrestrial and space use.

## BACKGROUND

[0003] Because of their high efficiency, conventional multi-junction solar cells have been widely used for terrestrial and space applications. Multi-junction solar cells include multiple diodes in series connection, known in the art as "junctions," realized by growing thin regions of epitaxy in stacks on semiconductor substrates. Each junction in a stack is optimized for absorbing a different portion of the solar spectrum, thereby improving efficiency of solar energy conversion.

[0004] Conventional multi-junction solar cells have features that reduce the efficiency of solar to electrical energy conversion. For example, a portion of solar energy incident on the front side of a solar cell cannot be absorbed due to metallic electrodes blocking a portion of the side facing the sun. Furthermore, a portion of the absorbed solar energy cannot be collected at the electrodes as electrical power because the energy is dissipated as heat (for example, as resistive loss) during lateral conduction in the emitter region of the top junction and in the metallic gridlines. For high-power devices, such as concentrated photovoltaic devices or large area solar cells, the dissipated heat may also result in substantially increased temperature, thereby further reducing the performance of the device. Typically there is a trade-off between these parameters and others. Multi-junction solar cells are typically designed to give the optimum solar to electrical energy conversion performance under desired conditions. It is desirable to improve efficiency in multi-junction solar cell devices.

**[0005]** Multi-junction solar cells can be used in space as well as terrestrially. In addition to the aforementioned design trade-offs, conventional space-qualified multi-junction solar cells are also required to exhibit radiation hardiness and metal interconnect structures integrated with the solar cells. Radiation hardiness is defined as minimal degradation in device performance when exposed to ionizing radiation including electrons and protons. For these space-qualified multi-junction solar cells, radiation hardiness is of great importance for preserving the material quality of the junctions and substrate for an extended lifetime. Typically a space-grade coverglass is used to provide radiation hardiness. The space-grade coverglass can be made of several materials including but not limited to borosilicate glass. The application of the coverglass on the cell and the attachment of the interconnect structures require special processing techniques that increase the cost of solar cells used in space. Techniques are, therefore, needed to improve long-term performance of a multi-junction solar cell for use in space while considering cost effectiveness, which is facilitated by the ease of production of solar cells with such covers and interconnects.

**[0006]** FIG. 1A shows a cross-section schematic of a typical (prior art) multi-junction solar cell device 100. The solar cell 100 shown in FIG. 1A consists of three sub-cells (junctions) 106-108 that are connected through tunnel junctions 167 and 178. It is to be understood that FIG 1A is merely an example of a typical multi-junction solar cell and that such solar cells may include any number of sub-cells. FIG. 1B is a simplified schematic of a typical (prior art) multi-junction solar cell.

**[0007]** Referring to FIG. 1A, the front surface field (FSF) region 4 is the window region that faces the sun after cap etch. Underneath the FSF region 4 is the emitter region 102 of the top p-n junction 106 that forms a diode. Similar junctions 107 and 108 are disposed below the top p-n junction thus forming a multi-junction solar cell. The top electrode includes gridlines 2 making contact with the FSF region 4 through cap region 3, wherein the cap region consists of semiconductor material patterned according to the shape of the metallic gridlines 2. The bottom electrode is a metal region 52 at the back surface of the solar cell in contact with the substrate 5.

The factors reducing the efficiency of multi-junction solar cells, shadowing loss, emitter loss, and grid loss are relevant to the present invention.

**[0008]** *Shadowing Loss:* In typical multi-junction solar cells the top electrode consists of regular grids of metal wires. The metal gridlines 2 and cap regions 3 block sunlight from entering the solar cell. For solar cells for which the width of the cap region is slightly larger

than the width of the metal gridlines, the cap width x determines the total width blocking the light for each gridline. Referring to FIG. 1B, the gridline width x' is typically related to the cap width x through a process constant $x_c$, such that $x=x'+x_c$. Hence, when the shadowing width x is increased or decreased as a design parameter, the metal width x' is also increased or decreased by the same amount. For gridlines spaced by a distance y, the shadowing loss is approximately x/y. Therefore, increasing the width x and/or decreasing the spacing y increases the shadowing loss.

**[0009]** *Emitter Loss:* Carriers are generated across a solar cell as a result of absorption of sunlight. Referring to FIG. 1A, photogenerated carriers that reach the emitter 102 have to move laterally towards the gridlines 2, as illustrated by arrows 28 in FIG. 2B. The emitter 102 and the FSF 4 are thin, doped semiconductor regions and together form a lateral conduction region 132. Carrier transport across the lateral conduction region 132 results in a resistive power loss that depends on the sheet resistivity of the conductive region and the distance the carriers have to travel to reach the gridlines 2. Hence, for a given sheet resistivity, the smaller the gridline spacing y the smaller the emitter loss is.

**[0010]** *Grid Loss:* Gridlines are metal resistors, resulting in resistive losses as the current moves toward the busbars 22, as illustrated with arrows 27. The grid loss is determined by the cross section area and the length of the gridlines and the metal resistivity of the gridlines. For larger cells the gridlines are longer, resulting in larger [grid loss] / [total loss] ratio compared to smaller cells.

**[0011]** The emitter and grid losses are resistive losses (i.e., $I^2R$ losses). Hence, when the concentration of incident sunlight increases, the current extracted from the solar cell increases and consequently the $I^2R$ losses increase even more. For example, going from a concentration of 500X to 1000X the resistive losses will approximately quadruple for a given cell design.

**[0012]** The grid loss can be made smaller by using more gridlines (hence reducing y) or increasing the cross-section area (hence increasing x). Hence, reducing the grid loss (for given process parameters) comes at the expense of increased shadowing loss. In prior art solar cells there is a need to reduce the grid loss component without increasing the shadowing loss component.

**[0013]** The prior art for space-qualified multi-junction solar cells includes a product consisting of a solar cell, interconnects, and coverglass (also referred to as CIC). In the fabrication of prior art solar cells, space-qualified coverglass is applied to the front of the

solar cell with a transparent adhesive to protect the solar cell from the harsh environment in space. Interconnects for routing power out of the cell are welded onto the front and the back sides of the cell. There is a need for a robust coverglass integration process that is part of the front-end process such that cells can be tested at the wafer-scale after coverglass integration.

**[0014]** Furthermore, the design of a solar cell top electrode and surface affect cover materials or coatings that may be added either on top, surrounding, or on the bottom of the solar cell to protect it from potentially damaging environments, such as environments with high radiation in space. There is a need for a robust coverglass integration process that can be streamlined with the process flow of the solar cell manufacturing.

**[0015]** A through substrate via (TSV), also known as a through wafer via (TWV), is an electrical interconnect between the top and bottom surfaces of a semiconductor chip. TSV structures have been routinely used for a variety of applications in the field of semiconductor devices. Fabrication methods to provide TSV structures are known to those skilled in the art of semiconductor devices. For example, Chen et al. (Journal of Vacuum Science and Technology B, Volume 27, Issue 5, "Cu-plated through-wafer vias for AlGaN/GaN high electron mobility transistors on Si") disclose a semiconductor device with through wafer vias for a high mobility electron transport device application.

**[0016]** Through-substrate via structures have also been applied to solar cell devices. One of the purposes of using TSV structures in solar cells is to provide a back-contact-only solar cell for packaging requirements. Some approaches for back-contact solar cells have been summarized by Van Kerschaver et al. (Progress in Photovoltaics: Research and Applications 2006; 14:107-123).

**[0017]** Kinoshita et al. (US 2008/0276981 A1) disclose a structure that provides a through-wafer-via structure incorporating metal with dielectric liner that connects the gridlines on the top surface to the backside of a solar cell. The structure disclosed by Kinoshita provides a back-contact-only solar cell. However the disclosed structure does not reduce grid losses substantially, since gridlines along the length of the cell are used for current transport.

**[0018]** Dill et al. (US 4,838,952 A) disclose a through-wafer-via structure that connects the emitter region of a solar cell to the backside. The structure disclosed by Dill et al. is not applicable to multi-junction solar cells. Multi-junction solar cells are comprised of a number of epitaxial semiconductor layers with a variety of doping schemas. Therefore, for multi-junction solar cells, it is not possible to use a single doping type around a through-wafer

metallic region to electrically isolate it from the semiconductor materials the metallic region is passing through.

**[0019]** Guha et al. (US 8,115,097 B2) disclose a gridline-free contact for a photovoltaic cell. The structure disclosed by Guha et al. employs laterally-insulated through-wafer vias connecting the surface portion of the photovoltaic cell (i.e. the emitter) to the back surface. Contact between the top surface of the metal in the through wafer via and the emitter region is within the substrate, such that there is a region of semiconductor between the top of the through wafer via and the top surface of the solar cell. The disclosure by Guha et al. does not teach how though-wafer via structure can be integrated in multi-junction solar cells, which employ various thin semiconductor epitaxial layers with different purposes. For example, it is a requirement in multi-junction solar cells to use a contact region 3 and a front surface field 4 between the emitter 102 and the metal contact 2.

**[0020]** Therefore, there is a need to increase the efficiency of multi-junction solar cells by reducing the grid losses while preventing the solar cell from degradation during use in space.

## SUMMARY

**[0021]** The present invention demonstrates a multi-junction solar cell that incorporates several embodiments using at least one through substrate via formed through the epitaxial region of the solar cell and the substrate to reduce losses associated with metal grid resistance. In particular, through-substrate vias are provided that are electrically isolated from the solar cell substrate and from each of the epitaxial regions overlying the solar cell substrate, except for the cap regions. In addition, the through-substrate vias cross-sectional dimensions are designed to minimize shadowing losses. The multi-junction solar cells of the present invention also provide cost-effective coverglass integration that also substantially reduces solar cell degradation for terrestrial and space use. The semiconductor materials used in the substrate may include, for example, gallium arsenide, silicon, and germanium. The epitaxial regions may include one or more lattice matched or metamorphic subcells including, for example tunnel junctions, front surface field (FSF), emitter, depletion region, base and back surface field. Semiconductor materials used in these subcells may include, but are not limited to, indium gallium phosphide, indium phosphide, gallium arsenide, aluminum gallium arsenide, indium gallium arsenide, germanium, and dilute nitride compounds such as GaInNAsSb, GaInNAsBi, GaInNAsSbBi, GaNAsSb, GaNAsBi, and GaNAsSbBi. For ternary and quaternary compound semiconductors, a wide range of alloy ratios can be used.

The cap regions can be patterned such that they encircle the via structures on the top surface of the solar cell. As a result, gridlines extending across the entire length of the solar cell can be eliminated and electrodes are accessible from the backside of the multi-junction solar cell.

**[0022]** In a first aspect, multi-junction solar cell devices are provided comprising an electrically conductive semiconductor substrate with at least one multi-junction solar cell element formed in an epitaxial region grown thereon; a plurality of cap regions formed on top of the epitaxial region; a plurality of through-substrate via heads corresponding to each of the plurality of cap regions formed on a back surface of the substrate; through-substrate vias that extend through the substrate from each of the plurality of cap regions to the corresponding through-substrate vias heads; conductive metal within the through-substrate vias and electrically connecting each of the plurality of cap regions to the corresponding through-substrate via heads; an electrically insulating liner disposed on the walls of each of the through-substrate vias insulating the substrate and the epitaxial region from the conductive metal inside the through-substrate vias; an optical cover material disposed upon an optically transparent adhesive material directly above each of the plurality of through- substrate via heads; and a back metal, patterned with a back metal pattern, in ohmic contact with the back surface of the electrically conductive semiconductor substrate, and electrically isolated from the through-substrate via heads.

**[0023]** In a second aspect, methods of forming a through-substrate via heads are provided, comprising providing a substrate having an epitaxial region grown thereon and a plurality of cap regions formed on top of the epitaxial region; depositing a photoresist region on the plurality of cap regions; etching a plurality of through-substrate vias from a backside of the substrate and using the photoresist region as an etch stop layer; depositing an electrically insulating liner within each of the plurality of through-substrate vias; removing the photoresist region to expose the plurality of cap regions; and depositing metal within the through-substrate vias to connect the plurality of cap regions.

**[0024]** In a third aspect, multi-junction solar cell devices are provided, comprising a semi-insulating semiconductor substrate having a back surface; an epitaxial region overlying the semi-insulating semiconductor substrate; an electrically conductive semiconductor region between the substrate and the epitaxial region; at least one multi-junction solar cell element formed in the epitaxial region, the epitaxial region being grown on the electrically conductive semiconductor region; a cap region overlying the epitaxial region; though-wafer vias that extend from the cap region to the back surface of the substrate; the cap region being shaped

according to a cap pattern including collars around the through-wafer vias; conductive metal within the through-wafer vias and electrically connected to the cap patterned collars; an electrically insulating liner on the walls of the through-wafer vias insulating the conductive metal inside the through-wafer vias from at least the epitaxial region and from the conductive semiconductor region; an optical cover material disposed upon an optically transparent adhesive material directly above the through-substrate via heads formed on top of the epitaxial region; and a back metal on the back surface of the substrate in electrical contact with the conductive metal in the through-wafer vias.

**[0025]** In a fourth aspect, multi-junction solar cell devices are provided, comprising an electrically conductive semiconductor substrate with at least one multi-junction solar cell element formed in an epitaxial region grown thereon; a plurality of cap regions formed on top of the epitaxial region; through-substrate vias that extend from the plurality of cap regions to a back surface of the substrate; conductive metal within the through-substrate vias and electrically connected to the plurality of cap regions; an electrically insulating liner disposed on the walls of the through-substrate vias insulating the substrate and the epitaxial region from the conductive metal inside the through-wafer vias; a through-substrate via head that electrically connects the conductive metal within the through-substrate vias with the plurality of cap regions, henceforth called; a temporary carrier substrate bonded directly above the through substrate via heads formed on top of the epitaxial region; and a back metal, patterned with a back metal pattern, in ohmic contact with the back surface of the electrically conductive semiconductor substrate, and electrically isolated from the conductive metal within the through-substrate vias.

**[0026]** In a sixth aspect, methods of forming a multi-junction solar cell devices are provided, comprising providing an electrically conductive semiconductor substrate with at least one multi-junction solar cell element formed in an epitaxial region grown thereon, and a plurality of cap regions formed on top of the epitaxial region; bonding a cover glass on top of the substrate and the plurality of cap regions; thinning the substrate; etching through-substrate vias from a back surface of the substrate; forming a patterned dielectric layer on the back surface of the substrate; and forming electrical connection between the patterned cap region and the back metal contacts pads with conductive metal inside the through-substrate vias, such that the contact pads are not directly electrically connected to the semiconductor substrate.

[0027] In a seventh aspect, methods of forming a multi-junction solar cell devices are provided, comprising providing an electrically conductive semiconductor substrate with at least one multi-junction solar cell element formed in an epitaxial region grown thereon, and a patterned cap region formed on top of the epitaxial region; bonding a polymer cover on top of the substrate and the patterned cap region; thinning the substrate; etching through-substrate vias from a back surface of the substrate; forming a patterned dielectric layer on the back surface of the substrate; forming a plurality of back metal contact pads; and forming electrical connection between the patterned cap region and the back metal contacts pads with conductive metal inside the through-substrate vias, such that the contact pads are not directly electrically connected to the semiconductor substrate.

[0028] In another aspect, multi-junction solar cells are disclosed, comprising: an electrically conductive semiconductor substrate with at least one multi-junction solar cell element formed in an epitaxial region grown thereon; an annular cap region formed on top of the epitaxial region; through-substrate vias that extend from the annular cap region to a back surface of the substrate; conductive metal within the through-substrate vias and electrically connected to the annular cap region; an electrically insulating liner disposed on the walls of the through-substrate vias insulating the substrate and the epitaxial region from the conductive metal inside the through-wafer vias; a through-substrate via head that electrically connects the conductive metal within the through-substrate vias with the annular cap region, henceforth called; and a back metal, patterned with a back metal pattern, in ohmic contact with the back surface of the electrically conductive semiconductor substrate, and electrically isolated from the conductive metal within the through-substrate vias.

[0029] In another aspect, multi-junction solar cells are disclosed, comprising: a semi-insulating semiconductor substrate having a back surface; an epitaxial region overlying the semi-insulating semiconductor substrate; an electrically conductive semiconductor region between the substrate and the epitaxial region; at least one multi-junction solar cell element formed in the epitaxial region, the epitaxial region being grown on the electrically conductive semiconductor region; a cap region overlying the epitaxial region; though-wafer vias that extend from the cap region to the back surface of the substrate; the cap region being shaped according to a cap pattern including collars around the through-wafer vias; conductive metal within the through-wafer vias and electrically connected to the collars; an electrically insulating liner on the walls of the through-wafer vias insulating the conductive metal inside the through-wafer vias from at least the epitaxial region and from the conductive

semiconductor region; and a back metal on the back surface of the substrate in electrical contact with the conductive metal in the through-wafer vias.

**[0030]** In another aspect, methods of making multi-junction solar cells incorporating an optical cover material during the process flow and having through-substrate vias such as those in the first and second aspects are disclosed. Such process flows for incorporating a through substrate via in the multi-junction solar cell are efficient and cost effective and use an optical cover glass as a carrier substrate during backside processing. The cover glass is also designed to then withstand reliability conditions for solar cell use, and in some cases, for use in space. In particular, the process flows disclose backside etching of the through substrate vias once the epitaxial wafer, on the front side, is already processed.

**[0031]** In the following description, reference is made to the accompanying drawings which form a part hereof wherein like numerals designate like parts throughout, and in which is shown by way of illustration specific embodiments in which the invention may be practiced.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0032]** The drawings described herein are for illustration purposes only. The drawings are not intended to limit the scope of the present disclosure.

**[0033]** FIG. 1A is a cross-sectional diagram of a multi-junction solar cell in which the invention may be used.

**[0034]** FIG. 1B is a simplified version of FIG. 1A.

**[0035]** FIG. 2A shows a typical prior art solar cell with gridlines 2 and busbars 22.

**[0036]** FIG. 2B shows where the grid losses and emitter losses occur.

**[0037]** FIG. 3A shows one specific embodiment of the invention.

**[0038]** FIG. 3B shows an aerial view of FIG. 3A.

**[0039]** FIG. 4A shows one specific embodiment of the invention.

**[0040]** FIG. 4B shows an aerial view of FIG. 4A.

**[0041]** FIG. 5A shows one specific embodiment of the invention.

**[0042]** FIG. 5B shows an aerial top view of FIG. 5A.

**[0043]** FIG. 5C shows the backside view of FIG. 5A.

**[0044]** FIG. 6A shows one specific embodiment of the invention.

**[0045]** FIG. 6B shows a cross-sectional diagram of FIG. 6A.

**[0046]** FIGS. 7A –7F illustrate the process flow for a specific embodiment of the invention.

[0047] FIGS. 8A – 8F illustrate the process flow for a specific embodiment of the invention.

[0048] FIG.. 9A – 9F illustrate the process flow for a specific embodiment of the invention.

[0049] Reference is now made in detail to embodiments of the present disclosure. While certain embodiments of the present disclosure are described, it will be understood that it is not intended to limit the embodiments of the present disclosure to the disclosed embodiments. To the contrary, reference to embodiments of the present disclosure is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the embodiments of the present disclosure as defined by the appended claims.

## DETAILED DESCRIPTION

[0050] In one embodiment of the invention, shown by Figure(s) 3A and 3B, the solar cell with one or more subcells forming the epitaxial region, has an annular cap region 21 formed on top of the epitaxial region 45. A metal region 63 on top of the annular cap 21 makes ohmic contact with the annular cap. The metal region 63 on top of the annular cap is also referred to as "the through substrate via head". FIG. 3B shows a top plan view of the solar cell of FIG. 3A.

[0051] In certain embodiments, the center-to-center distance between adjacent through-substrate vias is from about 100 μm to about 200 μm, from about 100 μm to about 150 μm, from about 150 μm to about 200 μm, and in certain embodiments, from about 125 μm to about 175 μm. In some embodiments, the center-to-center distance between adjacent through-substrate vias is approximately 60 μm and up to 1 mm or larger. The vias may be arranged in an appropriate configuration to optimize the performance of the solar cell.

[0052] It is an objective of certain embodiments to reduce the number of vias in the solar cell, for a given cell size by placing them further apart from each other in order to reduce shadowing loss. The present embodiment keeps the emitter loss small enough by use of metallic wires extending out from the via regions, such that the lateral distance current flows through the lateral conduction layer is not substantially increased. Since the metallic wires can be made much shorter compared to typical prior art gridlines, the resistive losses associated with them will be minimal. The metallic wires can follow a variety of patterns depending on the multi-junction solar cell design requirements. Since the metallic wires are typically short, it may not be necessary to use silver or other high conductive metals to make the metallic wires. Hence the present embodiment enables multi-junction solar cells without

silver metallization. Metallization that does not use silver may be advantageous for production and manufacturing. For example, silver is typically not allowed on production equipment sets that are used for making other products that do not contain silver. Therefore, the cost effective elimination of silver from the device may enable benefits for manufacturing the multi-junction solar cell device.

**[0053]** In some embodiments, as shown in Figures 4A and 4B, narrow metal gridlines 82 on the front side of a solar cell may be provided extending from the through substrate via head region along narrow cap regions 81 on top of the epitaxial regions 45. A through-substrate via 60 extends from the annular cap 21 to the backside of the substrate 5. A via metal 62 within the through-substrate via 60 extends from the annular cap to the backside of the substrate 5 in the inner region of the through substrate via. In some embodiments, this via metal may include gold or copper. In some embodiments a via metal does not fill the entire via. FIG. 4B is a planar view of the upper surface of the device shown in FIG. 4A, and includes narrow metal gridlines 82 overlying the narrow cap regions 81 disposed over through via 60 and epitaxial region 45.

**[0054]** An electrically insulating layer 61 lines the walls of the through substrate via around the conductive metal, thereby electrically insulating the substrate 5 and the epitaxial region 45 from the via metal 62 inside the through substrate vias. In some embodiments, this insulating layer may be a dielectric such as silicon dioxide or silicon nitride. In other embodiments, the insulating layer may be a polymer. The insulating layer 61 is patterned inside the via so that the via metal 62 makes ohmic contact with the through-substrate via head 21. In some embodiments, an insulating layer such as a polymeric material is patterned inside the via by a self-patterning process using selective deposition. In some embodiments, as shown in Figure 5A, the insulating layer 61 conformally covers a portion 64 of the backside of the substrate in addition to the inside of the vias, such that the insulating layer on the backside of the substrate is patterned in a back contact pattern, resulting in a patterned insulating layer on the backside. In other embodiments, the patterned insulating layer on the backside may be applied and patterned separately from the insulating layer inside the vias. Back metal 54, which may include back contact pads, may be applied on the backside of the substrate outside of the areas occupied by the patterned insulating layer 64 on the backside of the substrate such that the back metal makes ohmic contact with the substrate. In some embodiments, as shown in Figures 5A and 5B, there is a space or gap 55 between patterned

insulating layer 64 and back side metal contact 54. In some embodiments the back metal may include gold, titanium, and platinum.

**[0055]** Referring to Figures 5A-5B, via contact metal regions 65, which may include via contact pads may be attached to the patterned insulating layer on the backside of the substrate such that the via contact metal regions are in direct electrical contact with the via metal 62 but not electrically connected directly to the semiconductor substrate 5 or to the back metal 54. In some embodiments, metal regions 65 may include gold, titanium, platinum, and copper.

**[0056]** In some embodiments, as shown in Figure 5C, the patterned insulating layer 64 on the backside and the via contact metal regions 65 are patterned such that multiple via metals are electrically connected. In some embodiments, the via contact metal regions 62 and the back metal are patterned in a complementary pattern, henceforth referred to as an inter-digitating back contact pattern.

**[0057]** In some embodiments, a device contains no silver metal; that is, the narrow gridlines along the cap, the via head metal, the via metal, the via contact metal region, and the back metal do not contain silver.

**[0058]** In some embodiments, the cap regions and the vias can have other shape factors such as rectangles, squares, or other shapes not limited to the annular shape. Such shapes may include cap regions which form a closed circular, rectangular or other shape around the entire perimeter of the via hole. Or, such cap regions may not surround the entire perimeter of the via hole.

**[0059]** In another embodiment, the through substrate via head structures are covered with an optically transparent material with smooth edges.

**[0060]** In other embodiments, the through substrate via head forms a planar metal region.

**[0061]** In other embodiments, the via metal directly connects to the cap region such that through substrate via head and the via metal are formed in a single process step.

**[0062]** Referring to Figures 6A and 6B, in some embodiments, an optical cover material 91 is bonded permanently to the top side of a solar cell using a planarizing optical glue 92, such that no electrical connection is available from the top surface of the solar cell. In some embodiments, this optical cover material 91 is a space-grade coverglass, which may be made of a variety of space-grade materials, including but not limited to, borosilicate glass. In some embodiments, the optical cover glass may incorporate dome shapes and be made of a polymer material. In some embodiments, this optical cover material is bonded permanently

at the wafer-scale prior to substrate thinning, a process well known to those skilled in the art, and used also as a carrier substrate during substrate thinning and subsequent process steps.

**[0063]** In some embodiments, for example in Figure 6B, a carrier substrate is bonded temporarily at the wafer-scale prior to substrate thinning, a process well known to those skilled in the art, and used to provide mechanical support during subsequent process steps. This temporary carrier is removed from the final multi-junction device and serves as a mechanical support for the epitaxial layers during processing. In some embodiments, the carrier substrate may be a cover glass or other material.

**[0064]** In the embodiments comprising an optical cover material, which may be space-grade coverglass, as illustrated in FIGS. 7A-7F, the following process modules may be used for cost-effective process integration.

1. (Figure 7A) Front side processing is done using semiconductor processing techniques to form annular cap regions and the through substrate via heads on the front side of the solar cells. The cap region may be patterned in a disk shape at this process step. Through substrate via heads may be smoothly applied on top of the disk-shaped cap regions. The narrow metal gridlines may also be formed during front side processing. In some embodiments, anti-reflection coating may be applied at this process step. At the end of this process module a wafer with front side processing is obtained.

2. (Figure 7B) The wafer with front side processing is bonded permanently to an optical cover material using a planarizing glue. In some embodiments, the optical cover material may be space grade coverglass which may be made of borosilicate glass.

3. The substrate is thinned after being bonded to the optical cover material. The thickness range of the substrate after substrate thinning can range between 0 μm and 200 μm of substrate

4. (Figure 7C) The backside of the substrate is patterned with photoresist or applicable masking material in through-wafer-via pattern. The through-substrate vias are etched from the backside of the substrate such that the etch stops on the through substrate via heads, which act as a selective etch stop layer. As a result of the via etch, annular cap regions are formed in place of the disk-shaped cap regions. The patterned photoresist is removed after the patterning is done.

5. (Figure 7D) An insulating liner is applied. The insulating layer can be applied using standard deposition techniques, including but not limited to, plasma-enhanced chemical vapor deposition, atomic layer deposition, and electrografting.

6. Using standard photolithography techniques, the insulating liner is patterned so that the through-substrate via heads are exposed. The patterned insulating layer on the backside may also be formed at this step.

7. (Figure 7E) Via metal is applied inside the vias such that it makes electrical connection to the through-substrate via heads.

8. (Figure 7F) Via contact metal regions and back metal are applied. In some embodiments, these two metals can be applied in a single deposition step.

**[0065]** FIGS 7A-7F include the following elements: substrate 701, epitaxial layer 702, dielectric material 703, annular cap 704, through-substrate via head 705, planarizing adhesive 706, optical cover material 707, via 708, insulating liner 709, via metal 710, and back metal 711.

**[0066]** The process flow described herein is merely an example and other process flows with different steps can be used to achieve optical-cover material integrated wafer-level processing to realize through-substrate via solar cells. Using such an integrated process flow eliminates several steps and provides substantial cost savings.

**[0067]** In another embodiment of the above-described device, as shown in Figures 8A-8F, during front side processing step, the cap is patterned in an annular shape and a dielectric material is deposited inside the annular cap region. In some embodiments the dielectric inside the annular cap region may be antireflection coating. The through-substrate via head is applied such that it makes contact with the top side of the annular cap ring and the top side of the dielectric material inside the annular cap region. At the via etching step (Figure 8C), the etching stops at the dielectric inside the annular cap instead of the through substrate via head, wherein the dielectric material acts as an etch stop layer during etching of the through substrate vias. In an embodiment, at the insulating liner application step (Figure 8D), a selective deposition technology can be used such that insulating liner, which may be a polymer, deposits only on conductive and semiconductive surfaces and does not deposit on insulating surfaces, including but not limited to dielectrics (e.g., antireflection coatings) and polymers (e.g. photoresist). Using such a selective deposition technology the insulating liner covers the via sidewalls and the backside of the substrate, but not on the dielectric inside the annular cap region. In some embodiments, as shown in Fig. 8E, a photoresist pattern may be used on the backside of the substrate, preventing deposition of the selectively-deposited insulating liner on parts of the backside protected by the photoresist. The photoresist is removed after the deposition of the liner is completed. In some embodiments, electrografting

technique can be used to deposit the insulating liner selectively or non-selectively. Subsequently dielectric inside the cap region is removed prior to via metal deposition, which may include in some embodiments selective wet etching of the dielectric (e.g. antireflection coating) that does not etch the insulating polymer on the via sidewalls. The selective deposition technology may allow for achieving small via diameters and may eliminate additional photolithography steps during the process.

**[0068]** FIGS 8A-8F include the following elements: substrate 801, epitaxial layer 802, dielectric material 803, part of the dielectric material inside the via 813, annular cap 804, through-substrate via head 805, planarizing adhesive 806, optical cover material 807, via 808, insulating liner 809, via metal 810, and patterned photoresist 812.

**[0069]** In another embodiment of the above-described device, as shown in Figures 9A-9F, through substrate via head may be formed by a process flow integrating via metal deposition and through substrate via head deposition. In this process flow a photoresist region is deposited on the disk-shaped cap region (Figure 9A). This photoresist region is used as an etch stop layer when the through substrate vias are etched from the backside of the substrate (Figure 9C). Subsequently insulating liner is applied and patterned (Figure 9D). The selective deposition technology may also be used since photoresist is an insulator. Subsequently the photoresist region may be removed using standard semiconductor processing steps and the annular cap region is thus exposed (Figure 9E). Finally, a via metal and through-substrate via head may be deposited in a single deposition step such that the through substrate via head makes ohmic contact with the annular cap region (Figure 9F).

**[0070]** FIGS 9A-9F include the following elements: substrate 901, epitaxial layer 902, dielectric material 903, annular cap 904, photoresist 913, planarizing adhesive 906, optical cover material 907, via 908, insulating liner 909, and via metal 910.

**[0071]** Finally, it should be noted that there are alternative ways of implementing the embodiments disclosed herein. Accordingly, the present embodiments are to be considered as illustrative and not restrictive. Furthermore, the claims are not to be limited to the details given herein, and are entitled their full scope and equivalents thereof.

## CLAIMS

What is claimed is:

1. A multi-junction solar cell device comprising:

an electrically conductive semiconductor substrate with at least one multi-junction solar cell element formed in an epitaxial region grown thereon;

a plurality of cap regions formed on top of the epitaxial region;

a plurality of through-substrate via heads corresponding to each of the plurality of cap regions formed on a back surface of the substrate;

through-substrate vias that extend through the substrate from each of the plurality of cap regions to the corresponding through-substrate vias heads;

conductive metal within the through-substrate vias and electrically connecting each of the plurality of cap regions to the corresponding through-substrate via heads;

an electrically insulating liner disposed on the walls of each of the through-substrate vias insulating the substrate and the epitaxial region from the conductive metal inside the through-substrate vias;

an optical cover material disposed upon an optically transparent adhesive material directly above each of the plurality of through- substrate via heads; and

a back metal, patterned with a back metal pattern, in ohmic contact with the back surface of the electrically conductive semiconductor substrate, and electrically isolated from the through-substrate via heads.

2. The multi-junction solar cell device of claim 1, comprising:

a patterned insulating layer on the back surface of the substrate; and

metal regions comprising contact pads on the patterned insulating layer such that the metal regions are in direct electrical contact to the conductive metal inside the through-substrate vias and not electrically connected directly to the semiconductor substrate or to the back metal.

3. The multi-junction solar cell device of claim 2, wherein the contact pads are patterned to form a patterned back contact such that multiple contact pads are electrically interconnected.

4. The multi-junction solar cell device of claim 3, wherein the patterned back contact and the back metal are patterned in an interdigitated back contact pattern.

5. The multi-junction solar cell device of claim 1, comprising metal gridlines along cap regions that extend from exposed metal of the through-via region on the top side of the device.

6. The multi-junction solar cell device of claim 1, wherein materials forming the device do not contain silver metal.

7. The multi-junction solar cell device of claim 1, wherein the through-substrate via head comprises a planar metal region disposed upon a cap region defined during front-end processing such that the via metal is electrically connected to the cap region through the planar metal region.

8. The multi-junction solar cell device of claim 1, wherein the through-substrate via head comprises:

a metal region deposited on the cap region; and

a dielectric material encircled by the cap region; wherein the dielectric material acts as an etch stop layer during etching of through-substrate vias and is removed prior to via metal deposition.

9. A method of forming a through-substrate via head comprising:

providing a substrate having an epitaxial region grown thereon and a plurality of cap regions formed on top of the epitaxial region;

depositing a photoresist region on the plurality of cap regions;

etching a plurality of through-substrate vias from a backside of the substrate and using the photoresist region as an etch stop layer;

depositing an electrically insulating liner within each of the plurality of through-substrate vias;

removing the photoresist region to expose the plurality of cap regions; and

depositing metal within the through-substrate vias to connect the plurality of cap regions.

10. The method of claim 9, wherein the optical cover material is bonded to the top surface prior to a substrate thinning step.

11. A multi-junction solar cell device comprising:

a semi-insulating semiconductor substrate having a back surface;

an epitaxial region overlying the semi-insulating semiconductor substrate;

an electrically conductive semiconductor region between the substrate and the epitaxial region;

at least one multi-junction solar cell element formed in the epitaxial region, the epitaxial region being grown on the electrically conductive semiconductor region;

a cap region overlying the epitaxial region;

though-wafer vias that extend from the cap region to the back surface of the substrate;

the cap region being shaped according to a cap pattern including collars around the through-wafer vias;

conductive metal within the through-wafer vias and electrically connected to the cap patterned collars;

an electrically insulating liner on the walls of the through-wafer vias insulating the conductive metal inside the through-wafer vias from at least the epitaxial region and from the conductive semiconductor region;

an optical cover material disposed upon an optically transparent adhesive material directly above the through-substrate via heads formed on top of the epitaxial region; and

a back metal on the back surface of the substrate in electrical contact with the conductive metal in the through-wafer vias.

12. The multi-junction solar cell device of claim 11, comprising metal gridlines along cap regions that extend from exposed metal of the through-via region.

13. The multi-junction solar cell device of claim 11, wherein materials forming the device do not contain silver metal.

14. A multi-junction solar cell device comprising:

an electrically conductive semiconductor substrate with at least one multi-junction solar cell element formed in an epitaxial region grown thereon;

a plurality of cap regions formed on top of the epitaxial region;

through-substrate vias that extend from the plurality of cap regions to a back surface of the substrate;

conductive metal within the through-substrate vias and electrically connected to the plurality of cap regions;

an electrically insulating liner disposed on the walls of the through-substrate vias insulating the substrate and the epitaxial region from the conductive metal inside the through-wafer vias;

a through-substrate via head that electrically connects the conductive metal within the through-substrate vias with the plurality of cap regions, henceforth called;

a temporary carrier substrate bonded directly above the through substrate via heads formed on top of the epitaxial region; and

a back metal, patterned with a back metal pattern, in ohmic contact with the back surface of the electrically conductive semiconductor substrate, and electrically isolated from the conductive metal within the through-substrate vias.

15. The multi-junction solar cell device of claim 14, wherein the through-substrate via head comprises a planar metal region disposed upon a cap region defined during front-end processing such that the via metal is electrically connected to the cap region through the planar metal region.

16. The multi-junction solar cell device of claim 14, wherein the through-substrate via head comprises:

a metal region deposited on the cap region; and

a dielectric material encircled by the cap region; wherein the dielectric material acts as an etch stop layer during etching of through-substrate vias and is removed prior to via metal deposition.

17. A method of forming a multi-junction solar cell device, comprising:

providing an electrically conductive semiconductor substrate with at least one multi-junction solar cell element formed in an epitaxial region grown thereon, and a plurality of cap regions formed on top of the epitaxial region;

bonding a cover glass on top of the substrate and the plurality of cap regions;

thinning the substrate;

etching through-substrate vias from a back surface of the substrate;

forming a patterned dielectric layer on the back surface of the substrate; and

forming electrical connection between the patterned cap region and the back metal contacts pads with conductive metal inside the through-substrate vias, such that the contact pads are not directly electrically connected to the semiconductor substrate.

18. A method of forming a multi-junction solar cell device, comprising:

providing an electrically conductive semiconductor substrate with at least one multi-junction solar cell element formed in an epitaxial region grown thereon, and a patterned cap region formed on top of the epitaxial region;

bonding a polymer cover on top of the substrate and the patterned cap region;

thinning the substrate;

etching through-substrate vias from a back surface of the substrate;

forming a patterned dielectric layer on the back surface of the substrate;

forming a plurality of back metal contact pads; and

forming electrical connection between the patterned cap region and the back metal contacts pads with conductive metal inside the through-substrate vias, such that the contact pads are not directly electrically connected to the semiconductor substrate.

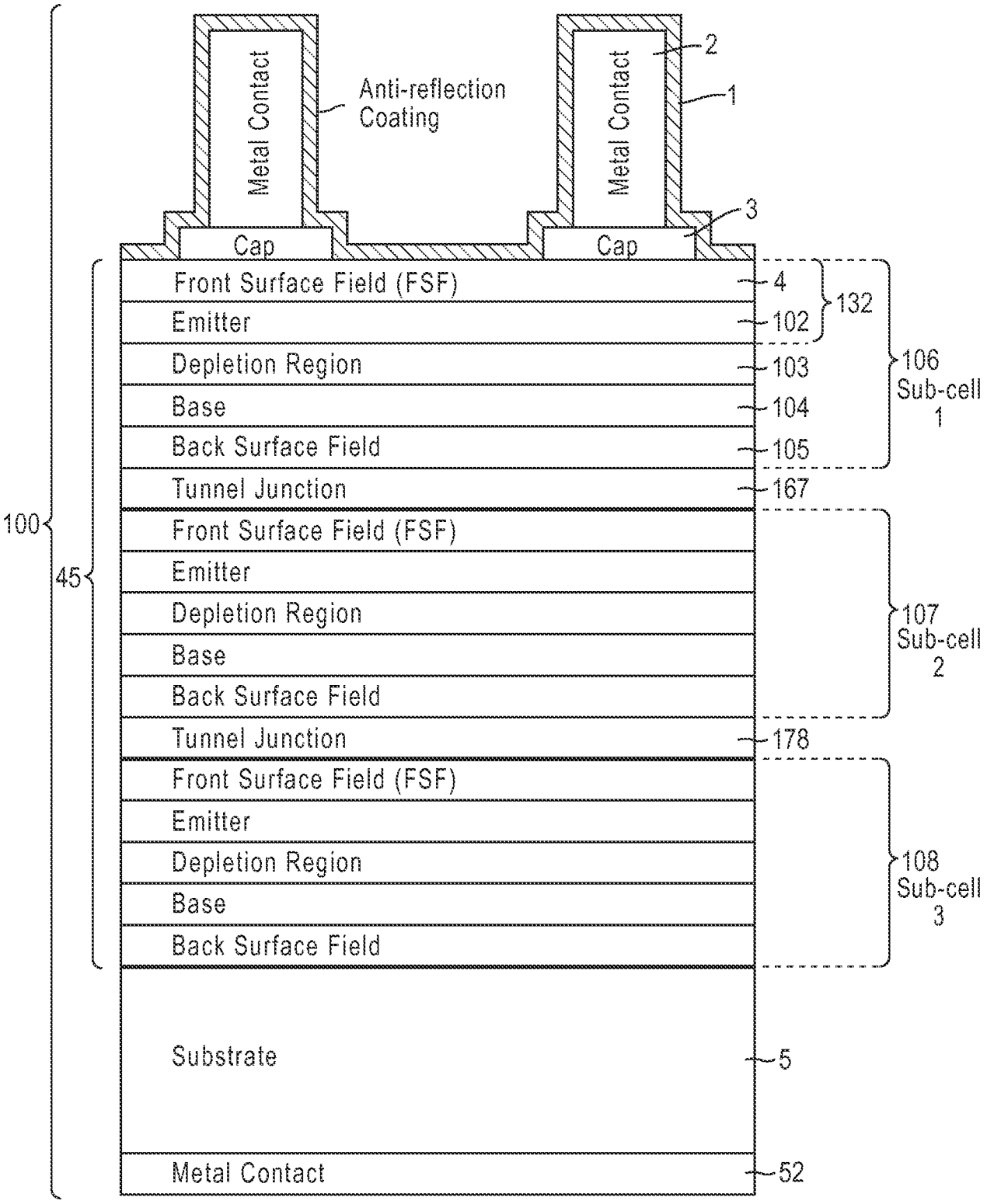



FIG. 1A
(Prior Art)

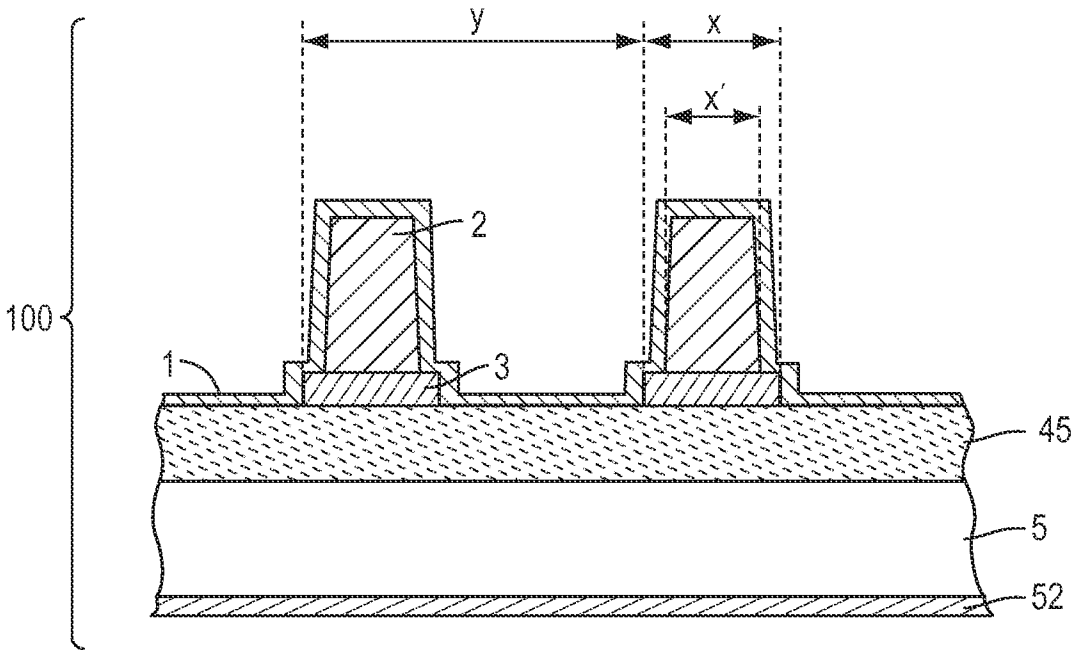



FIG. 1B
(Prior Art)

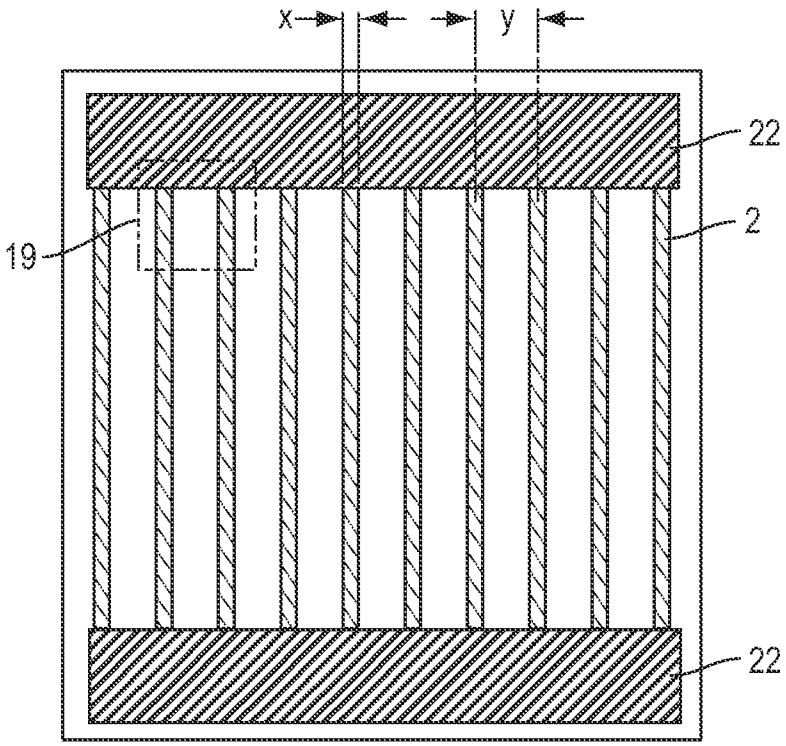



FIG. 2A
(Prior Art)

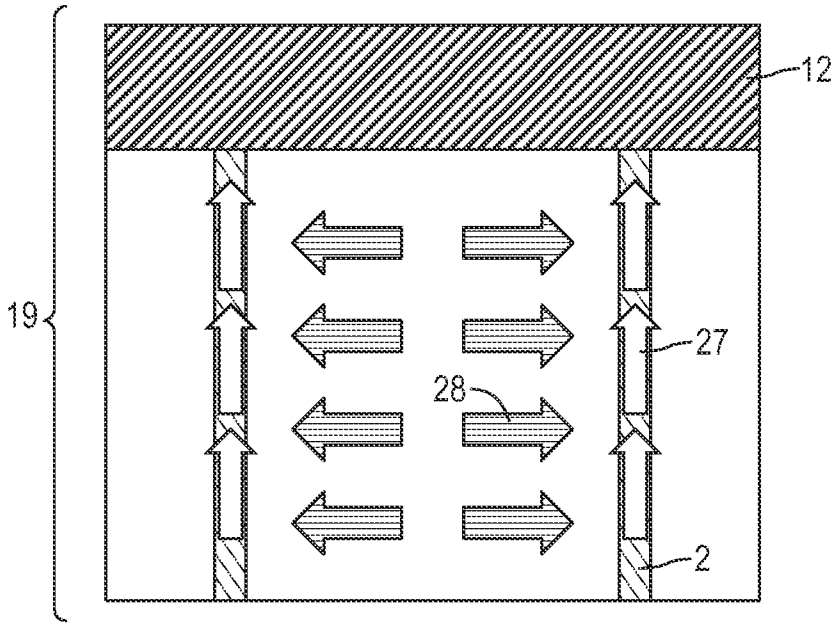



FIG. 2B
(Prior Art)

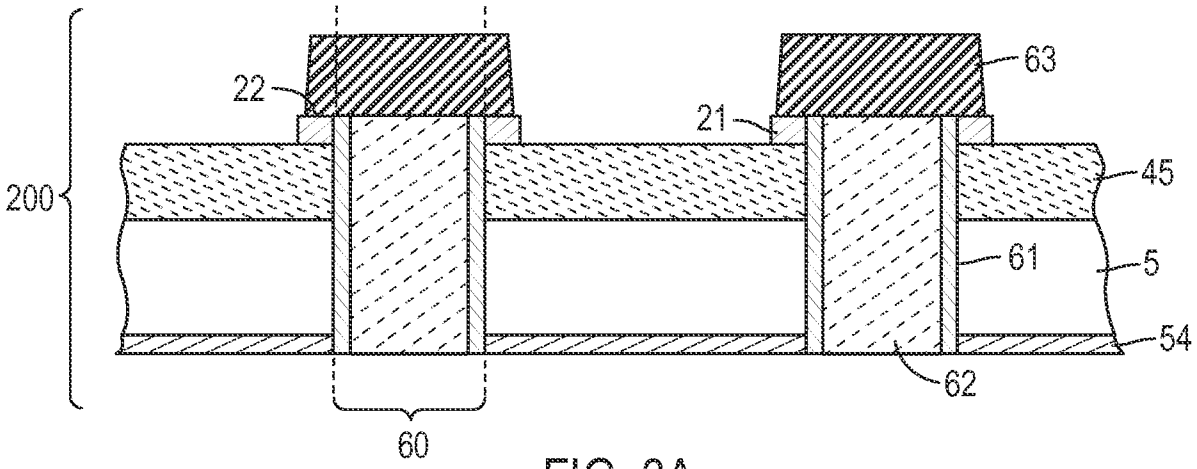



FIG. 3A

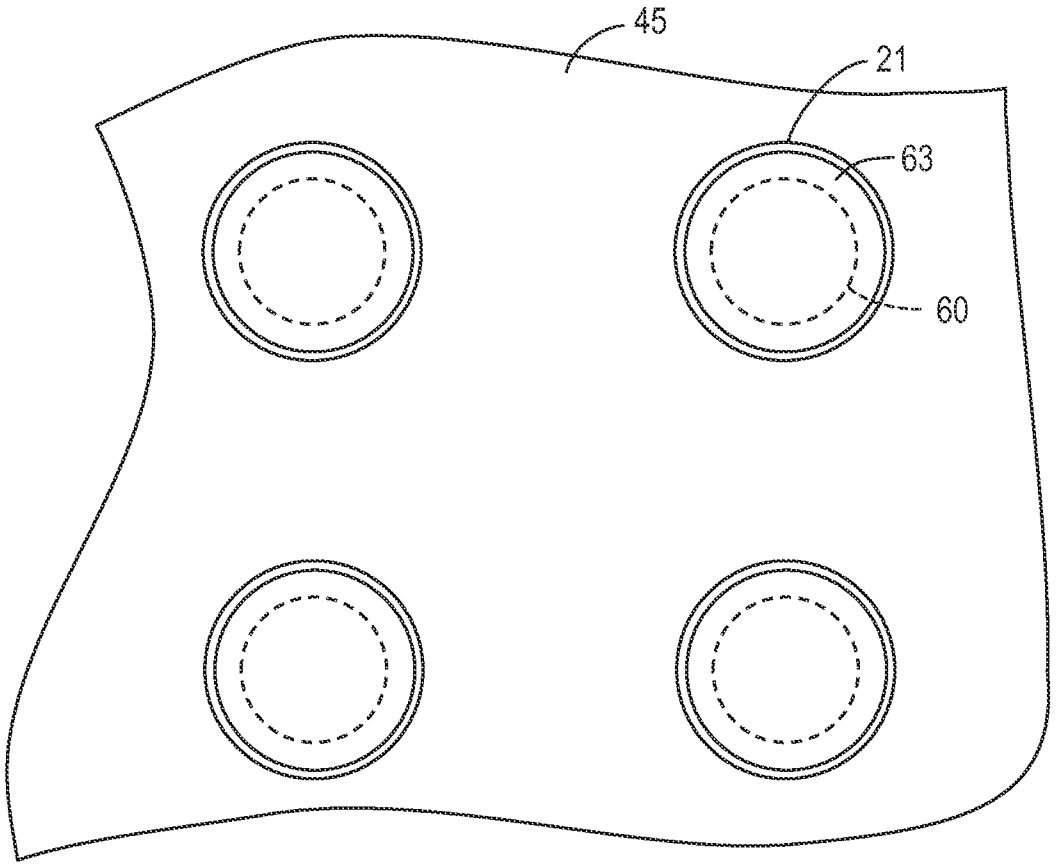



FIG. 3B

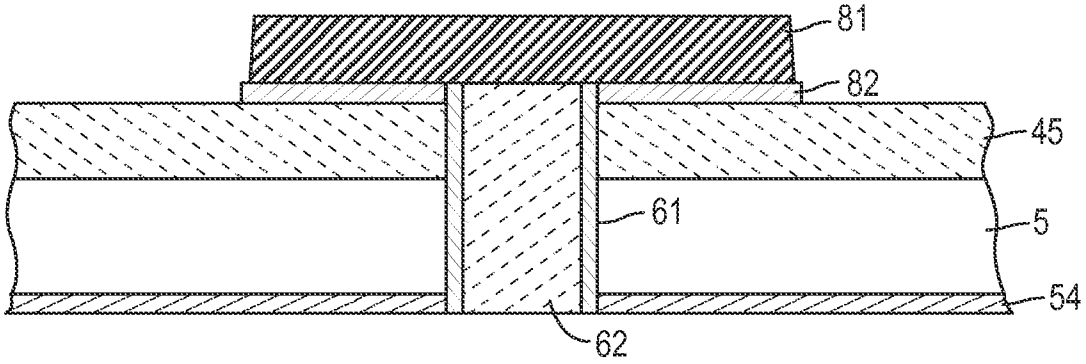



FIG. 4A

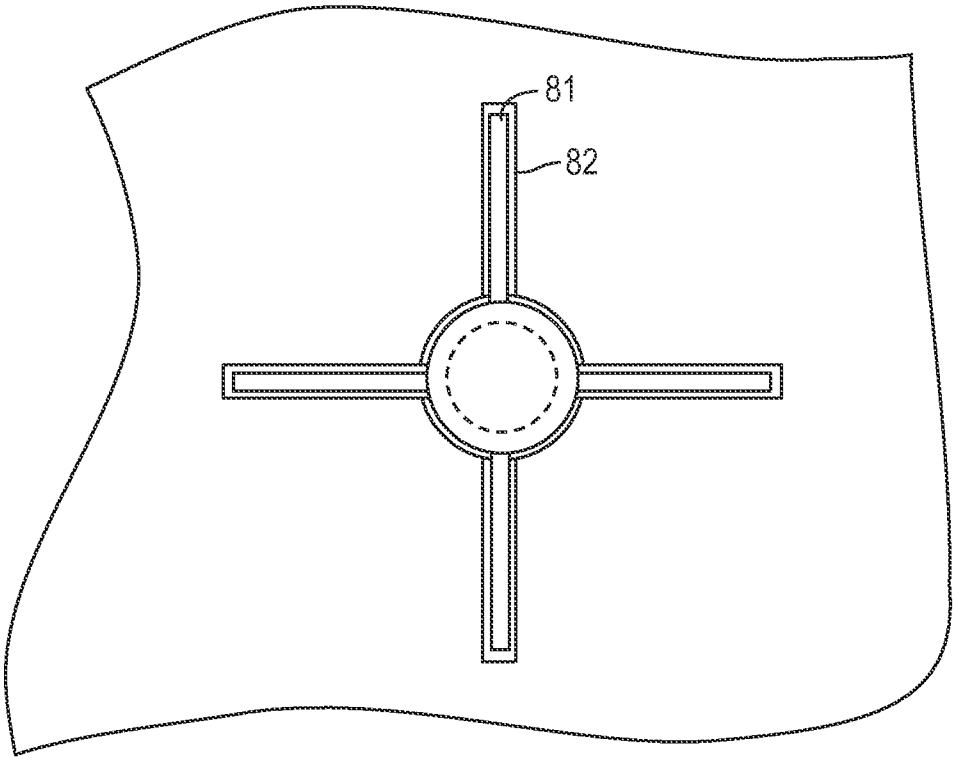



FIG. 4B

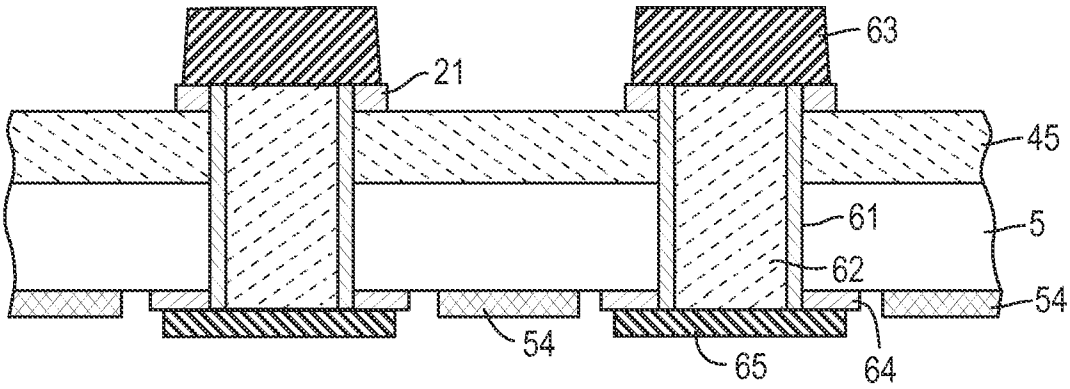



FIG. 5A

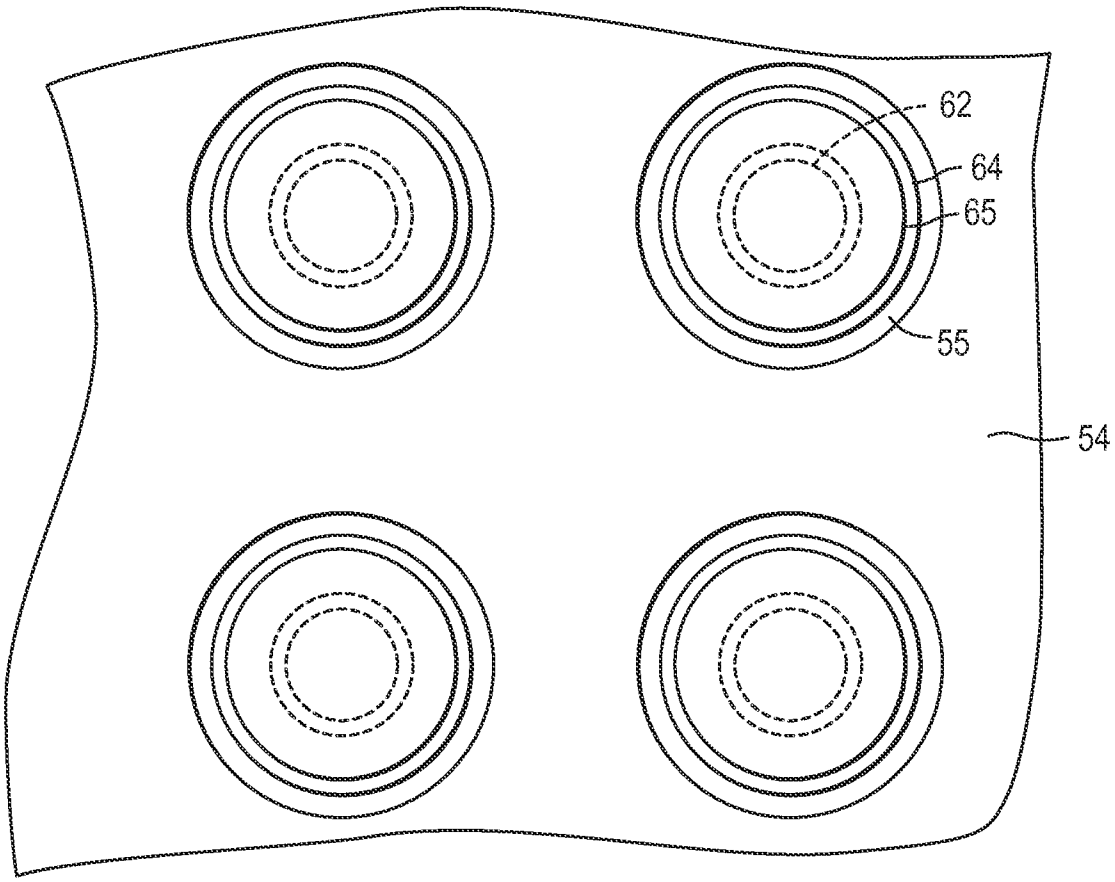



FIG. 5B

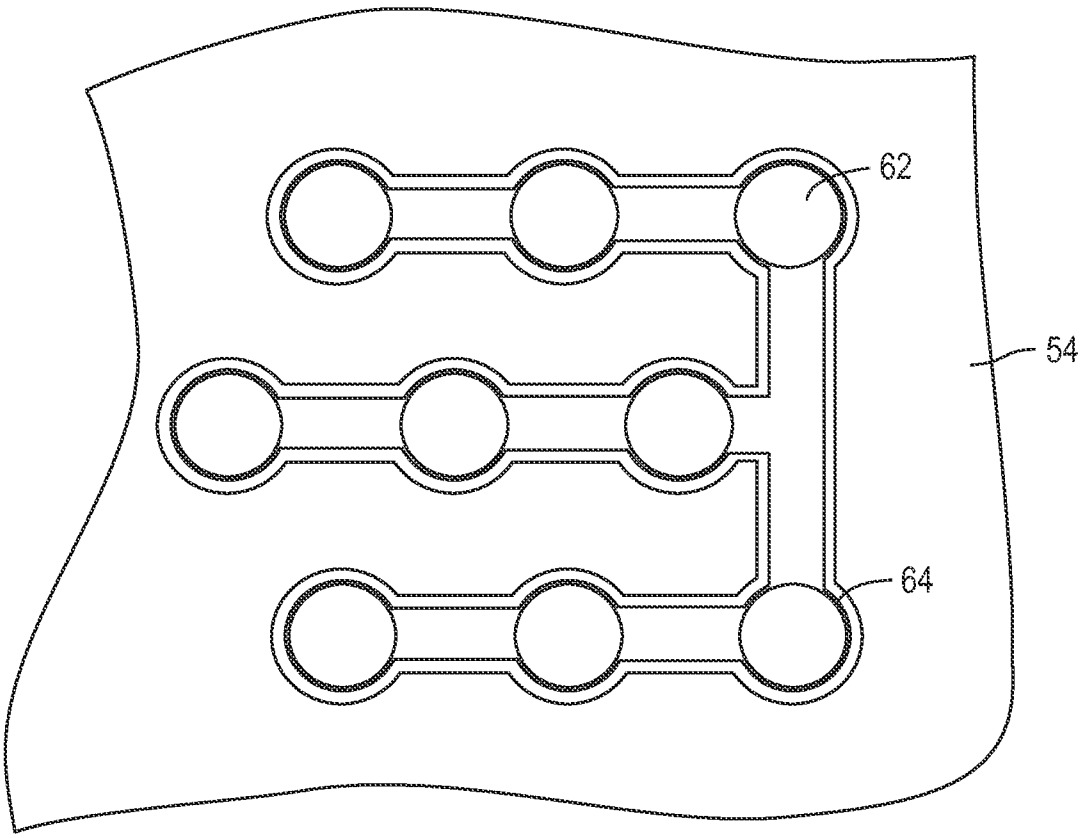



FIG. 5C

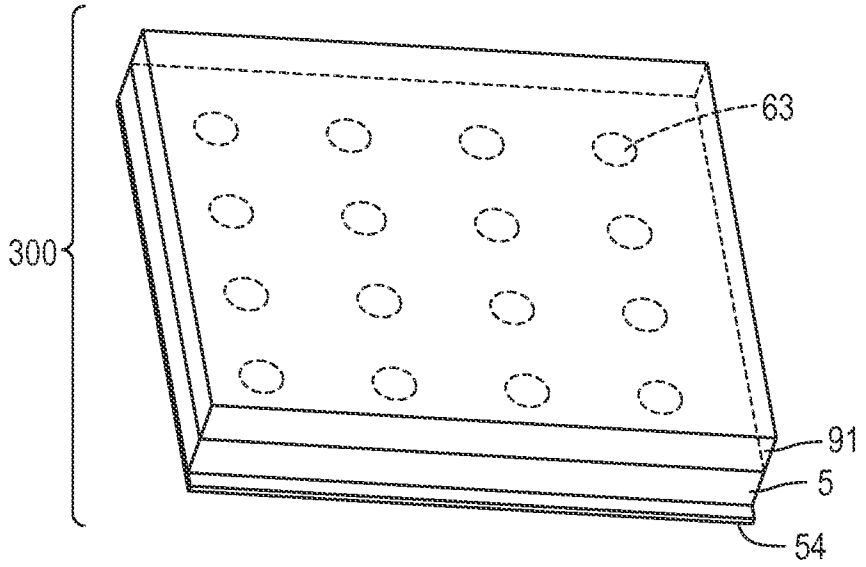



FIG. 6A

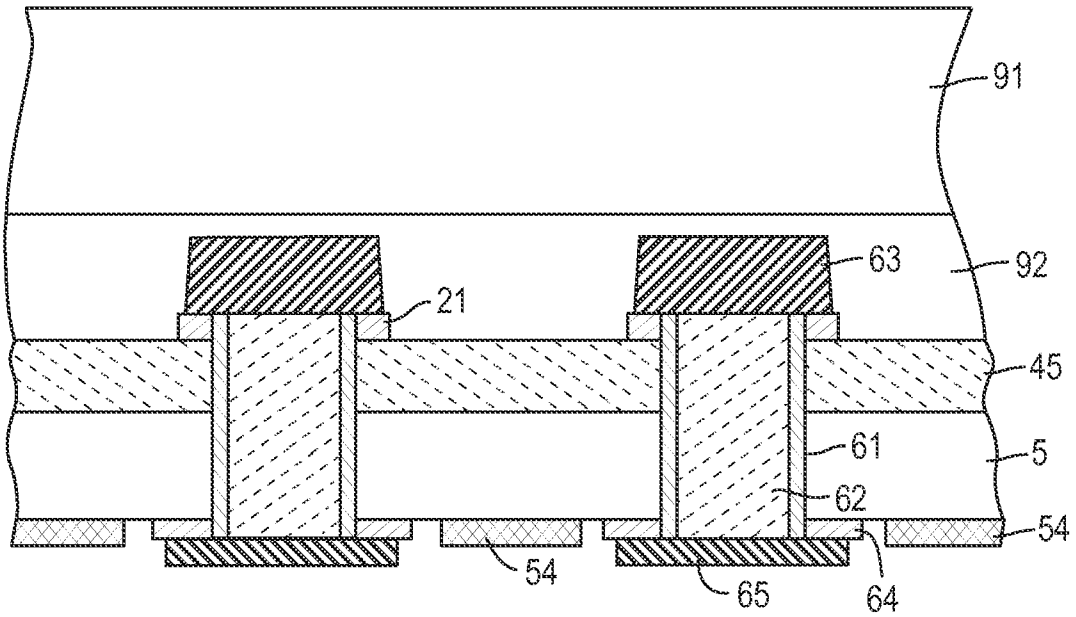



FIG. 6B

Front Side Processing

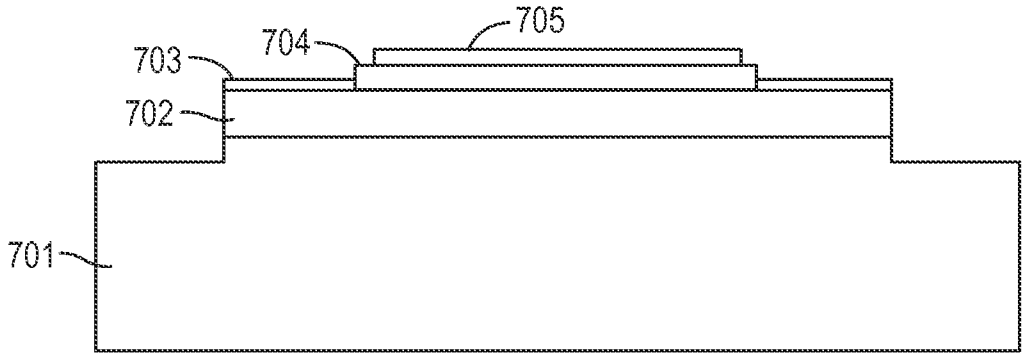



FIG. 7A

Optical Cover Material

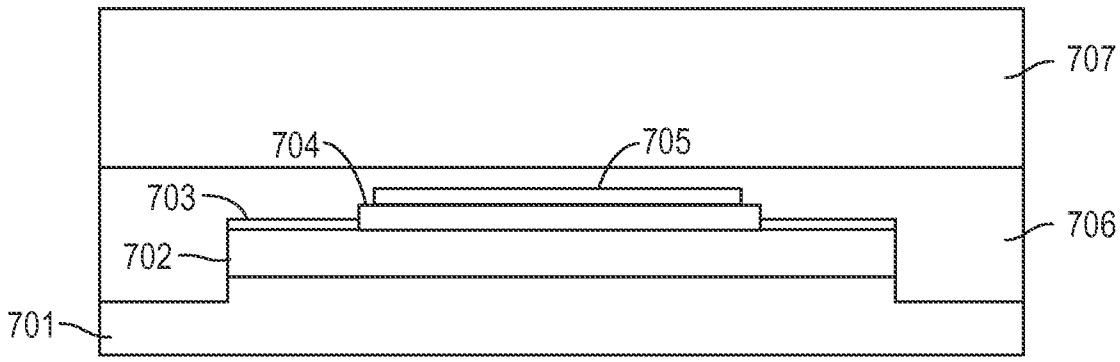



FIG. 7B

Via Opening

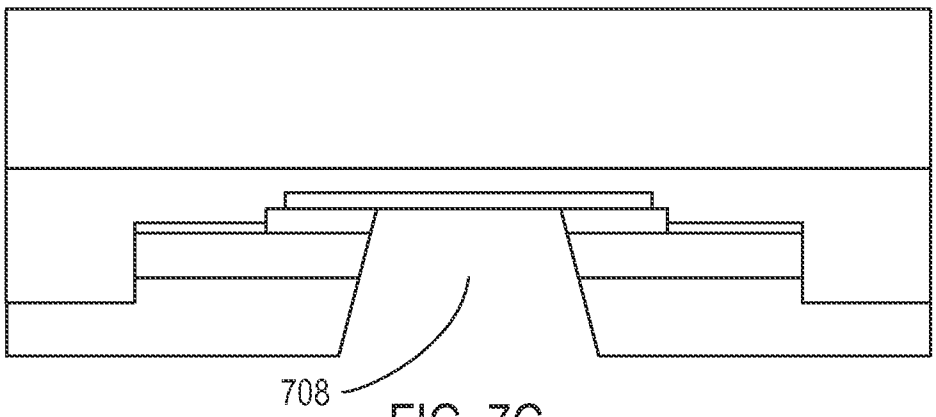



FIG. 7C

Insulating Liner

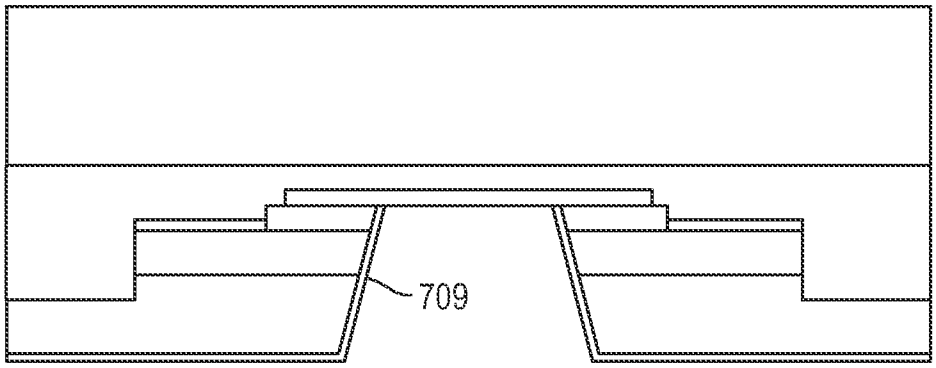



FIG. 7D

Via Metal

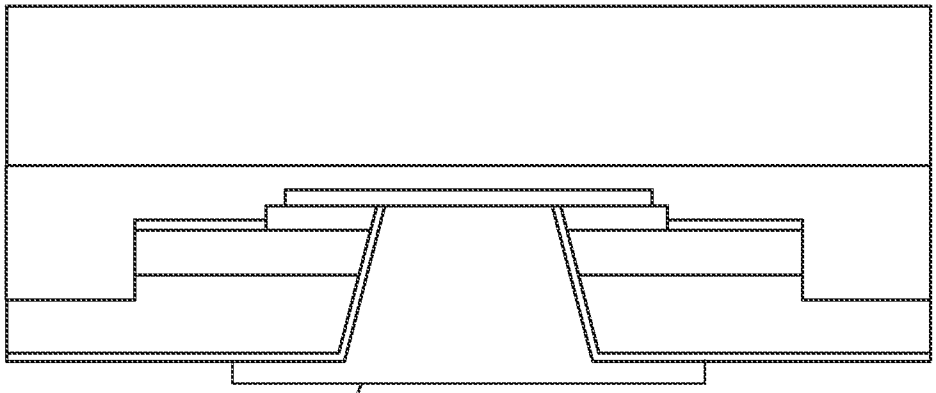



FIG. 7E

Via Contact Metal and Black Metal

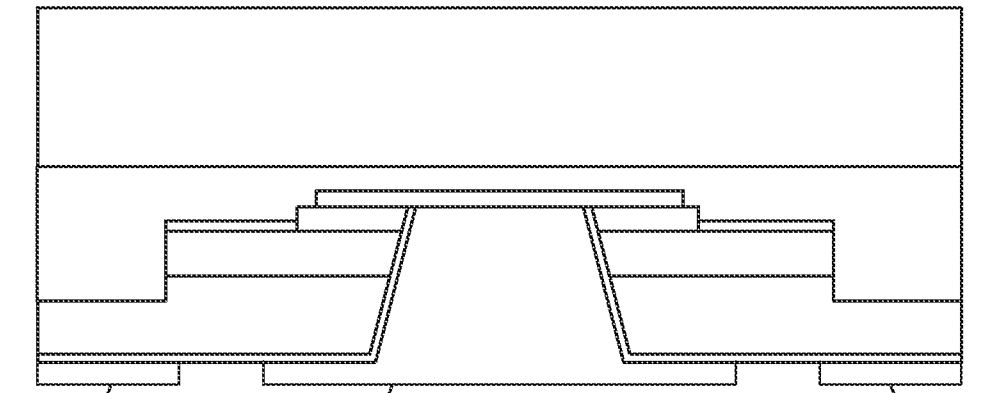



FIG. 7F

Front Side Processing

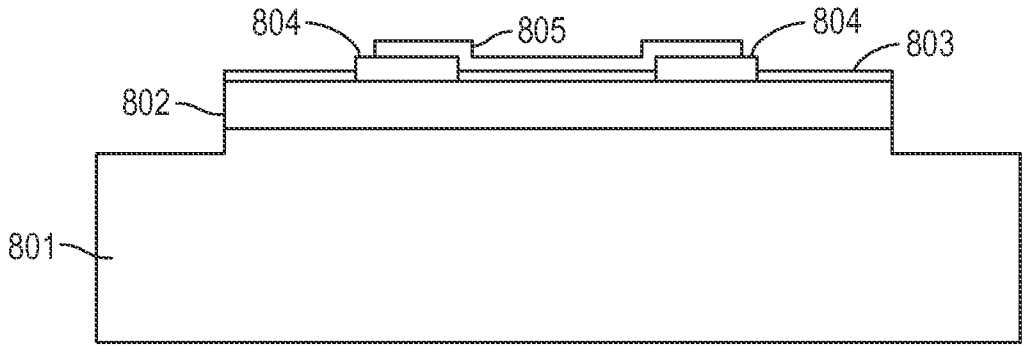



FIG. 8A

Optical Cover Material and Wafer Thinning

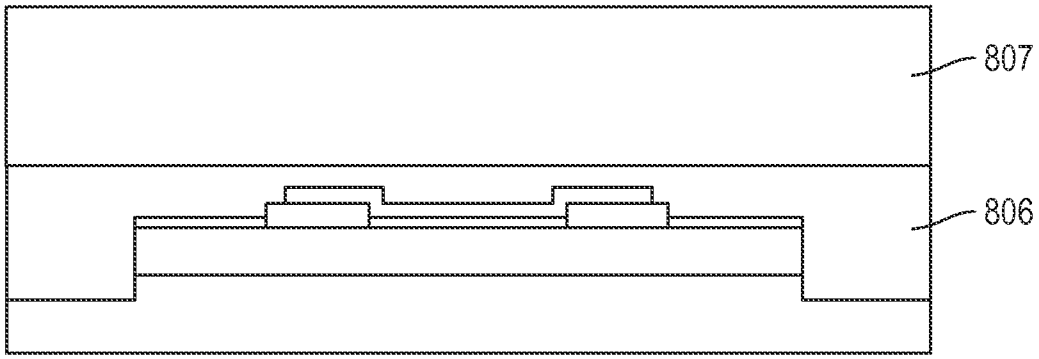



FIG. 8B

Via Etching

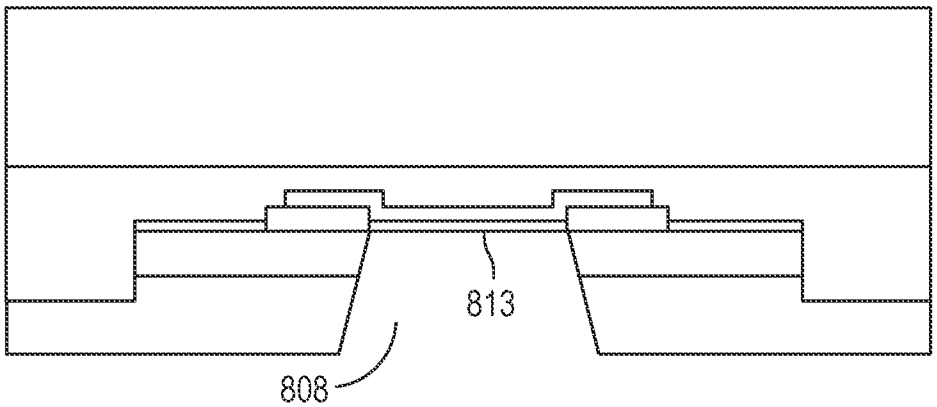



FIG. 8C

Insulating Liner (selective deposition)

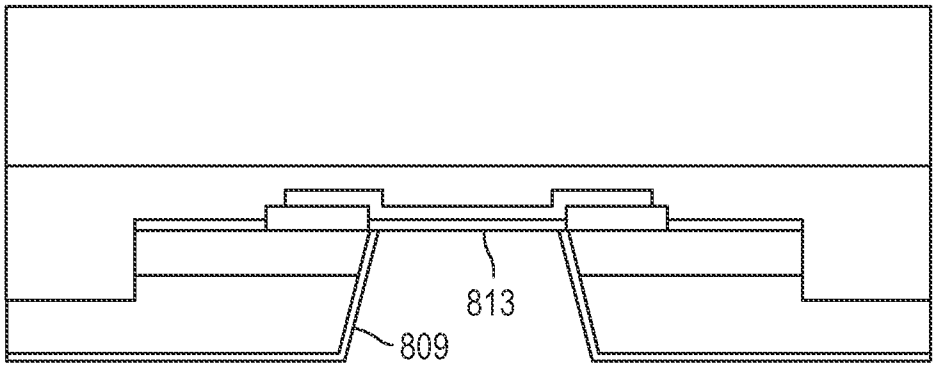



FIG. 8D

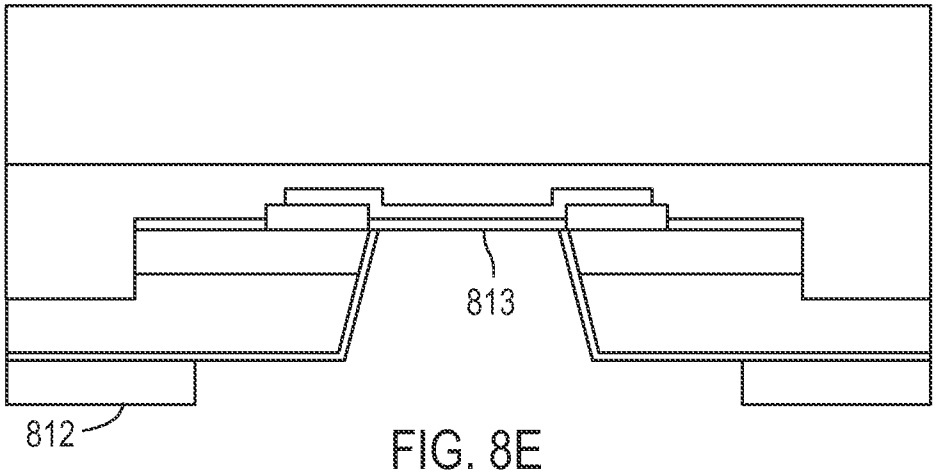



FIG. 8E

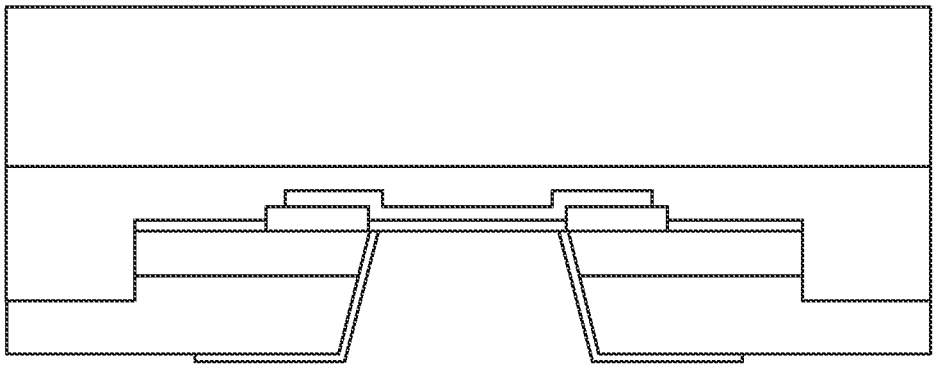


FIG. 8F

Front Side Processing

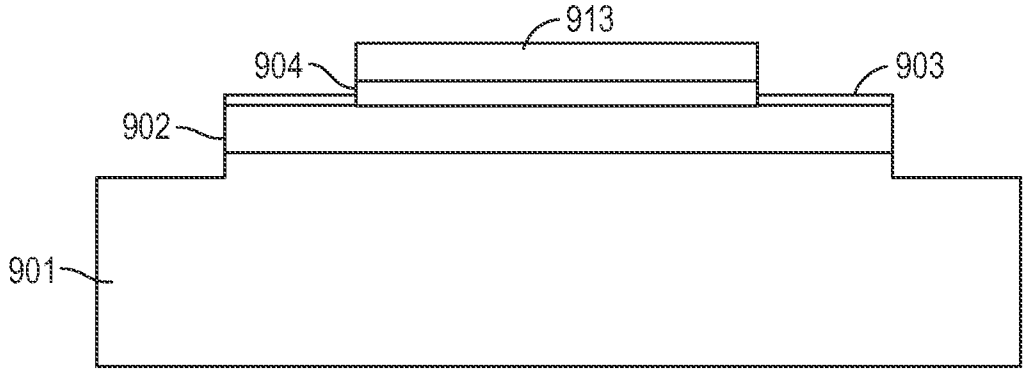



FIG. 9A

Optical Cover Material

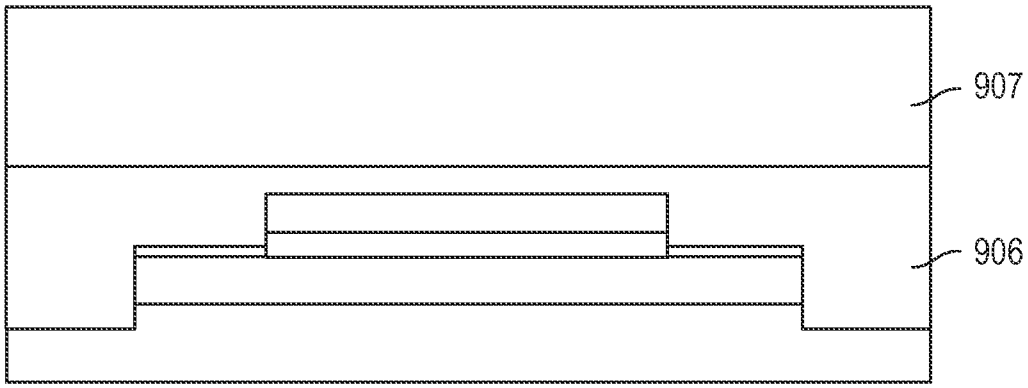



FIG. 9B

Via Opening

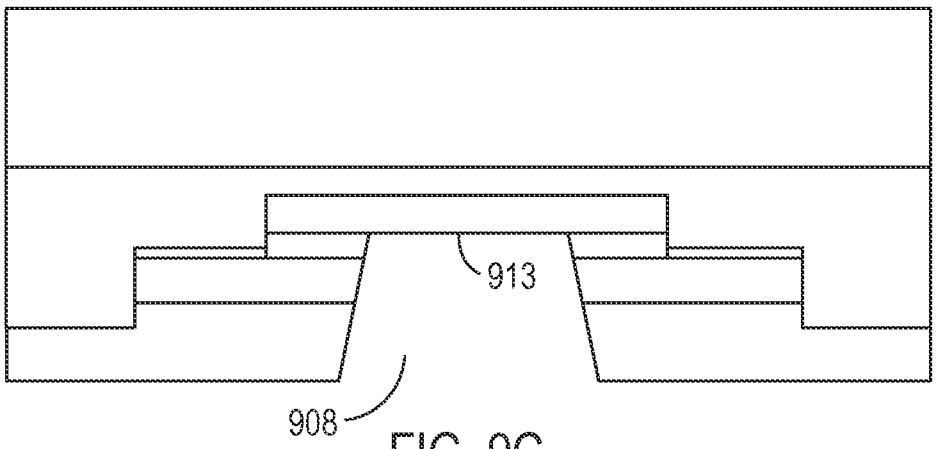



FIG. 9C

Insulating Liner (selective deposition)

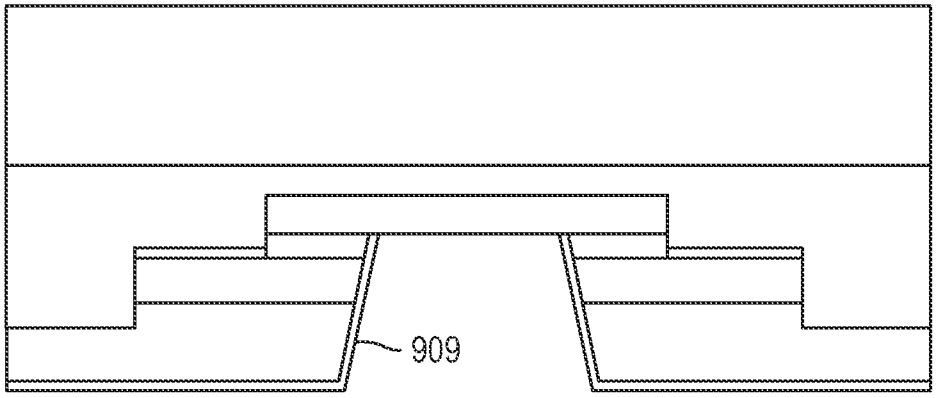



FIG. 9D

Removal of Photoresist exposes Annular Cap Region

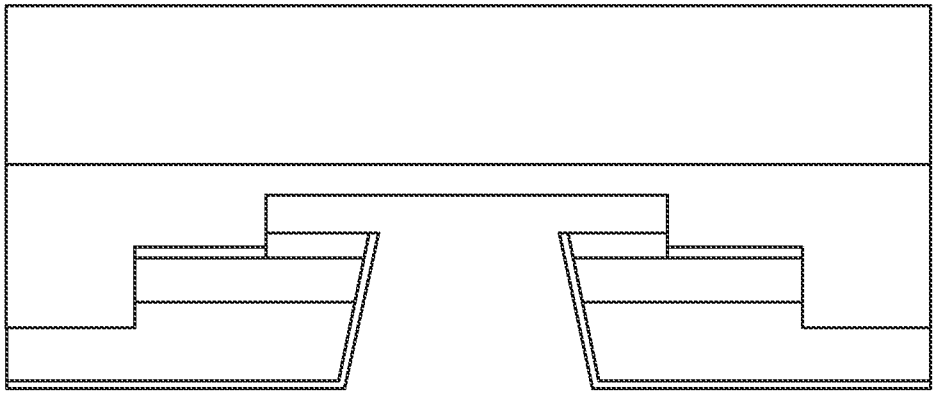


FIG. 9E

Via Metal and Through-substrate via head deposited in a single step

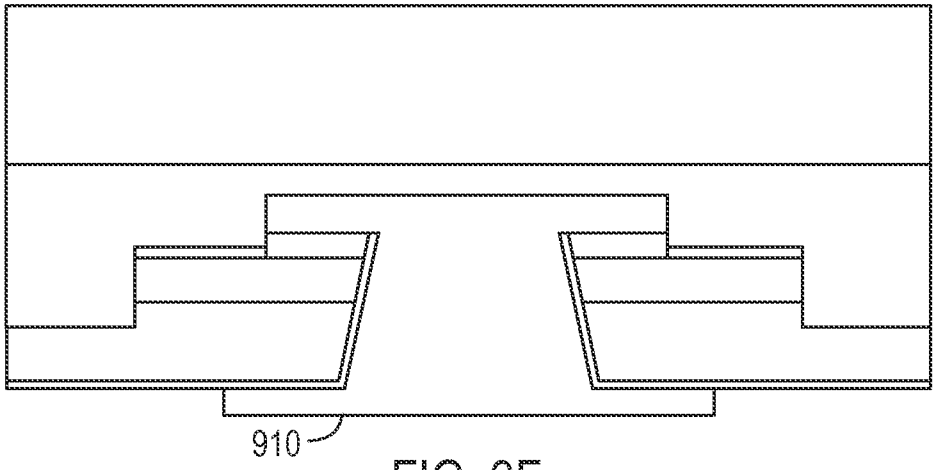



FIG. 9F

# INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/029494

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L31/0224 H01L31/0687 H01L31/0725 H01L31/18
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X<br><br><br>Y | US 8 115 097 B2 (GUHA SUPRATIK [US] ET AL)<br>14 February 2012 (2012-02-14)<br>cited in the application<br>abstract; figures<br>4A,4B,5B,6B,7B,9B,10B,11B,13B,14B,15B<br>column 2, line 66 - column 3, lines 7,<br>37-60<br>column 3, line 61 - column 4, line 7<br>column 5, lines 13-35<br>column 7, lines 9-15, 47-65<br>column 8, lines 29-64<br>column 9, line 9 - column 11, line 12<br>-----<br>-/-- | 1-9,<br>11-18<br><br>1,10,11,<br>14,17 |

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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| European Patent Office, P.B. 5818 Patentlaan 2<br>NL - 2280 HV Rijswijk<br>Tel. (+31-70) 340-2040,<br>Fax: (+31-70) 340-3016 | Cichos, Anna |

# INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/029494

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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| Y | US 2012/040487 A1 (ASTHANA ASHISH [US] ET AL) 16 February 2012 (2012-02-16) abstract; paragraphs [0008], [0035], [0041], [0042] - [0043], [0045]; figures ,4-5, 12 | 1,10,11, 14,17,18 |

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Information on patent family members

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