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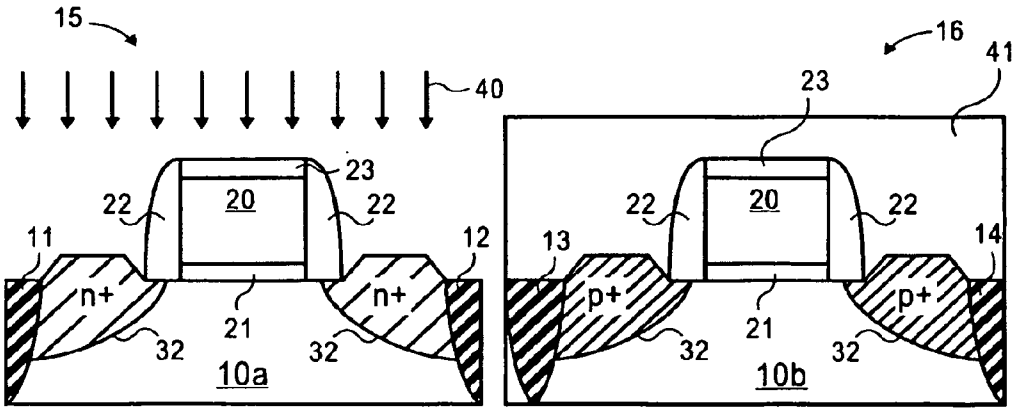
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(54) Title: EPITAXIAL SILICON GERMANIUM FOR REDUCED CONTACT RESISTANCE IN FIELD-EFFECT TRANSISTORS



(57) Abstract: A method for selectively relieving channel stress for n-channel transistors with recessed, epitaxial SiGe source and drain regions is described. This increases the electron mobility for the n-channel transistors without affecting the strain in p-channel transistors. The SiGe provides lower resistance when a silicide is formed.

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EPITAXIAL SILICON GERMANIUM FOR REDUCED CONTACT RESISTANCE IN FIELD-EFFECT TRANSISTORS

FIELD OF THE INVENTION

[0001] The invention relates to the field of silicon germanium regions in field-effect transistors.

PRIOR ART AND RELATED ART

[0002] Frequently in semiconductor devices, a silicide metal is formed on semiconductor regions to reduce resistance. At the interface between the silicide and a semiconductor, such as silicon, a Shottkey barrier is a source of resistance. This can be reduced by lowering the bandgap, as occurs when silicon germanium (SiGe) is used as the material in which the silicide or salicide is formed. The use of SiGe source and drain regions and a nickel silicide metal is described in U.S. Patent 6,949,482. The bandgap diagrams and related text in this patent describe the advantages of using, particularly nickel silicide, on the SiGe. (See Figures 5, 6 and 7 and related text.)

[0003] It is recognized that improved performance in PMOS transistors is obtained when a uniaxial compressive strain is imparted directly to the channel region of the transistor from, for instance, embedded SiGe source and drain regions. Similarly, it is known that increased performance is obtained in NMOS transistors when uniaxial tensile strain is placed on its channel. This is described in "A Tensile Strained NMOS Transistor Using Group III-N Source/Drain Regions," application serial number 11/323,688, filed December 29, 2005, assigned to the assignee of the present application.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Figure 1 is a cross-sectional, elevation view of two sections of an upper portion of a silicon substrate in which isolation trenches are formed.

[0005] Figure 2 illustrates the structure of Figure 1, with gate structures and with recesses etched into the silicon, adjacent the gate structures.

[0006] Figure 3 illustrates the structure of Figure 2, after SiGe source and drain regions are grown in the recesses.

[0007] Figure 4 illustrates the structure of Figure 3, after masking a p-channel transistor and during an ion implantation of the n-channel transistor.

[0008] Figure 5 illustrates the structure of Figure 3, in alternate processing, where after a masking step, some of the material in the isolation trenches is etched.

[0009] Figure 6 illustrates the structure of Figure 5 after a silicide is formed on the source and drain regions.

[0010] Figure 7 illustrates another embodiment, where for the n-channel transistor, the SiGe is not recessed.

DETAILED DESCRIPTION

[0011] A method is described for fabricating p-channel and n-channel transistors where a silicon germanium (SiGe) source and drain regions are used and where a silicide is formed on these regions. In the following description, numerous specific details are set forth such as implantation energy levels, etc. in order to provide a thorough understanding of the present invention. It will be apparent to one skilled in the art, that the present invention may be practiced without these specific details. In other instances, well-known fabrication processes are not described in detail in order not to unnecessarily obscure the present invention.

[0012] In Figure 1, the upper portion of a monocrystalline silicon substrate is shown. Two separate sections of the substrate identified as 10a and 10b are illustrated. On section 10a, as will be described, an n-channel transistor is formed in the region 15. On the substrate section 10b, a p-channel transistor is fabricated in the region 16. The region 15 is bounded by the two isolation trenches 11 and 12. Similarly, the region 16 is bounded by the isolation trenches 13 and 14. The trenches 11-14 are shallow isolation trenches formed by etching the upper region of the substrate and filling the trenches with a dielectric. In some cases, after the trenches are etched, a silicon dioxide is grown to form a dielectric liner within the trenches. Then, the trenches can be filled with a material such as a deposited silicon dioxide.

[0013] In Figure 1, only half a trench is shown for each of the four trenches 11-14. In some of the embodiments described below, as will be discussed, material filling the trench is etched. In some cases the material is etched across the entire trench, and in other cases it is etched from less than the entire width of the trench. The trench widths as shown in the drawings are not-to-scale, for instance, relative to the gate structure. For convenience, the trenches are shown to be much narrower relative to the gate structure than they are in an integrated circuit.

[0014] Gate structures are formed on the regions 15 and 16 and like regions of the substrate. Each resultant gate structure, shown in Figure 2, includes a gate dielectric 21 separating a gate 20 from a channel region in the substrate, and a hard mask 23 over the gate 20. Sidewall spacers 22 are disposed on opposite sides of the gates 20. Processing steps such as the n-type and p-type dopant tip implants, and the formation of the sidewall spacers, are not described here. These steps are known in the prior art. Moreover, the specific gate structure shown is by way of example and not critical to the present invention.

[0015] After the gate structures are formed, recesses 30 are etched into the silicon substrate at the sites of the source and drain regions for both the n-channel and p-channel transistors. In Figure 2 the recesses 30 extend approximately from the gate structure to an isolation trench. Note the recesses 30 in each case extends slightly under the spacers, and are bounded by an isolation trench.

[0016] Now, epitaxial growth is used to grow SiGe source and drain regions for both the n-channel and p-channel transistors. The source and drain regions may be raised above the original level of the substrate, as illustrated. Note these regions are immediately adjacent to the isolation trenches.

[0017] The growing of the SiGe in the recesses causes compressively strained channel regions for both the n-channel and p-channel transistors. In the case of the p-channel transistor, this strain is beneficial in that it improves hole mobility in the transistor. Unfortunately, in the case of the n-channel transistor, the same strain degrades electron mobility. Both the n-channel and p-channel transistors, however, will benefit from the lower silicide barrier height associated with the SiGe, once the silicide or salicide is formed.

[0018] Figure 4 illustrates one process for relieving the strain on the channel region of the n-channel transistor while leaving the strain on the p-channel transistor. First, a masking member, which may be photoresist 41, is formed over the p-channel transistors, covering the source and drain regions of these transistors. Then, as shown in Figure 4, ions 40 are implanted into the SiGe source and drain regions of the n-channel transistor to create dislocation defects that act as relaxation sites within the SiGe. This reduces the strain on the channel region, and consequently, improves the electron mobility in the channel region. The ion bombardment may be relatively shallow since the channel region of the n-channel transistor is near the surface of the silicon (directly below the gate insulator), thus, there is no need to disrupt the crystal lattice deep within the recesses. The ions which are implanted are not

nominally charge carriers, and therefore do not affect the semiconductor properties of the source and drain regions. Carbon, for instance, may be used. Implantation energy levels of 0.5-1.5 Kev are adequate, with a dose of approximately 1E16-5E16 atoms/cm^2.

[0019] Following this implantation, a silicide is formed in an ordinary manner, such as with nickel. The disruption to the lattice of the n-channel source and drain regions, assists in the formation of the silicide, when compared to the source and drain regions of the p-channel transistor.

[0020] As shown in Figure 4, the entire isolation trench 13 is included under the mask, whereas only half the isolation trench 14 is under the mask 41. This is to demonstrate that the alignment of the mask with the isolation regions is not critical for this embodiment. What matters is that the SiGe source and drain regions of the p-channel transistor are protected from the implantation.

[0021] In an alternate embodiment, the stress in the n-channel transistors is relieved by removing some, or all, of the material in the isolation trenches. Referring to Figure 5, again, a masking member (member 50) is placed over the p-channel transistors. The trenches bounding the n-channel transistors, such as trenches 11 and 12 of Figure 5, are exposed, at least in part. Then, the material in the trenches, such as the silicon dioxide, is etched out of the trench with either an isotropic or anisotropic etching process. As shown by the openings 52 and 53 of Figure 5, not all the material in the bottom of the trench needs to be etched. Only the strain in the channel regions, which is near the surface, needs to be relieved.

[0022] Where an isolation trench separates an n-channel transistor from a p-channel transistor, etching the entire width of the trench, may cause the relieving of strain in both the p-channel and n-channel transistor. This would eliminate one of the benefits of using SiGe in the p-channel transistor, specifically the higher hole mobility created by the strained channel.

[0023] In this case, the masking member should prevent the entire trench from being etched. For instance, masking member 51 of Figure 5 protects a portion of the material in the trench 11. Similarly, masking member 50 protects part of trench 14. The masks 50 and 51 prevent all the material filling the trench 14 and 11, respectively, from being etched away particularly if an anisotropic etchant is used. Consequently, if a p-channel transistor is disposed on the side of the isolation region 11 opposite the n-channel transistor shown in Figure 5, the strain in its channel will not be relieved. Similarly, the opening 55 would relive the strain from an n-channel transistor disposed on the side of trench 14 opposite region 16. Where a p-channel transistor does not share a isolation trench with an n-channel transistor, or where for some reason the entire trench can be etched, the masking member need not fall on the trench. This is shown by trench 12 in Figure 5.

[0024] As illustrated in Figure 6, once the strain has been relieved from the channel regions of the n-channel transistors, a silicide 57 may be formed on the SiGe surfaces. Subsequently, the trenches are re-filled with, for instance, an interlayer dielectric (ILD). This re-filling of the trenches does not create strain on the channels. Note in Figure 6 the openings 52 and 53 have been re-filled with a dielectric 58.

[0025] In Figure 7, an additional embodiment is illustrated. Recesses are not formed for the n-channel transistors, but rather the silicon is doped as shown by the source and drain regions 62 for the n-channel transistor on the substrate section 10a. Recesses, such as shown in Figure 2, for the p-channel transistors, are etched for the embodiment of Figure 7. Then, the SiGe is epitaxially grown, forming the regions 60 for the p-channel transistor, and the regions 63 for the n-channel transistor. The regions 63 are above the level of the channel region, and as a result do not cause strain on the channel region of the n-channel transistor. Again, as was the case in the other embodiments,

silicide 65 is formed on the SiGe surfaces. The advantage gained in the other embodiments of lowering the silicon/silicide resistance is therefore obtained.

[0026] Thus, processes have been described for relieving the strain in an n-channel transistor which uses a SiGe source/drain. This allows the advantages of a SiGe formed silicide to be used both on the p-channel and n-channel transistors.

CLAIMS

What is claimed is:

1. A method for fabricating n-channel and p-channel transistors comprising:

forming recesses in a silicon substrate for source and drain regions adjacent to gate structures for n-channel and p-channel transistors;

growing SiGe in the recesses to form source and drain regions for the n-channel and p-channel transistors; and

relieving strain in channel regions of the n-channel transistors resulting from growing the SiGe, without substantially affecting the strain in channel regions of the p-channel transistors.

2. The method defined by claim 1, wherein the relieving of the strain occurs by implanting ions into the source and drain regions of the n-channel transistors to amorphize the SiGe.

3. The method defined by claim 2, wherein the ions are normally non-charge carrying atoms.

4. The method defined by claim 3, wherein the ions comprise carbon ions.

5. The method defined by claim 1, wherein the relieving of the strain in the n-channel transistors is obtained by etching a dielectric material from isolation trenches disposed on one side of the source region and one side of the drain region of the n-channel transistors.

6. The method defined by claim 5, wherein not all the dielectric in all the trenches is etched.

7. The method defined by claim 1, including forming a silicide metal on the source and drain regions.

8. The method defined by claim 2, including forming a silicide metal on the source and drain regions.

9. The method defined by claim 5, including forming a silicide metal on the source and drain regions.

10. The method defined by claim 9, wherein the silicide metal comprises nickel.

11. A method for forming an n-channel transistor comprising:

forming isolation trenches filled with a dielectric material in a silicon substrate;

growing SiGe epitaxial source and drain regions in recesses formed in the substrate adjacent to the isolation trenches;

etching the dielectric material from at least part of the trenches so as to relax strain in the SiGe source and drain regions; and

forming a silicide metal on the source and drain regions

12. The method defined by claim 11, wherein the silicide is formed using nickel.

13. The method defined by claim 12, wherein the dielectric material in the trenches is silicon dioxide.

14. The method defined by claim 11, including masking a part of at least one of the trenches such that the masked part of the trench is not etched when an exposed part of the trench is etched.

15. An integrated circuit having both n-channel and p-channel transistors comprising:

strain inducing means for causing strain in the source and drain regions of both the n-channel and p-channel transistors; and

strain relieving means for preventing the strain in the source and drain regions of the n-channel transistor from causing strain on channel regions of the n-channel transistor while not preventing the strain in the channel regions of the p-channel transistors.

16. The integrated circuit of claim 15, wherein the strain inducing means is SiGe source and drain regions.

17. The integrated circuit of claim 16, wherein the strain relieving means comprises isolation trenches disposed on the sides of the source and drain regions of the n-channel transistors filled with a different dielectric in trenches disposed on the sides of the source and drain regions of the p-channel transistors.

18. The integrated circuit defined by claim 16, wherein the strain relieving means comprises an amorphous SiGe region in the source and drain region of the n-channel transistors.

19. The integrated circuit defined by claim 17, including silicide on the source and drain regions of the n-channel and p-channel transistors.

20. The integrated circuit defined by claim 18, including silicide on the source and drain regions of the n-channel and p-channel transistors.

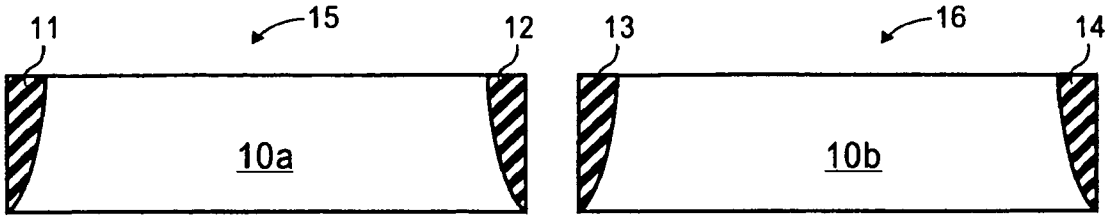


FIG. 1

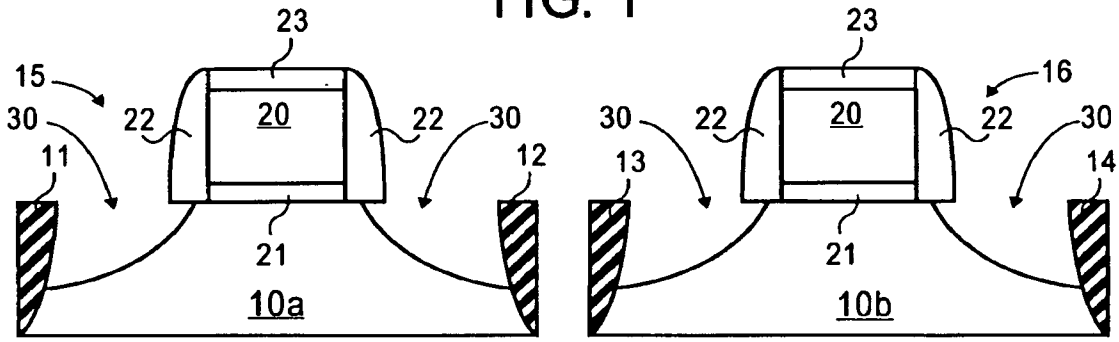


FIG. 2

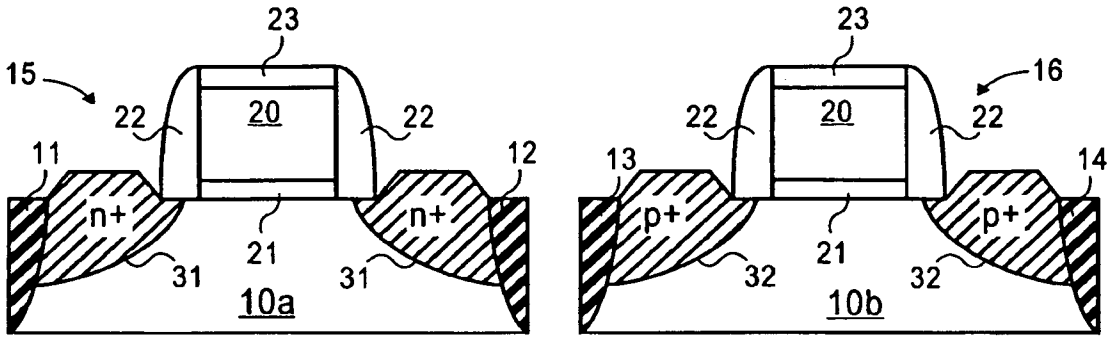


FIG. 3

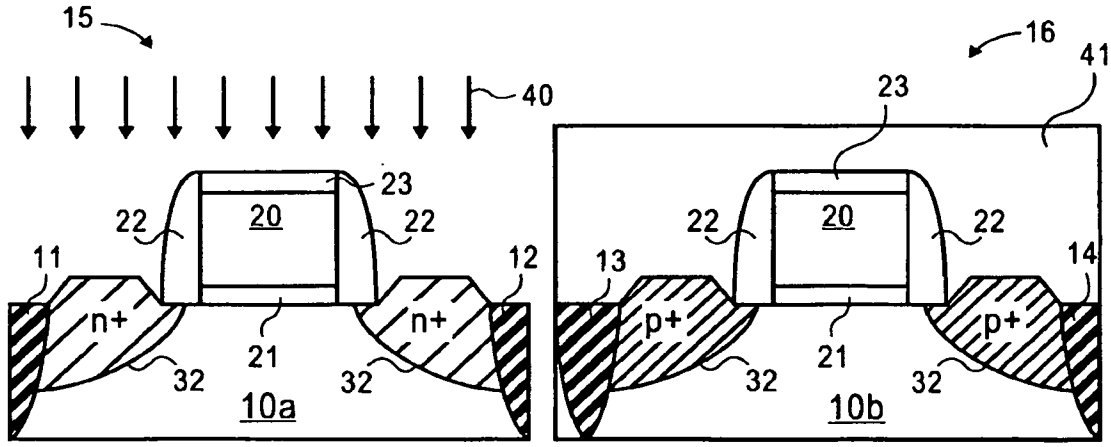


FIG. 4

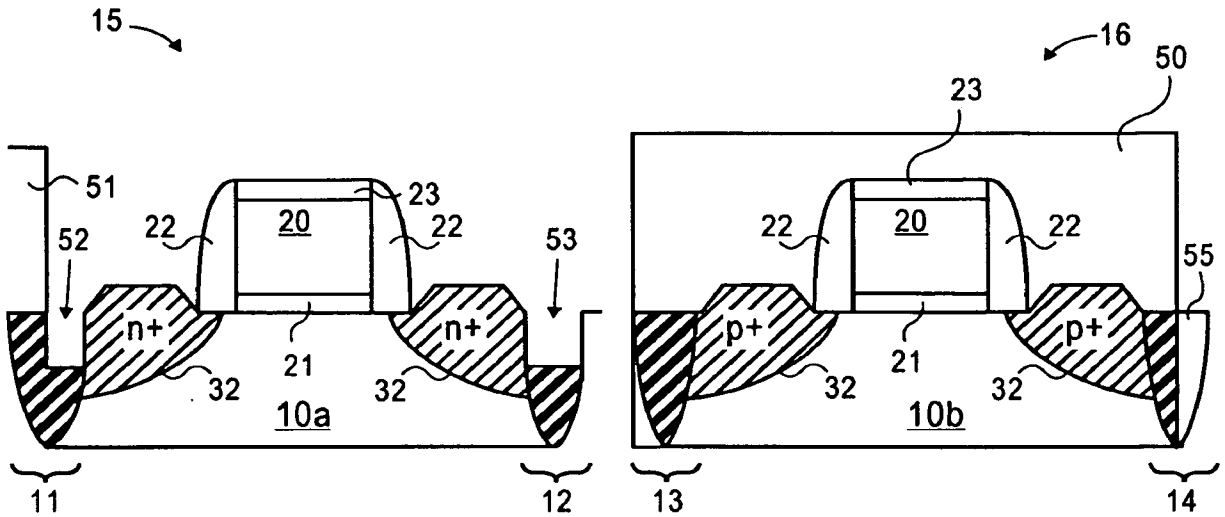


FIG. 5

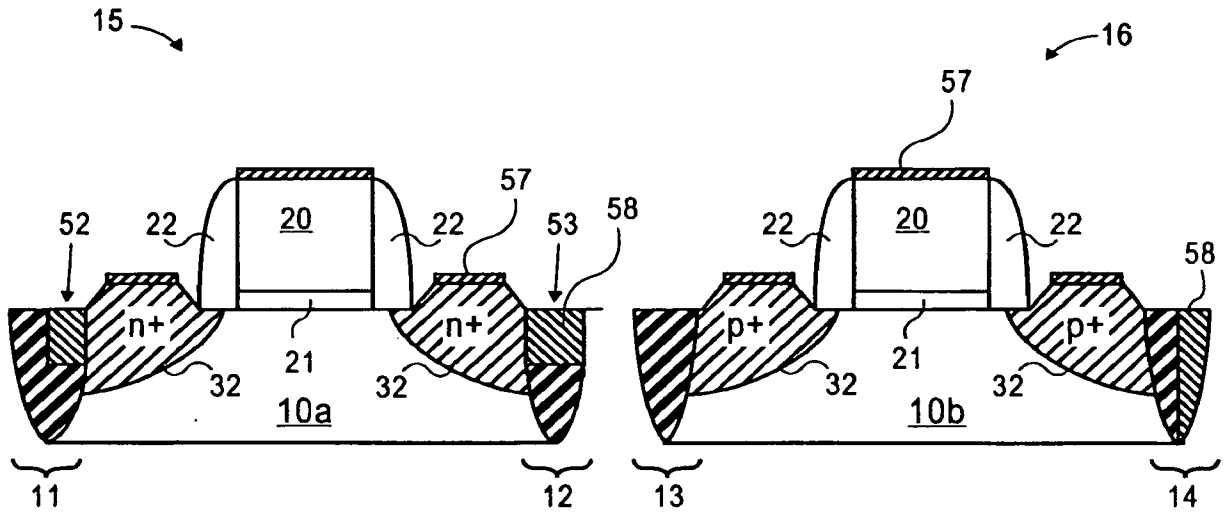


FIG. 6

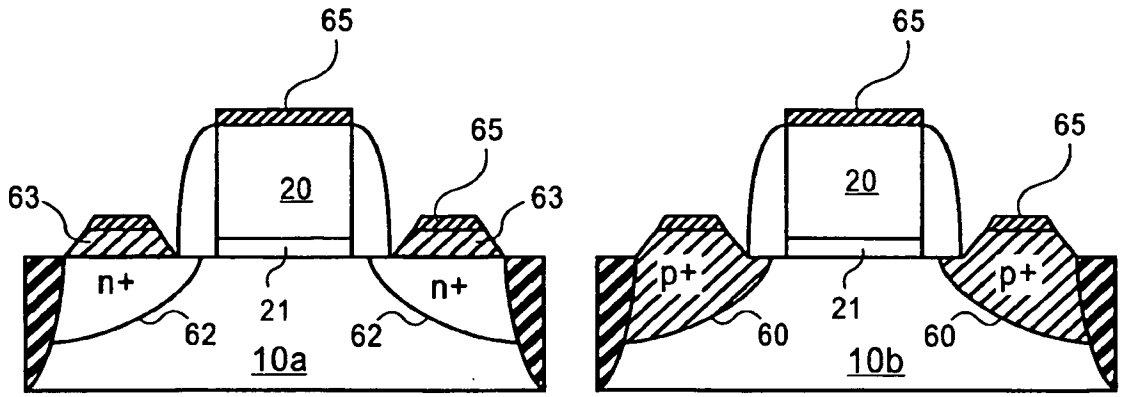


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2007/007707

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/8238(2006.01)i, H01L 27/092(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC8 : H01L 21/8238, H01L 27/092

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean Utility models and applications for Utility models since 1975

Japanese Utility models and applications for Utility models since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKIPASS(KIPO internal) "stress", "SiGe", "FET"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6,717,216 B1 (DORIS, BRUCE B. et al.) 06 APRIL 2004 See Claims 1-15, Figure 2	1-20
A	US 6,825,086 B2 (LEE, JONG-JAN et al.) 30 NOVEMBER 2004 See Claims 1-19, Figures 4, 10	1-20
A	US 6,838,728 B2 (LOCHTEFELD, ANTHONY J. et al.) 04 JANUARY 2005 See Claims 1-35, Figure 4	1-20
A	US 6,906,393 B2 (SAMAYA HIROKAZU et al.) 14 JUNE 2005 See Claims 1-6, Figures 1-20	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
04 SEPTEMBER 2007 (04.09.2007)	**04 SEPTEMBER 2007 (04.09.2007)**

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INTERNATIONAL SEARCH REPORT

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