(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
1 September 2011 (01.09.2011)

PCT

(10) International Publication Number
WO 2011/106751 A1

(51) International Patent Classification:
H05K 1/09 (2006.01)

(21) International Application Number:
PCT/US2011/026389

(22) International Filing Date:
26 February 2011 (26.02.2011)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/308,825 26 February 2010 (26.02.2010) US

(71) Applicant *(for all designated States except US)*: **SHOCKING TECHNOLOGIES, INC.** [US/US]; 5870 Hellyer Avenue, San Jose, CA 95138 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **KOSOWSKY, Lex** [US/US]; c/o Shocking Technologies, Inc., 5870 Hellyer Avenue, San Jose, CA 95138 (US). **FLEMING, Robert** [US/US]; c/o Shocking Technologies, Inc., 5870 Hellyer Avenue, San Jose, CA 95138 (US). **GRAYDON, Bhret** [US/US]; c/o Shocking Technologies, Inc., 5870 Hellyer Avenue, San Jose, CA 95138 (US). **VASQUEZ, Daniel** [US/US]; c/o Shocking Technologies, Inc., 5870 Hellyer Avenue, San Jose, CA 95138 (US).

(74) Agents: **KLINE, Keith** et al.; Carr & Ferrell LLP, 120 Constitution Drive, Menlo Park, CA 94025 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) **Title**: ELECTRIC DISCHARGE PROTECTION FOR SURFACE MOUNTED AND EMBEDDED COMPONENTS

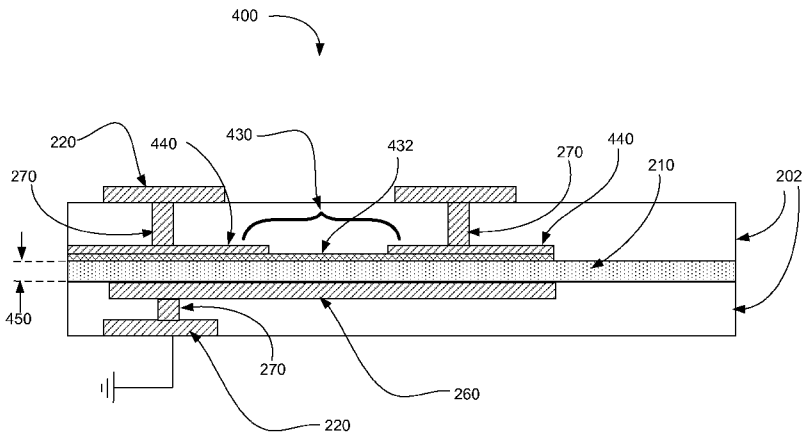

FIG. 4

(57) **Abstract**: Printed circuit boards including voltage switchable dielectric materials (VSDM) are disclosed. The VSDMs are used to protect electronic components, arranged on or embedded in printed circuit boards, against electric discharges, such as electrostatic discharges or electric overstresses. During an overvoltage event, a VSDM layer shunts excess currents to ground, thereby preventing electronic components from destruction or damage.

WO 2011/106751 A1

ELECTRIC DISCHARGE PROTECTION FOR SURFACE MOUNTED AND EMBEDDED COMPONENTS

BACKGROUND

FIELD OF THE INVENTION

[0001] This application relates generally to the protection of electronic devices against surge events, and more specifically to the application of voltage switchable dielectric materials for circuit boards to protect surface mounted and embedded electronic components thereof against electric discharge events.

DESCRIPTION OF RELATED ART

[0002] Electric discharge, such as electrostatic discharge (ESD), and electrical overstress (EOS) are among the leading causes of failure in electronic components and devices. The continuing trend to miniaturize electronic devices and the integration of increasingly smaller-scaled components into circuits causes an increase in ESD susceptibility problems. Consequently, these failures commonly lead to performance reduction or destruction of electronic devices due to unwanted overvoltage and/or overcurrent influence.

[0003] Various solutions have become available to protect electronic devices from ESD and EOS effects. To address ESD issues, engineers commonly use different capacitor based arrangements, Zener diodes, transient voltage suppression (TVS) diodes, multilayer varistors, Schottky diodes, and so forth. However, the aforementioned devices need to be mounted on circuit boards and, therefore, require additional space, in addition to increasing the complexity of the design. Moreover, most integrated circuits cannot be completely protected with existing ESD solutions.

SUMMARY OF THE CLAIMED INVENTION

[0004] Various embodiments relate to the use of voltage switchable dielectric materials in printed circuit boards to provide techniques for shunting currents to ground in case of an overvoltage and/or overcurrent event, thereby preventing damage to electronic components

[0005] In one embodiment, a printed circuit board is provided including at least one non-conductive layer, a conductor, a voltage switchable dielectric material (VSDM) applied to the conductor, and an electronic component having at least one lead, wherein the at least one lead is electrically coupled to the VSDM layer. The VSDM switches from being dielectric to being conductive when a voltage applied to the material exceeds a characteristic voltage level. The electronic component may be an embedded component or a surface mounted component. The electronic component may be a passive component such as a resistor, an inductor, or a capacitor. The electronic component may be an active component such as a diode, a transistor, a semiconductor device, a circuit, a chip, or an integrated circuit.

[0006] In another embodiment, a printed circuit board is provided including at least one non-conductive layer, a conductor, a voltage switchable dielectric material (VSDM) applied to the at least one non-conductive layer, and an electronic component having at least one lead, wherein the at least one lead is electrically coupled to the VSDM layer. The VSDM switches from being dielectric to being conductive when a voltage applied to the material exceeds a characteristic voltage level. The electronic component may be an embedded component or a surface mounted component. The electronic component may be a passive component such as a resistor, an inductor, or a capacitor. The electronic component may be an active component such as a diode, a transistor, a semiconductor device, a circuit, a chip, or an integrated circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Embodiments are illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar elements.

[0008] FIG. 1 illustrates an exemplary VSDM, according to an exemplary embodiment.

[0009] FIG. 2 illustrates a stackup incorporating a VSDM layer and a surface mounted electronic component, according to an exemplary embodiment.

[0010] FIG. 3 illustrates a stackup incorporating a VSDM layer and a surface mounted electronic component, according to an exemplary embodiment.

[0011] FIGS. 4-8 illustrate stackups incorporating VSDM layers and embedded electronic components, according to various exemplary embodiments.

[0012] Figs. 9A-C illustrate several circuits incorporating a VSDM element.

DETAILED DESCRIPTION

[0013] In some exemplary embodiments, protection against ESD or EOS may include using a VSDM. A VSDM may behave as an insulator at a lower voltage and a conductor at a higher voltage. A VSDM may have a specific switching voltage, which is a range between the states of low and high conductivity. The VSDM may provide a shunt to ground that protects a circuit and/or electronic component against voltage values above the switching voltage by allowing currents at the higher voltage values to pass to ground through the VSDM, rather than through the device or component being protected.

[0014] In this document, the terms "a" or "an" are used, as is common in patent documents, to include one or more than one. In this document, the term "or" is used to refer to a nonexclusive "or," such that "A or B" includes "A but not B," "B but not A," and "A and B," unless otherwise indicated. Furthermore, all publications, patents, and patent documents referred to in this document are incorporated by reference herein in their entirety, as though individually incorporated by reference. In the event of inconsistent usages between this document and those documents so incorporated by reference, the usage in the incorporated reference(s) should be considered supplementary to that of this document; for irreconcilable inconsistencies, the usage in this document controls.

[0015] The word "exemplary" is used herein to mean "serving as an example, instance, or illustration." Any embodiment described herein as "exemplary" is not to be construed as preferred or advantageous over other embodiments. Likewise, the term "embodiments" does not require that all embodiments include the discussed feature, advantage or mode of operation.

[0016] As used herein, the term printed circuit board (PCB) relates to a printed wiring board, an etched wiring board or similar substrate. PCBs are used to mechanically support and electrically connect discrete electronic components using conductive leads, wires, lines, pathways, tracks or signal traces laminated or attached onto a non-conductive substrate. In some cases, metallic leads may be included (e.g.,

as a layer of Cu which is subsequently etched) to provide electrical connectivity among various attached electronic components. According to some embodiments disclosed herein, the PCB can be implemented as a single substrate or a multi-layer substrate having the same or different conductivity at different layers.

[0017] As used herein, the term electronic component may refer to a passive component and/or an active component, and includes but is not limited to a resistor, an inductor, a capacitor, a diode, a transistor, a semiconductor device, a circuit, a chip, an integrated circuit, or the like. Typically, electronic components have conductive leads used for electrical connection thereof to other components or pathways. According to embodiments disclosed herein, electronic components include surface mounted components and embedded components. Electronic components can be implemented as discrete elements or as thin films (e.g. a resistive layer, a capacitance layer, etc.) and deposited or sputtered on substrates or layers of PCB.

[0018] As used herein, VSDM relates to any composition, or combination of compositions that has a characteristic of being dielectric or non-conductive, unless a field or voltage that exceeds a specific value is applied to the material, in which case the material becomes conductive. Thus, the VSDM is a dielectric unless voltage (or field) exceeding the value associated with the material (e.g. such as provided by ESD or EOS events) is applied to the material, in which case the VSDM switches to a conductive state.

[0019] The VSDM may further be defined as a nonlinear resistance material. In many applications, the characteristic voltage of VSDM ranges in values that exceed the operational voltage levels of the circuit or device several times over. Such voltage levels may be of the order of transient conditions (e.g., produced by electric charges, such as electrostatic discharge), although embodiments may include use of planned electrical events. Furthermore, one or more embodiments provide a VSDM that behaves similarly to a non-conductive or dielectric material in the absence of the voltage exceeding the characteristic voltage.

[0020] According to embodiments disclosed herein, the VSDM is a polymer-based material and may include filled polymers. The filled polymers may include a mixture

of insulator, conductor, and semiconductor materials. Examples of insulative materials include but are not limited to silicone polymers, epoxy, polyimide, polyethylene, polypropylene, polyphenylene oxide, polysulphone, solgel materials, creamers, silicone dioxide, aluminum oxide, zirconia oxide, and other metal oxide insulators. Examples of conductive materials include metals, such as copper, aluminum, nickel, stainless steel, or the like. Examples of semiconductive materials include both organic and inorganic semiconductors. Some inorganic semiconductors include silicon, silicon carbide, boron nitride, aluminum nitride, nickel oxide, zinc oxide, and zinc sulfide. Examples of organic semiconductors include poly-3-exylthiophene, pentacene, perylene, carbon nanotubes, fullerenes, or the like. A specific formulation and composition may be selected for mechanical and electrical properties well suited to the particular application of the VSDM.

[0021] Additionally, one or more embodiments disclosed herein incorporate a VSDM layer over a PCB. The VSDM layer may provide a shunt to ground that protects a circuit and/or electronic component against voltages above the switching voltage by allowing currents at these voltages to pass to ground through the VSDM layer, rather than through the circuit and/or electronic component being protected.

[0022] FIG. 1 illustrates an exemplary VSDM 100. The VSDM 100 may include a conductive phase 110 and an insulating and/or semiconducting phase 120. At low voltages, VSDM 100 may behave as an insulator. At voltages above a switching voltage (e.g., above a trigger voltage, above a clamp voltage, etc.), VSDM 100 may behave as a conductor. Typically, VSDM 100 may be connected to an electrical ground, and may shunt current to ground during the protection of a device.

[0023] FIG. 2 illustrates an exemplary stackup 200 incorporating a VSDM layer. The stackup 200 includes a non-conductive substrate 202 (e.g., a PCB and/or a layer thereof, such as a prepreg layer or the like). The stackup 200 also includes a VSDM layer 210, which may include any or all of a coating, a layer, a line, and a via. The VSDM may be of any shape, and may be connected to a conductor 220. Certain conductors 220 may be electrically connected to ground such that current is shunted

through the VSDM layer to ground during an overvoltage event. The conductor may include a conductive layer, wire, pathline, via, connector, or the like.

[0024] An electronic component 230 that is to be protected (e.g., a resistor, inductor, capacitor, diode, transistor, circuit, chip, and the like) may be mounted on the VSDM layer 210. In some cases, the electronic component 230 may be a surface mounted device. According to another embodiment, the electronic component 230 may be a substantially planar device deposited directly on the VSDM layer 210 (e.g., as resistive ink). Furthermore, the electronic component 230 may include one or more leads 240 (e.g., Cu leads). During an overvoltage event (e.g., an ESD or EOS event) involving the electronic component 230, current may be shunted from the leads 240 (and/or the component 230) through the VSDM layer 210 to the conductor 220. The current may bridge a gap 250 between the component 230 and/or the lead 240 and a conductive pad 260, which may be electrically connected to the conductor 220 by a via 270.

[0025] The electronic component 230 may be characterized by one or more specifications such as a resistance, an inductance, a capacitance, or the like. In some cases, the ability to withstand an overvoltage and/or overcurrent event may not be specified. For example, a resistor may be designed to provide a resistance of 1 ohm during normal use (e.g., at voltages up to 10 volts) but may be damaged by higher voltages, and a similar resistor designed to be damage resistant may be too large in scale for a given application. Protecting a smaller resistor using a VSDM may allow the use of smaller components, which may be advantageous in packages such as PCB assemblies. While larger resistors such as 0603 and 0402 resistors may be large enough to withstand an overvoltage or overcurrent event, smaller resistors such as 0201 and 01005 resistors may require protection to maintain the integrity of the circuit.

[0026] Any of the VSDM layer 210, the conductor 220, and the electronic component 230 may be disposed on the surface of the substrate 202, or be inside (e.g., embedded in) the substrate 202. In some embodiments, the VSDM layer 210 and the electronic component 230 are embedded in a PCB (e.g., fabricated as layers in a PCB

stackup). The stackup 200 may be embedded by adding and processing additional PCB components (e.g., additional layers of prepreg).

[0027] FIG. 3 illustrates an exemplary stackup 300 incorporating a VSDM layer. In this example, the stackup 300 may include a non-conductive substrate 202 (such as a printed circuit board and/or a layer thereof) and/or other assembly. A VSDM layer 210 may include a coating, a layer, a line, a via, and/or be of any other shape, and may generally be connected to a conductor 220. An electronic component 230 being protected (surface mounted or embedded) may be mounted onto or incorporated into the VSDM layer 210. During an overvoltage event (e.g., an ESD event) involving the component 230, current may be shunted from the leads (and/or the component 230 itself) through the VSDM layer 210 to the conductor 220. In some cases, an active volume may be associated with the portion of the VSDM layer 210 located in a gap 350 between leads 240 and/or component 230 and conductor 220. An active volume may be associated with a thickness of the VSDM layer and an area (e.g., of bounding conductors), and may predominantly describe a volume through which current passes during an overvoltage event. The stackup 300 may be embedded by adding and processing additional PCB components (e.g., additional layers of prepreg, or the like).

[0028] FIG. 4 illustrates a cross section of an exemplary stackup 400. As shown, the stackup 400 may include one or more non-conductive substrates 202 and at least one VSDM layer 210. The VSDM layer 210 may be implemented as a coating, film, line, via, wire, pathline, and/or be of any other appropriate shape according to the specific application. The VSDM layer 210 may generally be connected to ground via one or more conductors 220, a pad 260, a via 270, or a combination thereof. An electronic component 430 (e.g., a thin film resistive layer 432 and associated leads 440) being protected may be deposited, sputtered, or otherwise formed onto the VSDM layer 210.

[0029] During an overvoltage event (e.g., an ESD or EOS event) involving the component 430, excess current may be shunted to ground, rather than passing through the component 430 at a level that damages the component 430. The current may be shunted by passing through the VSDM layer 210, which may include a gap 450. In

some cases, additional layers (e.g., a film associated with the component 430) may be present in a condition that does not deleteriously affect the ESD/EOS protection capabilities of the VSDM layer 210 (e.g., a resistive film may be particularly thin, so the resistive layer 432 may be disposed beneath the leads 440 when the resistive layer 432 is particularly thin).

[0030] FIG. 5 illustrates a cross section of a stackup 500. In this example, the stackup 500 may include at least one non-conductive substrate 202 and a VSDM layer 210. The VSDM layer 210 may be implemented as a coating, film, line, via, wire, pathline, and/or be of any other appropriate shape according to the specific application. The VSDM layer 210 may generally be connected to ground via one or more conductors 220 disposed on the surface of the stackup 500, and also by means of a pad 260, a via 270, or a combination thereof. An electronic component 430 being protected may be deposited, sputtered or otherwise formed onto the VSDM layer 210. The electronic component 430 may be implemented as a thin film resistive layer 432 and include associated conductive leads 440, which may also be deposited or sputtered onto the resistive layer 432 and/or one of the stackup layers.

[0031] In case of an overvoltage event related to an ESD or EOS involving the component 430, overcurrent may be shunted to ground, rather than passing through the electronic component 430. The excess current may be shunted by passing through the VSDM layer 210, which may include a gap 550.

[0032] FIG. 6 illustrates a cross section of an exemplary stackup 600. According to this embodiment, the stackup 600 may include a non-conductive VSDM layer 210 protecting a plurality of regions of an electronic component 430. The VSDM layer 210 may generally be connected to ground via one or more conductors 220 arranged in the stackup 600, and by means of a pad 260, a via 270, or a combination thereof. The electronic component 430 being protected may be deposited, sputtered, or otherwise formed onto the VSDM layer 210. The electronic component 430 may be implemented as a thin film (e.g. resistive layer) and include at least one associated conductive lead 440. In the stackup 600, a first gap 650 and a second gap 652 define substantially

separate regions of the VSDM layer 210 through which current may pass during an overvoltage event.

[0033] FIG. 7 illustrates a cross section of an exemplary stackup 700. In this embodiment, the stackup 700 may provide for a VSDM layer 210 with one or more non-conductive substrates 202 between the VSDM layer and the electronic component 430 being protected. The stackup 700 may also include one or more conductors 220, one or more vias 270, and one or more pads 260, each of which may be interconnected between each other and to ground.

[0034] The VSDM layer 210 may include a gap 750. During an overvoltage event involving the electronic component 430, excess current may be shunted to ground via the gap 750 of the VSDM layer 210, rather than passing through the component 430 itself, thereby protecting component 430 from damage or destruction.

[0035] FIG. 8 illustrates a cross section of an exemplary stackup 800. As shown, the stackup 800 may include at least two non-conductive substrates 202, a VSDM layer 210 disposed between the substrates 202, an electronic component 430 including one or more conductive leads 440, and a plurality of connection elements, such as a conductor 220, a via 270, pads 260, or a combination thereof. The electronic component 430 may be arranged on a first substrate 202, and may not have a direct contact with the VSDM layer 210, but rather an electrical contact accomplished by the plurality of connection elements. The VSDM layer 210 may include a gap 850, which may be associated with an active region of current passage (e.g., between pads 260 on either side of the gap 850) during an overvoltage event.

[0036] Figs. 9A-C illustrate several circuit schemes incorporating a VSDM element. In these illustrations, a VSDM element 900 is shown schematically as an electrical valve with a lightning bolt symbol. In these examples, the VSDM element 900 is connected to a conductor that may be connected to ground, and is electrically (and sometimes physically) connected to an electronic device or electronic component to be protected.

[0037] FIG. 9A illustrates a VSDM 900 protecting a resistor 910, which may be a surface mounted or an embedded resistor. In this example, the VSDM 900 is electrically connected to a lead of the resistor 910. An overvoltage event, such as ESD

or EOS capable of damaging the resistor 910, may result in shunting excess current to ground via the VSDM element 900.

[0038] FIG. 9B illustrates a VSDM element 900 protecting a capacitor 920, which may be a surface mounted or an embedded capacitor. In this example, the VSDM element 900 is connected to leads on both sides of the capacitor 920. An overvoltage event that might damage the capacitor 920 may result in shunting excess current to ground via at least one of the VSDM elements 900.

[0039] FIG. 9C illustrates a VSDM element 900 protecting an inductor 930, which may be an embedded inductor. In this example, the VSDM element 900 is connected to a lead of the inductor 930. In case of an overvoltage event that might damage inductor 930, excess current is shunted to ground via the VSDM element 900.

[0040] Some embodiments may include sensors to sense various parameters (e.g., current, voltage, power, resistance, resistivity, inductance, capacitance, thickness, strain, temperature, stress, concentration, depth, length, width, switching voltage and/or voltage density (between insulating and conducting), trigger voltage, clamp voltage, off-state current passage, dielectric constant, time, date, and other characteristics). Various apparatuses may monitor various sensors, and systems may be actuated by automated controls (solenoid, pneumatic, piezoelectric, and the like). Some embodiments may include a computer-readable storage medium coupled to a processor and memory. Executable instructions stored on the computer readable storage medium may be executed by the processor to perform, control or monitor various methods of operating and/or protecting electronic components arranged in PCBs. Sensors and actuators may be coupled to the processor, providing input and receiving instructions associated with various methods. Certain instructions may be provided for closed-loop control of various parameters via coupled sensors providing input and coupled actuators receiving instructions to adjust parameters. Various embodiments may include different electronic devices such as telephones (e.g., cell phones), Universal Serial Bus (USB)-devices (e.g., a USB-storage device), personal digital assistants (PDAs), laptop computers, netbook computers, tablet Personal Computer (PC), light emitting diodes (LEDs), and the like.

[0041] The foregoing description is provided to enable any person skilled in the art to make or use specific embodiments. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without departing from the scope of the disclosure. Thus, the present disclosure is not intended to be limited to the embodiments described herein but is to be accorded the widest scope consistent with the principles disclosed herein.

What is claimed is:

1. A printed circuit board, comprising:

at least one conductor;

a voltage switchable dielectric material (VSDM) applied to the at least one conductor; and

an electronic component having at least one lead, wherein the at least one lead is electrically coupled to the VSDM.

2. The printed circuit board of claim 1, wherein the electronic component is an embedded component.

3. The printed circuit board of claim 2, wherein the embedded component includes one or more of a resistor, an inductor, and a capacitor.

4. The printed circuit board of claim 2, wherein the embedded component includes one or more of a diode, a transistor, a semiconductor device, a circuit, a chip, and an integrated circuit.

5. The printed circuit board of claim 1, wherein the electronic component is a surface mounted component.

6. The printed circuit board of claim 5, wherein the surface mounted component includes one or more of a resistor, an inductor, and a capacitor.

7. The printed circuit board of claim 5, wherein the surface mounted component includes one or more of a diode, a transistor, a semiconductor device, a circuit, a chip, and an integrated circuit.

8. The printed circuit board of claim 1, wherein the VSDM is a layer.

9. The printed circuit board of claim 8, wherein the VSDM layer is incorporated within a non-conductive layer.

10. The printed circuit board of claim 8, wherein the VSDM layer is disposed between at least two non-conductive layers.

11. A printed circuit board, comprising:

at least one non-conductive layer;

at least one conductor;

a voltage switchable dielectric material (VSDM) applied to at least one of the non-conductive layers; and

an electronic component having at least one lead, wherein the at least one lead is electrically coupled to the VSDM.

12. The printed circuit board of claim 11, wherein the electronic component is an embedded component.

13. The printed circuit board of claim 12, wherein the embedded component includes one or more of a resistor, an inductor, and a capacitor.

14. The printed circuit board of claim 12, wherein the embedded component includes one or more of a diode, a transistor, a semiconductor device, a circuit, a chip, and an integrated circuit.

15. The printed circuit board of claim 11, wherein the electronic component is a surface mounted component.

16. The printed circuit board of claim 15, wherein the surface mounted component includes one or more of a resistor, an inductor, and a capacitor.

17. The printed circuit board of claim 15, wherein the surface mounted component includes one or more of a diode, a transistor, a semiconductor device, a circuit, a chip, and an integrated circuit.

18. The printed circuit board of claim 11, wherein the VSDM is a layer.

19. The printed circuit board of claim 18, wherein the VSDM layer is incorporated within the at least one non-conductive layer.

20. The printed circuit board of claim 18, wherein the VSDM layer is disposed between at least two non-conductive layers.

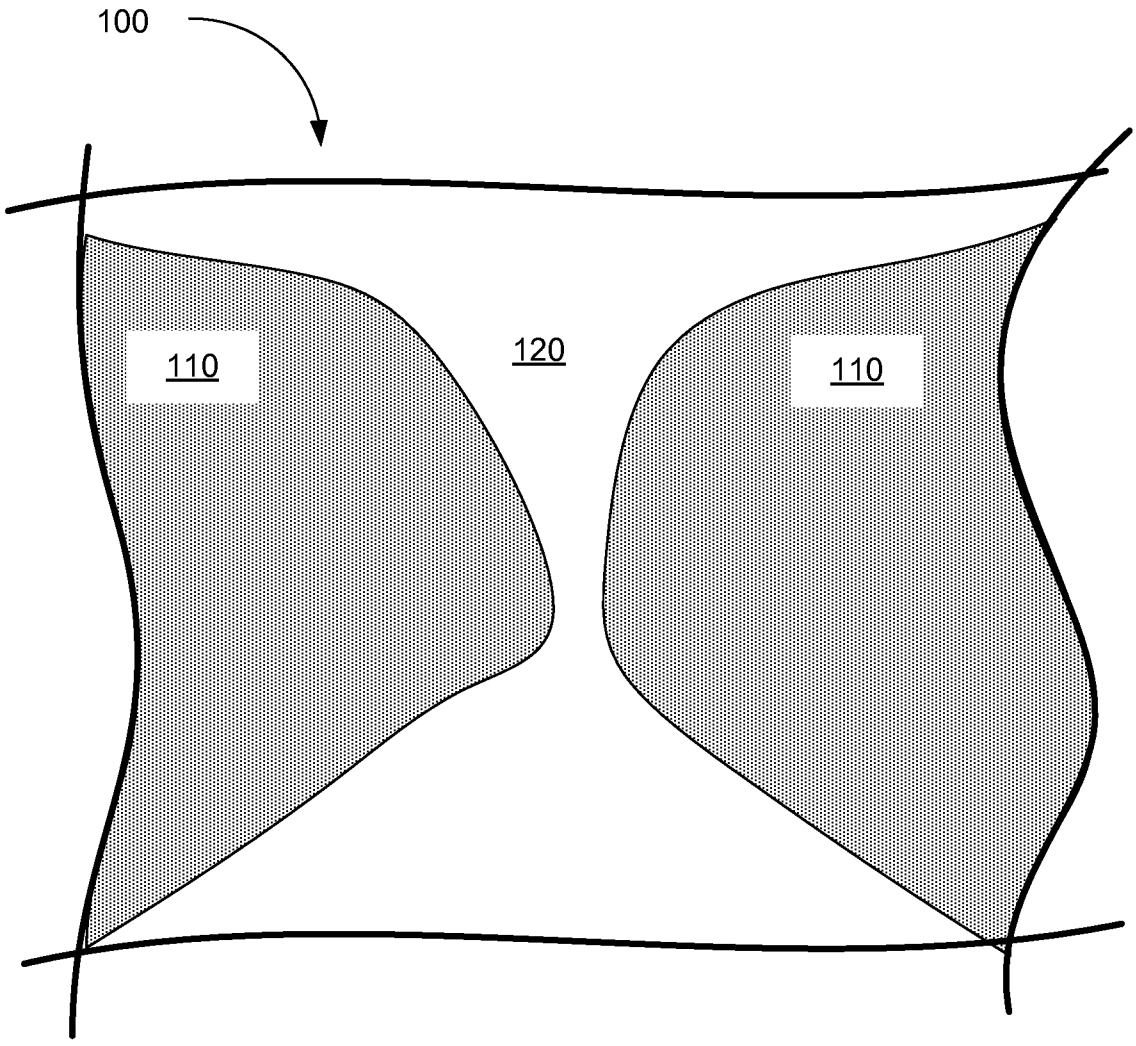

FIG. 1

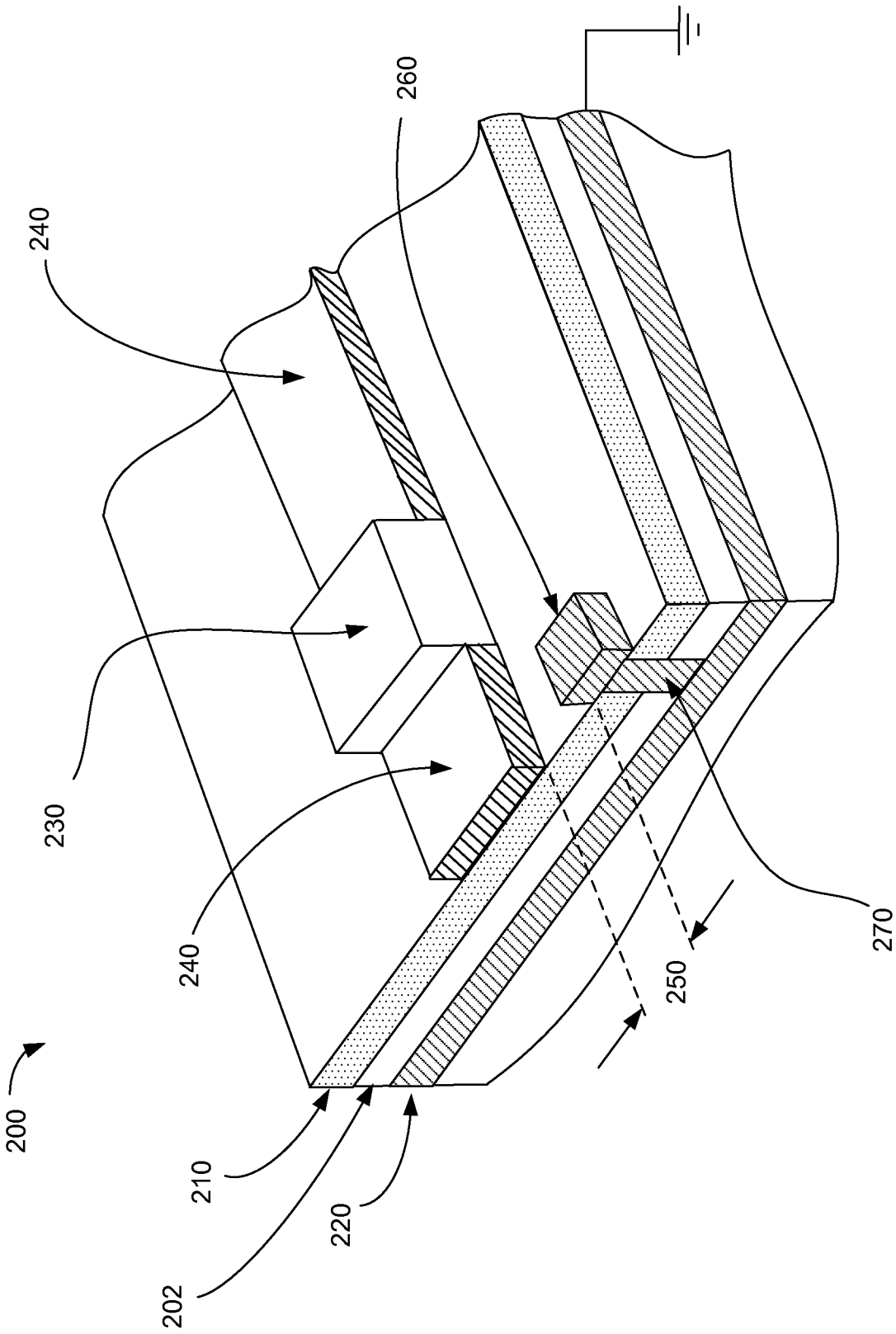

FIG. 2

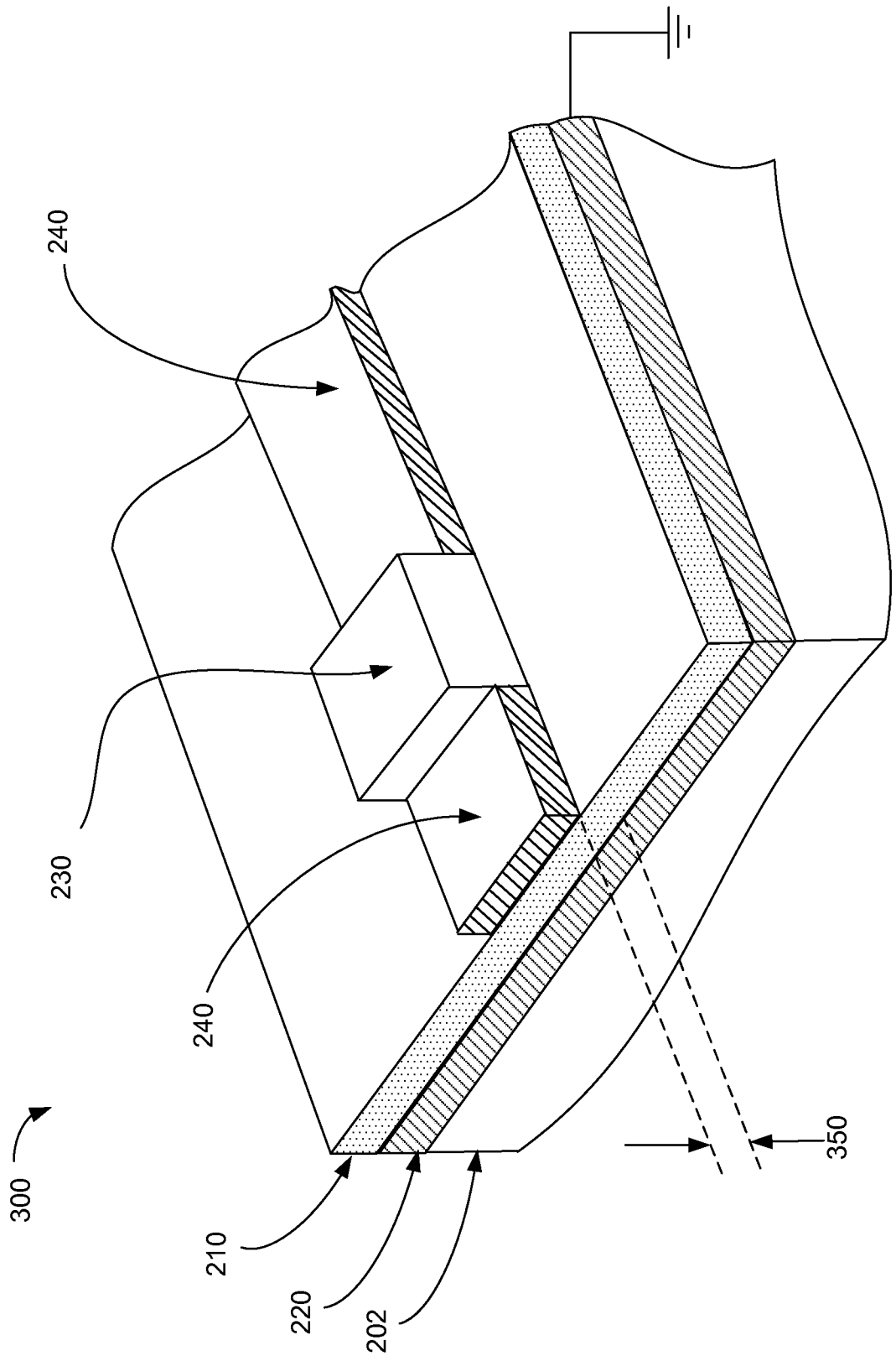

FIG. 3

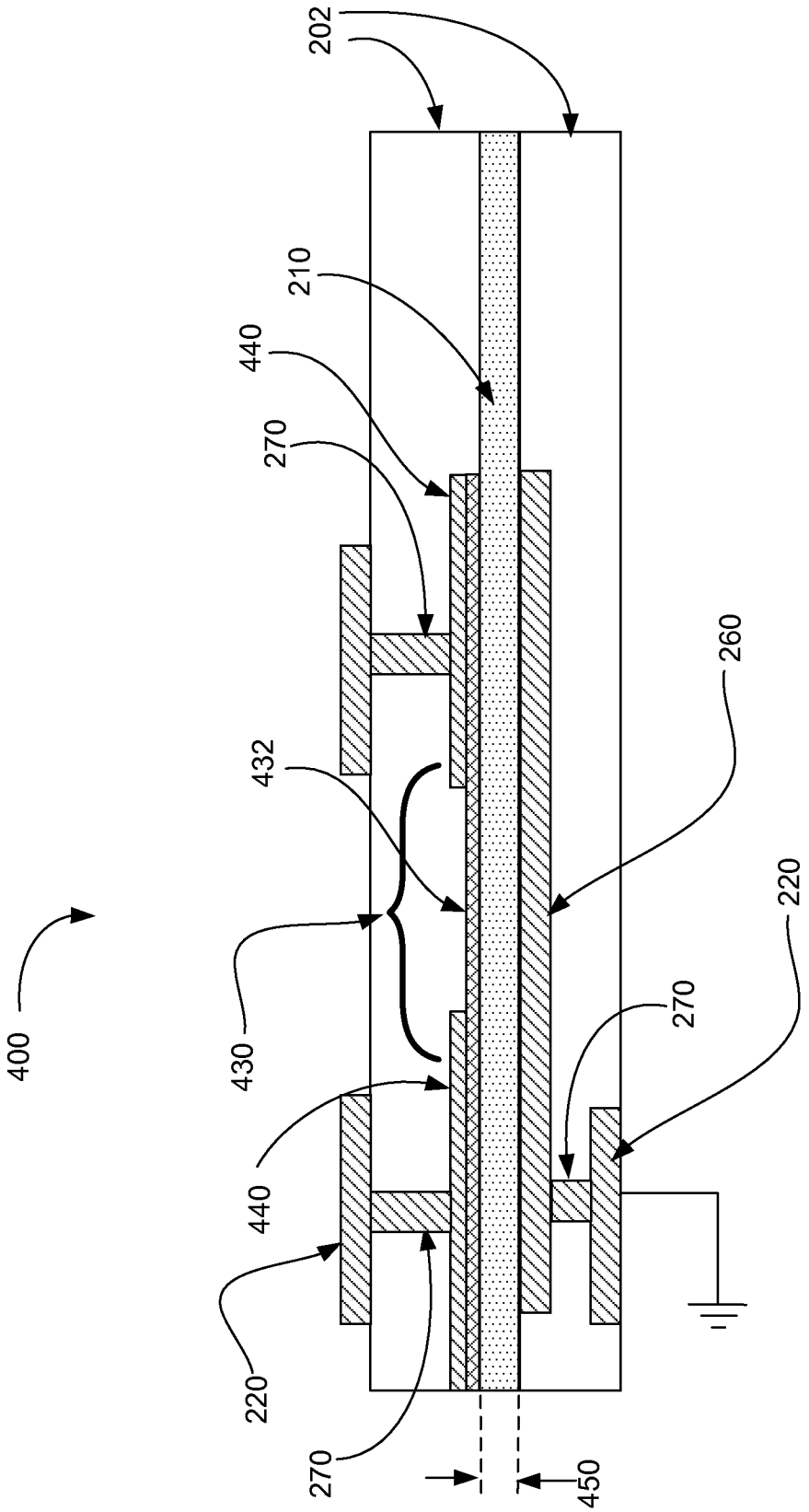

FIG. 4

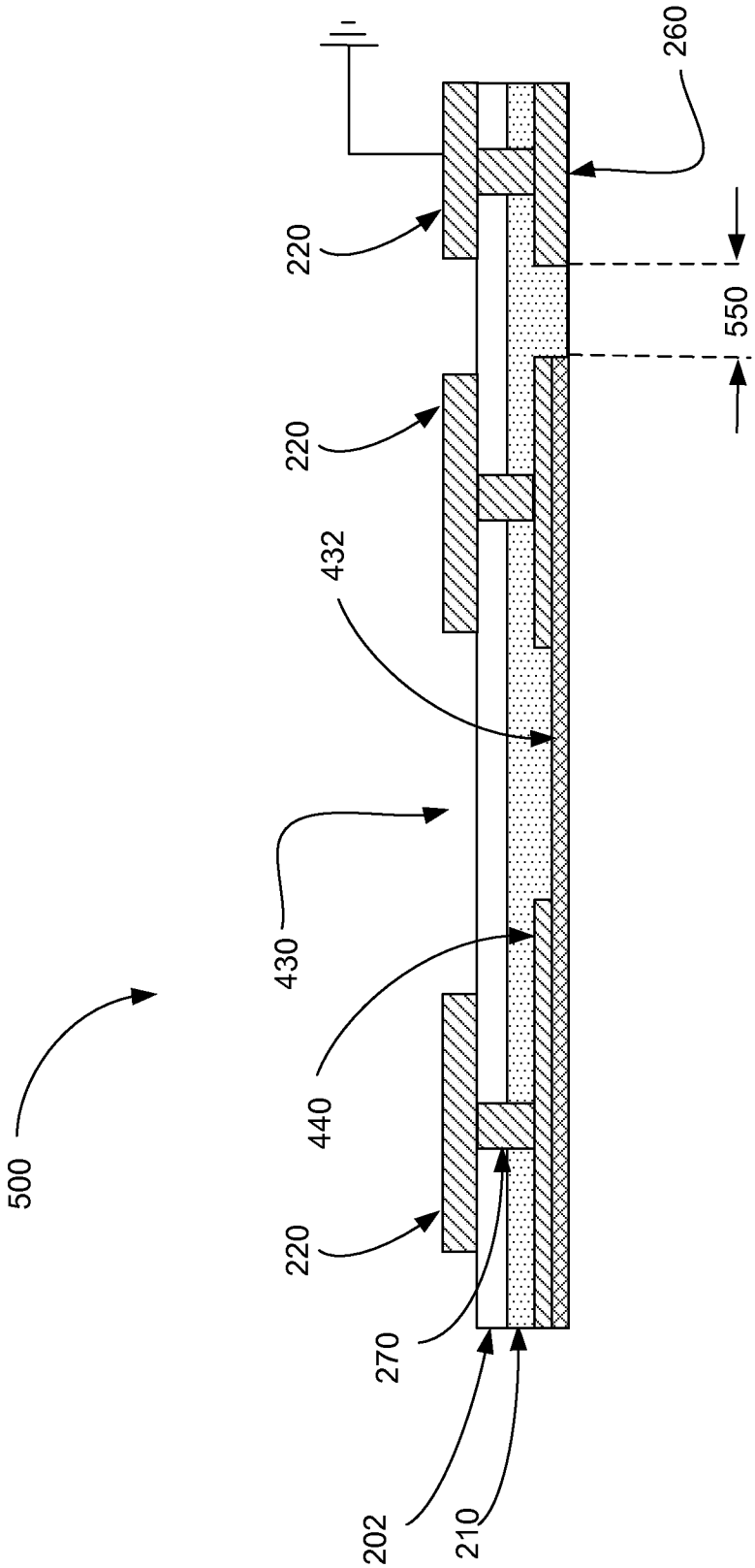

FIG. 5

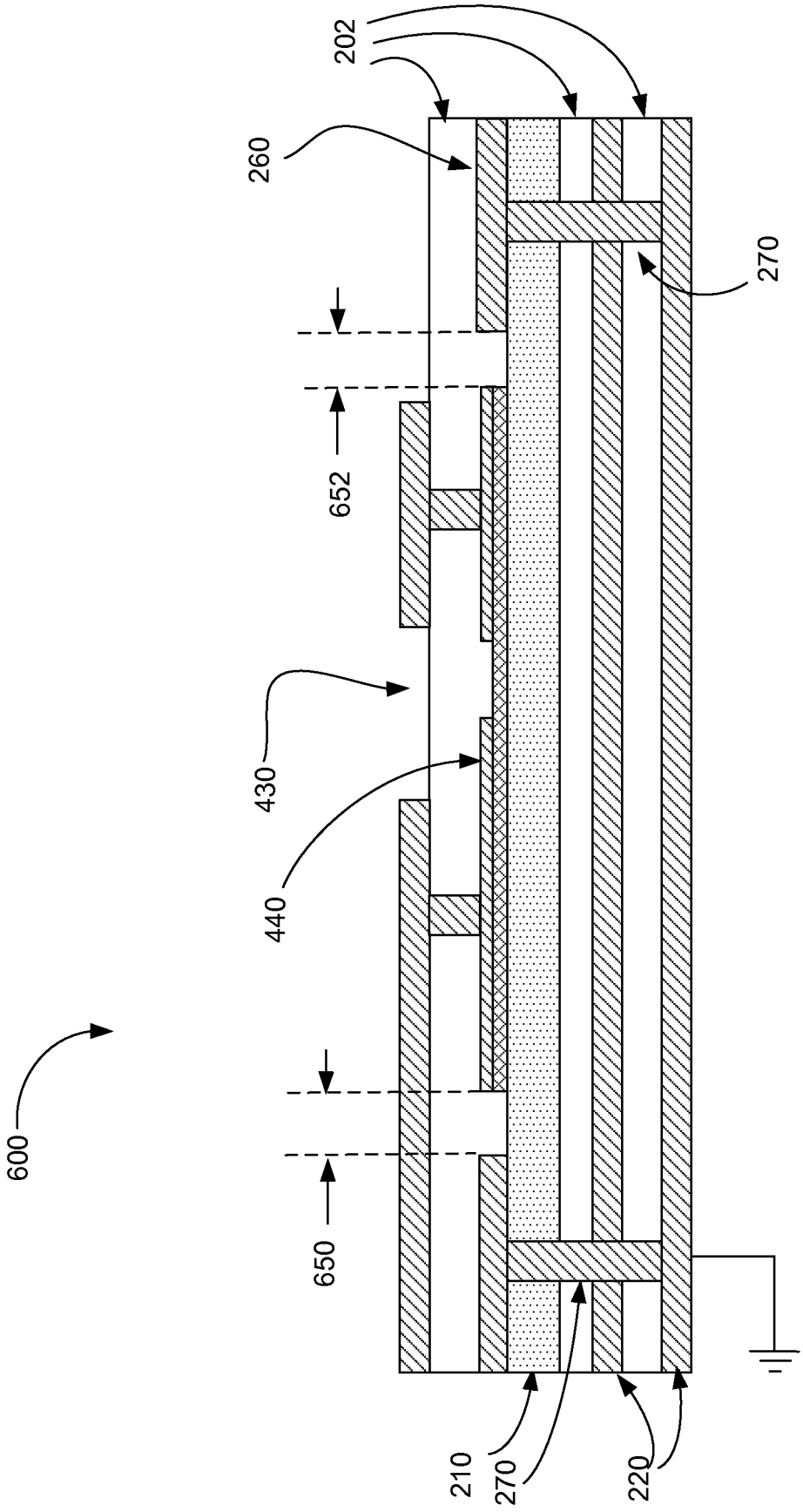

FIG. 6

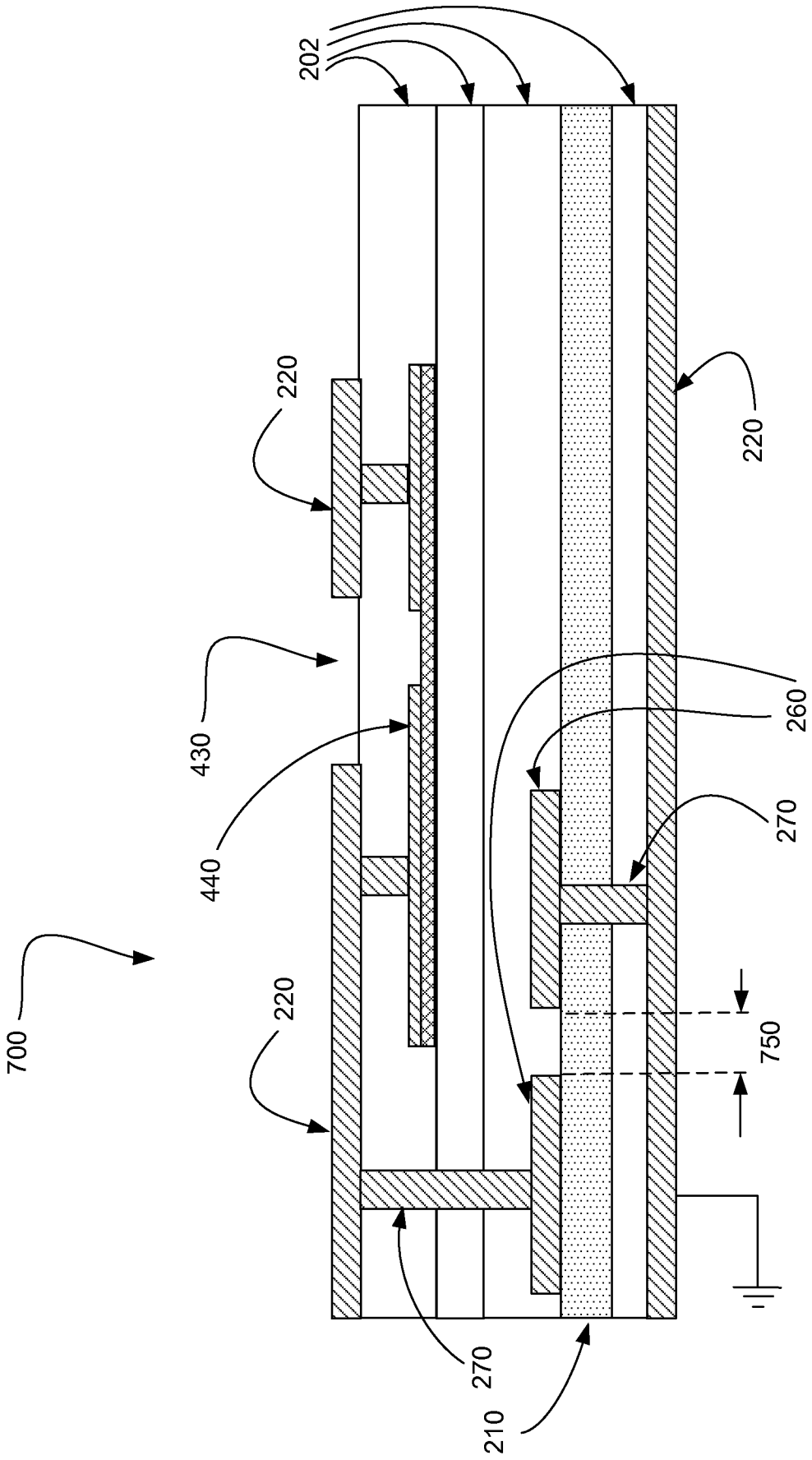

FIG. 7

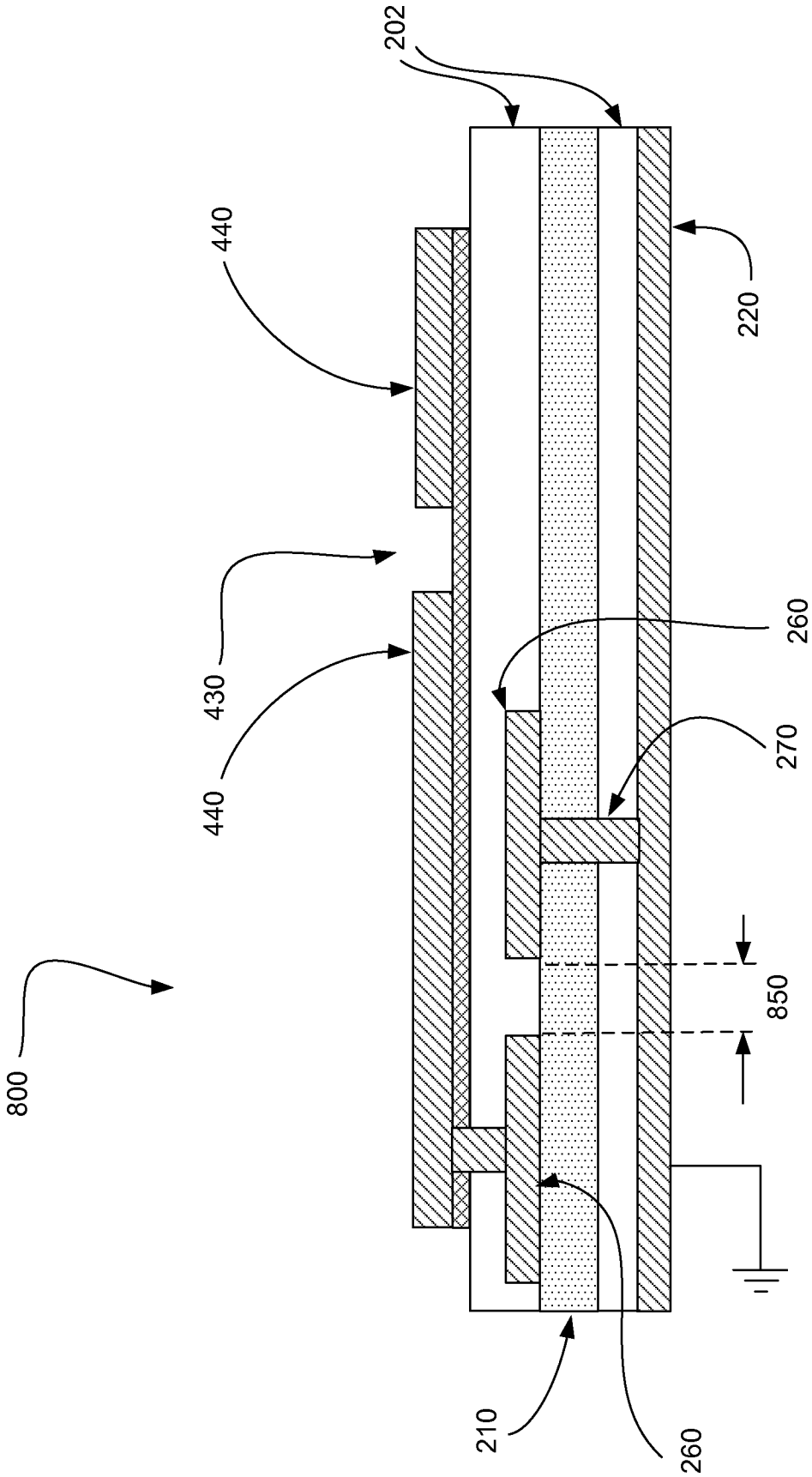

FIG. 8

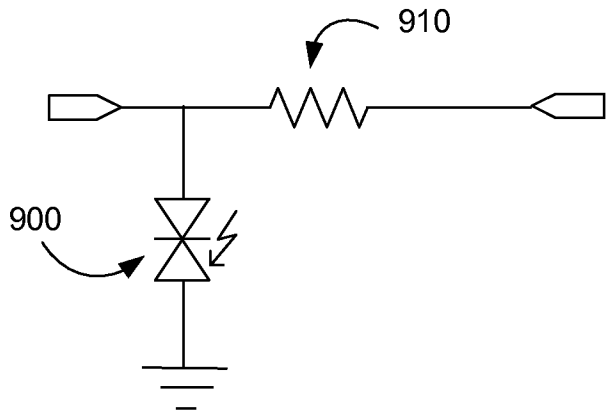

FIG. 9A

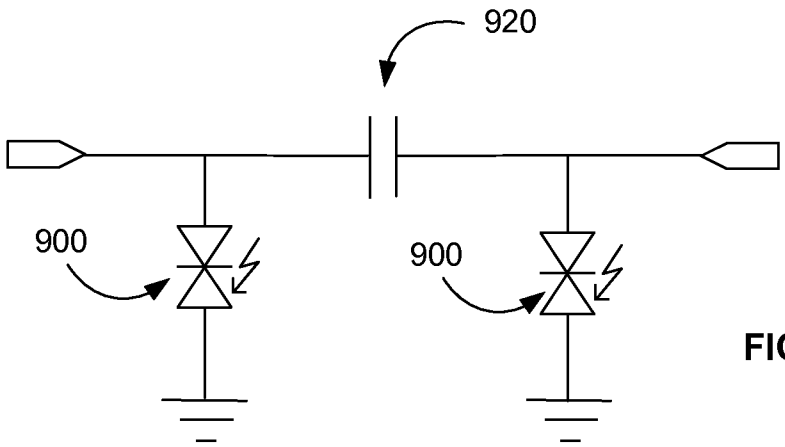

FIG. 9B

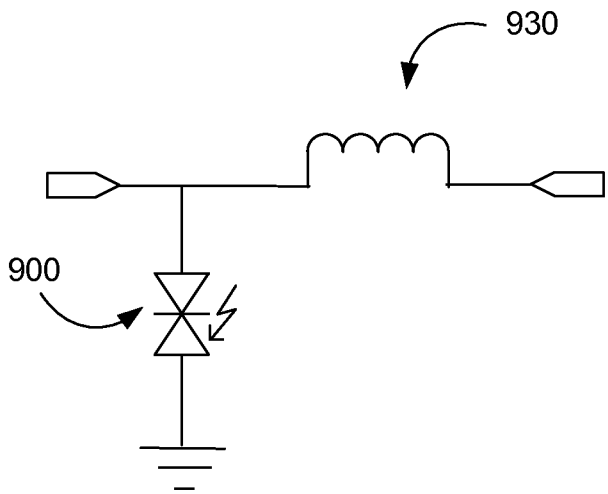

FIG. 9C

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/026389

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H05K 1/09 (2011.01)
USPC - 438/622
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H05K 1/09 (2011.01)
USPC - 174/256, 260, 261; 438/622

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Orbit, Google Scholar

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2009/0044970 A1 (KOSOWSKY) 19 February 2009 (19.02.2009) entire document	1-20
Y	US 4,714,952 A (TAKEKAWA et al) 22 December 1987 (22.12.1987) entire document	1-20
A	US 2003/0079910 A1 (KOSOWSKY) 01 May 2003 (01.05.2003) entire document	1-20
A	US 5,246,388 A (COLLINS et al) 21 September 1993 (21.09.1993) entire document	1-20
A	US 4,928,199 A (DIAZ et al) 22 May 1990 (22.05.1990) entire document	1-20

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
01 April 2011	12 APR 2011
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)