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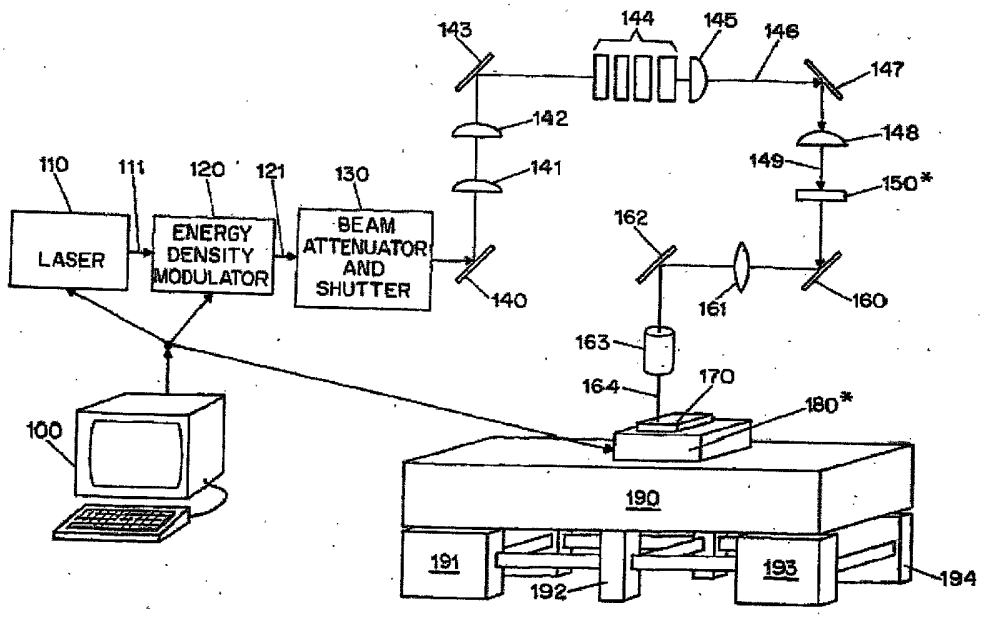
(54) **Title:** IMPROVED POLYCRYSTALLINE TFT UNIFORMITY THROUGH MICROSTRUCTURE MIS-ALIGNMENT



(57) **Abstract:** Methods of making a polycrystalline silicon thin-film transistor having a uniform microstructure. One exemplary method requires receiving a polycrystalline silicon thin film having a grain structure which is periodic in at least a first direction, and placing at least portions (410, 420) of one or more thin-film transistors on the received film such that they are tilted relative to the periodic structure of the thin film.

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A METHOD TO INCREASE DEVICE-TO-DEVICE UNIFORMITY FOR POLYCRYSTALLINE THIN-FILM TRANSISTORS BY DELIBERATELY MIS-ALIGNING THE MICROSTRUCTURE RELATIVE TO THE CHANNEL REGION

SPECIFICATION

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is based on United States provisional patent application serial no. 60/315,181, filed August 27, 2001, which is incorporated herein by reference for all purposes and from which priority is claimed.

BACKGROUND OF THE INVENTION

[0002] Technical Field. The present invention relates to semiconductor processing techniques, and more particularly, techniques for fabricating semiconductors suitable for use at thin-film transistor ("TFT") devices.

[0003] Background Art. Semiconductor films, such as silicon films, are known to be used for providing pixels for liquid crystal display devices and organic light emitting diode display devices. Such films are commonly processed via excimer laser annealing ("ELA") methods, where an amorphous silicon film is irradiated by an excimer laser to be crystallized.

[0004] Significant effort has gone into the refinement of "conventional" ELA (also known as line-beam ELA) processes in the attempt to improve the performance of the TFT devices placed on the processed semiconductor thin films. For example, U.S. Patent No. 5,766,989 issued to Maegawa et al., the entire disclosure of which is incorporated herein in its entirety by reference, describes the ELA methods for forming polycrystalline thin film and a method for fabricating a TFT. The '989 patent attempts to address the problem of non-uniformity of characteristics across the substrate, and provide certain options for apparently suppressing such non-uniformities.

[0005] However, the details of the beam-shaping approach used in conventional ELA methods make it extremely difficult to reduce the non-uniformities in the semiconductor films and to improve the performance characteristics of such films. For example, in a low-temperature polycrystalline silicon ("LTPS") process, when the size of the grains becomes

comparable to the dimensions of the channel region of the TFT, large device-to-device non-uniformity results. This is caused by the randomness of the microstructure, i.e., the random location of the grains and thus the grain boundaries. Such non-uniformity, especially when perpendicular to the current flow, can act as a current barrier. Further, when the transistor is in its off-state, carriers are generated at the grain boundary, which contribute to the off-current. This is especially the case when the grain boundary is in or close to the drain–channel junction.

[0006] Therefore, it has been realized that control over the microstructure is needed in order to ensure a uniform TFT process, both with respect to periodicity and location. Regarding the former, the film should be uniform, exhibiting periodicity in the location of the grains and thus the grain boundaries. Regarding the latter, the location of the grains and thus the grain boundaries should be controlled so that their contribution to the electrical characteristics is the same for every single device.

[0007] In an pulsed-laser, e.g., an excimer laser, irradiaton process to obtain LTPS films, control over the TFT microstructure may be obtained through the use lithography to induce such periodicity. The use of lithography also accounts for location control, since the accurate alignment procedure of the lithographic process is used. Unfortunately, the use of lithography requires at lease one extra processing step, which in turn increases complexity and thus costs.

[0008] Alternatively, control over the TFT microstructure may be obtained through the use of sequential lateral solidification ("SLS") techniques. For example, in U.S. Patent No. 6,322,625 issued to Im and U.S. patent application serial no. 09/390,537 (the "'537 application"), which is assigned to the common assignee of the present application, the entire disclosures of which are incorporated herein by reference, particularly advantageous apparatus and methods for growing large grained polycrystalline or single crystal silicon structures using energy-controllable laser pulses and small-scale translation of a silicon sample to implement sequential lateral solidification have been described. As described in these patent documents, at least portions of the semiconductor film on a substrate are irradiated with a suitable radiation pulse to completely melt such portions of the film throughout their thickness. In this manner, when the molten semiconductor material solidifies, a crystalline structure grows into the solidifying portions from selected areas of the semiconductor film which did not undergo a complete melting. Thereafter, the beam pulses irradiate slightly offset from the crystallized areas so that the grain structure extends into the molten areas from the crystallized areas.

[0009] Using the system shown in Fig. 1, an amorphous silicon thin film sample is processed into a single or polycrystalline silicon thin film by generating a plurality of excimer

laser pulses of a predetermined fluence, controllably modulating the fluence of the excimer laser pulses, homogenizing the modulated laser pulses in a predetermined plane, masking portions of the homogenized modulated laser pulses into patterned beamlets, irradiating an amorphous silicon thin film sample with the patterned beamlets to effect melting of portions thereof corresponding to the beamlets, and controllably translating the sample with respect to the patterned beamlets and with respect to the controlled modulation to thereby process the amorphous silicon thin film sample into a single or polycrystalline silicon thin film by sequential translation of the sample relative to the patterned beamlets and irradiation of the sample by patterned beamlets of varying fluence at corresponding sequential locations thereon.

[0010] While the system of Fig. 1 is highly advantageous in generating uniform, high quality polycrystalline silicon and single crystal silicon which exhibit periodicity and thereby solves a problem inherent with conventional ELC techniques, the technique does adequately not account for control over grain boundaries. For example, in the simplest form, SLS requires two pulses to crystallize the amorphous precursor into an LTPS film with partial periodicity, e.g., the 2-shot material shown schematically in Figure 2a. The periodicity is only in one direction, shown by long grain boundaries 210, 220, 230, 240, 250 that are parallel to each other and which also have a protrusion to them. However, the position of the short grain boundaries is not at all controlled. The spacing between the parallel grain boundaries can be increased, and this material is in general called n-shot material. Likewise, Figure 2b shows a so-called 4-shot material in which the grain boundaries are periodic in both directions. Again, the spacing between the grain boundaries can be increased, and is generally referred to as 2n-shot material.

[0011] While SLS techniques offer periodicity, such techniques do not offer accurate control of the location of grain boundaries. Referring to Figures 2c-d, the LTPS film produced includes a varying number of long grain boundaries perpendicular to the current flow, and the possibility of having a perpendicular grain boundary in or out of a TFT drain region. Both problems become more severe when grain size is increasing and/or when channel dimensions are decreasing, i.e., when the size of the grains becomes comparable to the dimensions of the channel region. While there has been a suggestion in United States Patent No. 6,177,301 to Jung to misalign TFT channel regions with respect to the grain growth direction, that suggestion is made without taking into account the underlying need to maintain uniformity in TFT microstructure. Accordingly, there exists a need for a TFT manufacturing technique that provides for control over both the periodicity of grain boundaries and the location of TFTs in order to provide for uniformity in TFT microstructure.

SUMMARY OF THE INVENTION

[0012] An object of the present invention is to provide a TFT manufacturing technique that provides for control over both the periodicity of grain boundaries and the location of TFTs in order to provide for uniformity in TFT microstructure.

[0013] Another object of the present invention is to provide a device having uniformity in TFT microstructure.

[0014] In order to meet these and other objects of the present invention which will become apparent with reference to further disclosure set forth below, the present invention provides methods of making a polycrystalline silicon thin-film transistor having a uniform microstructure. One exemplary method requires receiving a polycrystalline silicon thin film having a grain structure which is periodic in at least a first direction, and placing at least portions of one or more thin-film transistors on the received film such that they are tilted relative to the periodic structure of said thin film. The polycrystalline silicon thin film may be formed by a sequential lateral solidification process, e.g., a two shot sequential lateral solidification process.

[0015] Advantageously, the portions of said one or more thin-film transistors may be active channel regions having a width W. Where the periodic structure of the thin film is λ and m is a variable, the placing step involves placing active channel regions on the received film such that they are tilted at an angle θ relative to said periodic structure of said thin film, where $W \sin(\theta) = m \lambda$. The variable m is selected such that that the number of grain boundaries in any of the one or more thin-film transistors remains relatively controlled, and is preferably approximately equal to an integer.

[0016] The present invention also provides a device including a polycrystalline silicon thin-film transistor having a uniform microstructure. In an exemplary embodiment, the device includes polycrystalline silicon thin film having a grain structure which is periodic in at least a first direction, and at least portions of one or more thin-film transistors, placed on the thin film such that they are tilted relative to said periodic structure of the film.

[0017] The accompanying drawings, which are incorporated and constitute part of this disclosure, illustrate preferred embodiments of the invention and serve to explain the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] Fig. 1 is a functional diagram of a prior art system for performing semiconductor processing including sequential lateral solidification;

[0019] Figs. 2a-b are illustrative diagrams showing exemplary processed silicon samples using the prior art system of Fig. 1;

[0020] Figs. 2c-d are illustrative diagrams showing the prior art placement of active channel regions of TFTs on the exemplary processed silicon samples shown in Fig. 2a;

[0021] Figs 3a-b. are illustrative diagrams showing the placement of active channel region of TFTs on the exemplary processed silicon samples shown in Fig. 2a in accordance with the present invention;

[0022] Figs 4a-b. are illustrative diagrams showing the placement of active channel region of TFTs on the exemplary processed silicon samples shown in Fig. 2a in accordance with the present invention; and

[0023] Figs 5a-b. are illustrative diagrams showing the placement of active channel region of TFTs on the exemplary processed silicon samples shown in Fig. 2a in accordance with the present invention.

[0024] Throughout the Figs., the same reference numerals and characters, unless otherwise stated, are used to denote like features, elements, components or portions of the illustrated embodiments. Moreover, while the present invention will now be described in detail with reference to the Figs., it is done so in connection with the illustrative embodiments.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0025] Referring again to Figs. 2a-b, exemplary processed silicon thin films using the prior art SLS system of Fig. 1 are shown. In particular, Fig. 2a illustrates a sample processed by irradiating a region with a single excimer laser pulse, micro-translating the sample, and irradiating the region with a second excimer laser pulse. While the following exemplary description of the invention will be with respect to this so-called "2-shot" material as an example, those skilled in the art will appreciate that the present invention is more broadly applicable to silicon thin films that have been processed with n-shot and 2n-shot SLS techniques.

[0026] In accordance with the present invention, active channel regions of TFTs are deliberately tilted relative to the periodic microstructure of the processed thin film. Such tilting may be accomplished by tilting the placement of the channel region itself on the processed thin film, or alternatively, by fabricating a thin film during SLS processing which includes a tilted periodic grain structure. A combination of both alternatives may also be employed.

[0027] The precise methodology for placing TFTs on the processed thin film is not important to the present invention, and hence any known technique may be employed,. One exemplary technique is disclosed in U.S. Patent No. 5,766,989 to Maegawa et al., the contents of which are incorporated by reference herein.

[0028] When the active channel regions of TFTs are deliberately tilted relative to the periodic microstructure of the processed thin film., the spread in the number of perpendicular or long grain boundaries becomes less, leading to an increased device-to-device uniformity. In accordance with the present invention, the tilting angle (θ) should, however, not be too large, as not to increase the influence of the parallel, or short, grain boundaries. The ideal value of θ can be derived from equation (1), in which W is the width of the channel region, λ is the spacing between the perpendicular grain boundaries, and m is preferably close to an integer in value:

$$W * \sin(\theta) = m * \lambda, \quad (1)$$

[0029] In order to measure performance N of the TFT, equation (2) may be employed, where L is the length of the channel region, and n is a determined ratio:

$$L \cos(\theta) = n * \lambda, \quad (2)$$

[0030] In equation (2), a lower value of the ration n implies increased performance. L is often defined by the design rule of the process and is equal for all TFTs, and typically ranges from 3 to 6 μm. W, however, can be adjusted to match the requirements on the TFT properties, and typically ranges from 10 to 100s μm. The spacing λ between the perpendicular brain boundaries typically ranges from 2 to 10 μm , but smaller and larger values are possible.

[0031] Referring next to Figs. 3a-b, a first example of the present invention will be described. In this example, the ratio n =1, m =1, and θ = 10 degrees. As shown in Figs. 3a-b, all devices contain one perpendicular grain boundary, regardless of any translation of the TFT device, e.g., from the position shown in Fig 3a to that shown in Fig. 3b.

[0032] Referring next to Figs. 4a-b, a second example of the present invention will be described. In this example, the ratio n = 0.5, m = 1, and θ = 10 degrees. As shown in Figs. 4a-b, the channel region contains two portions, a first 410 in which one perpendicular grain boundary is present, and a second 420 in which no perpendicular grain boundary is present.

[0033] In latter portion 420, the device exhibits behavior as that of a TFT in fully directionally solidified material in which carriers are not hampered by grain boundaries. As shown in Figs. 4a-b, the relative contribution of each of these two parts is again invariable to any translation of the device, e.g., from the position shown in Fig 4a to that shown in Fig. 4b.

[0034] While the examples shown in Figs, 3-4 are considered to be the ideal scenarios, where m is an integer, small deviations from use of an integer value may be used in accordance with the present invention. However, the deviation from an integer value must be selected such that the number of grain boundaries in any given TFT remains relatively controlled.

[0035] Referring next to Figs. 5a-b, further examples of the present invention will be described. In Fig. 5a, the ratio $n = 2.1$, $m = 1$, and $\theta = 10$ degrees; in Fig. 5b, the ratio $n = 2.1$, $m = 0.5$, and $\theta = 5$ degrees. As shown in Figs. 5a-b, for the ideal value of θ, the number of grain boundaries is again invariable to any translation of the device. However, when θ deviates from this value, translations increasingly change the number of grain boundaries. When n equals, or is very close to, an integer the number of grain boundaries is essentially invariant for changes in θ. Of course it should exceed a certain value to assure that the fraction of perpendicular grain that is in the drain region is also invariant to translations.

[0036] The foregoing merely illustrates the principles of the invention. Various modifications and alterations to the described embodiments will be apparent to those skilled in the art in view of the teachings herein. It will thus be appreciated that those skilled in the art will be able to devise numerous systems and methods which, although not explicitly shown or described herein, embody the principles of the invention and are thus within the spirit and scope of the invention.

CLAIMS

1. A method of making a polycrystalline device including two or more thin-film transistors of substantially uniform microstructure, comprising the steps of:

(a) receiving a polycrystalline silicon thin film having a grain structure which is periodic in at least a first direction; and

(b) placing at least portions of two or more thin-film transistors on said received film tilted at an angle relative to said periodic structure of said thin film, such that that the number of long grain boundaries in any of said portions remains substantially uniform.

2. The method of claim 1, wherein said receiving step comprises the step of receiving a polycrystalline silicon thin film formed by a sequential lateral solidification process.

3. The method of claim 1, wherein said portions of said two or more thin-film transistors comprise active channel regions having a width W.

4. The method of claim 3, wherein said periodic structure of said thin film is λ, m is a variable, and said placing step comprises the step of placing said active channel regions on said received film such that said active channel regions are tilted at an angle θ relative to said periodic structure of said thin film, where $W \sin(\theta) = m \lambda$.

5. The method of claim 4, wherein m substantially equal to an integer.

6. The method of claim 4, wherein m is equal to an integer.

7. The method of claim 4, wherein m is equal to the integer 1.

8. A method of making a device including thin-film transistors, comprising the steps of:

(a) receiving a polycrystalline silicon thin film having a grain structure which is periodic in at least a first direction in an amount λ; and

(b) placing at least portions of one or more thin-film transistors having a width W on said received film tilted at an angle θ relative to said periodic structure λ of said thin film, such that $W \sin(\theta) = m \lambda$, where m is substantially equal to an integer.

9. The method of claim 8, wherein said receiving step comprises the step of receiving a polycrystalline silicon thin film formed by a sequential lateral solidification process.

10. The method of claim 8, wherein said portions of said one or more thin-film transistors comprise active channel regions having a width W.

11. The method of claim 10, wherein m is equal to an integer.

12. The method of claim 10, wherein m is equal to the integer 1.

13. A device including two or more polycrystalline silicon thin-film transistors of substantially uniform microstructure, comprising:

(a) a polycrystalline silicon thin film having a grain structure which is periodic in at least a first direction; and

(b) at least two or more thin-film transistor portions placed on said received film, each tilted at an angle relative to said periodic structure of said thin film, such that that the number of long grain boundaries in any of said portions remains substantially uniform.

14. The device of claim 13, wherein said polycrystalline silicon thin film comprises thin film formed by a sequential lateral solidification process.

15. The device of claim 13, wherein said portions of said two or more thin-film transistors comprise active channel regions having a width W.

16. The device of claim 13, wherein said periodic structure of said thin film is λ, m is a variable, and said active channel regions are tilted at an angle θ relative to said periodic structure of said thin film, where $W \sin(\theta) = m \lambda$.

17. The device of claim 16, wherein m is substantially equal to an integer.

18. The device of claim 16, wherein m is equal to an integer.

19. The device of claim 16, wherein m is equal to the integer 1.

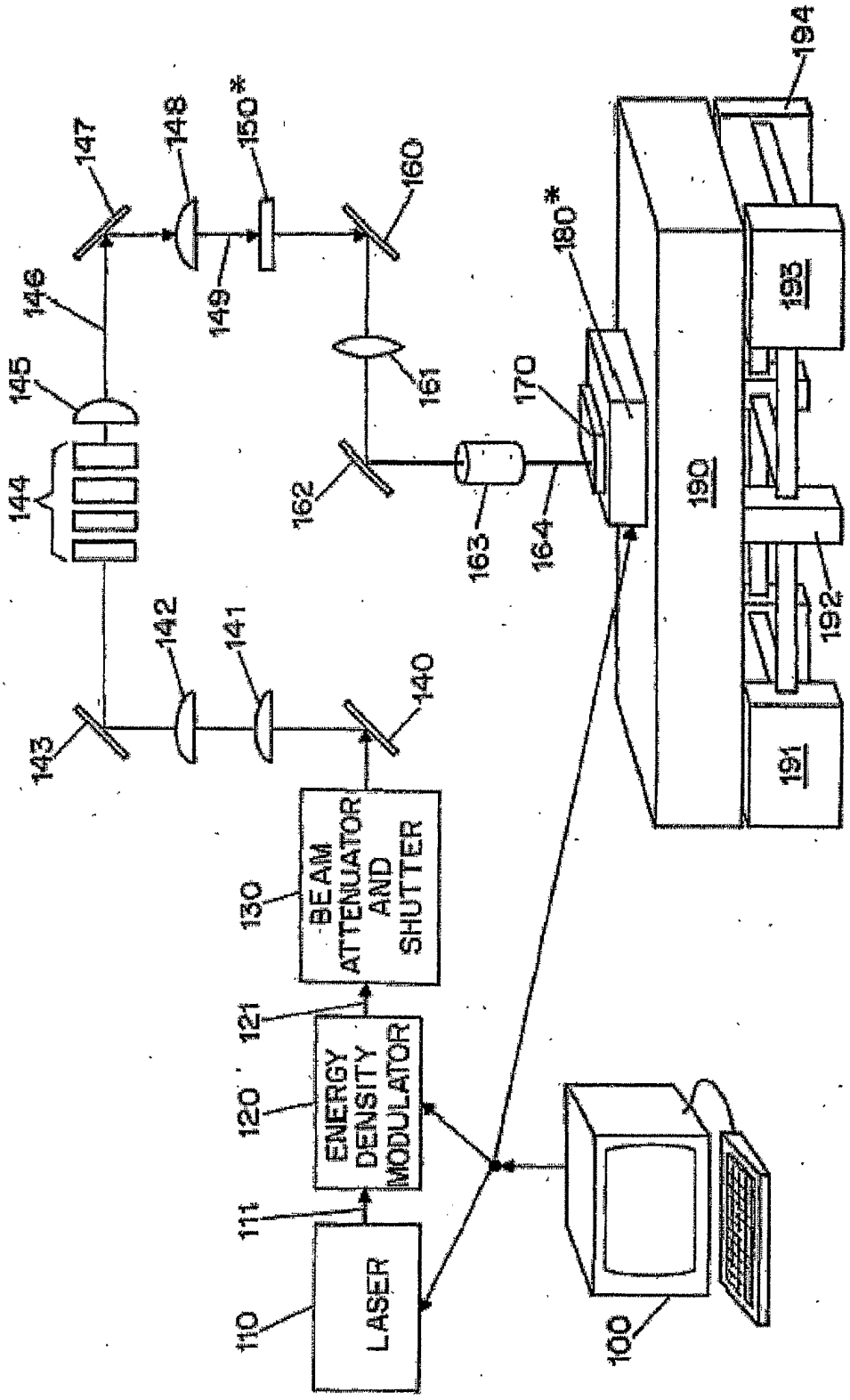

FIG. 1 (Prior Art)

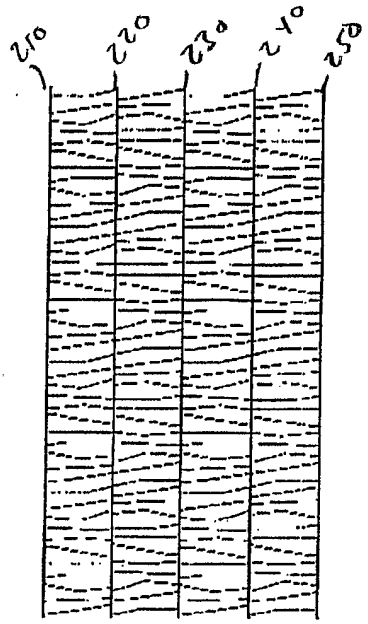

Figure 2a

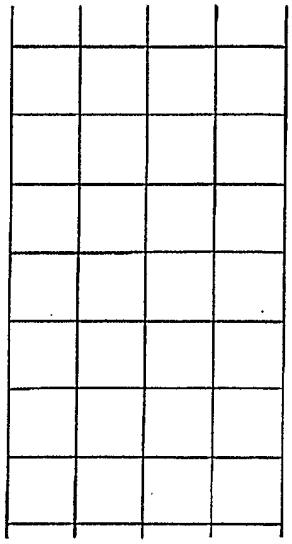

Figure 2b

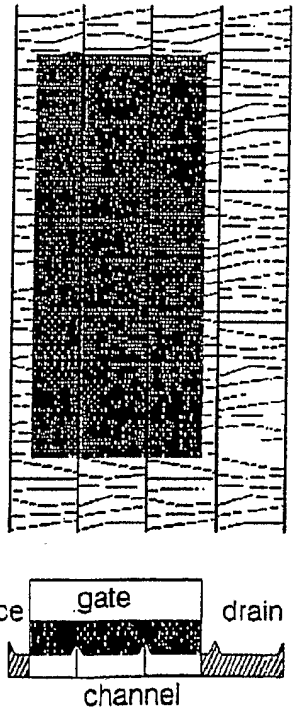

Figure 2c

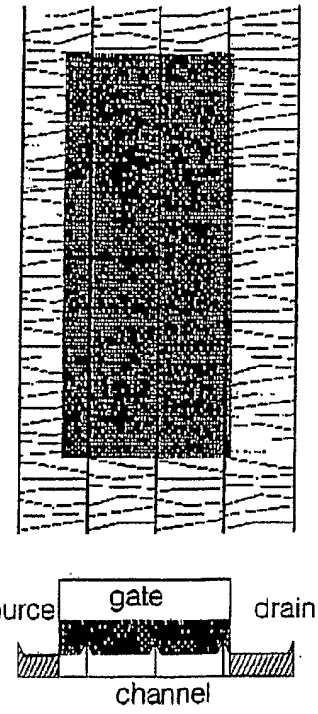

Figure 2d

Fig 3a

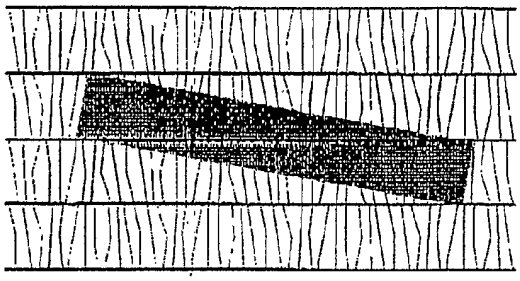

Fig 3b

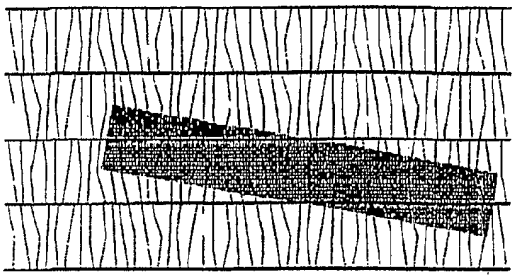

figure 3. n =1 and m = 1, θ = 10°

Fig 4a

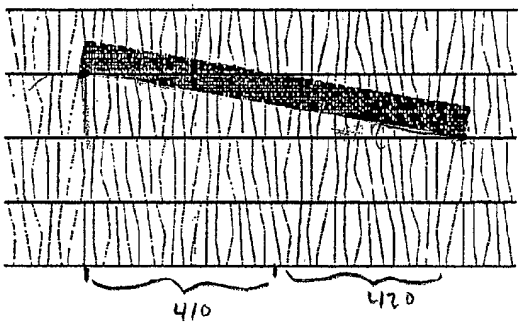

Fig 4b

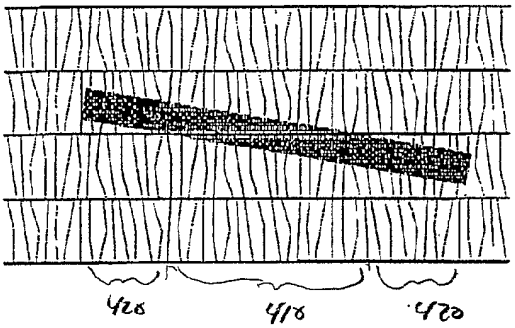

figure 4. n = 0.5, m = 1, θ = 10°

Fig 5a

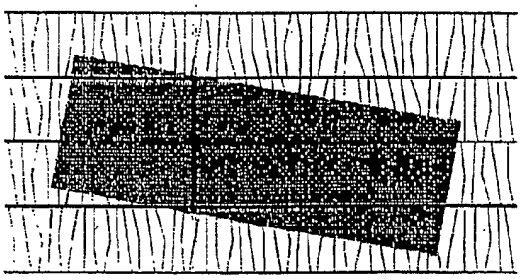

Fig 5b

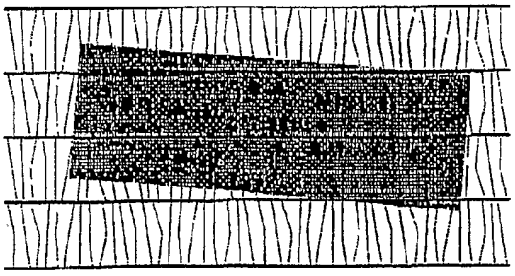

figure 5. left: n = 2.1, m = 1, θ = 10°, right: n = 2.1, m ~ 0.5, θ = 5°

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/27246

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : C30B 13/00
US CL : 117/43
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 117/37, 44, 45, 46, 54, 56, 73, 74, 904, 923; 438/149, 166, 479, 481, 486, 487, 488, 490, 779; 257/45, 75

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A,P	US 6,322,625 B2 (IM) 27 November 2001 (27.11.2001), Figs. 9 and 10 plus description.	1-19
A	US 4,977,104 A (SAWADA et al) 11 December 1990 (11.12.1990), Fig. 8.	1-19
A	US 6,162,711 A (MA et al) 19 December 2000 (19.12.2000), col. 5, lines 39-47.	1-19
A	US 2001/0001745 A1 (IM et al.) 24 May 2001 (24.5.2001), Figs. 9 and 10, and descriptions.	1-19

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
13 November 2002 (13.11.2002)	11 DEC 2002
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