(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(54) Title: A DC-DC CONVERTER WITH AN ACTIVE SNUBBER
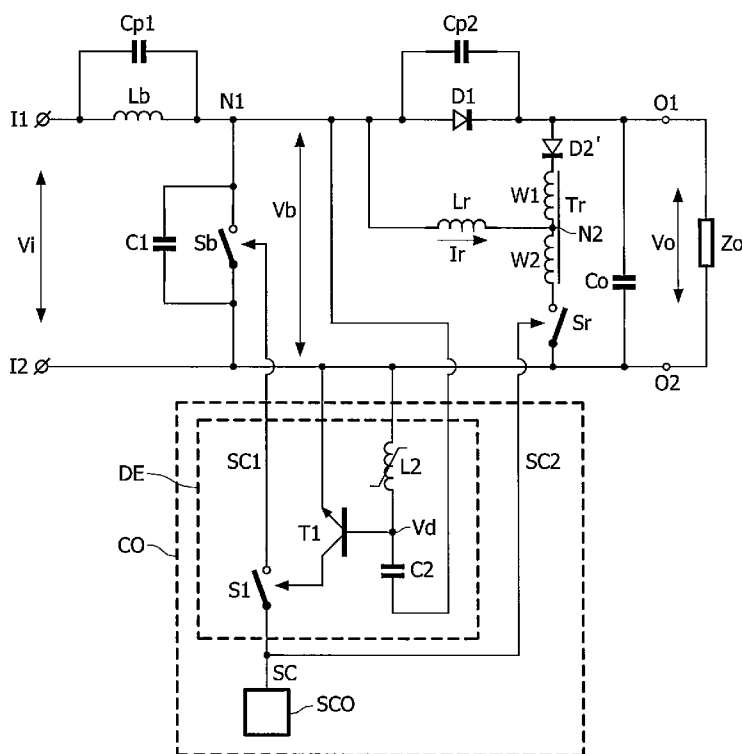
(57) Abstract: A DC-DC converter comprises input terminals (I1, I2) to receive a DC input voltage (Vi), and output terminals (O1, O2) to supply an output voltage (Vo) to a load (Zo). A main inductor (Lb) is coupled to the input terminals (I1, I2), a main electronic switch (Sb) is coupled to the main inductor (Lb) at a first node (N1), and a first rectifier (D1) is coupled between the main inductor (Lb) and at least one of the output terminals (O1, O2). An autotransformer (Tr) has a series arrangement of a first winding (W1) and a second winding (W2). A junction of the first winding (W1) and the second winding (W2) forms a second node (N2) being coupled to the first node (N1). A series arrangement of the second electronic switch (Sr) with the series arrangement of the first winding (W1) and the second winding (W2) is coupled between the output terminals (O1). A second rectifier (D2) is arranged between the first node (N1) and the second node (N2), or is arranged between the one of the first winding (W1) and the second winding (W2) not connected to the second electronic switch (Sr). The second rectifier (D2) is poled to conduct current through the load (Zo) in a same direction as the first rectifier (D1).

A DC-DC CONVERTER WITH AN ACTIVE SNUBBER

Field of the invention

The invention relates to a DC-DC converter with an active snubber, and a power factor corrector comprising such a DC-DC converter.

5 **Background of the invention**

The publication "High Power Factor Soft Switched Boost converter, of Yungtaek Jang et al, IEEE Transactions on Power Electronics Vol. 21, No. 1, January 2006 discloses an implementation of a high power factor boost converter with an active snubber circuit. The snubber circuit reduces the reverse-recovery losses of the rectifier

10 and also provides zero voltage switching for the boost switch and zero-current switching for the auxiliary switch. It is disclosed that at higher power levels, the continuous mode boost converter is the preferred mode of operation for the implementation of a front end with PFC (Power Factor Correction). The active snubber circuit comprises a series arrangement of a diode, a snubber inductor, a primary

15 winding of a transformer and an auxiliary switch. The series arrangement is arranged in parallel with the boost switch. The voltage of the secondary winding of the transformer is rectified and stored in a capacitor. The voltage stored in the capacitor is fed to the output via a further rectifier.

This prior art circuit is relatively complex.

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Summary of the invention

It is an object of the invention to provide a DC-DC converter with a less complex active snubber circuit.

A first aspect of the invention provides a DC-DC converter as claimed in

25 claim 1. A second aspect of the invention provides a power factor corrector as claimed in claim 7. Advantageous embodiments are defined in the dependent claims.

A DC-DC converter in accordance with the first aspect of the invention comprises input terminals to receive a DC input voltage, and output terminals to supply an output voltage to a load. A main inductor is coupled to the input terminals, a main

30 electronic switch is coupled to the main inductor at a first node, and a first rectifier is coupled between the main inductor and at least one of the output terminals. The switch is periodically closed and opened to obtain periods in time during which energy is stored in the inductor and periods in time during which energy is retrieved from the

inductor. The energy stored in the inductor is fed via the first rectifier to the load. The first rectifier may be a single diode or a bridge rectifier. Such DC-DC converters are well known in the art.

The DC-DC converter in accordance with the present invention further comprises an autotransformer with a series arrangement of a first winding and a second winding. A junction of the first winding and the second winding is referred to as a second node. The second node is coupled to the first node. The second node may be coupled directly to the first node, it has to be noted that the leakage inductance of the transformer may be considered to be present between the first and the second node. Alternatively, a lumped inductor may be added between the first and the second node. A series arrangement of the second electronic switch, the first winding and the second winding is coupled between the output terminals.

A second rectifier is arranged either between the first node and the second node, or between the one of the first winding and the second winding which is not connected to the second electronic switch. The second rectifier is poled to conduct current through the load in a same direction as the first rectifier.

By suitably selecting the ratio of turns of the first and the second windings, the voltage difference over the leakage inductance (or over the sum of the leakage inductance and a lumped inductor) is fixed on a desired level when the second electronic switch is closed. The leakage inductance, or the sum of the leakage inductance and the lumped inductor, are further also referred to as the resonance inductance. At the instant the second electronic switch is closed, the current through the resonance inductance starts increasing linearly until the first rectifier stops conducting any current because all the current is flowing through the resonance inductance. Now the resonance inductance starts resonating with (parasitic and lumped) capacitances in the circuit and the voltage on the first node decreases sinusoidal. Thus, as in the prior art, the main electronic switch can be switched on at a low voltage (zero voltage switching). The circuit in accordance with the present invention requires fewer components than the prior circuit. Only the transformer, the second switch and a single diode is required instead of a transformer, the switch, three diodes and a storage capacitor.

In an embodiment, the number of turns of the first winding is substantially identical to a number of turns of the second winding. If the numbers of turns is identical, half the output voltage will be present across the resonance inductance during the period in time the second switch is closed. Consequently the

voltage at the first node will change from approximately Vo (to which the diode forward voltage of the first rectifier is added) to approximately zero (due to losses the zero level may not be reached). However, although preferred, it is not essential that the main electronic switch is switched on at exactly zero voltage across it. Consequently, it is not required that the ratio of the turns is one to one. For example, a ratio in a range from 0,9 to 1,1 appeared to be very acceptable.

In an embodiment, the DC-DC converter further comprises a controller which controls on- and off-periods of the main electronic switch and of the second electronic switch. The second electronic switch is switched on when the main electronic switch is an its off state. A switch is defined to be on when the impedance of its main current path is low, usually in the order of ohms or milliohms. A switch is defined to be off when the impedance of its main current path is high, usually in the order of mega-ohms. Although in the now following is defined that the switch is on when the voltage on its control input has a high level, and that the switch is off when the voltage on its control input has a low level, this is to be understood as a simplification suitable for easy explanation of the operation of the circuit. In an actual implementation it depends on the type of electronic switch used what voltage level is required to have it switched on and off.

In an embodiment, the controller comprises a current sensing circuit for sensing a transformer current flowing into the junction of the first winding and the second winding, or said differently: through the resonance inductance. The transformer current is further also referred to as the resonance current. The controller switches on the main electronic switch at substantially an instant the resonance current becomes zero. In this manner the main electronic switch is switched on when the voltage across it is minimal. The resonance period may be very short with respect to the switching cycle of the main electronic switch to be able to use small components in the active snubber. At such a high frequency, the circuits involved may introduce delay times. Therefore it might be required to detect when the resonance current crosses a predetermined non zero level preceding the zero level to be able to switch the main electronic switch sufficiently on at the instant the resonance current is zero.

In an embodiment, the DC-DC converter is a boost converter wherein the input terminals comprise a first input terminal and a second input terminal and the output terminals comprise a first output terminal and a second output terminal. The main inductor is arranged between the first input terminal and the first node. The main electronic switch is arranged between the first node and the second input terminal. The

first rectifying circuit is arranged between the first node and at least the first output terminal, and the series arrangement of the first winding and the second winding is coupled between the first output terminal and the second output terminal. Especially if the boost converter is operating in the continuous mode as a power factor corrector,

5   the active snubber has a high impact on minimizing losses. Such a power factor corrector may be especially relevant in high power applications, for example operating at high switching frequencies with low EMI (Electro-Magnetic Interference) and low switching losses.

These and other aspects of the invention are apparent from and will be

10   elucidated with reference to the embodiments described hereinafter.

Brief description of the drawings

In the drawings:

Fig. 1 schematically shows a block diagram of an embodiment of a boost

15   converter with an active snubber,

Figs. 2A to 2D schematically show waveforms of signals occurring in the boost converter shown in Fig. 1,

Fig. 3 schematically shows a block diagram of another embodiment of a boost converter with an active snubber, and

20   Figs. 4A to 4C schematically show waveforms of signals relevant for obtaining the control signals for the switches.

It should be noted that items which have the same reference numbers in different Figures, have the same structural features and the same functions, or are the same signals. Where the function and/or structure of such an item has been explained,

25   there is no necessity for repeated explanation thereof in the detailed description.

Detailed description

Fig. 1 shows a block diagram of an embodiment of a boost converter with an active snubber.

30   The boost converter comprises input terminals I1 and I2 at which a DC input voltage Vi is received. The output voltage Vo is supplied to a parallel arrangement of a smoothing capacitor Co and a load Zo. The parallel arrangement is connected between the output terminals O1 en O2. The main inductor Lb is arranged between the input terminal I1 and a node N1. The main current path of the main electronic switch Sb

35   is arranged between the node N1 and the input terminal I2. The first rectifier is a diode

D1 which is arranged between the node N1 and the output terminal O1 whereby its anode is connected to the node N1. Parasitic capacitances Cp1 and Cp2 are present in parallel with the main inductor Lb and the diode D1, respectively. A dV/dt limiting capacitor C1 is arranged in parallel with the main current path of the main electronic

5   switch Sb. The second rectifier is a diode D2 which has an anode connected to the node N1 and a cathode connected to the node N2. The voltage at the node N1 is indicated by Vb.

An autotransformer Tr has a first winding W1 and a second winding W2 which are mutually magnetically coupled and which are arranged in series. A junction

10   of the first winding W1 and the second winding W2 is connected to the node N2. The yet free end of the first winding W1 is connected to the output terminal O1, and the yet free end of the second winding W2 is connected to the output terminal O2 via the main current path of the electronic switch Sr. The leakage inductance of the transformer Tr, or the sum of this leakage inductance and a lumped inductor is indicated by Lr. The

15   current through the resonance inductance Lr is indicated by Ir. The leakage inductance alone if no lumped inductor is present, or the sum of the leakage inductance and the lumped inductor are both referred to as the resonance inductance Lr.

A controller CO supplies a control signal CS1 to the switch Sb and a control signal SC2 to the switch Sr. The operation of the boost converter shown in Fig.

20   1 will be elucidated with respect to the signal waveforms shown in Fig. 2.

Figs. 2A to 2D show waveforms of signals occurring in the boost converter shown in Fig. 1. Fig. 2A shows the on/off state of the switch Sb, and Fig. 2B shows the on/off state of the switch Sr. A high level indicates that the respective switch

25   is on (closed) and a low level that the respective switch is off (open). Fig. 2C shows the current through the resonance inductance Lr, and Fig. 2D shows the voltage at the node N1 which is the voltage across the main switch Sb.

It is assumed that the boost converter is operating in a stable continuous conduction mode, and that at instant t0 both the switches Sb and Sr are open. To

30   simplify the elucidation it is assumed that the forward voltages of the diodes D1 and D2 and the voltage drop across the switches Sb and Sr are zero, and that the number of turns of the windings W1 and W2 are equal. Due to the fact that the number of turns of the windings W1 and W2 are equal, and the fact that the switch Sr is periodically opened and closed, the voltage at the node N2 is equal to ½ Vo (half of the output

35   voltage Vo).

From the instant t0 to the instant t1, the switch Sr is open, the current through the resonance inductance Lr is zero and the current flowing through the main inductor Lb flows via the diode D1 towards the load Zo. The current flowing through the main inductor Lb may be considered to be (almost) constant. The voltage at the node N1 is equal to the output voltage Vo because the diode D1 is conductive.

At the instant t1, the switch Sr is closed and the current Ir through the resonance inductance Lr starts increasing linearly according to ½ Vo / Lr. Because the current through the main inductor Lb is still larger than the current through the resonance inductor Lr, the diode D1 is still conductive and the voltage Vb is still equal to Vo, while on the other hand, the voltage at the node N2 is ½ Vo.

At the instant t2, the current Ir through the resonance inductor Lr becomes equal to the current through the main inductor Lb. Thus, the current through the diode D1 becomes zero and this diode D1 switches off. Now, a resonance period starts which is determined by the resonance inductor Lr and the capacitances C1, Cp1 and Cp2 and which lasts until the instant t4. During the resonance period the current Ir in the resonance inductor Lr changes sinusoidal from a starting value SV at the instant t2 via a maximum value MV at the instant t3 half way the instants t2 and t4 to the starting value SV at the instant t4. The voltage Vb at the node N1 changes sinusoidal and symmetrically around ½ Vo and thus ends at zero volts at the instant t4. Consequently, when the main switch Sb is switched on at the instant t4 the voltage across the main switch Sb is zero.

From instant t4 onward, the voltage Vb will stay at zero volts as long as the main switch Sb is switched on. Because the voltage at node N2 is still ½ Vo, the voltage across the resonance conductance Lr changes polarity and the current Ir through the resonance conductance Lr starts decreasing linearly according to – ½ Vo / Lr and reaches zero at the instant t5. The main switch Sb is switched off at the instant t6 and the switch Sr has to be switched off in the period of time from instant t5 to instant t6. This is indicated by the dotted cross in Fig. 2B. In an embodiment, both switches Sb and Sr are switched off at the same instant t6. At the instant t6, the current flowing in the main inductor Lb starts charging the capacitances C1, Cp1 and Cp2 and the voltage Vb at node N1 rises until the output voltage Vo is reached and the diode D1 starts conducting. The on-period of the switch Sb may be controlled to stabilize the output voltage Vo.

At the instant t2 when the diode D1 switches off, while the current increase through the resonance inductance Lr and thus the current decreased through

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the diode D1 is changing linearly in accordance with ½ Vo / Lr. Thus, the derivative of the current through the diode D1 can be controlled by selecting the value of the resonance inductance Lr. Further, the reverse recovery current of the diode D1 flows into the resonance inductance Lr.

5   It has further to be noted that the current Ir through the resonance inductance Lr divides equally over the windings W1 and W2 if the number of turns are equal. Thus, halve of the current Ir flows to the load Zo via the winding W1.

An advantage of the active snubber circuit in accordance with the invention is that (parasitic and lumped) capacitances in the power converter have a

10   minor effect on the operation of the power converter. Thus, tolerances on the parasitic capacitances of the switch Sb or the diode D1 (or if another type of switch Sb or diode D1 is used with other parasitic capacitance values) do not require a change in the snubber circuit. The duration of the resonant period lasting from instant t2 to instant t4 is relatively short with respect to the switching cycle of the power converter. For

15   example, the resonant period may last approximately 150 ns while the switching cycle takes about 7 μs. Consequently, a change of the resonant period has almost no effect on the operation of the power converter. Further, because the snubber circuit oscillates around ½ Vo, the voltage Vb across the main switch Sb will always reach the substantially zero level, independent on the total value of the capacitors. In fact, only

20   the duration of the resonant part of the voltage Vb varies dependent on the value of the capacitors, the voltage levels of the resonant part do not change. Only the current Ir through the resonance inductance Lr varies with the value of the capacitors.

Fig. 3 shows another embodiment of a boost converter with an active

25   snubber. The boost converter shown in Fig. 3 differs from the boost converter shown in Fig. 1 in that the diode D2 is omitted and a diode D2' is added in series with the winding W1. The cathode of the diode D2' is connected to the output terminal O1. Further, the controller CO now comprises a standard boost converter controller SCO and a delay circuit DE. The delay circuit DE receives the single switch control signal

30   SC of the standard controller SCO and generates the two control signals SC1 and SC2. The basic operation of the boost converter does not change by replacing the diode D2 by the diode D2' and therefore is not elucidated again. Only the construction of the controller CO is further defined with respect to Fig. 3 and its operation is elucidated with respect to Fig. 4.

In the embodiment of the controller CO shown, the control signal SC2 for switching the switch Sr is identical to the switch control signal SC. The control signal SC1 is the control signal SC when the electronic switch S1 is closed. The switch Sb is open as long the switch S1 is open and the switch Sb is closed when the switch S1 is

5   closed and the control signal SC has the high level.

The delay circuit comprises a relatively small capacitor C2 which senses the differentiated voltage Vb at the node N1 and thus the current Ir through the resonance inductor Lr. In a practical implementation, the value of the capacitor C2 may be selected approximately 0.001 times the sum of the capacitor values of the

10   capacitances C1, Cp1 and Cp2. The coil (or more general: inductor) L2 differentiates the sensed current. The series arrangement of the capacitor C2 and the inductor L2 is arranged between the node N1 and the input terminal I2. A transistor T1 has a control input connected to the junction of the capacitor C2 and the inductor L2. The main current path of the transistor T1 is coupled to control the switch S1 which is connected

15   between the output of the standard controller SCO and the control input of the switch Sb.

Figs. 4A to 4C show waveforms of signals relevant for obtaining the control signals for the switches. Fig. 4A and Fig. 4B show the resonant part of the

20   voltage Vb of Fig. 2D and the current Ir of Fig. 2C, respectively. The time instants t1, t2, t3 and t4 are the same as shown in Figs. 2A to 2D. Fig. 4C shows the voltage Vd at the junction of the capacitor C2 and the coil L2.

The switch Sb should be switched on at the instant t4 when the voltage Vb has its minimal value (which is zero if the components have no losses). However, it

25   takes some time for the transistor T1 and the switch Sb to change their conductive state. This time is called the delay time dT. The transistor T1 starts conducting when the voltage Vd reaches the diode forward voltage level V1. The value of the capacitor C2 and the inductor L2 are selected such that the voltage Vd reaches the level V1 at the instant t3' which occurs the delay time dT before the instant t4. The level V1 may

30   be adjustable by moving a core of the inductor L2.

From Fig. 2B it follows that the control signal SC goes high at the instant t1 such that the switch Sr is closed. The delay circuit DE keeps the switch S1 open until a predetermined instant in-between the instant t3' and the instant t4. The predetermined instant is selected such that the switch Sb closes at the instant t4.

It has to be noted that the implementation of the delay circuit shown in Fig. 3 is an exemplary embodiment only. Instead of the bipolar transistor T1 a FET or any other controllable electronic switching element may be used. Alternatively, instead of the bipolar transistor T1, a comparator may be used which compares the voltage Vd

5   with a reference level. The reference level may be adjustable.

By way of example only, in a practical embodiment the main components of the boost converter are:

Lb = 0.4 mH

Lr = 1 to 2 μH

10   W1 : W2 = 1: 1

C2 = 100 pF

L2 = 130 nH

It should be noted that the above-mentioned embodiments illustrate

15   rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims.

For example all the electronic switches (Sb, Sr and S1) may be bipolar transistors, FET's, or any other suitable semiconductor device with a main current path

20   and a control input which controls the impedance of the main current path, such as for example IGBT's.

Although the invention is discussed with respect to a boost converter, the same approach may be implemented in other DC-DC converters.

It has to be noted that for the ease of explanation the invention is

25   elucidated with respect to components which have no losses, and have no other parasitic effects than their parasitic capacitance. Consequently, in an actual implementation more components may be present than shown in the Figures to mitigate at least one of these non-ideal properties of the components. Further, the signal waveforms may deviate from what is shown in the Figures due to these non-

30   ideal properties of the components.

In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. Use of the verb "comprise" and its conjugations does not exclude the presence of elements or steps other than those stated in a claim. The article "a" or "an" preceding an element does not exclude the presence of a

35   plurality of such elements. The invention may be implemented by means of hardware

comprising several distinct elements, and by means of a suitably programmed computer. In the device claim enumerating several means, several of these means may be embodied by one and the same item of hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

CLAIMS

1.   A DC-DC converter comprising:
            input terminals (I1, I2) for receiving a DC input voltage (Vi),
            output terminals (O1, O2) for supplying an output voltage (Vo) to a load
(Zo),
            a main inductor (Lb) coupled to the input terminals (I1, I2),
            a main electronic switch (Sb) coupled to the main inductor (Lb) at a first
node (N1),
            a first rectifier (D1) coupled between the main inductor (Lb) and at least
one of the output terminals (O1, O2),
            a second electronic switch (Sr),
            an auto transformer (Tr) having a series arrangement of a first winding
(W1) and a second winding (W2), a junction of the first winding (W1) and the second
winding (W2) forming a second node (N2) being coupled to the first node (N1), a series
arrangement of the second electronic switch (Sr) with the series arrangement of the
first winding (W1) and the second winding (W2) being coupled between the output
terminals (O1), and
            a second rectifier (D2) arranged between the first node (N1) and the
second node (N2), or arranged between the one of the first winding (W1) and the
second winding (W2) not connected to the second electronic switch (Sr), wherein the
second rectifier (D2) is poled to conduct current through the load (Zo) in a same
direction as the first rectifier (D1).

2.   A DC-DC converter as claimed in claim 1, wherein a number of turns of
the first winding (W1) is substantially identical to a number of turns of the second
winding (W2).

3.   A DC-DC converter as claimed in claim 1 or 2, wherein a further inductor
(Lr) is arranged between the first node (N1) and the second node (N2).

4.   A DC-DC converter as claimed in any one of the preceding claims,
further comprising a controller (CO) for controlling on and off periods of the main
electronic switch (Sb) and the second electronic switch (Sr) for switching the second
electronic switch (Sr) on when the main electronic switch (Sb) is off.

5.   A DC-DC converter as claimed in claim 4, wherein the controller (CO) comprises a current sensing circuit for sensing a transformer current flowing into the junction of the first winding (W1) and the second winding (W2), and wherein the controller (CO) is constructed for switching-on the main electronic switch (Sb) at substantially an instant the transformer current becomes zero.

6.   A DC-DC converter as claimed in any of the preceding claims being a boost converter wherein:

        the input terminals (I1, I2) comprise a first input terminal (I1) and a second input terminal (I2), and the output terminals (O1, O2) comprise a first output terminal (O1) and a second output terminal (O2),

        the main inductor (Lb) is arranged between the first input terminal (I1) and the first node (N1),

        the main electronic switch (Sb) is arranged between the first node (N1) and the second input terminal (I2),

        the first rectifying circuit (D1) is arranged between the first node (N1) and at least the first output terminal (O1), and

        the series arrangement of the first winding (W1) and the second winding (W2) is coupled between the first output terminal (O1) and the second output terminal (O2).

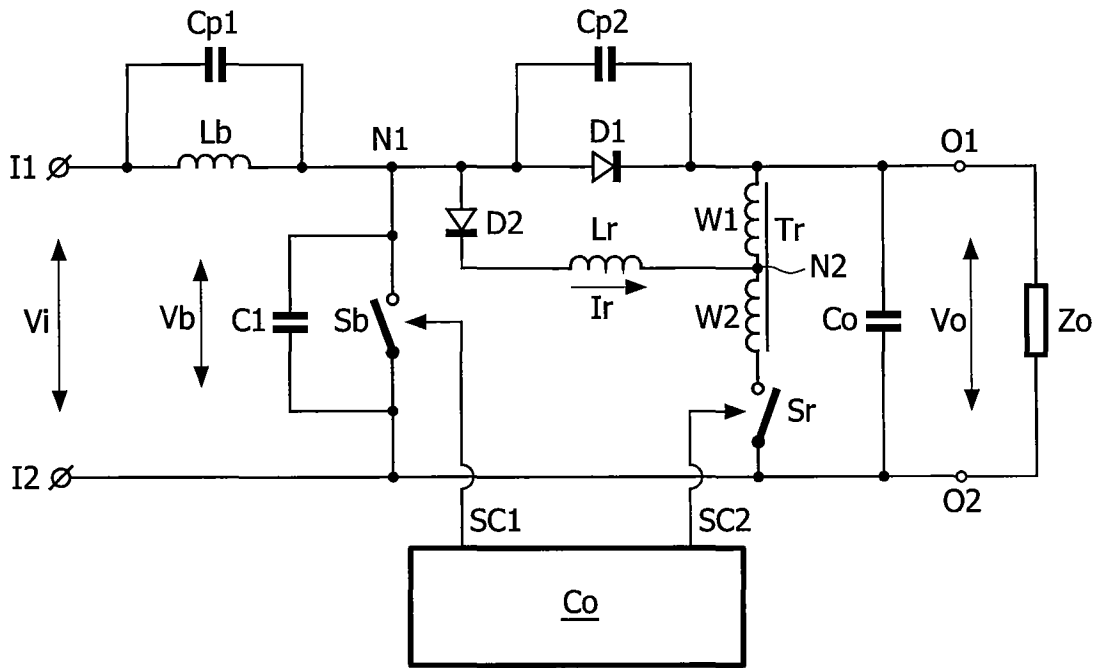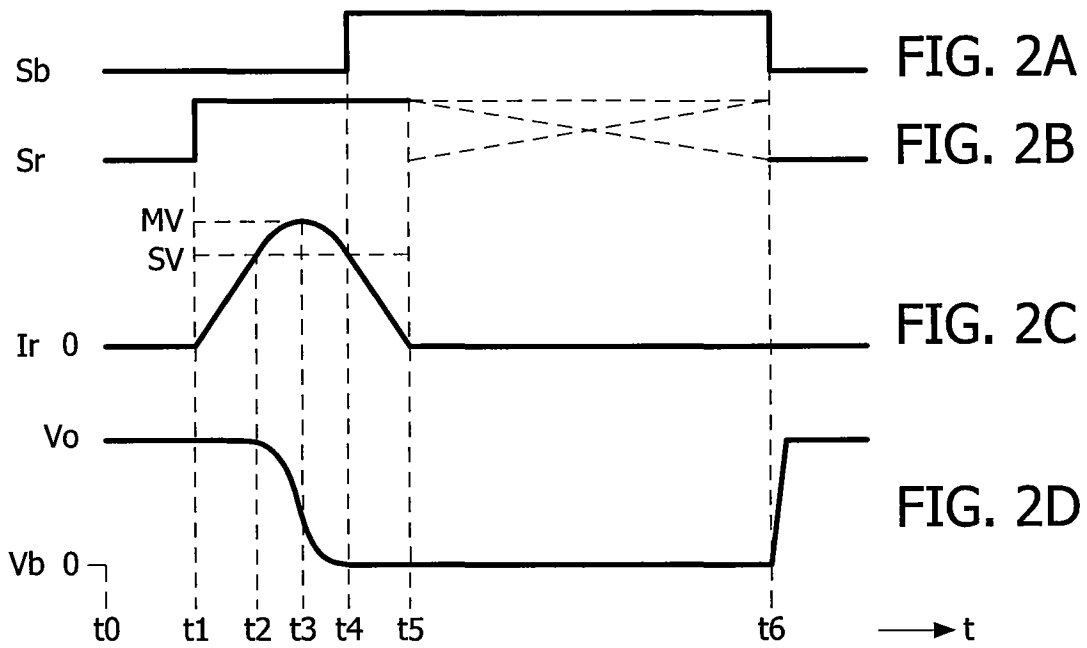7.   A power factor corrector comprising the boost converter as claimed in any of the preceding claims.
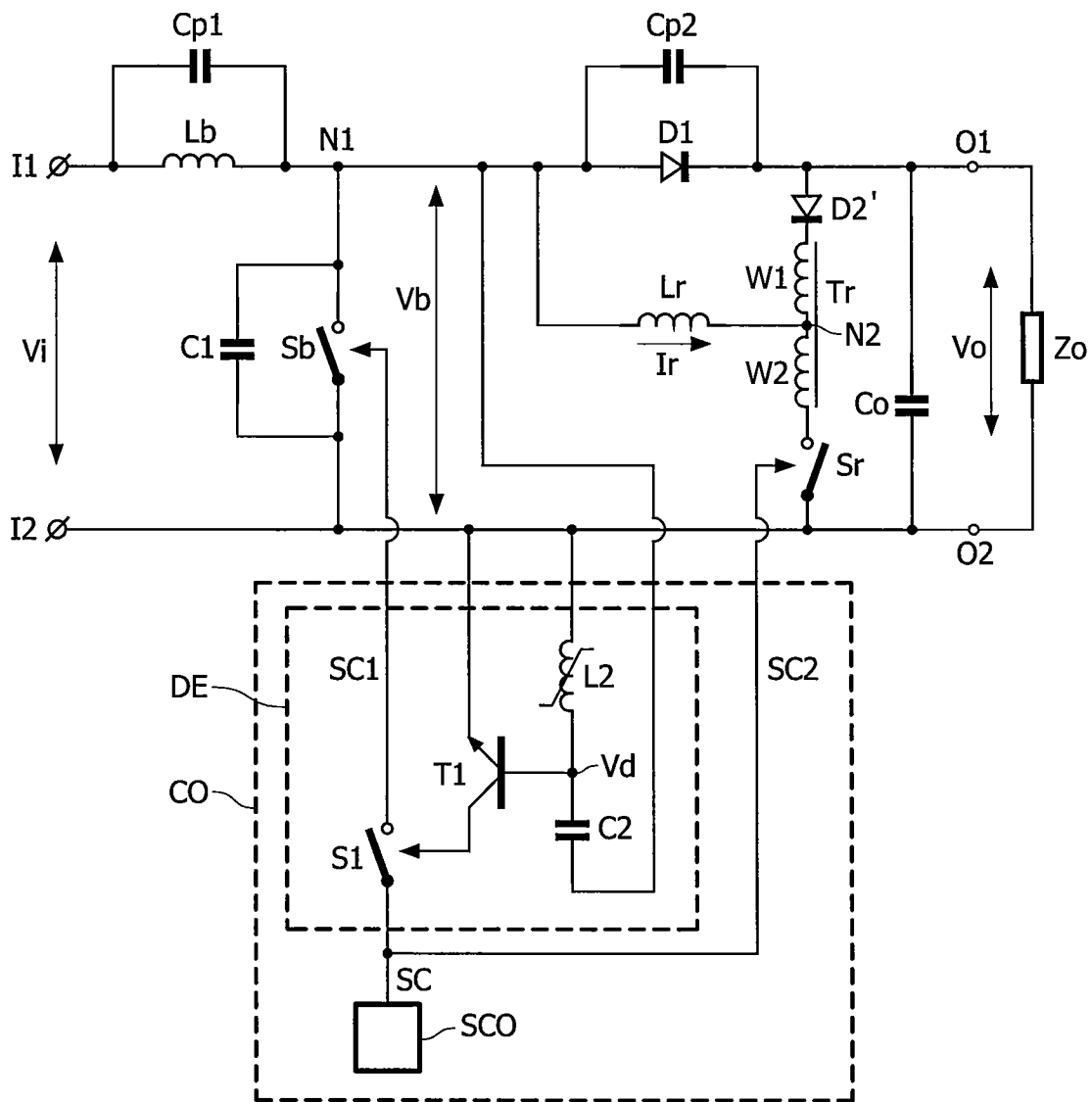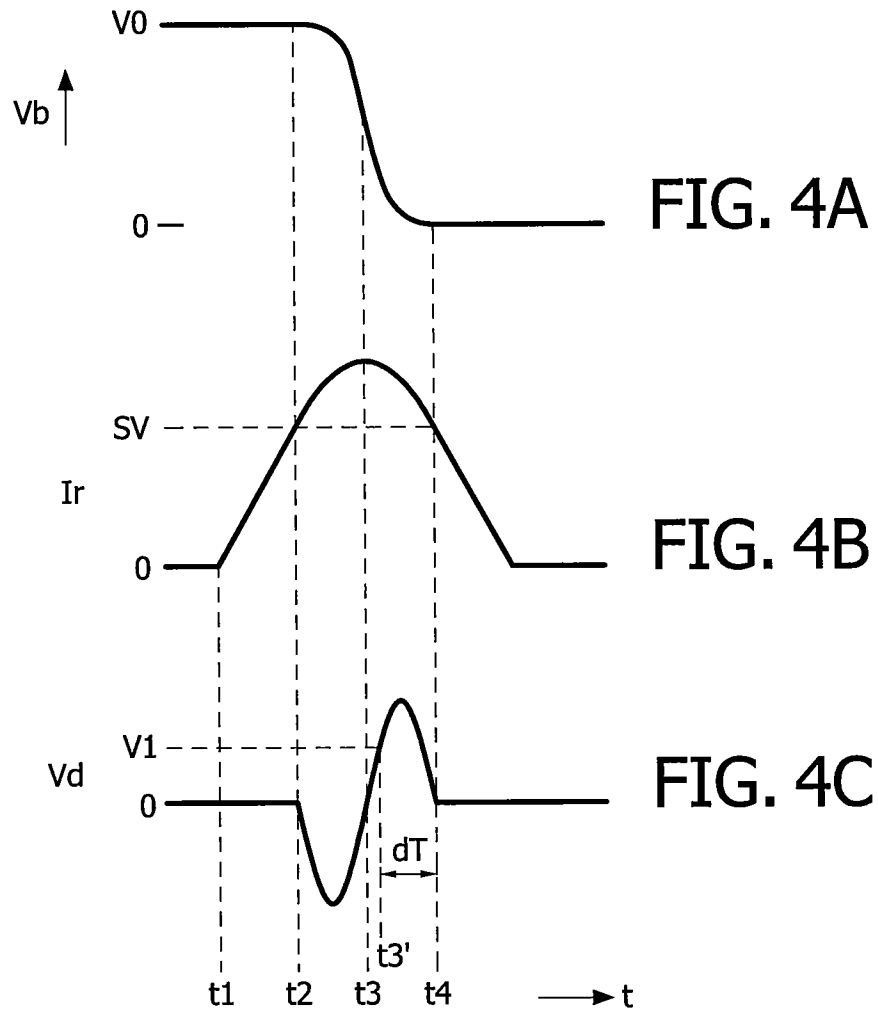
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FIG. 1

FIG. 2A

FIG. 2B

FIG. 2C

FIG. 2D

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FIG. 3

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FIG. 4A

FIG. 4B

FIG. 4C

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M3/158

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DE 10 2004 022136 A1 (DELTA ELECTRONICS INC [TW]) 16 December 2004 (2004-12-16) paragraphs [0015], [0035] figures 1,5	1-7
A	US 6 028 418 A (JOVANOVIC MILAN M [US] ET AL) 22 February 2000 (2000-02-22) abstract figure 1	1-7
A	US 6 236 191 B1 (CHAFFAI RACHID [CA]) 22 May 2001 (2001-05-22) column 2, line 65 - column 3, line 38 figures 3,4	1-7

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| X | Further documents are listed in the continuation of Box C. | X | See patent family annex. |

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

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Date of the actual completion of the international search	Date of mailing of the international search report
11 December 2007	02/01/2008

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Roider, Anton

Form PCT/ISA/210 (second sheet) (April 2005)

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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INTERNATIONAL SEARCH REPORT
Information on patent family members

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