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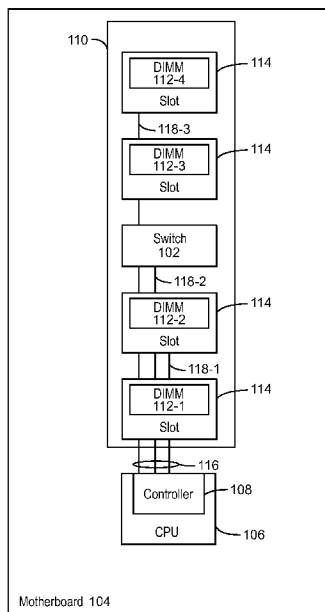
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Declarations under Rule 4.17:

— as to the identity of the inventor (Rule 4.17(i))

[Continued on next page]

(54) **Title:** MODIFICATION OF A BUS CHANNEL



100A
FIG. 1A

(57) **Abstract:** A system and methods related to modification of a bus channel are provided herein. The system may include a processor and a memory controller electrically connected to the processor. The system may include a memory bus and memory slots electrically connected to the memory controller via the memory bus. Each memory slot may include a connector to receive a memory module and to couple the memory module to the memory bus. The system may include at least one switch electrically connected to the memory controller via the memory bus, where the switch is to isolate at least one memory slot from the memory bus.



— *as to applicant's entitlement to apply for and be granted
a patent (Rule 4.17(ii))*

Published:

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MODIFICATION OF A BUS CHANNEL

BACKGROUND

[0001] Electronic components, such as processors, memory modules, controllers, and input/output (I/O) devices, can be electrically connected to a communications bus in a computing system. The number of attached components, the physical configuration of the components with respect to one another, and the speed at which each component operates, among other factors, can limit the speed at which the communications bus operates. The speed of the communications bus refers to the amount of data that can move between the electronic components within a given amount of time. The more data the communications bus can transmit at one particular time, the faster the transmission of data between the components. Thus, computing resources may benefit from communication buses that provide optimal performance speed.

DESCRIPTION OF THE DRAWINGS

[0002] The advantages of the present techniques are better understood by referring to the following detailed description and the attached drawings, in which:

[0003] Fig. 1A is a block diagram of a system including a mounted switch and populated memory slots;

[0004] Fig. 1B is a block diagram of the system including the mounted switch and unpopulated memory slots;

[0005] Fig. 2A is a block diagram of a topology for a motherboard that includes mounted switches;

[0006] Fig. 2B is a block diagram of another topology for the motherboard that includes the mounted switches and a stub connection;

[0007] Fig. 3 is a block diagram of a topology for a motherboard that includes mounted switches and multiple stub connections;

[0008] Fig. 4 is an example of a PIN diode used as a switching mechanism;

[0009] Fig. 5 is a block diagram of a topology for a motherboard that includes switch logic used to configure a PIN diode used as a switching mechanism;

[0010] Fig. 6 is a process flow diagram of a method for manufacturing a system board; and

[0011] Fig. 7 is a block diagram showing a non-transitory, computer-readable medium that stores code configured to reduce the number of loads on a memory bus of a system board.

DETAILED DESCRIPTION

[0012] A bit is a unit of data that can be transferred internally within the circuitry of a computing system and along multiple communication channels. The multiple communication channels, collectively referred to as a communications bus, can transfer data between the various components of the computing system. For example, the computing system may include a memory communications bus to transfer data between a central processing unit (CPU) and a memory module, among other components. However, the number of memory slots and the number of memory modules populated in the memory slots may affect the performance of the bus by increasing capacitive loading. The speed at which the memory communications bus transfers data between the components may decrease, thus reducing the memory bandwidth and degrading the signal integrity of the memory communications bus. Generally, speed and bandwidth are two of the primary factors indicative of the performance level of the memory communications bus.

[0013] Examples described herein provide a system to maintain or improve memory bus performance. The system can include components mounted on a motherboard, including a processor, a memory controller, memory slots, memory modules, a memory bus, and one or more switches, among others. The memory modules may populate the memory slots that may be electrically connected to the memory bus. The switches may be mounted adjacent to the memory modules and connected to the memory bus. The placement of the switches may reconfigure the memory bus by disconnecting at least

one memory slot from the memory bus to electrically isolate a memory module populated in the at least one memory slot.

[0014] Fig. 1A is a block diagram of a system 100A including a mounted switch 102 and populated memory slots. The system 100A may be a server, personal computer, mobile computing device, and the like. A motherboard 104 may provide a foundation for the system 100A on which various electronic components are mounted and electrically connected to one another. As shown in Fig. 1A, the motherboard 104 may enable communication between electronic components including a CPU 106 with a memory controller 108, a RAM device 110 including DIMMs 112-1 to 112-4, and the switch 102. The motherboard board 104 may include additional components to perform various system functionalities. However, for simplicity, components related to the memory function of the system 100A are illustrated in Fig. 1A.

[0015] The CPU 106 includes circuitry used to execute stored instructions, for example, memory data stored in the RAM device 110. The CPU 106 can be a single core processor, a multi-core processor, a computing cluster, or any number of other configurations. The memory controller 108 may be integrated into the CPU 106 to control the RAM device 110, as shown in Fig. 1A. In other examples, the memory controller 108 may be a separate circuit chip or integrated into the RAM device 110, among other configurations. The memory controller 108 may manage the flow of data between the RAM device 110 and the CPU 106.

[0016] The DIMMs 112-1 to 112-4 may be composed of several RAM integrated circuits mounted on small-scale circuit boards. Each DIMM 112-1 to 112-4 can be inserted into a memory slot 114 mounted on the motherboard 104. The DIMMs 112-1 to 112-4 may incorporate volatile memory, for example, dynamic random access memory (DRAM) or synchronous DRAM (SDRAM). The DIMMs 112-1 to 112-4 may act as the main memory of the system 100A to store and transfer data including programs, applications, and other data to be executed by the CPU 106. In other examples, the RAM device 110 may be configured with other types of memory modules, such as double data rate fourth generation (DDR4) RAM or Single In-Line Memory Modules (SIMMs), among others.

[0017] A memory bus 116 may enable the communications between the DIMMs 112-1 to 112-4 and the CPU 106 using parallel wires, herein referred to as channels 118-1 to 118-3. As shown in Fig. 1A, the channels 118-1 to 118-3 may physically connect the memory controller 108 to the memory slots 114 to transmit bus signals, *e.g.*, memory data, to and from the DIMMs 112-1 to 112-4. The channels 118-1 to 118-3 may perform other functions such as determining the amount of data and the speed of the data transferred between the DIMMs 112-1 to 112-4 and the CPU 106.

[0018] The performance of the memory bus 116 may be directly related to the number of DIMMs 112-1 to 112-4 on each channel 118-1 to 118-3. For example, increasing the number of memory modules, or even the existing memory modules, on the memory bus 116 may slow the electrical transitions, such as voltage, frequencies, and so forth, on the bus 116. The delay may increase the capacitive load on the memory bus 116. Consequently, reductions in the bandwidths, the signal integrity and the transmission speeds of the memory bus 116 may decrease performance factors. If the reduction continues, the performance of the system 100A may also decrease. The capacitive load may include the sum of the input capacitance of all of the DIMMs 112-1 to 112-4 on the channels 118-1 to 118-3.

[0019] The switch 102 may be configured in a default-closed configuration so that signals can flow through it. However, when configured to an open position, the switch 102 may create a gap in the circuitry of the system 100A by inhibiting transmission of the signals. In other words, the switch 102 in an open position may act as a termination end-point to discontinue the routing of bus signals along the memory bus 116 with minimum bouncing, noise, and other signal interferences.

[0020] The memory bus 116 may electrically connect the switch 102 to the DIMMs 112-1 to 112-4, the CPU 106, and other components on the motherboard 104. The switch 102 may be mounted on the channels 118-1 to 118-3 along with the DIMMs 112-1 to 112-4, however, the number and the location of the switch 102 may vary based on manufacturer specifications.

[0021] The switch 102, when configured to an open position, may reconfigure the memory bus 116 by reducing the number of DIMMs, memory slots, or both, electrically

connected to the bus 116. In the present examples, an end-user may use the switch 102 to remove the DIMMs 112-3 and 112-4 electrically from the channel 118-3. The switch may receive bus signals routed on the memory bus 116 before the DIMMs 112-3 and 112-4 receive the bus signals. Due to the open position of the switch 102, the bus signals may be prevented from continuing along the memory bus 116. In this manner, the DIMMs 112-3 and 112-4 may be disconnected so as to not receive the routed bus signals from the memory bus 116.

[0022] Although physically present on the memory bus 116, the disconnected DIMMs 112-3 and 112-4 may be electrically removed to reduce the capacitive load on the channel 118-3 and thus, on the memory bus 116. The connected DIMMs 112-1 and 112-2 may operate at an increased bandwidth to maintain or improve the electrical characteristics and performance of the memory bus 116, the system 100A, or both. Since the switch 102 may have a low capacitance, it may be positioned on the motherboard 104 to directly receive signals for the memory controller 108 to improve the electrical characteristics of the circuitry in the system 100A.

[0023] Fig. 1B is a block diagram of the system 100B including the mounted switch 102 and unpopulated memory slots. Like numbered items are as described with respect to Fig. 1A. As shown in Fig. 1B, the system 100B may operate at less than optimal memory capacity, for example, when only the memory slots 114-1 and 114-2 are populated. However, the unpopulated memory slots 114-3 and 114-4 that continue to receive routed bus signals create an additional capacitive load on the memory bus 116. The additional capacitive load may delay the electrical characteristics of the memory bus 116. Consequently, transmission speeds and the speed at which the CPU 106 executes instructions may decrease the performance of the bus 116, the system 100B, and possibly other components on the motherboard 104.

[0024] To reduce the capacitive load, the switch 102 may be mounted on the memory bus 116 to isolate the unpopulated memory slots 114-3 and 114-4 electrically from the routed bus signals. Specifically, the switch 102 may receive signals routed on the memory bus 116 before the signals reach the unpopulated memory slots 114-3 and 114-4. However, the bus signals may terminate at the switch 102 when configured to

an open position to prevent the flow of current further along the memory bus 116.

Although the unpopulated memory slots 114-3 and 114-4 remain physically mounted on the motherboard 104, the slots 114-3 and 114-4 may be electrically disconnected from the memory bus 116. The electrical isolation of the slots 114-3 and 114-4 may reduce the capacitive load and improve the electrical characteristics of the memory bus 116.

[0025] The switch 102 can be controlled by firmware, such as basic input/output system (BIOS) firmware 120, located in a ROM device 122 electrically connected to the CPU 106. The firmware 120 may control the switch 102 to operate in an opened position to prevent the flow of current through the switch 102. However, with respect to Fig. 1B, an end-user may desire to mount DIMMs in the unpopulated memory slots 114-3 and 114-4 to increase memory capacity of the system 100B. Once populated, the BIOS firmware 120 may configure the switch 102 to a closed position to allow routed bus signals to pass through the switch 102 in order to electrically connect the memory slots 114-3 and 114-4 with the memory bus 116.

[0026] In examples, the switch 102 may support the bandwidth frequencies and additional electrical characteristics of the memory bus 116. In particular, the switch 102 may provide the appropriate bandwidth frequencies to allow the routed bus signals to pass from one component to another on the motherboard 104 while maintaining or increasing the performance of the memory bus 116. The switch 102 may include a device to enable switching between applications, an analog cross circuit switch, a PIN diode, a FET-based switching technology, or other components that can behave as an isolation feature to inhibit the flow of electricity in the circuitry of the system 100B.

[0027] Fig. 2A is a block diagram of a topology 200A for a motherboard 202 that includes mounted switches. For example, the electrical components may include several DIMMs 204-1 to 204-4, 206-1 to 206-4 mounted on opposite sides of a CPU 208, respectively. The DIMMs 204-1 to 204-4, 206-1 to 206-4 may store volatile memory data for the system 200A. A memory bus 210 may enable the transfer of the data between the DIMMs 204-1 to 204-4, 206-1 to 206-4, the CPU 208, and other electrical components on the motherboard 202. In the present examples, the memory bus 210 may be made of parallel wires, such as channels 212-1 to 212-3, that can

electrically transmit data between the DIMMs 204-1 to 204-4, 206-1 to 206-4 and the CPU 208.

[0028] Switches 214 may be mounted on both sides of the CPU 208 and adjacent to the DIMMs 204-1 to 204-4, 206-1 to 206-4. The configuration of the electrical components mounted each side of the CPU 208 may be identical, as illustrated in Fig. 2A. In other examples, the configuration of the electrical components on each side of the CPU 208 may vary based on the specifications of a manufacturer, an end-user, or both.

[0029] As previously discussed, additional DIMMs connected to the memory bus 210 may decrease transmission speeds. The transmission speeds may also decrease due to the number of existing DIMMs 204-1 to 204-4, 206-1 to 206-4 on the memory bus 210. However, the mounting of the switches 214 on the motherboard 202 may reduce the capacitive load on the memory bus 210 by electrically removing one or more DIMMs. For instance, the switches 214 configured in an open position may electrically isolate and prevent the transmission of routed bus signals to the DIMMs 204-4 and 206-4. In this manner, the electrically disconnected DIMMs 204-4 and 206-4 may not receive the routed bus signals transmitted on the memory bus 210. The electrical isolation of the DIMMs 204-4 and 206-4 may reduce the capacitive load and improve the electrical characteristics of the memory bus 116. Consequently, the performance of the memory bus 210 may be improved or maintained since a lower number of DIMMs, *i.e.*, DIMMs 204-1 to 204-3, 206-1 to 206-3, may be electrically connected within the system 200A.

[0030] Fig. 2B is a block diagram of another topology 200B for the motherboard 202 that includes the mounted switches 214 and stub connections. Like numbers are as described with respect to Fig. 2A. The DIMMs 204-3 and 206-3 may form stub connections 216-1 and 218-1 on the channel 212-3. The stub connections 216-1 and 218-1 may include an interconnection that branches off the memory bus 210.

[0031] While multiple stub connections may increase memory capacity, the addition of the stub connections 216-1 and 218-1 may also increase the capacitive load on the memory bus 210 to produce an impedance mismatch. The mismatch may produce

electrical reflections that may degrade bus signals and thus, inhibit the performance of the memory bus 210. The switches 214 configured in an opened position may electrically disconnect the stub connections 216-1 and 218-1 so that the routed bus signals fail to reach the DIMMs 204-3 and 206-3. In this way, the electrical isolation of the DIMMs 204-3 and 206-3 may reduce or alleviate the mismatch to reduce the capacitive load created by the stub connections 216-1 and 218-1. By improving the integrity of the routed bus signals, the bandwidth efficiency of the memory bus 210 may increase to provide optimal performance of the system 200B.

[0032] Fig. 3 is a block diagram a topology 300 for a motherboard 302 that includes mounted switches 304 and multiple stub connections 306-1 to 306-3 and 308-1 to 308-3. The length of the stubs connections 306-1 to 306-3 and 308-1 to 308-3 may increase the capacitive load on the memory bus 310 that may cause slower transmission speeds. To remove the additional loads created by the stub connections 306-1 to 306-3 and 308-1 to 308-3, the DIMMs 310-1, 310-3, 310-5 and 312-1, 312-3, 312-5 may be electrically disconnected from the memory bus 310. Since routed bus signals transmitted on the memory bus 310 may terminate at the switches 304, the DIMM 310-1, 310-3, 310-5 and 312-1, 312-3, 312-5 may not affect signal frequencies and reduce the capacitive loading. The remaining electrically connected DIMMs 310-2, 310-4, 310-6 and 312-2, 312-4, 312-6 may operate at an increased bandwidth to maintain or improve the electrical characteristics and performance of the memory bus 310.

[0033] Fig. 4 is an example of a PIN diode 402 used as a switching mechanism. The PIN diode 402 is a semiconductor device that operates as a variable resistor at radio frequencies (RF) and microwave frequencies. Generally, the resistance of the PIN diode 402 may vary depending on the amount of current that may flow through it, for example, from less than 1 ohm (Ω) (forward biased or "ON") to more than 10 kilo-ohm ($k\Omega$) (reverse biased or "OFF"). Accordingly, when used as a switch, the PIN diode 402 may implement logic to switch its control current between ON and OFF modes. In the ON mode, the PIN diode 402 as a switch may be designed to have the least possible loss, *e.g.*, reduced isolation, of an input bus signal. In the OFF mode, the PIN diode 402 as a switch may exhibit a high loss, *e.g.*, isolation, to an input bus signal.

[0034] The selection of the PIN diode 402 as a switching mechanism may be due to its high-switching speeds, low capacitance, and low frequency limit, among others. As shown in Fig. 4, the PIN diode 402 may be electrically connected to a controller 406 embedded in a CPU 408 and memory modules 410 and 412, such as DIMMs, as will be further described with respect to Fig. 5.

[0035] Fig. 5 is a block diagram of a topology 500 for a motherboard 502 that includes switch logic 504 used to configure the PIN diode 402 of Fig. 4 as a switching mechanism. Like numbered items are as described with respect to Fig. 4. The switch logic 504 shown in Fig. 5 may indicate the location of a mounted PIN diode, such as the PIN diode 402 of Fig. 4. DIMMs 506-2, 506-3, 506-5, 506-6, 508-2, 508-3, 508-5, and 508-6 may be electrically connected to CPU 510 and the switch logic 504 via memory bus 512. Specifically, the DIMMs 506-2, 506-3, 506-5, 506-6, 508-2, 508-3, 508-5, and 508-6 may form various stub connections 514-1 to 514-4 and 516-1 to 516-4, as shown in Fig. 5.

[0036] To remove the additional loads created by the stub connections 514-1 to 514-4 and 516-1 to 516-4, the DIMMs 506-2, 506-3, 506-5, 506-6, 508-2, 508-3, 508-5, and 508-6 may be electrically disconnected from the memory bus 512. In particular, the switch logic 504 mounted on the motherboard 502 may control the flow of bus signals transmitted by the memory bus 512. The switch logic 504 may switch the PIN diodes to an OFF mode to terminate routed bus signals. Accordingly, the bus signals may not flow pass the PIN diodes 402 but terminate at the switch logic 504. Since the memory bus 512 and the DIMMs 506-2, 506-3, 506-5, 506-6, 508-2, 508-3, 508-5 may not be electrically connected, the signal frequencies and the capacitive loading of the memory bus 512 may be reduced. The remaining electrically connected DIMMs 506-1, 506-4, 508-1, and 508-4 may operate at an increased bandwidth to improve the electrical characteristics and performance of the memory bus 510.

[0037] Fig. 6 is a block diagram of a method 600 of manufacturing a system board. At block 602, the method 600 may include positioning at least one memory modules in memory slots located on the system board. The memory slots may receive bus signals from a memory controller on a memory bus. The system board may be located in a

computing device such as a server, computer, mobile devices, and the like. The memory modules may include DIMMs, SIMMs, DDR4 RAM devices, and so forth.

[0038] At block 604, the method 600 may position at least one switch on the system board. The switch may be coupled, via the memory bus, to at least one memory slot that can be populated with a memory module. The method may include using the switch to isolate the at least one memory slot from the bus signals. In some examples, the use of the switch may control system capacitance and bandwidth to maintain or improve performance of the memory bus, the system board, or both.

[0039] Fig. 7 is a block diagram of a system 700 that includes a non-transitory, computer-readable medium 702 that stores code configured to reduce the number of loads on a memory bus of a system board. In particular, an increased capacitive load on the memory bus may reduce the transmission speeds, the signal integrity, and the bandwidth of the memory bus. However, the mounting of switches on the system board may reduce the capacitive load to provide improved memory bus performance. The computer-readable medium 702 can include RAM, such as DRAM or SRAM. A processor 704 may access the computer-readable medium 702 over a memory bus 706. In examples, the processor 704 may include code configured to perform methods described herein.

[0040] Various software components discussed herein may be stored on the computer-readable medium 702. The software components may include various modules to disconnect and electrically remove memory slots from the memory bus. An identify module 708 may identify at least one memory slot coupled on a memory bus that is to be disconnected and electrically removed from the memory bus. An isolation module 710 may isolate the at least one identified memory slot by routing bus signals to a switch coupled on the memory bus. The bus signals may terminate at the switch when positioned in an open position so that the at least one memory slot fails to receive the bus signals.

[0041] While the present techniques may be susceptible to various modifications and alternative forms, the embodiments discussed above have been shown only by way of example. However, it should again be understood that the techniques is not intended to

be limited to the particular embodiments disclosed herein. Indeed, the present techniques include all alternatives, modifications, and equivalents falling within the true spirit and scope of the appended claims.

CLAIMS

What is claimed is:

1. A system comprising:
a processor;
a memory controller electrically connected to the processor;
a memory bus;
a plurality of memory slots electrically connected to the memory controller via the memory bus, wherein each memory slot comprises a connector to receive a memory module and to communicatively couple the memory module to the memory bus; and
at least one switch electrically connected to the memory controller via the memory bus, wherein the switch is to isolate at least one memory slot from the memory bus.
2. The system of claim 1, wherein the at least one switch is to receive signals routed on the memory bus before the at least one memory slot receives the signals.
3. The system of claim 1, wherein signals routed on the memory bus terminates at the at least one switch, wherein the at least one switch operates in an open position.
4. The system of claim 1, wherein the at least one memory slot is disconnected from the memory bus when the at least one switch receives signals routed on the memory bus before the at least one memory slot receives the signals, wherein the at least one switch operates in an open position.
5. The system of claim 1, wherein a memory slot disconnected from the memory bus is electrically unavailable to receive signals routed on the memory bus.

6. The system of claim 1, wherein the at least one switch is positioned to directly receive signals from the memory controller on the memory bus.

7. The system of claim 1, wherein the at least one switch comprises a device to enable switching between applications, an analog cross circuit switch, a PIN diode, or an FET based switching feature, in any combination, thereof.

8. A method of manufacturing a system board comprising:
positioning at least one memory module in memory slots located on the system board, wherein at least one memory slot is to receive signals from a memory controller on a memory bus; and
positioning at least one switch on the system board, wherein the switch is coupled to the at least one memory slot via the memory bus, and wherein the switch is to isolate the at least one memory slot from the signals.

9. The method of claim 8, positioning the at least one switch to receive the signals before the at least one memory slot receives the signals.

10. The method of claim 8, comprising configuring the at least one switch to an open position to prevent transmission of the signals to the at least one memory slot.

11. The method of claim 8, wherein the at least one memory slot is electrically removed and disconnected from the memory bus when isolated.

12. The method of claim 8, wherein performance of the memory bus is improved when the at least one memory slot fails to receive the signals.

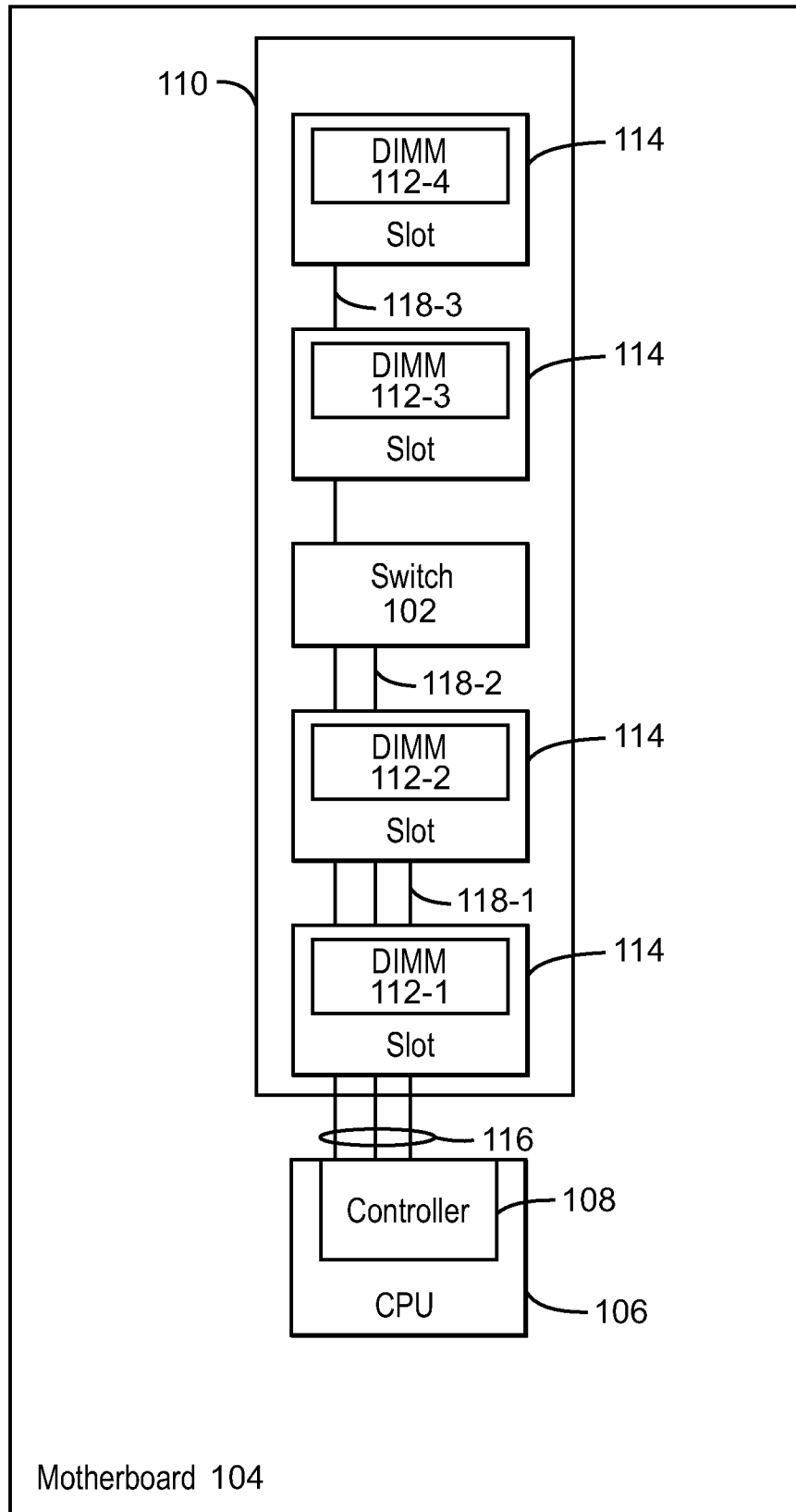
13. A non-transitory, computer-readable medium, comprising code configured to direct a processor to:

identify at least one memory slot coupled on a memory bus that is to be electrically removed; and
isolate the at least one identified memory slot from bus signals by routing bus signals to a switch coupled on the memory bus, wherein the bus signals terminate at the switch, and wherein the at least one identified memory slot fails to receive the bus signals.

14. The non-transitory, computer-readable medium of claim 13, comprising code configured to direct the processor to detect that the at least one identified memory slot is populated with a memory module, empty, or both.

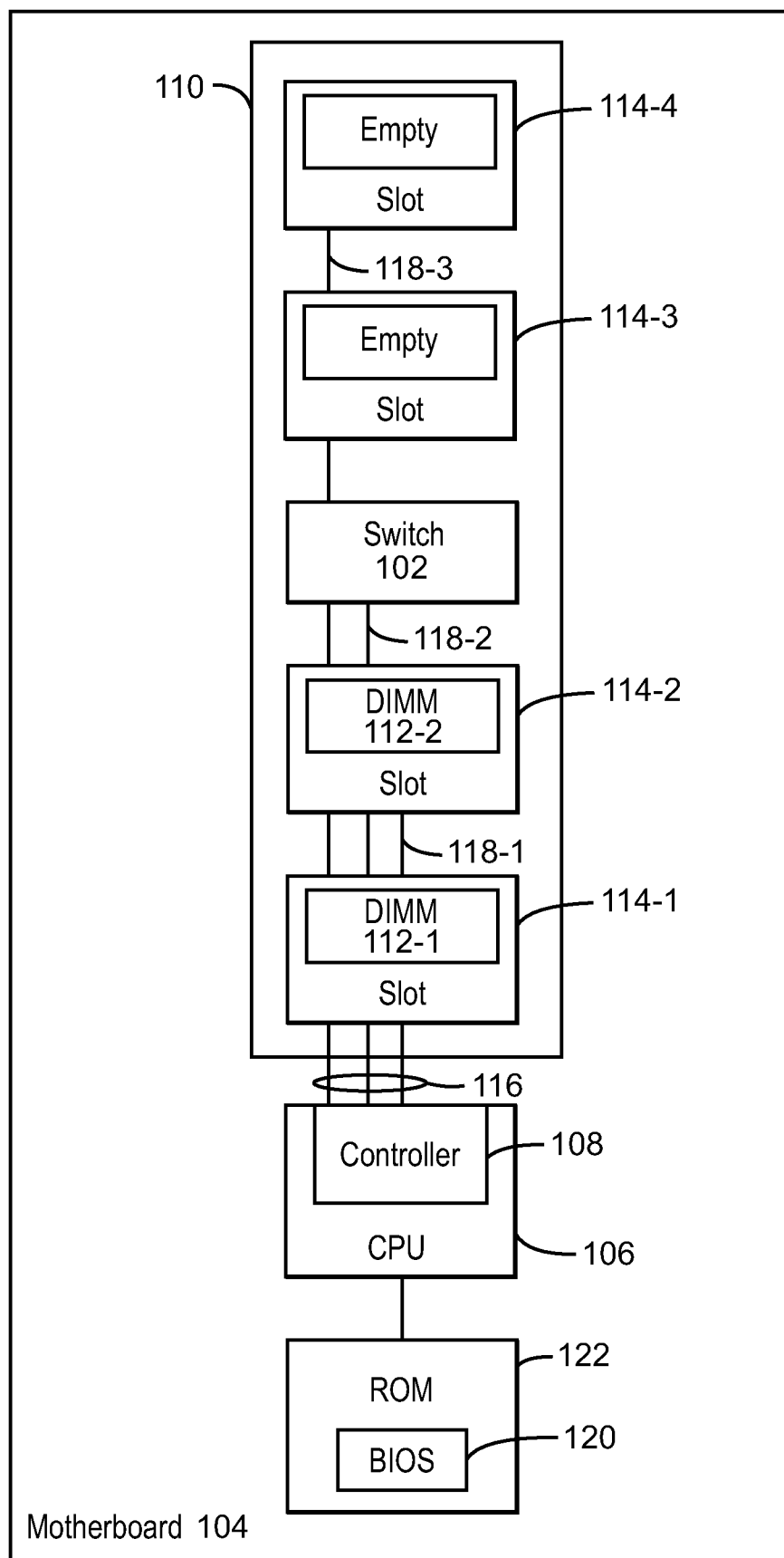
15. The non-transitory, computer-readable medium of claim 13, wherein the switch receives the bus signals before the at least one identified memory slot receives the bus signals.

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100A
FIG. 1A

2/9



100B

FIG. 1B

3/9

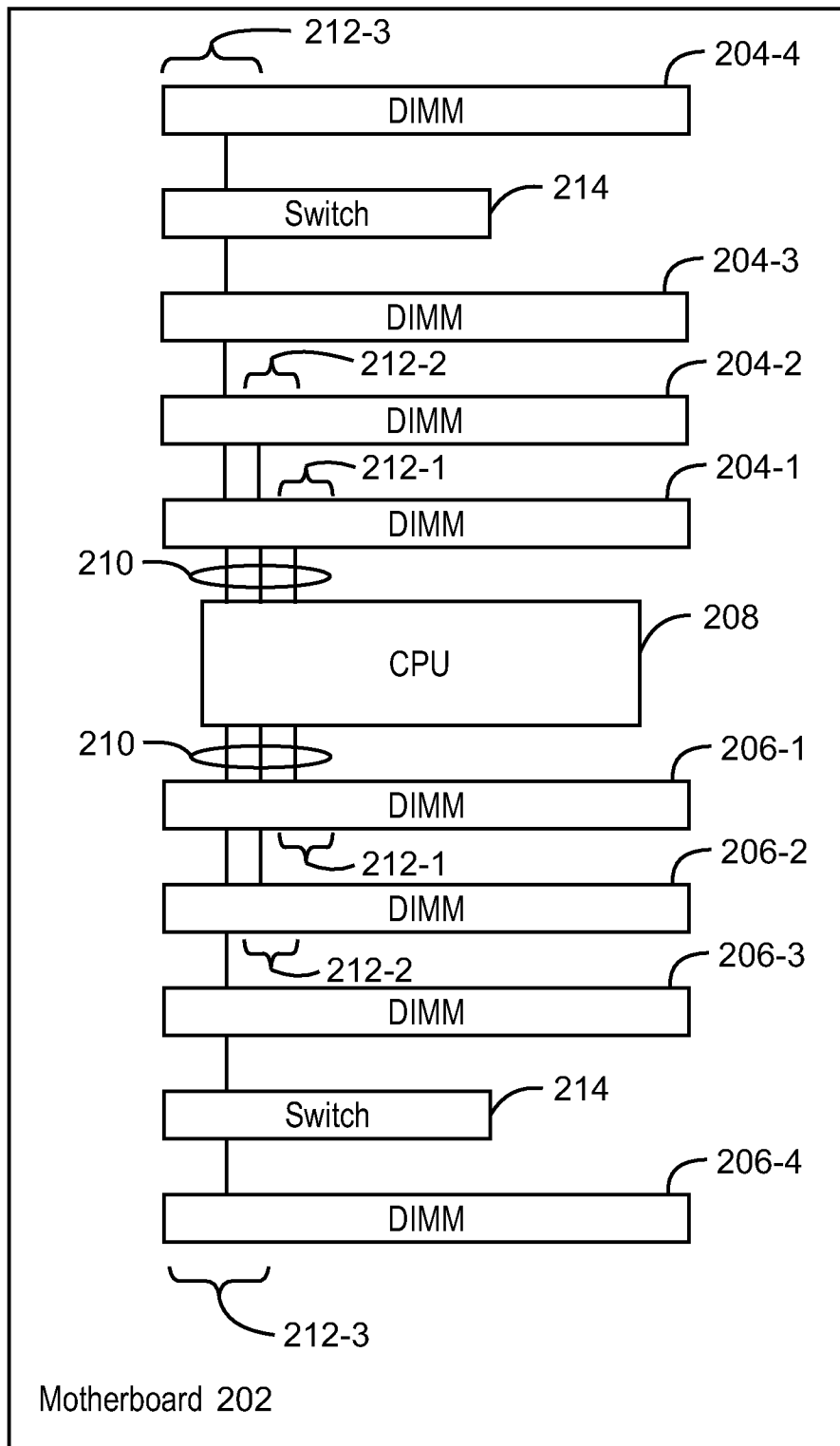
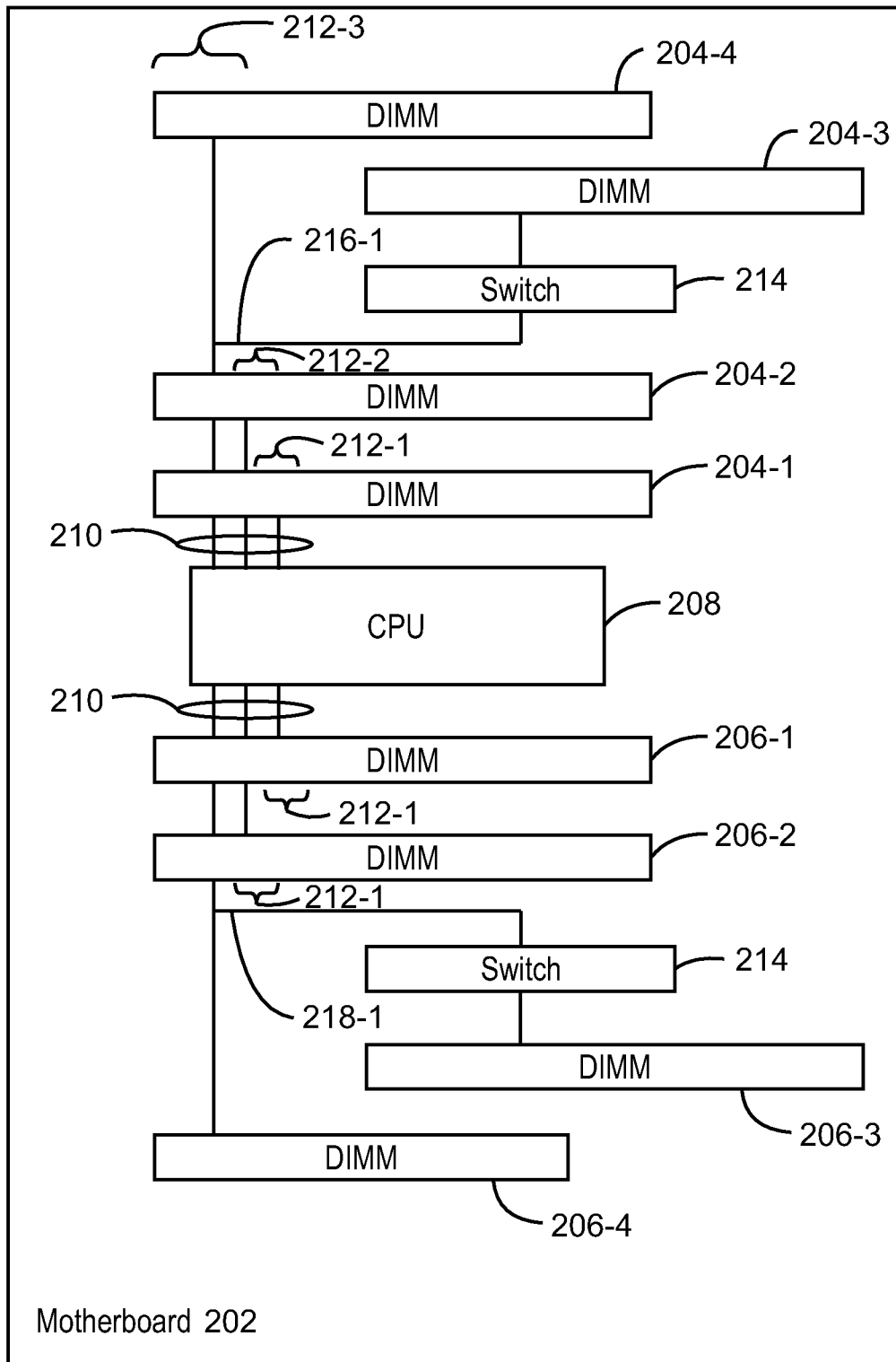
200A

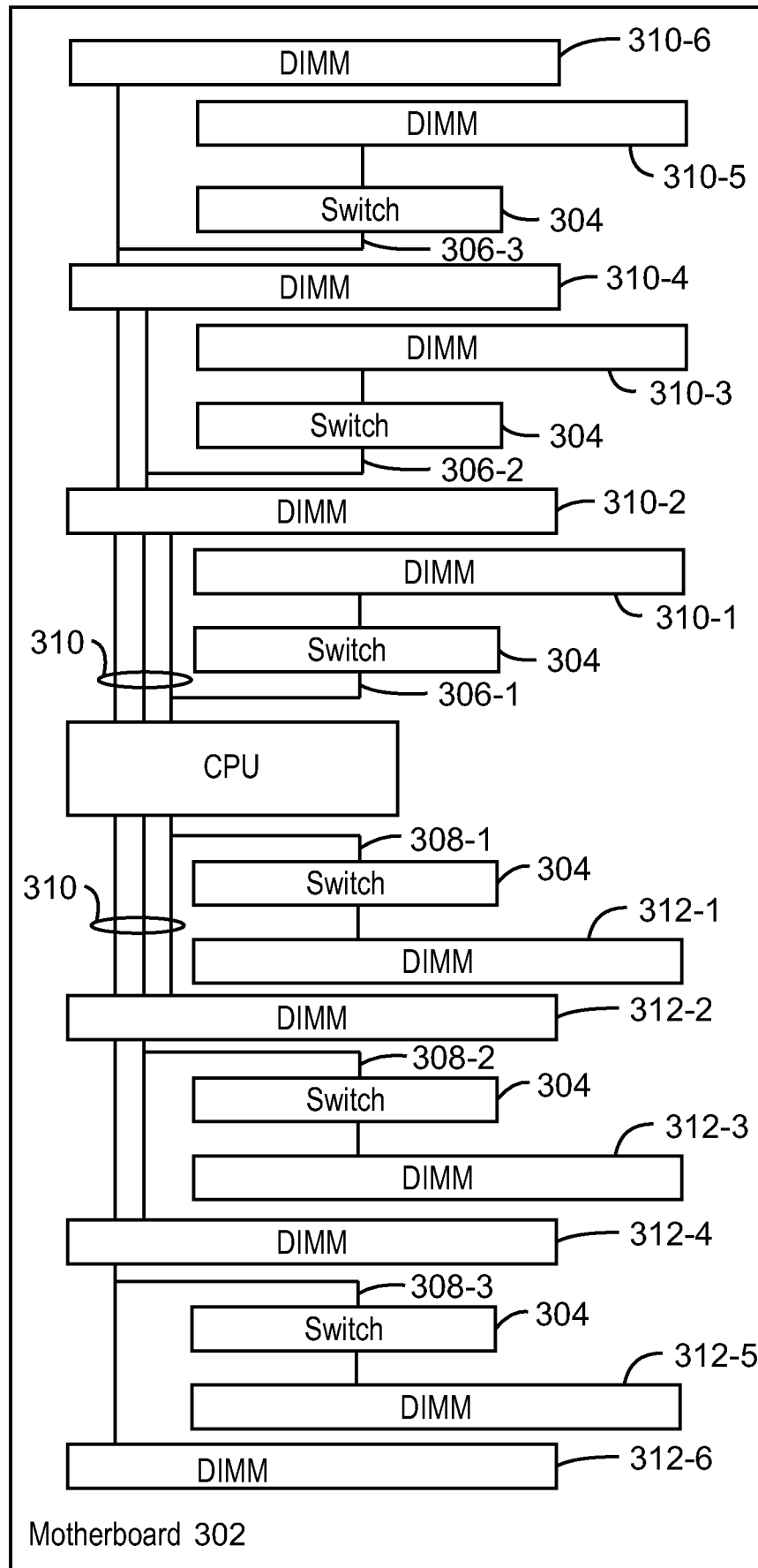
FIG. 2A

4/9



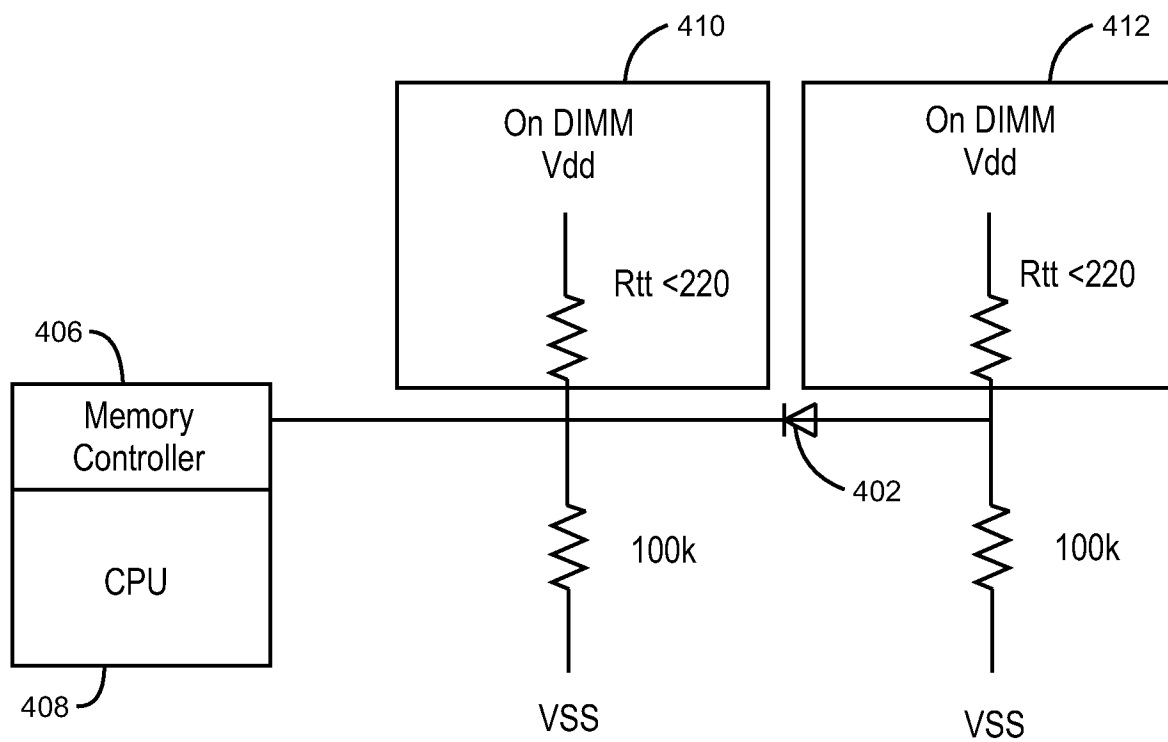
200B
FIG. 2B

5/9



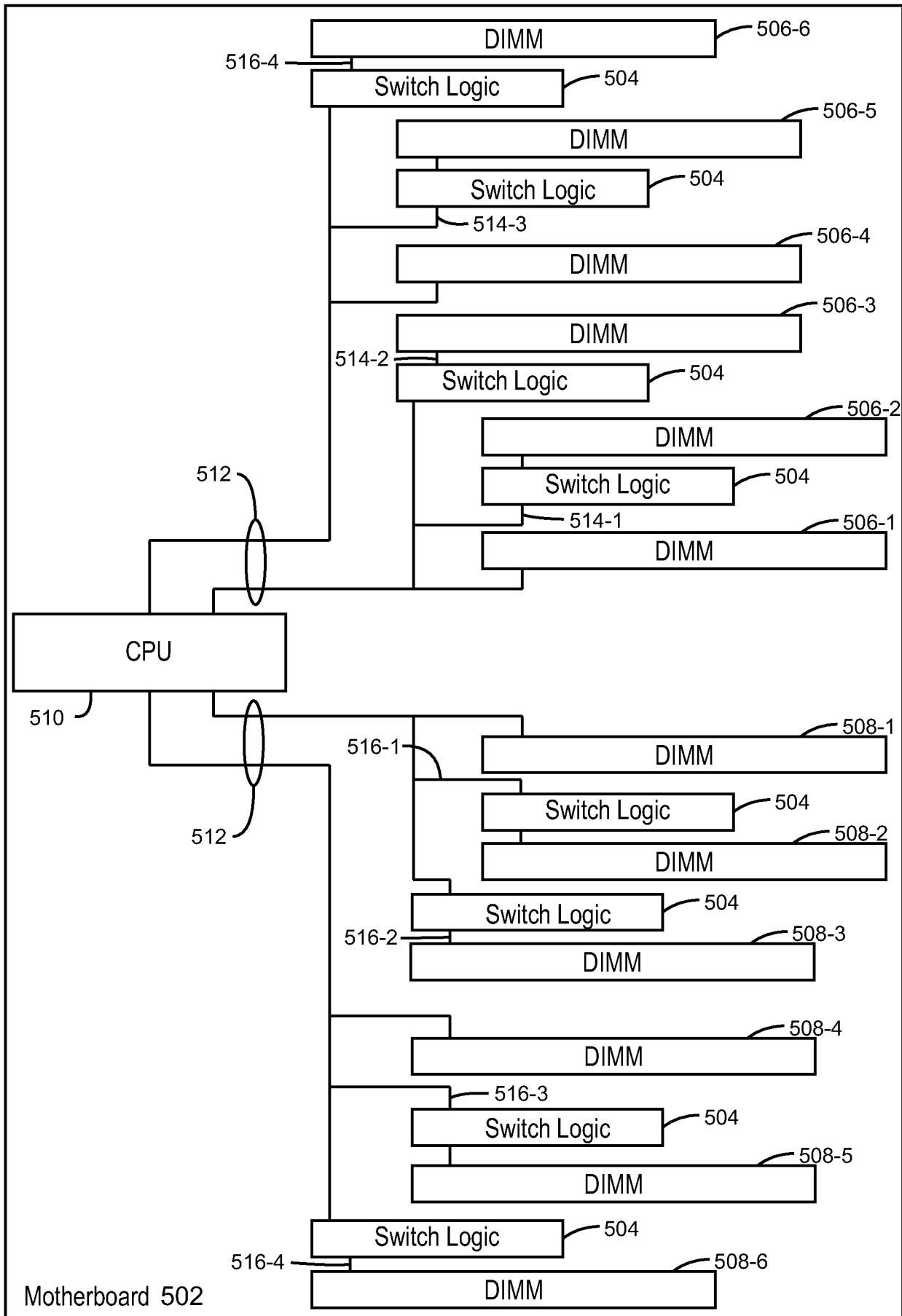
300
FIG. 3

6/9



400
FIG. 4

7/9



500

FIG. 5

8/9

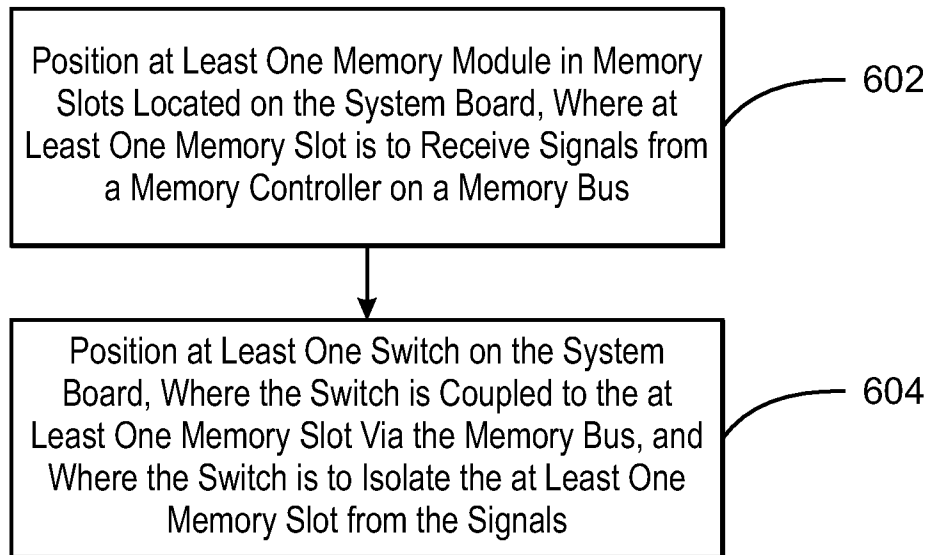
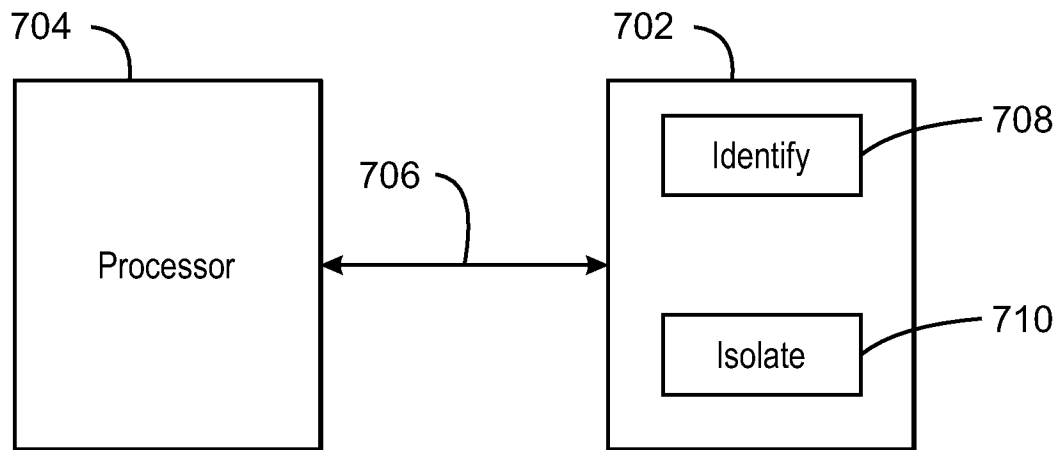
600

FIG. 6

9/9



700
FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/042004**A. CLASSIFICATION OF SUBJECT MATTER****G06F 13/16(2006.01)i, G06F 12/02(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHEDMinimum documentation searched (classification system followed by classification symbols)
G06F 13/16; G06F 12/06; G06F 13/40; H01L 23/498; G06F 13/42; G06F 13/00; G06F 12/02Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility modelsElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: memory, bus, connect, switch, isolate, and similar terms.**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012-0110229 A1 (STEVEN C. WOO et al.) 03 May 2012 See paragraphs [0015]–[0019], [0024]–[0026], [0032], [0041]–[0042], [0050], [0053], [0066], and [0076]; claim 15; and figures 1A-1B and 4-5.	1–15
A	US 2009-0248969 A1 (LARRY WU et al.) 01 October 2009 See paragraphs [0037]–[0047] and figures 1-3.	1–15
A	WO 2010-144624 A1 (GOOGLE INC.) 16 December 2010 See page 5, line 8 – page 6, line 19; page 22, line 16 – page 23, line 7; and figures 1A-1F and 7.	1–15
A	US 2009-0204736 A1 (YAOQIANG (GEORGE) XIE et al.) 13 August 2009 See paragraph [0053] and figure 4.	1–15
A	US 2013-0341790 A1 (MICHAEL W. LEDDIGE et al.) 26 December 2013 See paragraphs [0023]–[0025] and figure 3.	1–15



Further documents are listed in the continuation of Box C.



See patent family annex.

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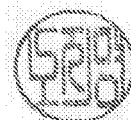
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/042004

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