



(86) Date de dépôt PCT/PCT Filing Date: 2019/07/02
(87) Date publication PCT/PCT Publication Date: 2020/02/06
(45) Date de délivrance/Issue Date: 2023/03/07
(85) Entrée phase nationale/National Entry: 2020/12/14
(86) N° demande PCT/PCT Application No.: US 2019/040372
(87) N° publication PCT/PCT Publication No.: 2020/027972
(30) Priorité/Priority: 2018/07/31 (US16/051,058)

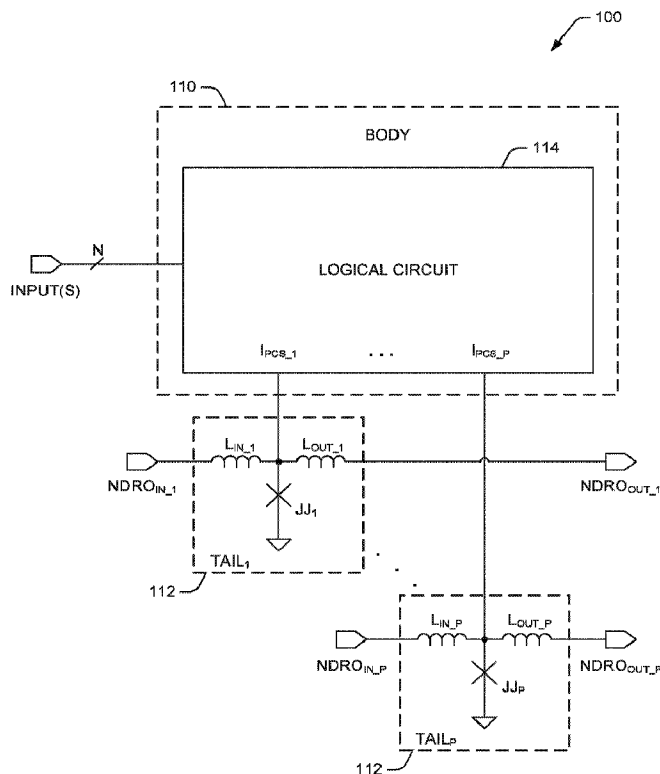
(51) Cl.Int./Int.Cl. *G11C 11/44* (2006.01),
G11C 8/16 (2006.01), *H03K 19/195* (2006.01),
H03K 3/38 (2006.01)

(72) Inventeurs/Inventors:
HERR, ANNA Y., US;
HERR, QUENTIN P., US;
CLARKE, RYAN EDWARD, US;
BRAUN, ALEXANDER LOUIS, US;
HEARNE, HAROLD CLIFTON, III, US;
BURNETT, RANDALL M., US;
LEE, TIMOTHY CHI-CHAO, US

(73) Propriétaire/Owner:

(54) Titre : CIRCUITS DE LECTURE NON DESTRUCTIVE SUPRACONDUCTEURS

(54) Title: SUPERCONDUCTING NON-DESTRUCTIVE READOUT CIRCUITS



(57) Abrégé/Abstract:

Non-destructive read out (NDRO) circuits are provided for use in reciprocal quantum logic (RQL) superconducting systems. Each NDRO circuit includes a "body" circuit that provides a single or multi-state sub-critical bias current to one or many independent "tail"

(73) **Propriétaires(suite)/Owners(continued)**:NORTHROP GRUMMAN SYSTEMS CORPORATION, US

(74) **Agent**: BERESKIN & PARR LLP/S.E.N.C.R.L.,S.R.L.

(57) **Abrégé(suite)/Abstract(continued)**:

circuitries. Each "tail" has minimal effect on the "body" thereby preventing any interference or destruction to the state of the "body" circuitry. The circuits reduce device count and thereby increase circuit density, simplify and reduce the cost of fabrication, and provide functionality not available in existing designs, such as the ability to write a state and read it in the same operation cycle. The NDRO circuits provide more compact unit cells useful in memory or logic arrays, demanding fewer resources with increased functionality. The circuits also provide compact cells for AND, AND-OR, A-NOT-B, inverter, multiplexer, and demultiplexer gates.

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property

Organization

International Bureau

(43) International Publication Date

06 February 2020 (06.02.2020)



(10) International Publication Number

WO 2020/027972 A1

(51) International Patent Classification:

G11C 11/44 (2006.01) H01L 39/22 (2006.01)

G11C 8/16 (2006.01) H03K 3/38 (2006.01)

H03K 19/195 (2006.01)

(21) International Application Number:

PCT/US2019/040372

(22) International Filing Date:

02 July 2019 (02.07.2019)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

16/051,058 31 July 2018 (31.07.2018) US

(71) Applicant: **NORTHROP GRUMMAN SYSTEMS CORPORATION** [US/US]; 2980 Fairview Park Drive, Falls Church, Virginia 22042-4511 (US).

(72) Inventors: **HERR, Anna Y.**; 8987 Furrow Avenue, Ellicott City, Maryland 21042 (US). **HERR, Quentin P.**; 8987 Furrow Avenue, Ellicott City, Maryland 21042 (US). **CLARKE, Ryan Edward**; 6439 Skipton Drive, Hanover, Maryland 21076 (US). **BRAUN, Alexander Louis**; 1543 Covington Street, Baltimore, Maryland 21230 (US). **HEARNE, III, Harold Clifton**; 3538 Beech Av-

enue, Baltimore, Maryland 21211 (US). **BURNETT, Randall M.**; 409 Westside Blvd., Catonsville, Maryland 21228 (US). **LEE, Timothy Chi-Chao**; 11304 Amberlea Farm Drive, Gaithersburg, Maryland 20878 (US).

(74) Agent: **HARRIS, Christopher P.**; Tarolli, Sundheim, Covell & Tummino, LLP, 1300 East Ninth Street, Suite 1700, Cleveland, Ohio 44114 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV,

(54) Title: SUPERCONDUCTING NON-DESTRUCTIVE READOUT CIRCUITS

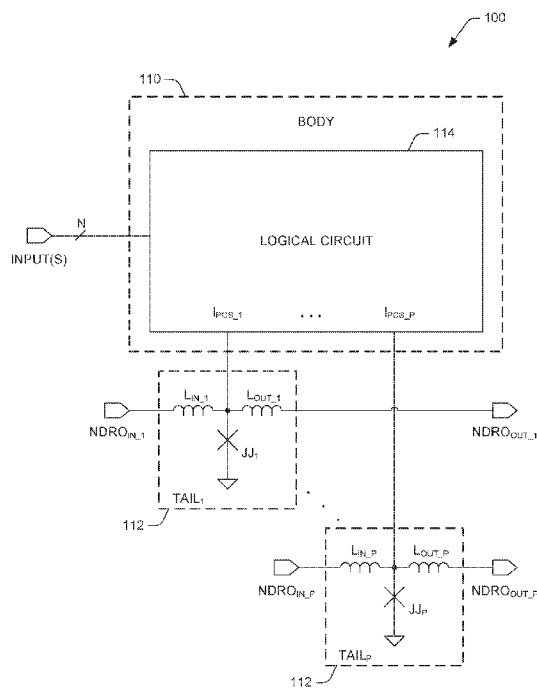


FIG. 1

(57) Abstract: Non-destructive read out (NDRO) circuits are provided for use in reciprocal quantum logic (RQL) superconducting systems. Each NDRO circuit includes a "body" circuit that provides a single or multi-state sub-critical bias current to one or many independent "tail" circuitries. Each "tail" has minimal effect on the "body" thereby preventing any interference or destruction to the state of the "body" circuitry. The circuits reduce device count and thereby increase circuit density, simplify and reduce the cost of fabrication, and provide functionality not available in existing designs, such as the ability to write a state and read it in the same operation cycle. The NDRO circuits provide more compact unit cells useful in memory or logic arrays, demanding fewer resources with increased functionality. The circuits also provide compact cells for AND, AND-OR, A-NOT-B, inverter, multiplexer, and demultiplexer gates.

WO 2020/027972 A1

MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,
TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW,
KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- *as to the identity of the inventor (Rule 4.17(i))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

- *with international search report (Art. 21(3))*
- *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

SUPERCONDUCTING NON-DESTRUCTIVE READOUT CIRCUITS

RELATED APPLICATIONS

[0001] This application claims priority from U.S. Patent Application Serial No. 16/051058, filed 31 July 2018.

GOVERNMENT INTEREST

[0002] The invention was made under Government Contract Number W911NF-14-C-0115. Therefore, the US Government has rights to the invention as specified in that contract.

TECHNICAL FIELD

[0003] The present invention relates generally to quantum and classical digital superconducting circuits, and specifically to superconducting non-destructive readout circuits.

BACKGROUND

[0004] In the field of digital logic, extensive use is made of well known and highly developed complementary metal-oxide semiconductor (CMOS) technology. As CMOS has begun to approach maturity as a technology, there is an interest in alternatives that may lead to higher performance in terms of speed, power dissipation computational density, interconnect bandwidth, and the like. An alternative to CMOS technology comprises superconductor based single flux quantum circuitry, utilizing superconducting Josephson junctions, with typical signal power of around 4 nanowatts (nW), at a typical data rate of 20 gigabits per second (Gb/s) or greater, and operating temperatures of around 4 kelvins.

[0005] A non-destructive readout (NDRO) circuit is a circuit that can retrieve a stored information state (e.g., one or multiple bits) for transmission to other circuitry for processing or output without erasing, destroying, changing, or otherwise corrupting the stored information state. For the purposes of this application, the term should not be interpreted to include circuits that destructively retrieve a stored information state but then thereafter perform a restorative write-back.

[0006] Latches and flip-flops are circuits that can be used to store state information and to change state by signals applied to one or more control inputs. In modern computing and communications electronics, these are basic storage elements in memories and sequential logic. A latch is asynchronous, with its output changing as soon as its data input does (or at least after a small propagation delay), provided the latch is enabled via an enable input. A flip-flop is synchronous and edge-triggered and only changes state when a clocking control signal goes from high to low or low to high. Thus, a conventional D flip-flop, e.g., one implemented in CMOS, has two binary inputs, a data input D and a clock input, and at least one output, Q. The D flip-flop captures the value of the D input at a definite portion of an input clock cycle, e.g., a rising edge or a falling edge, known as the capture time. That captured value becomes the Q output. The output Q does not change except at the capture time (or some small propagation delay thereafter). In practical implementations it is required that a data input D be stable for some setup time prior to the capture time and for some hold time after the capture time for the input to be reliably captured and propagated to the output. A conventional D latch, with an enable input rather than a clock input, behaves similarly, except that the output can change according to the data input so long as an enable input remains asserted.

[0007] In the context of superconducting reciprocal quantum logic (RQL) circuits, phase-mode logic (PML) allows digital values to be encoded as superconducting phases of one or more Josephson junctions. For example, a logical “1” may be encoded as a high phase and a logical “0” may be encoded as a low phase. For example, the phases may be encoded as being zero radians (meaning, e.g., logical “0”) or 2π radians (meaning, e.g., logical “1”). These values persist across RQL AC clock cycles in PML because there is no requirement for a reciprocal pulse to reset the Josephson junctions phase. In contrast to PML, in wave-pipelined logic (WPL), a logical “1” is encoded as a positive single flux quantum (SFQ) pulse followed by a reciprocal negative pulse, whereas a logical “0” is encoded as the absence of either such pulse.

SUMMARY

[0008] One example includes a reciprocal quantum logic (RQL) non-destructive readout (NDRO) gate that includes a body circuit and one or more tail circuits connected to the body circuit. The body circuit has at least one single flux quantum (SFQ) logical input. The body circuit is configured to store at least one logical state. Each tail circuit in the NDRO gate includes a tail input inductor connected between an NDRO read-enable input port and the body circuit and configured to receive an SFQ pulse NDRO read-enable signal on the NDRO read-enable input port, a tail Josephson junction connected between the body circuit and a circuit ground, and a tail output inductor connected between the body circuit and an NDRO output port and configured to transmit an SFQ pulse NDRO output signal based on the stored logical state and the NDRO read-enable signal without affecting the stored logical state.

[0009] Another example includes an RQL demultiplexer circuit (demux). The demux has respective ports for a selector input, a data input, a first output, and a second output. The demux further has a selector Josephson junction connected between a first node and a circuit ground and configured to trigger upon assertion of a selector input signal from the selector input port. The demux further has first and second circuit branches diverging from the first node and converging at a second node configured to receive the data input at the data input port. The first branch includes an inductor connected between the first node and a second node. The first branch further includes a pulse generator connected to the second node, comprising two Josephson junctions and an AC bias source. The first branch further includes an escape Josephson junction connected between the second node and a third node. The first branch further includes a first output Josephson junction connected between the third node and the circuit ground. The second branch includes an inductor connected between the first node and a fourth node. The second branch further includes a second output Josephson junctions connected between a fifth node and the circuit ground. The second branch further includes a third output Josephson junction connected between the fourth node and the circuit ground. Non-assertion or assertion of the selector signal respectively selects between a signal arriving on the data input

port being propagated through the third node to the first output port, or the signal arriving on the data input port being propagated through the fifth and fourth nodes to the second output port.

[0010] Yet another example includes an RQL central processing unit (CPU) that includes a register file having an array of RQL non-destructive readout (NDRO) gate circuits. Each NDRO gate circuit includes a body circuit having one of a D latch or a D flip-flop configured to store a logical state. Each body circuit is connected to at least two tail circuits in the NDRO gate circuit and is configured to supply a pre-critical state current to a respective tail Josephson junction in each of the at least two tail circuits. Each pre-critical state current is representative of the same stored logical state. Each tail circuit is configured to propagate to an NDRO output port of the respective tail circuit an output signal corresponding to the logical AND of the stored logical state with a respective NDRO read enable signal provided to an NDRO input port of the respective tail circuit. The propagation of any output signal from any of the tail circuits does not affect the logical state stored in the body circuit connected to said tail circuits. Each body circuit in the register file array of NDRO gate circuits can include a data input port and a logical clock input port. Word lines of the register file can be connected to the logical clock input ports of the body circuits across word-lines of the respective NDRO gate circuits in the array, and bit lines of the register file can be connected to the NDRO inputs of the tail circuits of the NDRO gate circuits in the array. Each NDRO gate circuit in the array can be configured to have its logical state both writable and readable in the same operation cycle.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] FIGS. 1 is a block/circuit diagram of an example reciprocal quantum logic (RQL) is non-destructive readout (NDRO) gate.

[0012] FIG. 2 is a logical block diagram for an example RQL single-read NDRO register.

[0013] FIG. 3 is a circuit diagram of an example RQL single-read NDRO register.

[0014] FIG. 4 is a logical block diagram for an example RQL dual-read NDRO register.

[0015] FIG. 5 is a circuit diagram of an example RQL dual-read NDRO register.

[0016] FIG. 6 is a logical block diagram for an example RQL single-read NDRO register.

- [0017]** FIG. 7 is a circuit diagram of an example RQL single-read NDRO register having a body-tail topology.
- [0018]** FIG. 8 is a logical block diagram for an example RQL dual-read NDRO register.
- [0019]** FIG. 9 is a circuit diagram of an example RQL dual-read NDRO register having a body-tail topology.
- [0020]** FIG. 10 a timing diagram for the RQL single-read NDRO register circuit of FIG. 7.
- [0021]** FIG. 11 is a circuit diagram of another example RQL single-read NDRO register having a body-tail topology.
- [0022]** FIG. 12 is a circuit diagram of another example RQL dual-read NDRO register having a body-tail topology.
- [0023]** FIG. 13 is a circuit diagram of an example RQL single-read NDRO register, having a body-tail topology, that is flip-flop-based rather than latch-based.
- [0024]** FIG. 14 is a circuit diagram of an example RQL multiplexer.
- [0025]** FIG. 15 is a circuit diagram of an example RQL AND-OR gate.
- [0026]** FIG. 16 is a circuit diagram of an example RQL demultiplexer.
- [0027]** FIG. 17 is a circuit diagram of an example RQL AND gate.
- [0028]** FIG. 18 is a circuit diagram of an example RQL A-NOT-B gate.
- [0029]** FIG. 19 is a circuit diagram of an example RQL inverter (NOT gate).
- [0030]** FIG. 20 is an oscilloscope screenshot capture of measured waveforms for the RQL single-read NDRO register circuit of FIG. 7.
- [0031]** FIG. 21 is a block diagram of an example array of multi-tail NDRO gates.

DETAILED DESCRIPTION

- [0032]** A non-destructive readout (NDRO) circuit topology includes one or more readout “tails” used to propagate, as one or more non-destructive output signals, a state stored in a logical circuit “body” to which the one or more tails are connected. In part because signals used to trigger readout and the output signals corresponding to the stored state can be propagated as

single flux quantum (SFQ) pulses, the readout circuit topology is compatible with circuit designs of the reciprocal quantum logic (RQL) family of superconducting logic for ultra-low-power superconducting computing. The examples provided herein expand and improve on RQL technology in many areas of logic and memory circuitry, in terms of reducing device count, improving functionality, and minimizing or eliminating large transformers.

[0033] FIG. 1 is a block/circuit diagram of an example NDRO gate 100, which includes body 110 and one or more tails 112. The a logical circuit 114 in the body provides a single or multi-state sub-critical bias current to an integer number P of independent circuitries 112, one or more, each referred to herein as a tail. Logical circuit 114 of the body 110 has an integer number N of input(s), one or more, upon which any type of logic operation or logical gate functionality can be performed by logical circuit 114 in order to produce one or more outputs each stored as an internal state of body 110. Thus, body 110 can have one or many (i.e., P) internal states that can produce a combination of independent pre-critical state bias currents (I_{PCS_1} through I_{PCS_P}) supplied to one or many (i.e., P) tails 112. All inputs and pre-critical state currents can be encoded either in wave-pipelined or phase-mode logic. The states can be non-transitory inasmuch as they can persist in the body until changed by inputs to the body. The body outputs to the tail(s) are not considered as inputs to the body since the gate 100 is an NDRO readout gate.

[0034] In FIG. 1, first tail $TAIL_1$ is provided a first pre-critical state current I_{PCS_1} from logical circuit 114, while P th tail $TAIL_P$ is provided a P th pre-critical state current I_{PCS_P} from logical circuit 114. Each tail is also provided a non-destructive readout enable signal $NDRO_{IN_1}$ through $NDRO_{IN_P}$, respectively, and outputs a read output signal $NDRO_{OUT_1}$ through $NDRO_{OUT_P}$, respectively, these output signals corresponding to the state of logical circuit 114.

[0035] Each tail 112 can consist of as few as three components. Specifically, each tail 112 can consist of as little as just one Josephson junction (e.g., JJ_1 , JJ_P) having an input end and a grounded end, an input inductor (e.g., L_{IN_1} , L_{IN_P}) connected to the input end of the Josephson junction through which the input non-destructive readout enable signal (e.g., $NDRO_{IN_1}$, $NDRO_{IN_P}$) is supplied, and an output inductor (e.g., L_{OUT_1} , L_{OUT_P}) connected to the input end of the Josephson junction through which an output non-destructive readout signal (e.g.,

NDRO_{OUT_L}, NDRO_{OUT_P}) is supplied to other circuitry (not shown). Josephson transmission lines (JTLs) (not shown in FIG. 1) can be connected to the NDRO input and output of each tail 112 to carry SFQ pulses to and from the tails.

[0036] Thus, in an example, logical circuit 114 can provide the functionality of a simple memory storage element such as a flip-flop or latch, effectively storing one bit of data. In other examples, logical circuit 114 can be a logical gate or any combination of logical gates, including AND, OR, XOR, and NOT (i.e., inverter) gates, multiplexers, demultiplexers, and shift registers. The pre-critical state currents I_{PCS_L} through I_{PCS_P} can represent a multiplicity of states or, in some examples, they can all represent a single state. In any case, logical circuit 114 supplies its logical state(s) to be output to the one or more tails 112. Each tail 112 has minimal effect on the body, thereby preventing any interference or destruction to the state of the body circuitry 114.

[0037] NDRO gate 100 thus uses a state-produced pre-critical bias current from body logical circuitry 114 to pre-critically bias a Josephson junction, JJ_L through JJ_P , in the circuitry of each tail 112, allowing each tail 112 to act as an output enabler, in other words, effectively providing a logical AND between the state of the body logical circuitry 114 and a corresponding non-destructive readout enable signal, NDRO_{IN_L} through NDRO_{IN_P}. This NDRO input of any tail 112 reads and outputs the internal state inside the body 110 without disrupting the internal state inside the body 110. The body 110 can be combinational logic in nature or not at all, and thus, can have one or multiple inputs and one or multiple outputs to its associated tails 112.

[0038] FIGS. 2-5 illustrate logical diagrams for registers 200, 400 and corresponding superconducting register circuits 300, 500 that do not use the body-tail architecture of FIG. 1 but instead build registers with D-latch and AND-gate stages. FIG. 2 shows a logical block diagram for an example RQL single-read NDRO register 200 that is implemented by combining circuitry for a D latch 202 with circuitry for an AND gate 204. A data input signal DI provided to the data input D of D latch 202 is stored as an output state Q upon being “latched” by an assertion of logical clock signal LCLK provided to enable input E of D latch 202. This signal is logically ANDed with a read enable signal RE by AND gate 204, the output of which is the read output signal QO. An intermediary Josephson transmission line (JTL) can be provided between

D latch 202 and AND gate 204, and/or between AND gate 204 and a circuit (not shown) that receives output signal QO, for signal amplification, signal distance transmission, and signal isolation purposes.

[0039] FIG. 3 shows a circuit diagram implementing the single-read register 200 of FIG. 2 as an example RQL-compatible superconducting circuit 300. An input stage 302 of circuit 300 includes two input ports DI and LCLK, three Josephson junctions J2, J3, and J4, two input inductors L1 and L2, and a first transformer for inductively coupling a DC flux bias from a DC flux bias line. Input stage 302 corresponds to, and provides the functionality of, D latch 202 from FIG. 2. An output stage 304 of circuit 300 includes an input port RE, an output port QO, two inductors L3, L4, two Josephson junctions J5, J6, and a second transformer for inductively coupling a DC flux bias from a DC flux bias line. Output stage 304 corresponds to, and provides the functionality of, AND gate 204 from FIG. 2. An intermediary JTL can be provided between input stage 302 and output stage 304, and/or between output stage 304 and a circuit (not shown) that receives output signal QO, for signal amplification, signal distance transmission, and signal isolation purposes.

[0040] FIG. 4 shows a logical block diagram for an example dual-read register 400 that is implemented by combining circuitry for a D latch 402 with circuitry for two AND gates 404, 406. As shown in logical diagram 400, the output of the D latch 402 is forked between the two AND gates 404, 406. The functioning of D-latch 402 and each AND gate 404, 406 is the same as has been described above with respect to FIG. 2. A data input signal DI provided to the data input D of D latch 402 is stored as an output state Q upon being “latched” by an assertion of logical clock signal LCLK provided to enable input E of D latch 402. This output signal is logically ANDed with each of two read enable signals RE_A and RE_B by AND gates 404, 406, respectively, the outputs of which are the read output signals QO_A and QO_B. As discussed above, intermediary JTLs can be provided between D latch 402 and AND gates 404, 406 and/or between AND gates 404, 406 and circuits (not shown) that receive output signals QO_A and QO_B, for signal amplification, signal distance transmission, and signal isolation purposes.

[0041] FIG. 5 shows a circuit diagram implementing the dual-read register 400 of FIG. 4 as an example RQL-compatible superconducting circuit 500. Input stage 502 of circuit 500 includes two input ports DI and LCLK, three Josephson junctions J2, J3, and J4, two input inductors L1 and L2, and a first transformer for inductively coupling a DC flux bias from a DC flux bias line. Input stage 502 corresponds to, and provides the functionality of, D latch 402 from FIG. 4. First output stage 504 of circuit 500 includes an input port RE_A, an output port QO_A, two inductors L3_A, L4_A, two Josephson junctions J5_A, J6_A, and a second transformer for inductively coupling a DC flux bias from a DC flux bias line. First output stage 504 corresponds to, and provides the functionality of, AND gate 404 from FIG. 4. Second output stage 506 of circuit 500 includes an input port RE_B, an output port QO_B, two inductors L3_B, L4_B, two Josephson junctions J5_B, J6_B, and a third transformer for inductively coupling a DC flux bias from a DC flux bias line. Second output stage 506 corresponds to, and provides the functionality of, AND gate 406 from FIG. 4.

[0042] Between input stage 502 and output stages 504, 506, fork stage 503 can provide an output signal from input stage 502 as input signals to each of output stages 504, 506. Fork stage 503 includes three Josephson junctions JF1, JF2_A, and JF2_B, four inductors LF1, LF2, LF3_A, and LF3_B, and a fifth inductor LF_CLK to an AC bias signal source AC CLK. Intermediary JTLs can be provided between input stage 502 and fork stage 503, and/or between output stages 504, 506 and circuits (not shown) that receive output signals QO_A, QO_B, for signal amplification, signal distance transmission, and signal isolation purposes.

[0043] Circuits 300 and 500, as logically symbolized in diagrams 200 and 400, respectively, each connect a D-latch output to one or more AND gates via JTL(s) depending on the number of read ports desired. Despite their superficial simplicity, device count and resource utilization is relatively high in these designs. In addition to this, the illustrated configurations lack the functionality of being able to read and write at the same time, which is a desirable performance feature for a register file to have in the realm of CPU architecture.

[0044] Dual-read register circuit 500 of FIG. 5 is relatively complicated, has a high part count (having 24 components not including those in JTLs, ports, and AC bias source), and

relatively high resource utilization (e.g., requiring three DC flux bias line connections as well as AC bias source connections to power the JTLs and fork stage 503). However, in view of the purpose of circuit 500 as implementing the logical functionality illustrated in block diagram 400 of FIG. 4, it may not be apparent how circuit 500 might be simplified given that each of its stages 502, 503, 504, 506 implements a logical component or signal split from diagram 400. Additionally, the need for signal propagation (from left to right in the circuits as illustrated) means that circuits 300 and 500 do not permit writing a data input signal and reading that same data input signal at substantially the same time (e.g., within the same operation cycle). The examples of FIGS. 6-9 reconceptualize the logical designs and implementations of FIGS. 2-5, reducing part count while providing improved functionality, e.g., by permitting simultaneous writing of a state and reading of the written state. In view of these examples, it is clear that even single-read register circuit 300 of FIG. 3 is unduly complicated and has a higher part count than desirable.

[0045] FIG. 6 shows a logical block diagram for an example single-read RQL D-register 600 that has at least all of the functionality of single-read register 200 from FIG. 2 but is capable of providing non-destructive readout without the D-latch-to-AND-gate staging shown in FIGS. 2 and 3. A data input signal DI provided to the data input D of NDRO-latch 602 is stored as an internal state of NDRO-latch 602 upon being “latched” by an assertion of logical clock signal LCLK provided to the same-named input of NDRO-latch 602. Upon assertion of a non-destructive readout signal NDRO, provided to input NDROA of NDRO-latch 602, which can be substantially contemporaneous with (e.g., within the same operation cycle as) the logical clock signal assertion, the internal state is read out from output Q as read output signal QO.

[0046] FIG. 7 shows a circuit diagram implementing the single-read RQL D-register 600 of FIG. 6 as an example RQL-compatible superconducting circuit 700. Body stage 702 of circuit 700 includes two input ports DI and LCLK, three Josephson junctions J2, J3, and J4, two input inductors L1 and L2, and transformer(s) for inductively coupling a DC flux bias from a DC flux bias line. At circuit initialization, the DC flux bias transformers bias Josephson junction J2 with a fraction of a Φ_0 offset (e.g., $\frac{1}{2} \Phi_0$). (Φ_0 is a single flux quantum, equal to

approximately 2.07 mA-pH.) Body stage 702 can correspond to body 110 in FIG. 1. Tail stage 704 of circuit 700 includes an input port NDRO, an output port QO, one inductor L3, and one Josephson junction J5. Tail stage 704 can correspond to a tail 112 in FIG. 1. Body stage 702 can be connected to tail stage 704 by a linking inductor LL. A more detailed description of the functioning of the single-read register circuit 700 of FIG. 7 follows with reference to the simulation timing diagram 1000 of FIG. 10.

[0047] Tail stage 704 does not have two Josephson junctions, nor does it have a second transformer for inductively coupling a DC flux bias from a DC flux bias line, as may be found in the output stage 304 of FIG. 3. Circuit 700 also does not include an intermediary JTL between body stage 702 and tail stage 704, although a JTL may, as illustrated in FIG. 7, be provided between tail stage 704 and a circuit (not shown) that receives output signal QO, for signal amplification, signal distance transmission, and signal isolation purposes.

[0048] FIG. 8 shows a logical block diagram for an example dual-read RQL D-register 800 that has at least all of the functionality of dual-read register 400 from FIG. 4 but is capable of providing non-destructive readout without the D-latch-to-AND-gate staging shown in FIGS. 4 and 5. A data input signal DI provided to the data input D of NDRO-latch 802 is stored as an internal state of NDRO-latch 802 upon being “latched” by an assertion of logical clock signal LCLK provided to the same-named input of NDRO-latch 802. Upon assertion of a first non-destructive readout signal NDRO_A, provided to input NDROA of NDRO-latch 802, which can be substantially contemporaneous with (e.g., within the same operation cycle as) the logical clock signal assertion, the internal state is read out from output QA as read output signal QO_A. Upon assertion of a second non-destructive readout signal NDRO_B, provided to input NDROB of NDRO-latch 802, which can be substantially contemporaneous with (e.g., within the same operation cycle as) the logical clock signal assertion, the internal state is read out from output QB as read output signal QO_B.

[0049] FIG. 9 shows a circuit diagram implementing the dual-read RQL D-register 800 of FIG. 8 as an example RQL-compatible superconducting circuit 900. Body stage 902 of circuit 900 includes two input ports DI and LCLK, three Josephson junctions J2, J3, and J4, two

input inductors L1 and L2, and transformer(s) for inductively coupling a DC flux bias from a DC flux bias line. Body stage 902 can correspond to body 110 in FIG. 1. First and second tail stages 904, 906 of circuit 900 include respective input ports NDRO_A, NDRO_B, respective output ports QO_A, QO_B, respective inductors L3_A, L3_B, and respective Josephson junctions J5_A, J5_B. Tail stages 904, 906 can correspond to tails 112 in FIG. 1. Body stage 902 can be connected to tail stages 904, 906 by a linking inductors LL_A, LL_B.

[0050] The functioning of the body stage 902 and tail stages 904, 906 in circuit 900 of FIG. 9 is substantially the same as the functioning of body stage 702 and tail stage 704 in circuit 700 of FIG. 7, except that, since in the particular example of circuit 900 both tail stages 904, 906 are connected to the same “output” of body stage 902 and thus receive the same stored state from body stage 902, the output current from body stage 902 is required to be large enough to drive two tails instead of one. Consequently, the sizes of the Josephson junction devices in body stage 902 may be larger as compared to those in body stage 702 of circuit 700.

[0051] In circuit 900, tail stages 904, 906 do not have two Josephson junctions each, nor do they each have a second transformer for inductively coupling a DC flux bias from a DC flux bias line, as may be found in the output stages 504, 506 of FIG. 5. Circuit 900 also does not include intermediary JTLs between body stage 902 and tail stages 904, 906, although JTLs may, as illustrated in FIG. 9, be provided between tail stages 904, 906 and respective circuits (not shown) that receive output signals QO_A, QO_B, these JTLs being for the purposes of signal amplification, signal distance transmission, and signal isolation.

[0052] Summarizing the component-economy structural advantages of body/tail circuits 700 and 900 over D-latch/AND-gate circuits 300 and 500, respectively, single-read body/tail circuit 700 uses four Josephson junctions and one JTL whereas single-read D-latch/AND-gate circuit 300 uses five Josephson junctions and two JTLs, for a savings of one Josephson junction and one JTL (which itself includes one or more Josephson junctions); dual-read body/tail circuit 900 uses five Josephson junctions and two JTLs as compared to the ten Josephson junctions and three JTLs used in D-latch/AND-gate dual-read circuit 500, for a savings of five Josephson junctions and one JTL. Furthermore, dual-read body/tail circuit 900

has fewer inductors and fewer inductive couplings than dual-read D-latch/AND-gate circuit 500. Since a reduction in number of Josephson junctions and inductors leads to a higher count of memory cells or logic cells per fabricated die area or chip area, example body/tail circuits 700 and 900 reduce cost by greatly increasing density of a memory array or logic array.

[0053] FIG. 10 presents a timing diagram 1000 illustrating the functioning of the RQL single-read NDRO register circuit 700 of FIG. 7. Each of seven plots in diagram 1000 is presented as a function of time in nanoseconds. The DI signal plot represents a data input provided to the circuit to set a circuit state, e.g., a memory or logic state. The LCLK signal plot represents a logical clock input that acts as a write enable signal. The NDRO signal plot represents a non-destructive readout input that acts as a read enable signal. The QO signal plot represents a non-destructive readout output that can be provided as an input signal to another circuit. Also included to assist in understanding the functioning of circuit 700 are the superconducting phases of Josephson junctions J2, J4, J5, and J3, where phase is defined as the time-integral of voltage at every node. Text legends along the top of the timing diagram specify the circuit operation invoked, i.e., the underlying meaning of the particular combination of inputs and output, according to the following truth table, where “previous state” is indicated by the phase of Josephson junction J2 during the end of the previous operation cycle:

	DI	LCLK	NDRO	Previous state	New state	QO
No inputs	0	0	0	0 or 1	Prev.	0
Read 0	0	0	1	0	0	0
Read 1	0	0	1	1	1	1
Write 0	0	1	0	0 or 1	0	0
Write 0 and read	0	1	1	0 or 1	0	0
Half select (no read)	1	0	0	0 or 1	Prev.	0
Half-select (with read 0)	1	0	1	0	0	0
Half-select (with read 1)	1	0	1	1	1	1
Write 1	1	1	0	0 or 1	1	0
Write 1 and read	1	1	1	0 or 1	1	1

[0054] For each operation cycle, NDRO (i.e., read enable) input signals are timed to come after a set-up and hold time from the beginning of any LCLK (i.e., write enable), such that a data value written to the body stage 702 can be read out from the tail stage 704 within the same operation cycle. This timing can be enforced by support circuitry outside of circuit 700 and can employ, for example, JTLs configured to provide various signal time delays. A “half-select” condition is defined as an application of a logical “high” signal to data input DI without a corresponding logical “high” write enable signal on logical clock input LCLK.

[0055] Single-read RQL D-register circuit 700 uses the phase of Josephson junction J2 in body stage 702 to encode a stored state value and to source a stable pre-critical bias current to Josephson junction J5 in tail stage 704. Although this pre-critical bias current is insufficient to cause Josephson junction J5 to trigger, it sufficiently biases Josephson junction J5 such that its triggering is directly correlated to the value of the non-destructive readout input signal NDRO. Specifically, a positive NDRO pulse will trigger Josephson junction J5 and thereby send out an SFQ pulse to output QO, and a negative NDRO pulse will reset Josephson junction J5. The bias from input NDRO can be made weak, and isolation between the tail stage 704 to the body stage 702 (i.e., in the tail-to-body direction) can be sufficiently high to avoid any corruption of the body-stored state by NDRO signals, which is what makes the readout “non-destructive.”

[0056] In single-read RQL D-register circuit 700, Josephson junction J2 junction triggers when the logical lock input LCLK goes “high” (i.e., when a positive SFQ pulse is provided on the logical clock input LCLK to assert the logical clock input), bringing the superconducting phase of Josephson junction J2 to 2π radians (“high”). The phase of Josephson junction J2 remains “high” if the data input DI is asserted (i.e., with a positive SFQ pulse introduced to data input DI) upon the falling edge of the logical clock signal provided on input LCLK. Josephson junction J2 will “flip back” (i.e., its phase will return to 0 radians, “low”) if data input DI is unasserted (“low”) during this time. Consequently, the superconducting phase of Josephson junction J2 determines the internal state of the body 702 of RQL D-register circuit 700. Thus, for example, Josephson junction J2 having a 2π radian superconducting phase can correspond to a stored “1” (logical “high”) value, whereas Josephson junction J2 having a 0 radian

superconducting phase can correspond to a stored “0” (logical “low”). In particular, the stored state corresponds to the phase of state-storing Josephson junction J2 during the latter half of an operation cycle, as can be noted in timing diagram 1000, particularly during “write 0” operations.

[0057] A stored “1” from a triggered Josephson junction J2 in body 702 provides a pre-critical bias current to Josephson junction J5 in tail 704. Under this biased condition, tail Josephson junction J5 does not trigger unless the read-enabling input NDRO is asserted (goes “high”), which then passes the body-stored state to output QO. The triggering of Josephson junction J5 does not affect the internal state of the body 702 (encoded as the superconducting phase of Josephson junction J2), giving the readout of circuit 700 its non-destructive property.

[0058] Because tail Josephson junction J5 can only trigger when body-state storage Josephson junction J2 has triggered to bring it into its 2π radian superconducting phase and the non-destructive readout input NDRO is asserted with a positive SFQ pulse, the NDRO input and corresponding output QO can be either wave-pipelined logic (WPL) or phase-mode logic (PML) encoded, and the assertion of the non-destructive readout input NDRO must arrive after Josephson junction J2 has been properly setup or logical clock signal provided on input LCLK is de-asserted. With proper phase timing of the logical lock and non-destructive readout signals provided on inputs LCLK and NDRO, data can be written and read during the same clock cycle, speeding memory and computing operations.

[0059] The various operational states of circuit 700 will now be explored with reference to the simulation timing diagram 1000 of FIG. 10, reading its operation cycles (separated by vertical broken lines) in chronological order from left to right.

[0060] **“Quiescent inputs”:** The circuit 700 begins with no state value stored in its body 702. When all three inputs DI, LCLK, and NDRO are unasserted, the circuit is in a “quiescent inputs” operational state, and output QO is therefore “low.”

[0061] **“Read 0”:** The next operation cycle is a read cycle, in which an NDRO pulse 1002 introduced in the latter half of the cycle “reads out” the body-stored state, which is

still “low,” since no write operation has changed it from its initial value. Thus, output QO remains “low.”

[0062] “Write 1 and read”: The next cycle sees all three inputs DI, LCLK, and NDRO asserted to write a logical “high” value as the body-stored state and enable the reading out of this state to output QO all within the same operation cycle. The superconducting phase of Josephson junction J2 goes “high” (e.g., to 2π radians) 1004 as soon as the write-enabling signal provided on logical clock input LCLK goes “high.” It stays high after an assertion SFQ pulse supplied to the data input DI triggers 1006 Josephson junction J4. When LCLK transitions low, the “high” superconducting phase of state-storing Josephson junction J2 is maintained. Instead of Josephson junction J2 untriggering, escape Josephson junction J3 triggers 1008. The combination of the logical clock input LCLK going “high” and data input DI going “high” puts circuit 700 into a “write 1” state, causing a “1” to be written to the body-stored state by maintaining Josephson junction J2 in a 2π radian superconducting phase. The phase of Josephson junction J2 goes “high,” even before the data input DI goes “high,” but without data input DI being asserted, Josephson junction J2 would return “low” after the write enable signal LCLK goes “low” (as can be seen at the “Write 0” operation, discussed below). As long as Josephson junction J2 is in a “high” state of 2π radians, it provides pre-critical bias current to tail Josephson junction J5, preparing tail Josephson junction J5 to propagate any pulse it receives at input NDRO to output QO.

[0063] The written state is read out on output QO immediately, within the same operation cycle. The NDRO command is timed later in the operation cycle than the LCLK command, because any time the write enable signal of logical clock input LCLK goes high, Josephson junction J2 is asserted to a “high” superconducting phase, meaning that a premature read-out attempt will result in a readout value of “1” regardless of whether a “1” or a “0” is being written. Because the read enable signal NDRO is delayed in time, the read-out state will, appropriately, be the same state that is written earlier in the same operation cycle.

[0064] The superconducting phase of Josephson junction J5 signifies the readout of a “1,” and can be interpreted as a logical AND of the superconducting phase of Josephson

junction J2 and the read-enabling NDRO command. Thus, sending input NDRO “high” when Josephson junction J2 is in a 2π radian superconducting phase (“high”) causes the superconducting phase of Josephson junction J5 to transition to 2π radians (“high”) and propagates an SFQ pulse toward output QO. (Accordingly, the plot for output QO finally falls to “low” when the plot for the phase of Josephson junction J5 also falls to “low.”) An attempt to perform a readout when the superconducting phase of Josephson junction J2 is 0 radians is not sufficient to trigger Josephson junction J5, so the output QO reads “0.” Once again emphasizing the non-destructive readout operation of circuit 700, a triggering of Josephson junction J5 does not affect the phase of Josephson junction J2 (or any of the other Josephson junctions in circuit 700) and thus does not change the body-stored logical circuit state (i.e., the memory element state, when circuit 700 is used in a memory).

[0065] “Write 0 and read”: The write-enabling logical clock signal provided on input LCLK goes “high,” but now when the data input DI remains unasserted, the phase of state-storing Josephson junction J2 drops back to 0 radians, as can be seen in the J2 phase plot at the midpoint of the cycle. In the same cycle, a read-enabling command is issued (i.e., input NDRO goes “high”), reading out the written state as “0” on QO, because Josephson junction J5 does not trigger.

[0066] 2nd “Write 1 and read,” followed by “Read 1”: These two cycles show the correct non-destructive readout behavior expected from two back-to-back operations. The first readout does not destroy the written “1” state, so when it is followed immediately by another read operation, the same “1” is still read-out again, meaning that the first readout has not corrupted the body-stored state. In the second of these two operations, when the read-enabling signal provided on input NDRO goes “high,” the superconducting phase of Josephson junction J2 is already “high,” so the superconducting phase of Josephson junction J5, and thus output QO, likewise go “high.”

[0067] “Write 0”: The logical clock signal provided on input LCLK goes “high” to activate the write enable while data input DI is “low.” There being no read operation enabled, the output QO is appropriately “low” at the end of the operation cycle. The superconducting

phase of state-storing Josephson junction J2 goes “low,” indicating that a “0” has been written to the state-storing body 702.

[0068] “Read 0”: The read-enabling signal provided on input NDRO goes “high,” but not causing the superconducting phase of Josephson junction J2 to go “high,” indicating that the “low” stored memory state is preserved, uncorrupted by the read-enabling signal provided on input NDRO. As can be seen later at the beginning of the next “Write 1” operation, even the combination of inputs NDRO and LCLK both going “high” is insufficient to cause Josephson junction J5 to trigger and produce an output at the beginning of an operation cycle.

[0069] “Half select without read (0 state)”: The “half-select” condition can arise, for example, during the sending of data to a memory array, when the subject circuit is a particular memory element that is not part of the addressed bit-line. In such a case, it may be that, as an artifact of the array architecture, the “1” signal sent on data input DI is delivered in parallel to every bit-line of the memory array. Thus, although data input DI may be “high,” write-enabling logical clock input LCLK is “low.” Under such a half-select condition, the stored state should not change. This cycle of diagram 1000 illustrates the correct behavior. Even when data input DI is “high,” the combination of “high” data input DI and “low” write enable input LCLK are insufficient to trigger state-storing Josephson junction J2 and change its superconducting phase to 2π radians. Thus, the written state stored in the circuit body 702 remains “low.” The phase of escape Josephson junction J3 is likewise unaffected. Read-enabling input NDRO is “low,” meaning no read signal is sent, and output QO remains low.

[0070] “Half select with read (0 state)”: This operation cycle illustrates the combined effect of an asserted data input DI and an asserted read enable input NDRO on the stored state, i.e., the superconducting phase of state-storing Josephson junction J2. Even when the memory state is “0,” inputs DI and NDRO going high do not cause Josephson junction J2 to trigger. The superconducting phase of Josephson junction J2 remains at 0 radians. This cycle thus illustrates again the non-destructive readout functionality of circuit 700, even when the circuit is a half-selected cell in a memory or logic array.

[0071] “**Write 1**”: Data input DI goes “high” and is write-enabled by an assertion of logical clock input LCLK. State-storing Josephson junction J2 therefore also triggers to transition to a “high” superconducting phase, but output QO remains “low,” there being no read-enabling signal NDRO and therefore no readout.

[0072] “**Half select without read (1 state)**”: Data input DI is “high,” but write enable LCLK is “low,” expressing the half-select condition. This combination does not affect the “high” superconducting phase of state-storing Josephson junction J2. Escape Josephson junction J3 retains its “low” superconducting phase. Read enable input NDRO is “low,” and output QO remains “low,” even though the stored state is “high.”

[0073] “**Read 1**”: This read cycle proves again that the half-select condition of the previous cycle did nothing to corrupt the stored “high” state. When read enable input NDRO is asserted, output QO is likewise asserted, indicating successful readout of the “1” state written two cycles prior.

[0074] “**Write 0**”: Write enable input LCLK is asserted “high” while data input DI is “low,” causing the superconducting phase of state-storing Josephson junction J2 to drop to 0 radians. The phase of escape Josephson junction J3, meanwhile, flips back. Thus, at the end of timing diagram 1000, circuit 700 is reset to its starting state.

[0075] In timing diagram 1000 of FIG 10, signals provided to inputs LCLK and NDRO are temporally shifted relative to each other, with the indicated LCLK state in the above description being the state that LCLK goes shortly after the start of the cycle and the indicated NDRO state in the above description being the state that NDRO goes around the time that LCLK goes “low,” e.g., shortly after halfway through the cycle. The phase of Josephson junction J4 is substantially in phase with data input DI, while the phase of Josephson junction J5 is substantially in phase with output QO. In the above description, the indicated DI state, and thus also the indicated phase of Josephson junction J4, is the state or phase at the middle of the operation cycle. The indicated QO state, like with the indicated phases of Josephson junctions J2 and J5, is the state or phase at the end of the operation cycle. As an example, the circuit can be designed such that LCKL and NDRO are out of phase with each other, e.g., 180° out of phase

with each other, or 225° degrees out of phase with each other, so that a previous-cycle read has no effect on the operation in a current cycle.

[0076] FIG. 11 shows a circuit diagram implementing the single-read RQL D-register 600 of FIG. 6 as an example RQL-compatible superconducting circuit 1100, similar in form and function to circuit 700 of FIG. 7, but reducing, from two to one, the number of DC flux bias transformers in the circuit by implementing a Y- Δ transform of the central inductance network in the body stage 702 to arrive at body stage 1102, having inductors LL_1 and LL_2 . Tail stage 1104 is unchanged from tail 704. Circuit 1200 of FIG. 12 provides a similar variation of the dual-read RQL D-register 800 of FIG. 8 as compared to circuit 900 of FIG. 9, illustrating that the variation of the latch-based NDRO circuit shown in FIG. 11 can be built to a dual-read or multiple-read configuration by adding on NDRO tail stages 1204, 1206 to nodes 1208, 1210. Tail stages 1204, 1206 are unchanged from tail stages 904, 906; only the topology of body stage 1202 differs from the topology of body stage 902.

[0077] FIG. 13 provides a flip-flop-based NDRO gate 1300 containing the same tail stage 1304 as latch-based NDRO circuit 700 and nearly the same components in body stage 1302 (as compared to body stage 702) except for inductors L_4 , L_5 substituted for the DC flux bias transformers of circuit 700. Body stage 1302 includes a tri-stable flip-flop. In contrast to the D-latch circuit 700 of FIG. 7, which has two states and a fraction of a Φ_0 (e.g., $\frac{1}{2} \Phi_0$) offset, D flip-flop circuit 1300 has three states and no phase offset. The Josephson junction J2 in circuit 1300 remains the state storage element, but the process of writing is different than with circuit 700. Logical clock input LCLK remains asserted (“high”) when not performing a write operation, which prevents a positive pulse from data input DI from triggering Josephson junction J2. To perform a write operation, logical clock input LCLK is de-asserted (goes “low”), allowing Josephson junction J2 to trigger upon assertion of data input DI with a positive SFQ pulse (i.e., DI going “high”). Data input DI remains high until logical clock input LCLK is reasserted “high” again, thereby “locking” or storing the data input value as the superconducting phase of Josephson junction J2. Data input DI can then return “low” after logical clock input

LCLK goes “high.” Readout functionality is unchanged from the latch-based circuit 700, as the two circuits contain same tail stage circuitry.

[0078] Variants of the flip-flop-based NDRO circuit 1300 provided in FIG. 13 are contemplated. Although not illustrated, a flip-flop based circuit similar to that of FIG. 13 can be provided having multiple tails, in accordance with the example illustrated in FIG. 9. Although not illustrated, a flip-flop based circuit similar to that of FIG. 13 can be provided having the delta body configuration rather than the Y-topology illustrated in FIG. 13, in view of the delta-configuration circuits illustrated in FIGS. 11 and 12 as compared to their Y-configuration counterparts in FIGS. 7 and 9. Although not illustrated, a flip-flop based circuit similar to that of FIG. 13 can be provided having both the delta body configuration and multiple tails, in accordance with the example illustrated in FIG. 12.

[0079] The body-tail topologies described above can be adapted to create new combinational logic gate circuits, such as those illustrated in FIGS. 14-16. Primitive gates are also described with reference to FIGS. 17-19.

[0080] As one example, FIG. 14 illustrates a multiplexer circuit 1400 composed of two tail structures arranged to perform two AND functions on the left and right sides of circuit 1400, with a pulse generator portion of the circuit 1400 at the upper-right of FIG. 14 providing an invert function. Assertion of selector input S sends a signal provided at input B to output O, while de-assertion (or non-assertion) of selector input S sends a signal provided at input A to output O. Asymmetric multiplexer circuit 1400 is organized as two logical halves: an AND half on the left and an A-NOT-B half on the right. Selector input S splits between left and right paths from Josephson junction J2, where it either goes through an inversion via escape Josephson junction J3 to Josephson junction J4A on the right path, or non-inversion through to Josephson junction J4B on the left path.

[0081] Pulse generator Josephson junctions JP1 and JP2, fed with an AC bias from AC bias source 1402, aid in the inversion process at escape Josephson junction J3. Pulse generator Josephson junctions JP1 and JP2 are biased to spontaneously trigger positively and reciprocally every clock cycle. When selector input S is asserted “high” with a positive SFQ pulse,

Josephson junction J2 triggers, splitting bias current toward both left and right paths. This bias current, combined with clock pulse current via Josephson junctions JP1 and JP2, causes escape Josephson junction J3 to trigger, eliminating provision of a pre-critical bias current to Josephson junction J4A that would otherwise permit SFQ pulses applied at input A to propagate left and out through output O. The pulse generator portion of circuit 1402 formed from Josephson junctions JP1 and JP2 and AC bias source 1402, combined with escape Josephson junction J3, effectively performs a NOT-S inversion of the selector signal in order to provide multiplexer functionality. On the left side of circuit 1400, when selector input S is asserted, bias current from Josephson junction J2 applies a pre-critical bias current to Josephson junction J4B, thus permitting SFQ pulses applied at input B to triggers Josephson junction J4B, in turn triggering Josephson junction J5B, and sending the B-input pulses out the output.

[0082] When selector input S is unasserted (“low”) to select input A as the source for output O, Josephson junction J2 does not trigger, such that, on the left side of the circuit, Josephson junction J4B is deprived of biasing current needed to allow pulses provided at input B to propagate rightward toward output O, and such that, on the right side of the circuit, the pulse generator at upper right provides bias to Josephson junction J4A so that pulses introduced at input A are propagated to output O. In contrast to an RQL multiplexer circuit made from primitive AND and inverter gates, circuit 1400 greatly improves component economy and thus circuit density and cost.

[0083] As another example, FIG. 15 illustrates an AND-OR gate circuit 1500 provided as a combination of two AND primitive gates (as shown in FIG 17) with the outputs logically OR’d together in a similar fashion to what is demonstrated with multiplexer 1400 of FIG. 14. Instead of having selector input S, as in circuit 1400 of FIG. 13, AND-OR gate circuit 1500 has two inputs at the top, input C and input D, to provide the logical function $O = (A \text{ AND } D) \text{ OR } (B \text{ AND } C)$. No inversion is needed on either input C or D, so the circuit does not include the pulse generator portion found in multiplexer circuit 1400. Assertion of input C with a positive SFQ pulse to send that input “high” enables pulses provided at input B to

propagate to output O. Likewise, assertion of input D with a positive SFQ pulse to send that input “high” enables pulses provided at input A to propagate to output O.

[0084] As yet another example, FIG. 16 illustrates a demultiplexer gate circuit 1600 similar in structure to multiplexer 1400 of FIG. 14 but with the direction of the data path reversed, such that output O from multiplexer circuit 1400 is arranged instead as data input DI in demultiplexer circuit 1600, and inputs A and B from circuit 1400 are arranged as outputs OA and OB, respectively, in demultiplexer circuit 1600. The selector input S remains the same as in circuit 1400. Input DI splits between two paths to Josephson junctions J4A and J4B. Based on the assertion value of the selector input S, SFQ pulses applied at data input DI are propagated either to output OA or to output OB, but not to both. Assertion of selector input S (to send it “high”) bias Josephson junction J4B, and dc-biases Josephson junction J4A, allowing signals applied at data input DI propagate to the left, to output OB. Conversely, if select input S is unasserted (“low”), Josephson junction J4B is no longer biased, blocking the propagation of data input signals toward output OB, and biasing Josephson junction J4A with current from the pulse generator portion at the upper right of circuit 1600, such that signals applied at data input DI are steered to the right, to output OA. Demultiplexor 1600 offers simplicity and scalability of use in decoders.

[0085] FIG. 17 provides an AND gate circuit 1700 according to the body-tail topology described herein, where the body stage is reduced to a single input B and associated inductor L1 and Josephson junction J2, which body stage supplies a pre-critical bias current to tail stage Josephson junction J5 via linking inductor LL. With a positive SFQ pulse at input A to assert that input, Josephson junction J5 triggers and produces an output of “1” at output Z, fulfilling the AND logical function of $Z = A \text{ AND } B$.

[0086] FIG. 18 provides an A-NOT-B gate circuit 1800 sharing structural similarities to the multiplexer circuit 1400 described previously. The upper-right portion of the circuit provides a pulse generator signal, indicated in FIG. 18 as “PULSE GEN.,” as a return-to-zero (RZ) tie-high signal. When combined with an assertion signal (“1”) provided at input B, the pulse generator signal causes escape Josephson junction J3 to trigger, thereby starving tail Josephson

junction J5 of a pre-critical bias current that would otherwise allow SFQ pulses provided at input A to propagate to output Z. Thus, when input B is “high,” input A pulses are blocked. In absence of a “1” on input B, circuit 1800 allows for the pulse generator to provide the requisite pre-critical bias current to tail Josephson junction J5, thereby activating input A to trigger tail Josephson junction J5 and thus produce a “1” at the output Z.

[0087] FIG. 19 provides an inverter 1900, otherwise known as a NOT gate, similar in structure to the A-NOT-B gate 1800 of FIG. 18, except that the input A is replaced with a second pulse generator circuit portion that includes Josephson junctions JP1B and JP2B. When combined with an assertion signal (“1”) provided at input I, the first pulse generator signal (from first pulse generator circuit portion including Josephson junctions JP1A and JP2A and AC bias source 1902) causes escape Josephson junction J3 to trigger, thereby starving tail Josephson junction J5 of a pre-critical bias current that would otherwise allow second pulse generator SFQ pulses provided from second pulse generator (including Josephson junctions JP1B and JP2B and AC bias source 1904) to propagate to output Z. Thus, when input I is “high,” pulses are blocked from output Z, and when input I is “low,” pulses are propagated to output Z. As such, circuit 1900 accomplishes RQL signal inversion at a relatively low component cost of seven Josephson junctions and nine inductors, plus those in any output JTL (as illustrated) and without requiring any physically large and high-efficiency transformers as may be involved in other RQL inverter designs.

[0088] FIG. 20 displays an oscilloscope screen capture 2000 from a successful test of latch-based NDRO circuit 700. The waveforms on the upper half of the plot 2002 show the I and Q clock, while the waveform on the lower half of the plot 2004 show the non-destructive readout output. The oscilloscope screen capture demonstrates the correct response from an NDRO memory cell to a series of commands switching the D-latch from a logical “0” state to a logical “1” state under a variety of half-select and full-select conditions on back-to-back clock cycles. This also includes simultaneous operations of write and read within same cycle. There are a total of eight read commands: four while storing a logical “0” state and four of a logical “1”

state, resulting in the four logical “1” outputs 2006 that are displayed. The series of commands is repeated three times, 2006, 2008, 2010, for the screen capture shown.

[0089] Circuits 100, 700, 900, 1100, and 1200 can form the basis of RQL register file or other memory designs. In particular, the dual-port (or, more generally, multi-port) read functionality of circuits 100, 900, and 1200 provide the capability greatly simplify register files for CPUs and caches, which require such multi-port output. These circuits therefore enable much more compact register file architectures than previously possible. A “register file” is a hardware array of processor registers in a central processing unit (CPU). Apart from memory, register files are very close to the computation unit in the CPU layout and they require very fast access and multiple ports, reading in many directions. When a circuit 100, 700, 900, 1100, or 1200 serves as a memory element in an array of such circuits, DI can serve as a data input, LCLK can serve as a word write enable, and NDRO can serve as a word read enable. Word write enable lines and word read enable lines can run parallel across the bit-length of a word in the memory. These signals can run orthogonal to the write bit lines and read bit lines, which can run along the word dimension. Thus, in an array of such memory elements, word write enable lines can be connected to LCLK inputs of the respective elements and word read enable lines can be connected to NDRO inputs of the respective elements, while bit write data lines can be connected to the DI inputs of the respective elements, and bit read data lines can be connected to the QO outputs of the respective elements (to use the signal line nomenclature of FIGS. 6-7).

[0090] Thus, FIG. 21 shows an example of an array 2100 of multi-tail NDRO gates 2102 arranged as memory or logic elements, each of which can correspond, for example, to any of circuits 100, 900, 1200, or a multi-tail version of circuit 1300 as described above. Each gate 2102 can have a body B and multiple tails T. Read lines are illustrated as solid and write lines are illustrated as dashed. Word lines are illustrated as thin horizontal lines and bit lines are illustrated as thick vertical lines. Word read enable lines 2104 are represented as thinner solid lines each connecting to the NDRO inputs of tails T in a row. Word write enable lines 2106 are represented as thinner broken lines each connecting to the LCLK inputs of bodies B in a row. Bit read data lines 2108 are represented as thicker solid lines each connecting to the QO outputs

of tails T in a column. Bit write data lines 2110 are represented as thicker broken lines each connecting to the DI inputs of bodies B in a column. While the bit lines are defined as columns and word lines as rows in this particular image, this arrangement is arbitrary and could be reversed. Other connections (e.g., for AC clocks or ground) are omitted from FIG. 21 for clarity. The array 2100 can be of any suitable size (i.e., having any number of columns and rows), and can be used as a memory or as a logic array, e.g., a programmable logic array (PLA) or field-programmable gate array (FPGA) to output evaluated logic functions. In the illustrated example of FIG. 21, two word read enable lines 2104 are associated with each row of NDRO gates 2102 and two bit read data lines 2108 are associated with each column of NDRO gates 2102, but the number of such lines can correspond to the number of tails in each NDRO gate 2102 and thus can be fewer or greater than two.

[0091] The examples described herein provide for memory cells, logic cells, registers, register files, memory arrays, logic arrays, logic gates, and logic structures of higher performance, higher speed, reduced device count (e.g., fewer Josephson junctions and inductors), and greater functionality than existing designs. The examples provide efficient, compact cells for AND, A-NOT-B, and inverter logical functions, and for gates such as multiplexer, demultiplexer, and AND-OR gates. The examples also lead to more compact memory unit cells demanding less resources with increased functionality (e.g., the capability to write and read at the same time).

[0092] The NDRO circuits and other gates described herein have very good parametric operating margins, a low component count, and provide efficiency and cost advantages as compared to other implementations. As one example, by eliminating high-efficiency transformers as compared to other designs, the NDRO circuits and other gates described herein can save a number of metal layers, e.g., two metal layers, in the fabrication process, which sets the number of process steps and yield and thereby determines cost. As another example, by not using non-transformer-based, direct-coupled designs that contain negligible numbers of transformers, the NDRO circuits and other gates described herein avoid high device counts and large inductances.

[0093] What have been described above are examples of the invention. It is, of course, not possible to describe every conceivable combination of components or methodologies for purposes of describing the invention, but one of ordinary skill in the art will recognize that many further combinations and permutations of the invention are possible. Accordingly, the invention is intended to embrace all such alterations, modifications, and variations that fall within the scope of this application, including the appended claims. Additionally, where the disclosure or claims recite “a,” “an,” “a first,” or “another” element, or the equivalent thereof, it should be interpreted to include one or more than one such element, neither requiring nor excluding two or more such elements. As used herein, the term “includes” means includes but not limited to, and the term “including” means including but not limited to. The term “based on” means based at least in part on.

CLAIMS

What is claimed is:

1. A reciprocal quantum logic (RQL) non-destructive readout (NDRO) gate comprising:
a body circuit having at least one single flux quantum (SFQ) logical input, the body circuit being configured to store at least one logical state; and
at least one tail circuit connected to the body circuit, the at least one tail circuit comprising:
a tail input inductor connected between an NDRO read-enable input port and the body circuit and configured to receive an SFQ pulse NDRO read-enable signal on the NDRO read-enable input port;
a tail Josephson junction connected between the body circuit and a circuit ground;
and
a tail output inductor connected between the body circuit and an NDRO output port and configured to transmit an SFQ pulse NDRO output signal based on the stored logical state and the NDRO read-enable signal without affecting the stored logical state.
2. The NDRO gate of claim 1, wherein the at least one tail circuit is configured to receive the logical state from the body circuit as a pre-critical state bias current that biases the tail Josephson junction to trigger upon receipt of the NDRO read-enable signal and thereby to propagate the NDRO output signal to the NDRO output port.
3. The NDRO gate of claim 1, wherein the at least one tail circuit comprises no more than one Josephson junction and no more than two inductors, exclusive of any output Josephson transmission line (JTL) connected to the tail output inductor.
4. The NDRO gate of claim 1, comprising exactly two tail circuits providing exactly two NDRO read-enable input ports and exactly two NDRO output ports, the tail circuits being configured to respectively transmit an SFQ pulse NDRO output signal based on the same stored logical state but on different respective NDRO read-enable signals provided from the respective NDRO read-enable input ports.

5. A register file comprising an array of multiple instances of the NDRO gate of claim 4.
6. The NDRO gate of claim 1, wherein the body circuit comprises a D latch having a data input port and a logical clock input port each configured to receive SFQ pulses.
7. The NDRO gate of claim 6, wherein the D latch comprises:
 - a data input inductor connected between the data input port and a first node;
 - a data input Josephson junction connected between the first node and the circuit ground;
 - a state storage Josephson junction connected between a second node and the circuit ground;
 - a first DC flux bias transformer connected between a third node and the first node and to a DC flux bias line;
 - a second DC flux bias transformer connected between the second node and the third node and to the DC flux bias line;
 - a logical clock input inductor connected between the logical clock input port and a fourth node;
 - an escape Josephson junction connected between the fourth node and the second node;
 - and
 - at least one linking inductor connected between the third node and the at least one tail circuit,wherein the first and second DC flux bias transformers are configured to provide at an initialization time a fraction of a Φ_0 of phase to the data input Josephson junction and the state storage Josephson junction.
8. The NDRO gate of claim 7, wherein the D latch comprises at least two linking inductors connected between the third node and respective at least two tail circuits.
9. The NDRO gate of claim 6, wherein the D latch comprises:
 - a data input inductor connected between the data input port and a first node;
 - a data input Josephson junction connected between the first node and the circuit ground;

a state storage Josephson junction connected between a second node and the circuit ground;
 only a single DC flux bias transformer connected between the second node and the first node and to a DC flux bias line;
 a logical clock input inductor connected between the logical clock input port and a fourth node;
 an escape Josephson junction connected between the fourth node and the second node;
 a first linking inductor connected between the first node and the at least one tail circuit;
 and
 a second linking inductor connected between the second node and the at least one tail circuit,
 wherein the single DC flux bias transformer is configured to provide at an initialization time a fraction of a Φ_0 of phase to the data input Josephson junction and the state storage Josephson junction.

10. The NDRO gate of claim 9, wherein the gate comprises at least two tail circuits, and wherein the D latch further comprises:

a third linking inductor connected between the first node and a second tail circuit; and
 a fourth linking inductor connected between the second node and the second tail circuit.

11. The NDRO gate of claim 1, wherein the body circuit comprises a D flip-flop having a data input port and a logical clock input port each configured to receive SFQ pulses.

12. The NDRO gate of claim 11, wherein the D flip-flop comprises:

a data input inductor connected between the data input port and a first node;
 a data input Josephson junction connected between the first node and the circuit ground;
 a state storage Josephson junction connected between a second node and the circuit ground;
 a first inductor connected between a third node and the first node;
 a second inductor connected between the second node and the third node;

a logical clock input inductor connected between the logical clock input port and a fourth node;
an escape Josephson junction connected between the fourth node and the second node;
and
at least one linking inductor connected between the third node and the at least one tail circuit,
wherein the D flip-flop does not include a DC flux bias transformer connected to a DC flux bias line.

13. The NDRO gate of claim 1, configured as a multiplexer, comprising exactly two tail circuits having their respective output ports both connected to a single output, and wherein the body circuit comprises a pulse generator comprising two Josephson junctions and an AC bias source, and wherein a logical input to the body provides a selector signal that selects between:

a signal arriving on an input port of a first of the two tail circuits being propagated to the single output, or

a signal arriving on an input port of a second of the two tail circuits being propagated to the single output.

14. The NDRO gate of claim 1, configured as an AND-OR gate, comprising exactly two tail circuits having their respective output ports both connected to a single output, and wherein the body circuit comprises two logical inputs configured such that:

an assertion of a first of the two logical inputs permits a signal arriving on an input port of a first of the two tail circuits to be propagated to the single output, and

an assertion of a second of the two logical inputs permits a signal arriving on an input port of a second of the two tail circuits to be propagated to the single output.

15. The NDRO gate of claim 1, configured as an AND gate, the gate having only a single tail circuit, and wherein the body circuit consists solely of:

a logical input inductor connected between a logical input port and a first node;

a state relay Josephson junction connected between the first node and the circuit ground;

and

a linking inductor connected between the first node and the single tail circuit,
wherein the tail circuit outputs a signal representing a logical AND of the NDRO read-enable signal and a body input signal provided at the logical input port of the body circuit.

16. The NDRO gate of claim 1, configured as an A-NOT-B gate, the gate having only a single tail circuit, and wherein the body circuit comprises:

- a logical input inductor connected between a logical input port and a first node;
- a state relay Josephson junction connected between the first node and the circuit ground;
- a second inductor connected between the first node and a second node;
- a pulse generator connected to the second node, comprising two Josephson junctions and an AC bias source, and providing a return-to-zero (RZ) tie-high signal; and
- an escape Josephson junction connected between the second node and the single tail circuit,

wherein the tail circuit outputs a signal representing the NDRO read-enable signal only when a body input signal provided at the logical input port of the body circuit is unasserted.

17. The NDRO gate of claim 1, configured as an inverter, the gate having only a single tail circuit, and wherein the body circuit comprises:

- a logical input inductor connected between a logical input port and a first node;
- a state relay Josephson junction connected between the first node and the circuit ground;
- a second inductor connected between the first node and a second node;
- a first pulse generator connected to the second node, comprising two Josephson junctions and an AC bias source, and providing a return-to-zero (RZ) tie-high signal; and
- an escape Josephson junction connected between the second node and the single tail circuit,

wherein a second pulse generator is connected to the NDRO read-enable input port of the tail circuit, the second pulse generator comprising two other Josephson junctions and another AC bias source and providing a return-to-zero (RZ) tie-high signal as the NDRO read-enable signal, such that the tail circuit outputs a signal representing the logical inversion of a body input signal provided at the logical input port of the body circuit.

18. The NDRO gate of claim 1, configured as a demultiplexer, comprising exactly two tail circuits having their respective input ports both connected to a single data input port, and wherein the body circuit comprises a pulse generator comprising two Josephson junctions and an AC bias source, and wherein a logical input to the body circuit provides a selector signal that selects between:

a signal arriving on the single data input port being propagated to a first output port of a first of the two tail circuits, or

the signal arriving on the single data input port being propagated to a second output port of a second of the two tail circuits.

19. A reciprocal quantum logic (RQL) central processing unit (CPU) comprising:

a memory comprising an array of RQL non-destructive readout (NDRO) gate circuits, each NDRO gate circuit comprising a body circuit comprising one of a D latch or a D flip-flop configured to store a logical state, the body circuit being connected to at least two tail circuits in the NDRO gate circuit and configured to supply a pre-critical state current to a respective tail Josephson junction in each of the at least two tail circuits, each pre-critical state current being representative of the same stored logical state;

wherein each tail circuit is configured to propagate to an NDRO output port of the respective tail circuit an output signal corresponding to the logical AND of the stored logical state with a respective NDRO read enable signal provided to an NDRO input port of the respective tail circuit, and

wherein the propagation of any output signal from any of the tail circuits does not affect the logical state stored in the body circuit connected to said tail circuits.

20. The RQL CPU of claim 19, wherein each NDRO gate circuit in the array is configured to have its logical state both writable and readable in the same operation cycle.

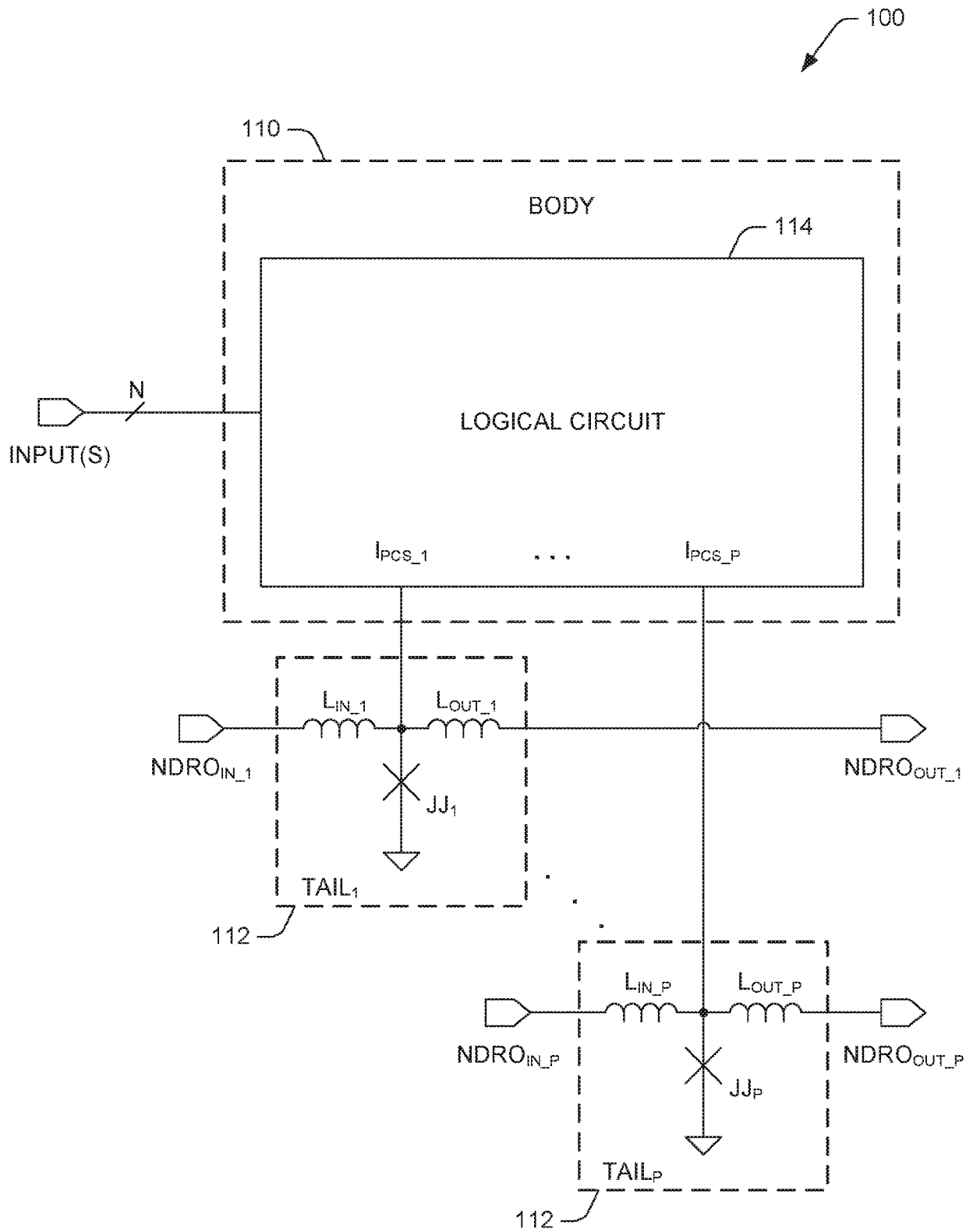
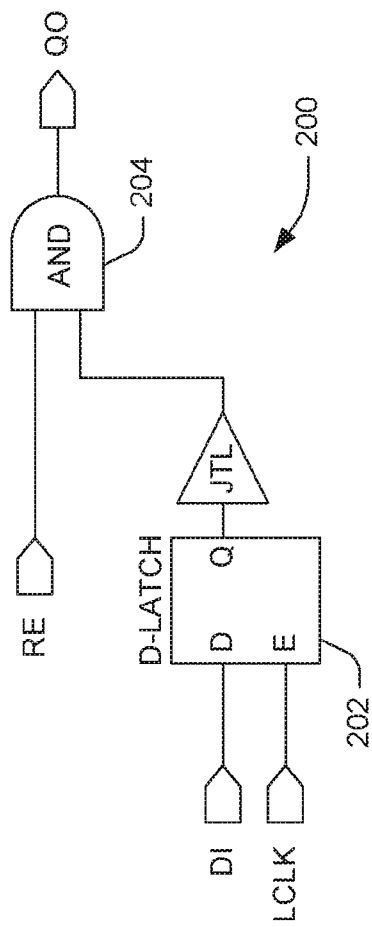
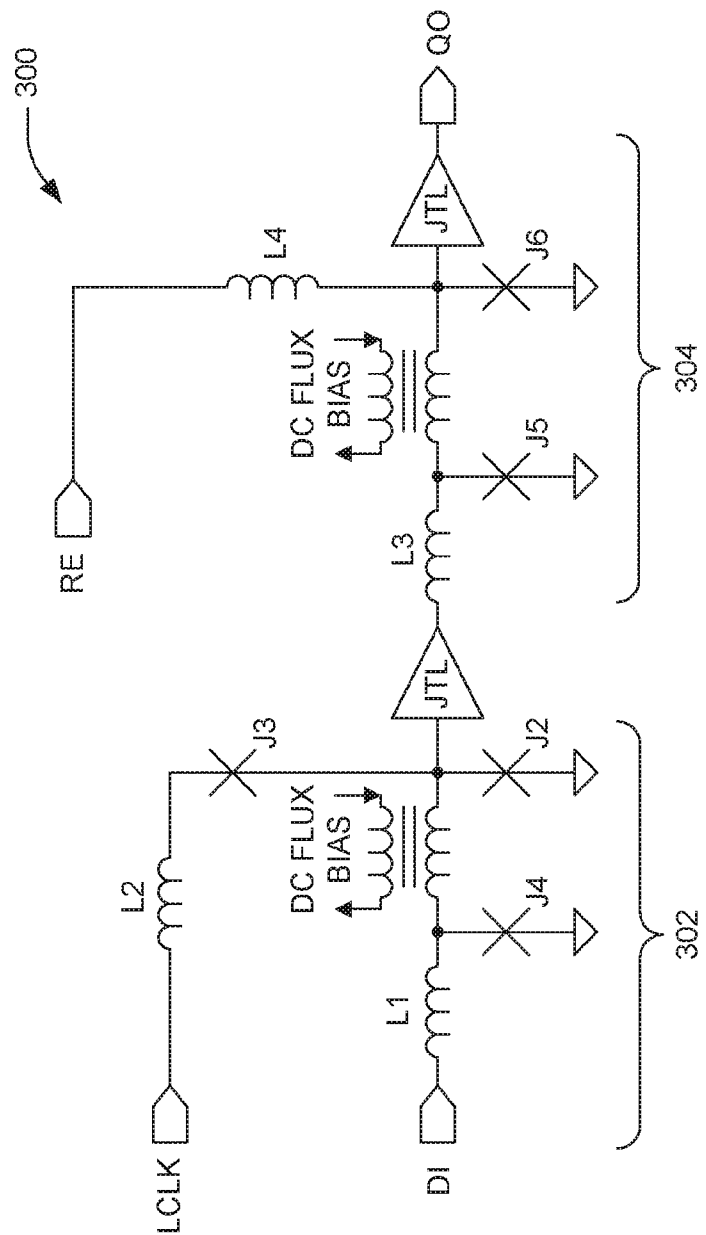
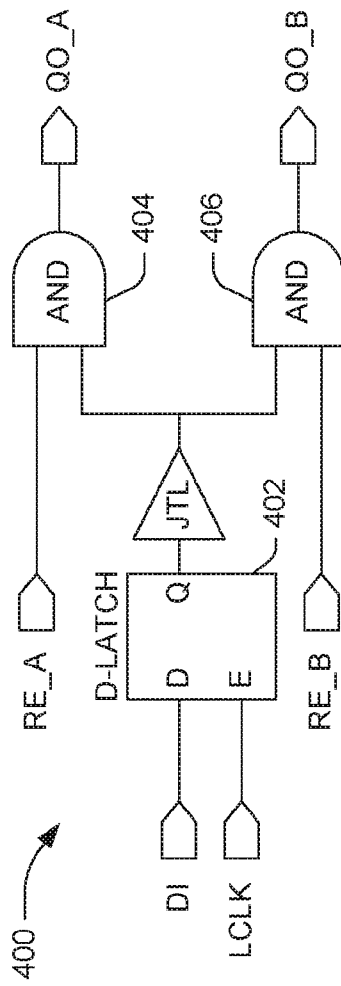


FIG. 1

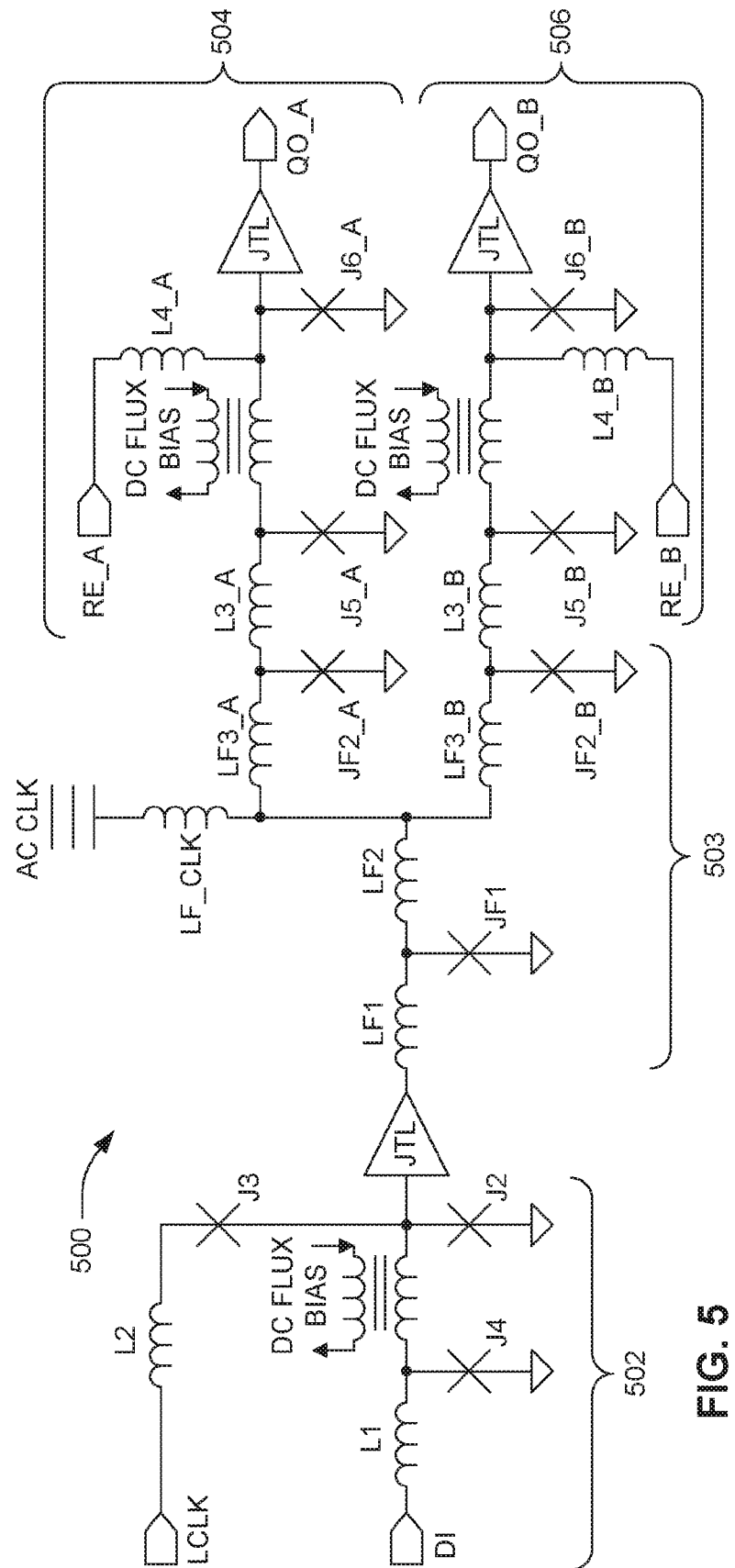


2025









10
11
12
13
14

4/16

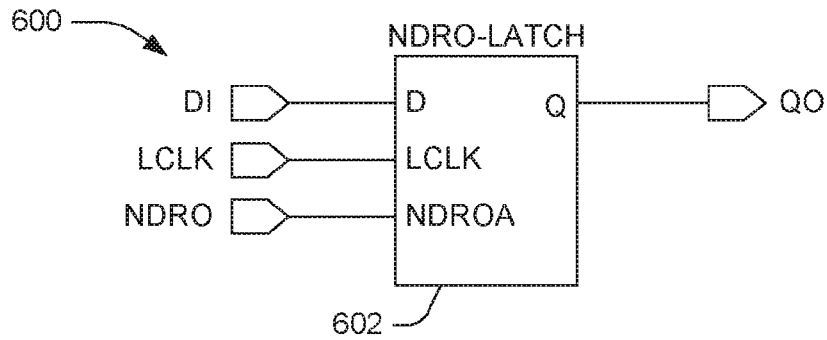


FIG. 6

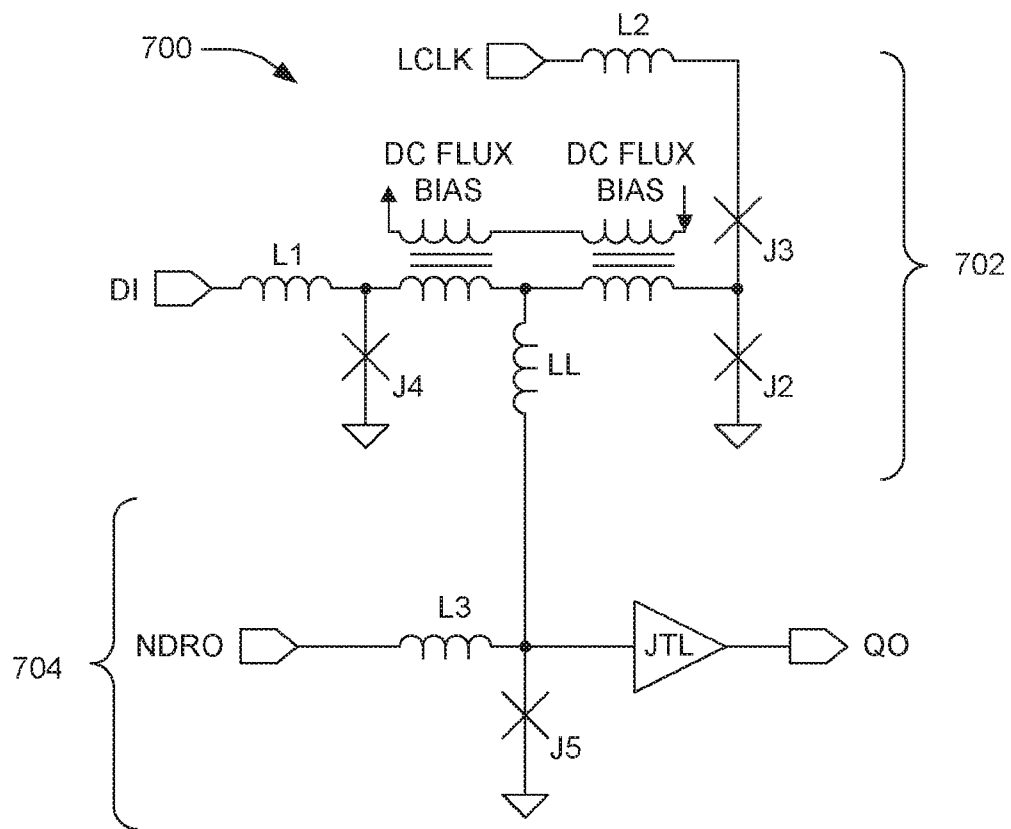
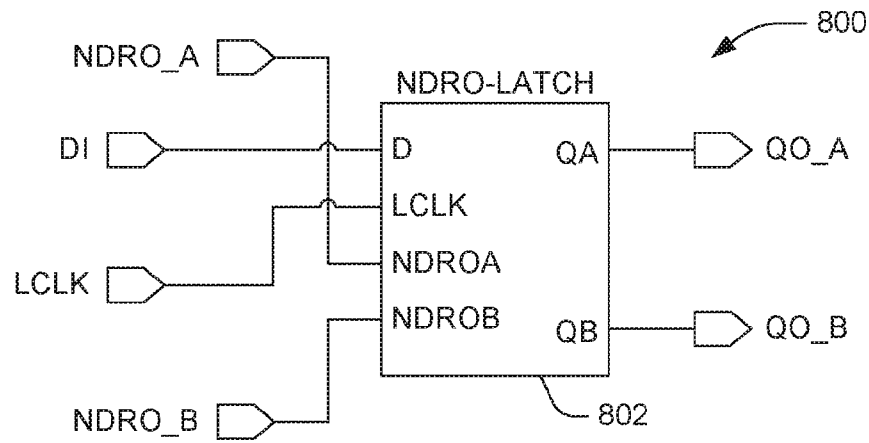
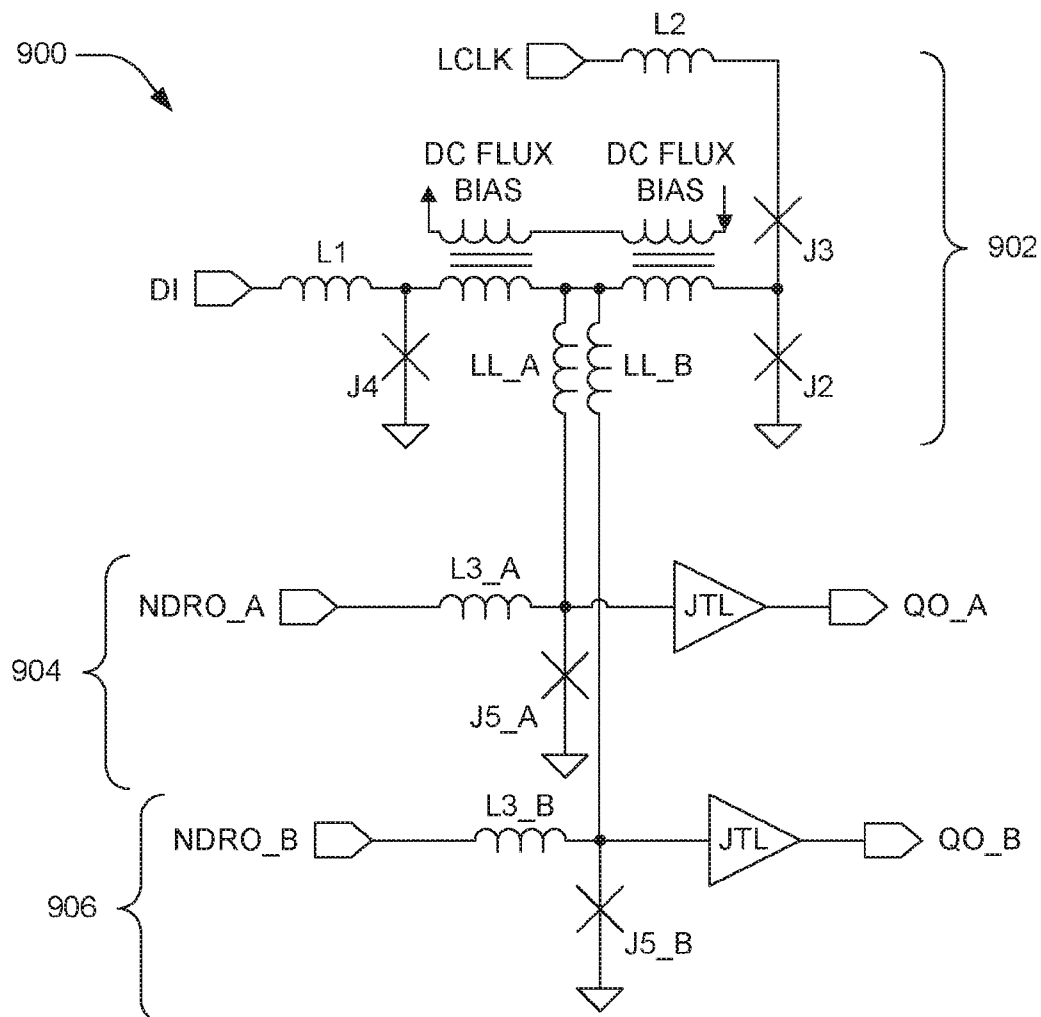


FIG. 7

5/16

**FIG. 8****FIG. 9**

6/16

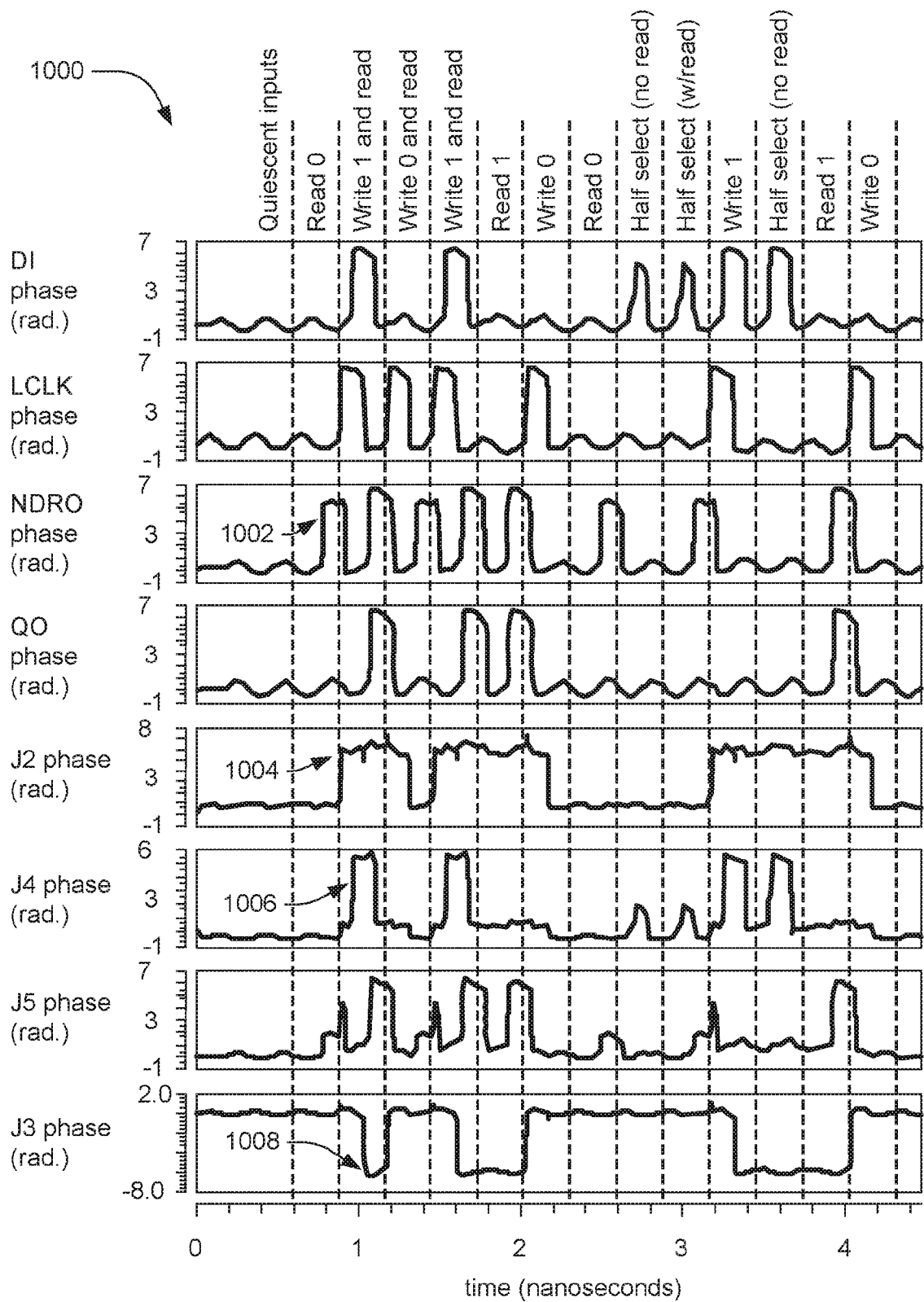


FIG. 10

7/16

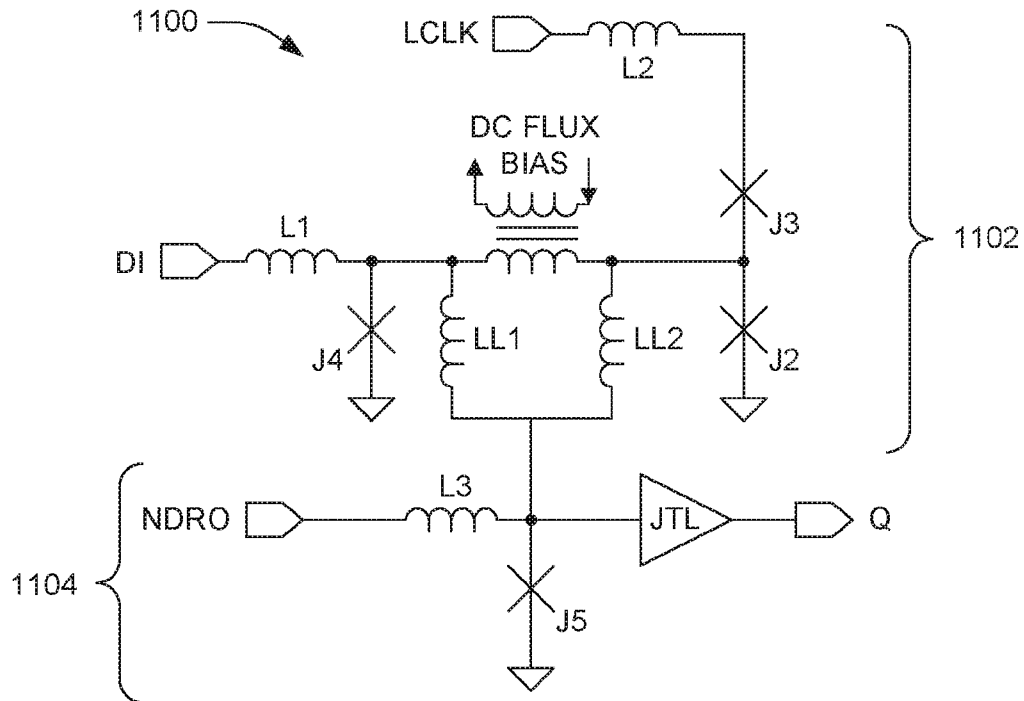


FIG. 11

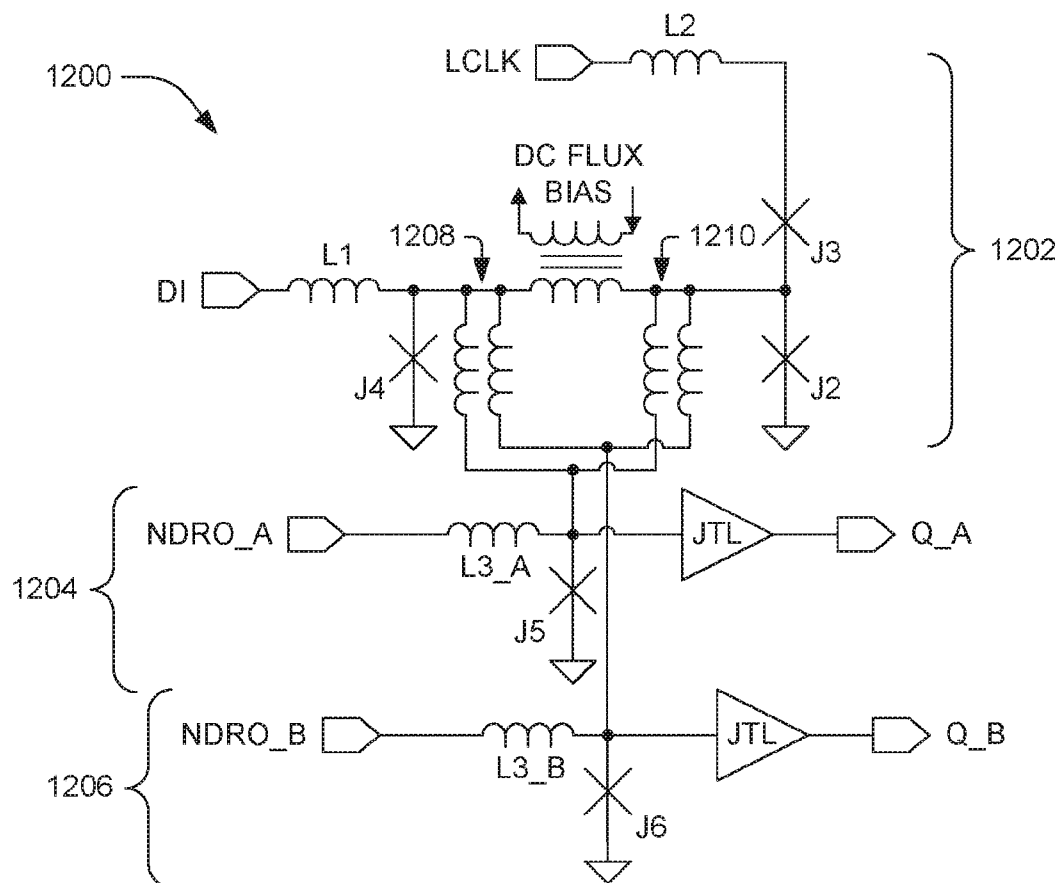


FIG. 12

8/16

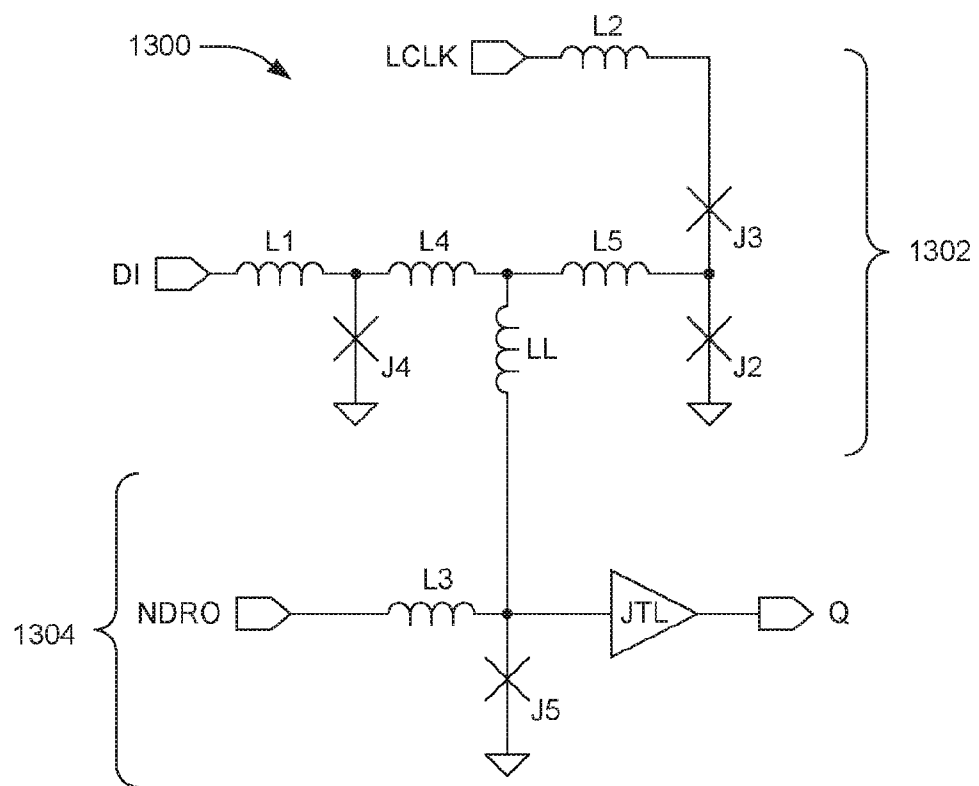


FIG. 13

9/16

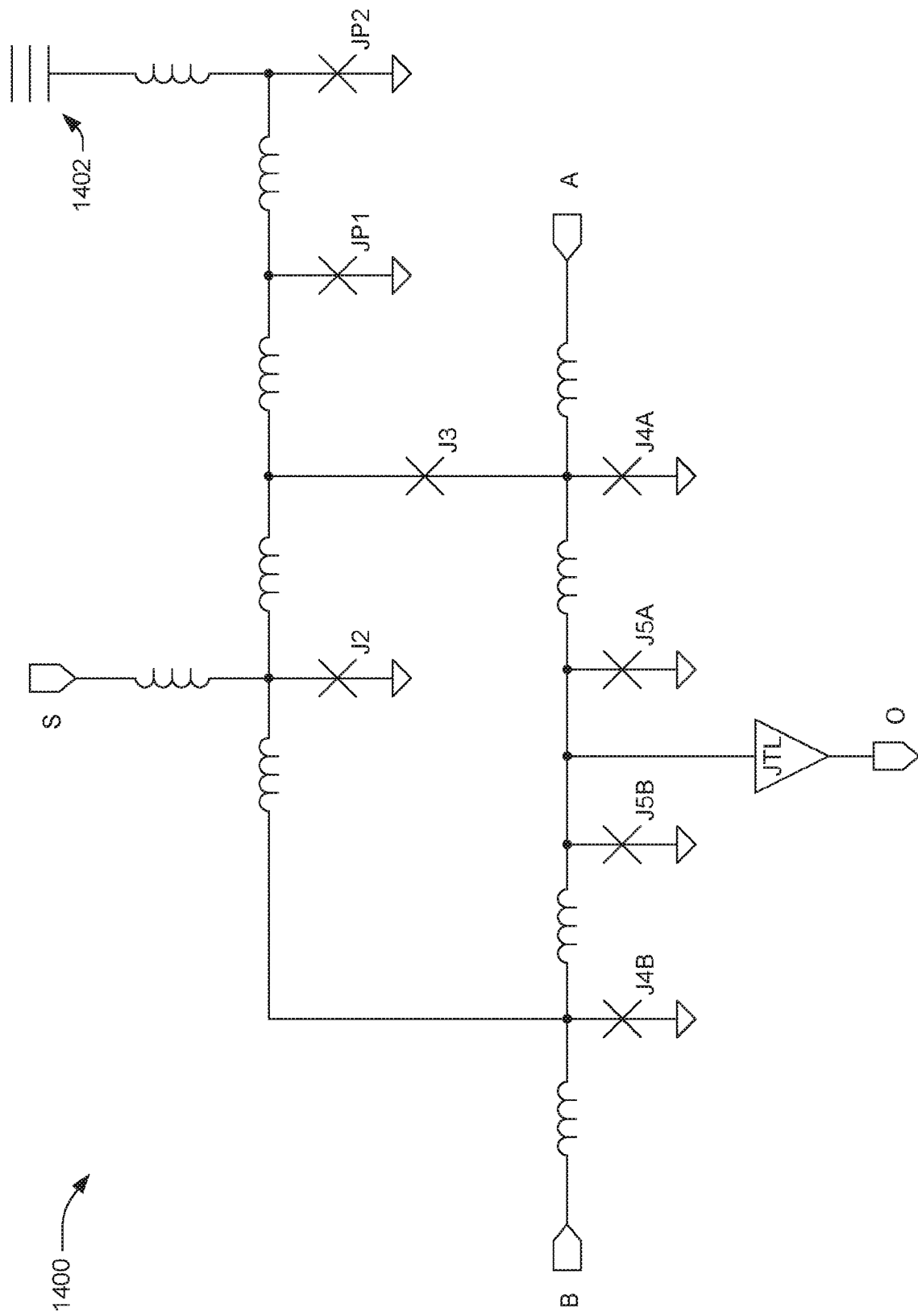


FIG. 14

10/16

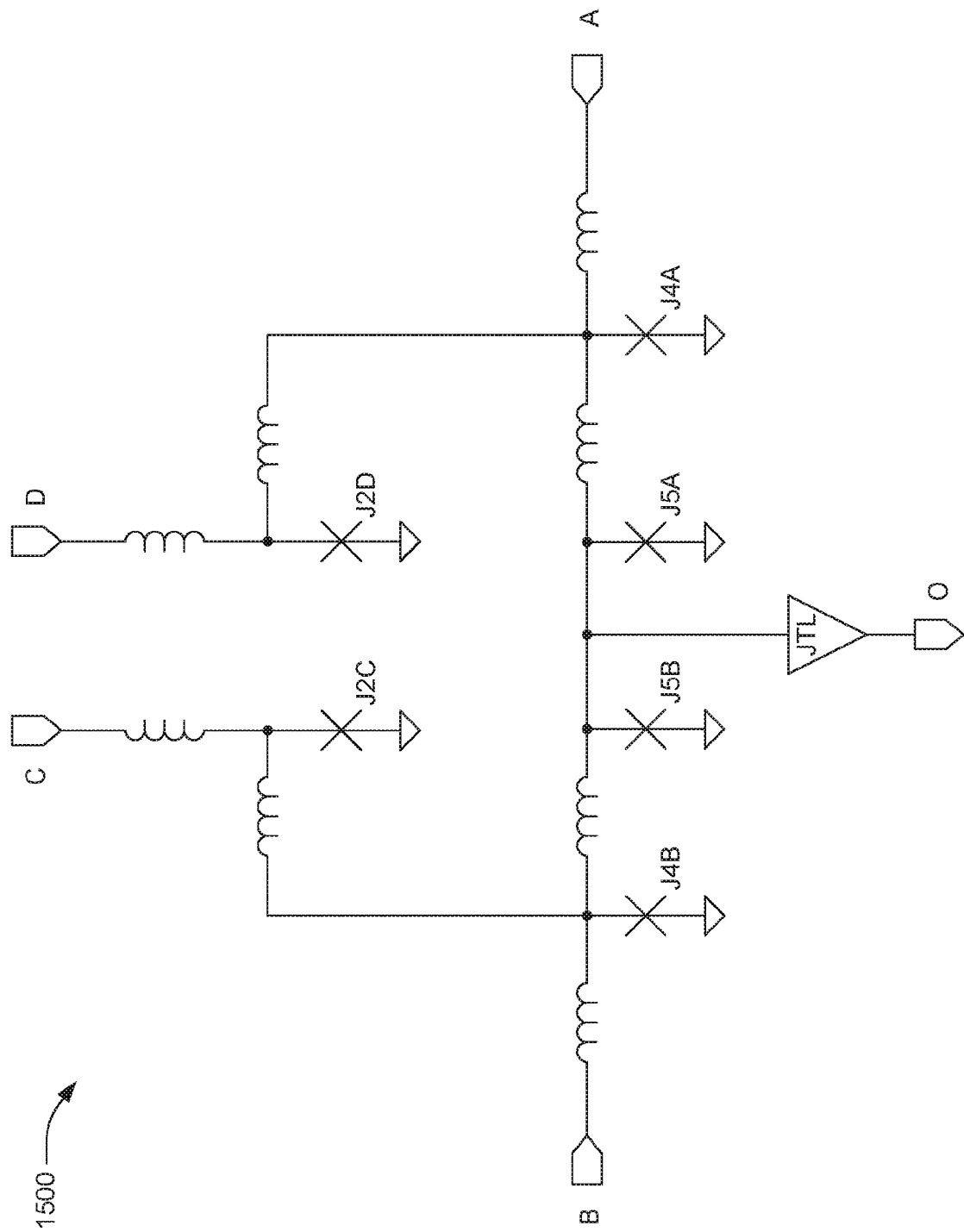


FIG. 15

11/16

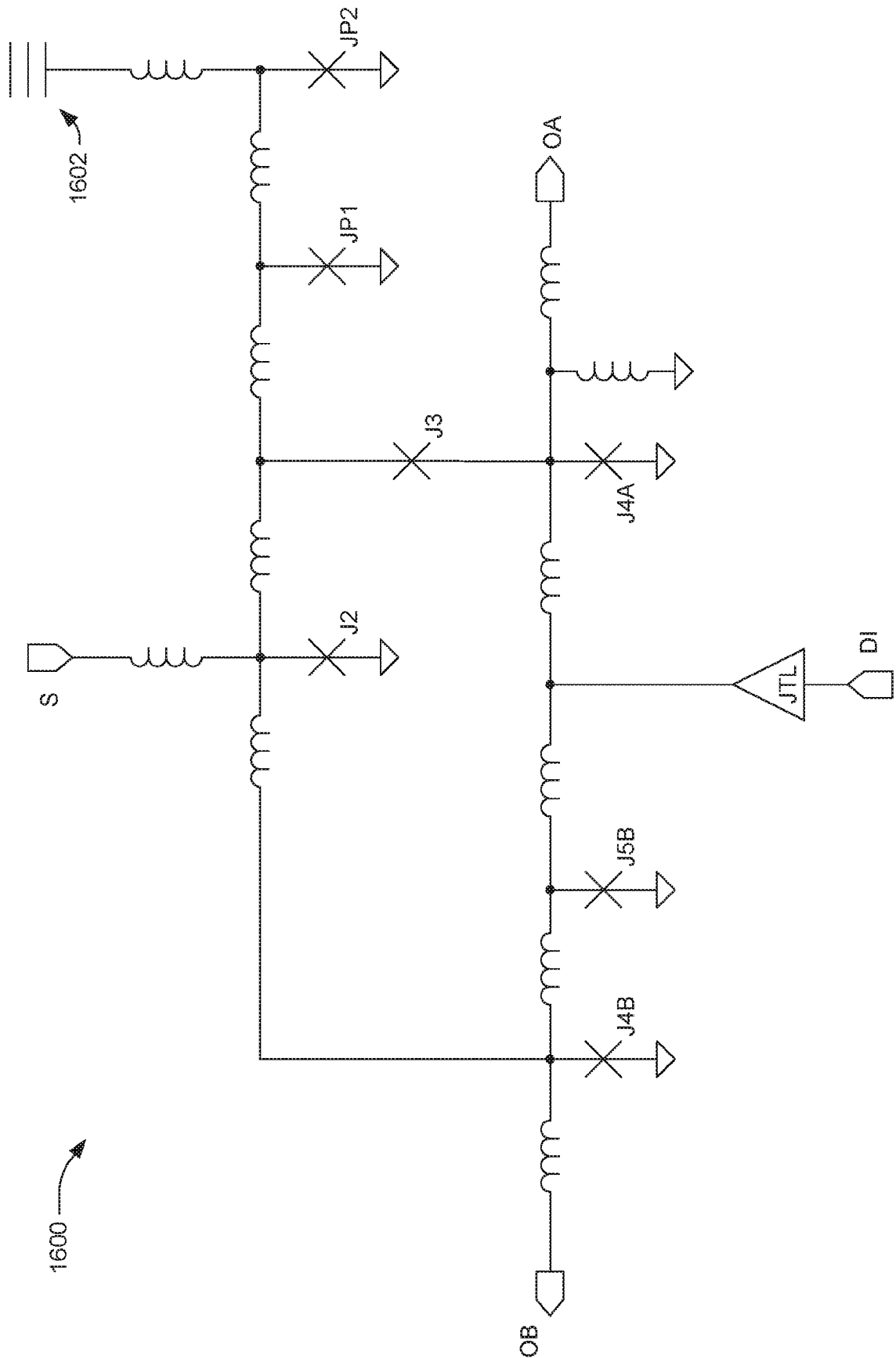


FIG. 16

1700

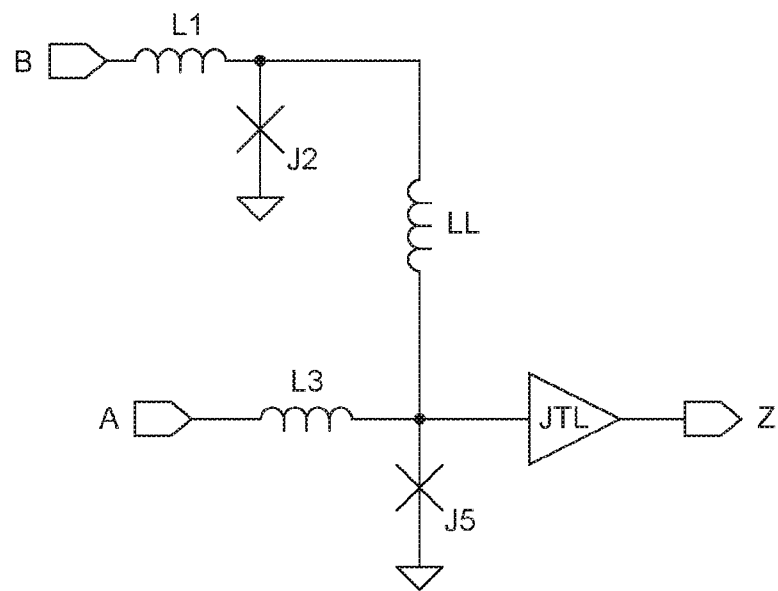


FIG. 17

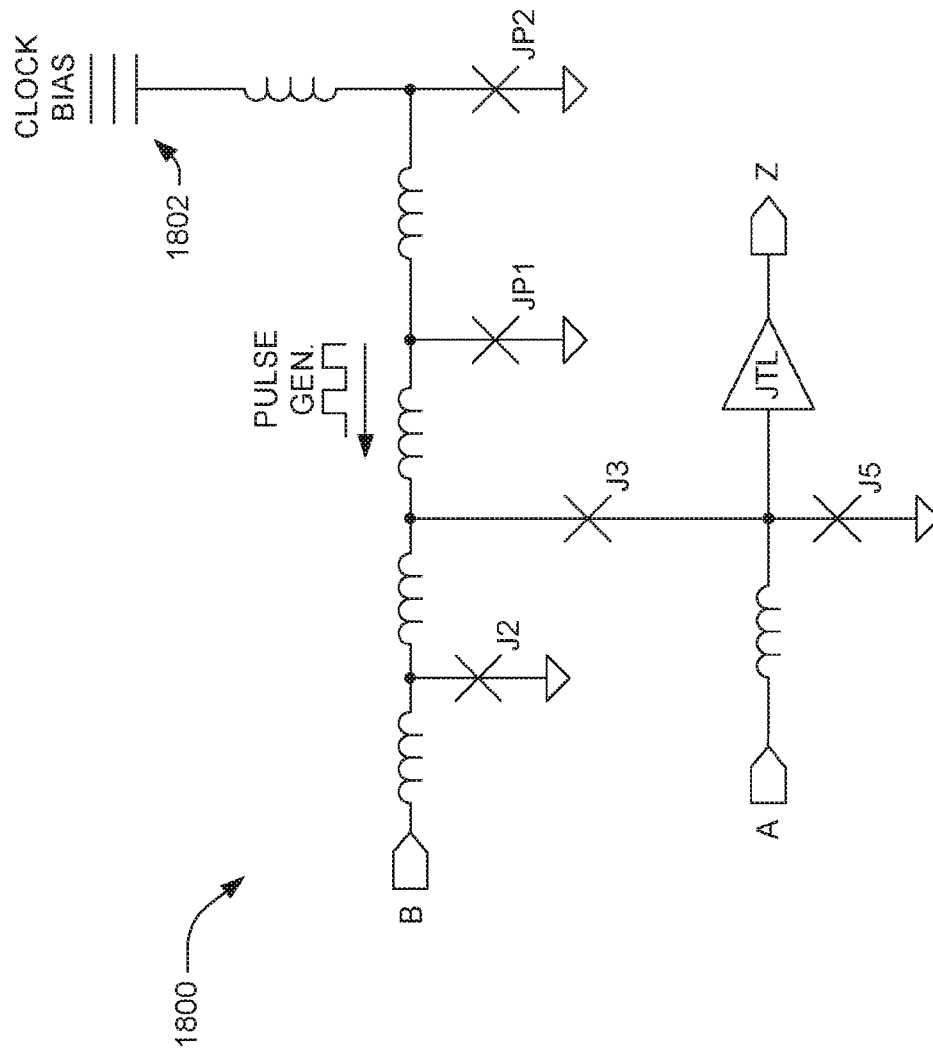


FIG. 18

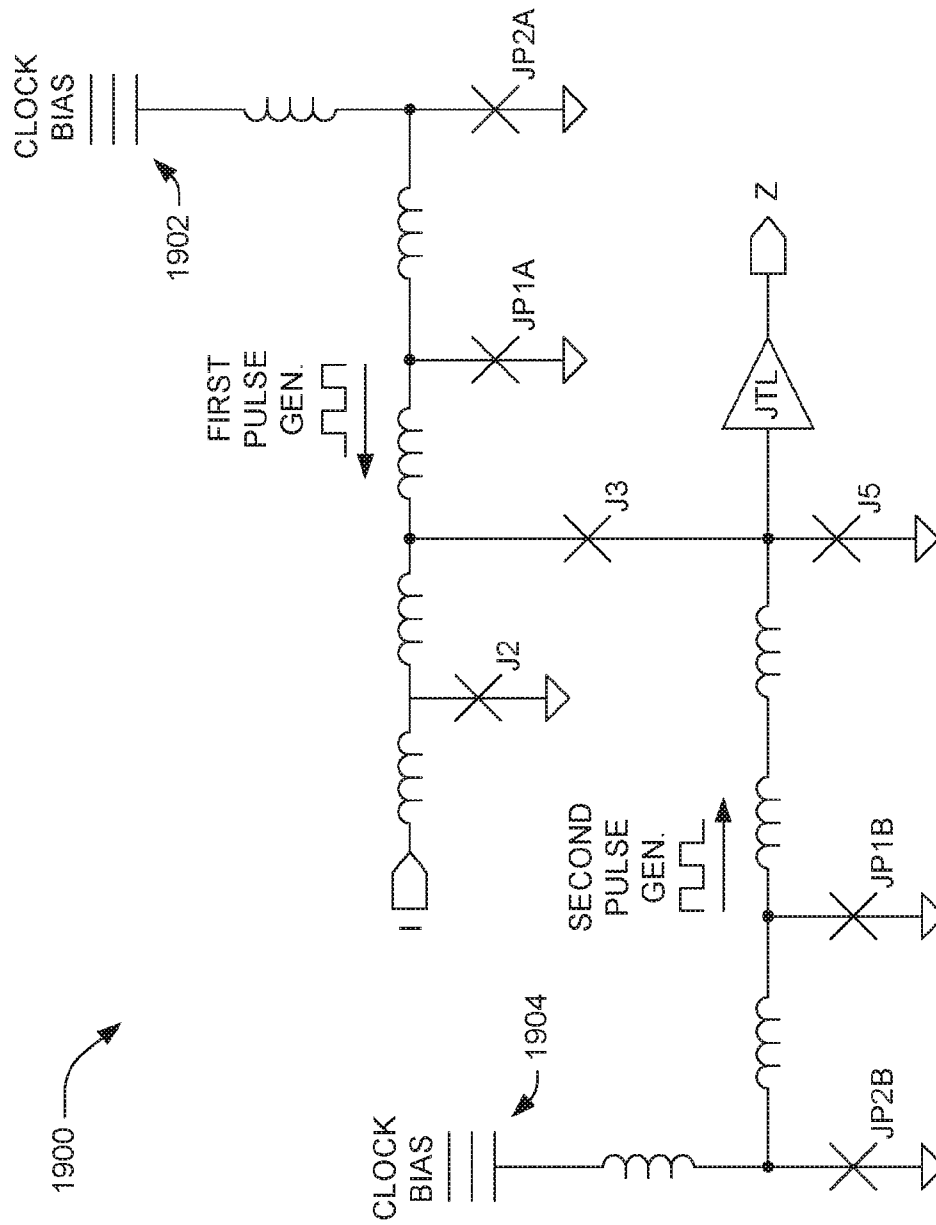


FIG. 19

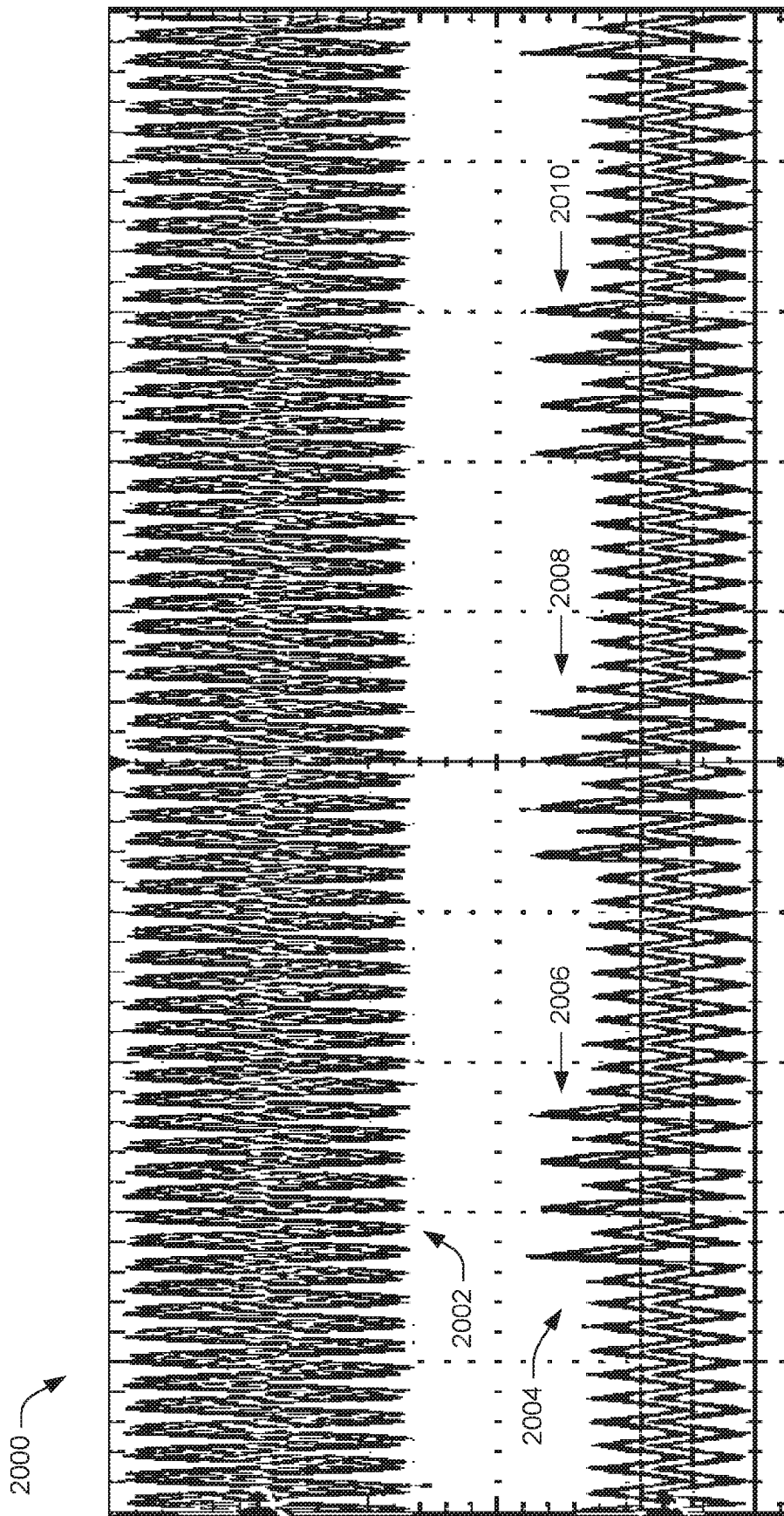


FIG. 20

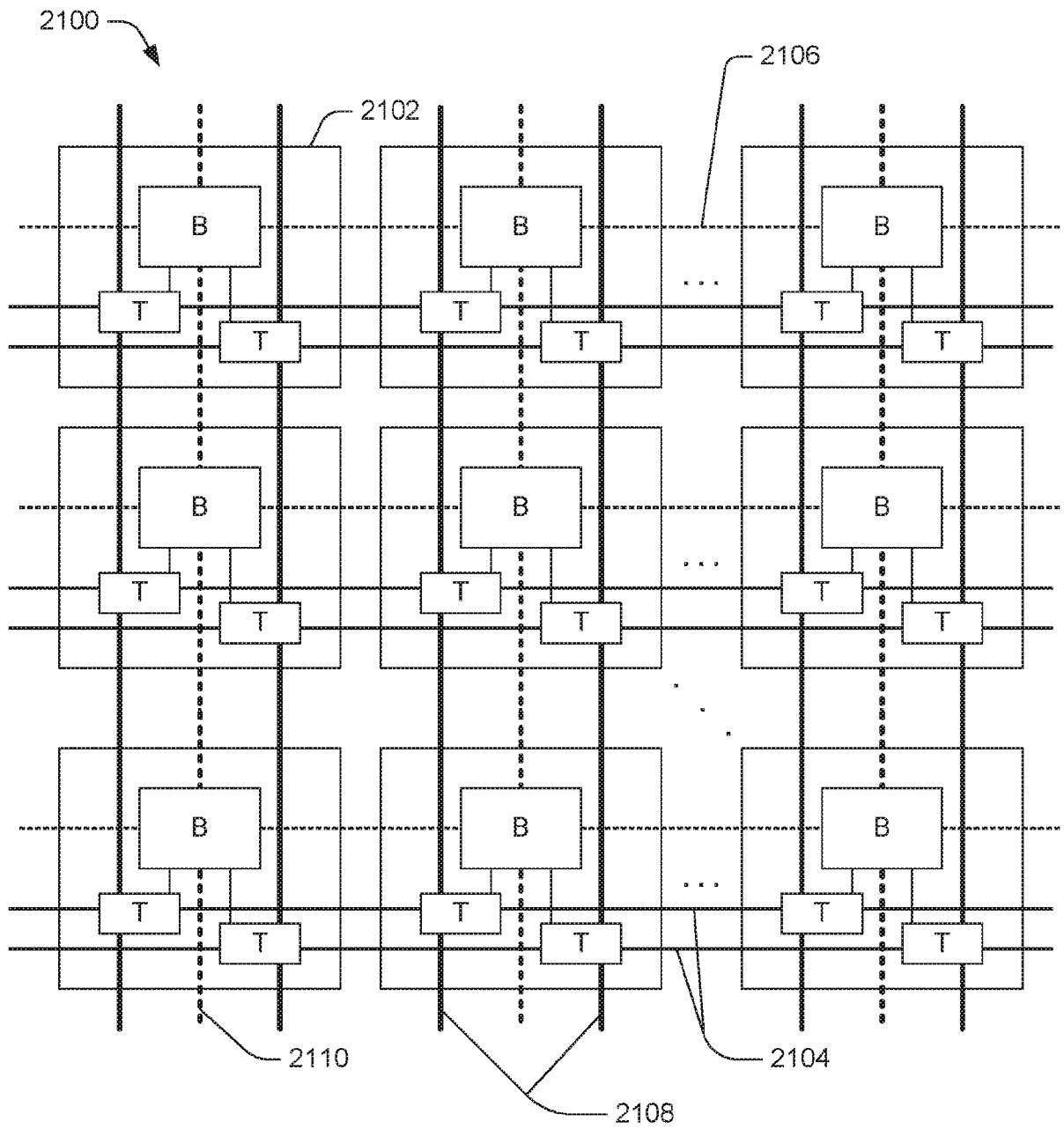


FIG. 21

