US 20070125657A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2007/0125657 A1**

Sun et al. (43) **Pub. Date: Jun. 7, 2007**

(54) **METHOD OF DIRECT PLATING OF COPPER ON A SUBSTRATE STRUCTURE**

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(21) Appl. No.: **11/255,368**

(22) Filed: **Oct. 21, 2005**

Related U.S. Application Data

(63) Continuation-in-part of application No. 11/007,857, filed on Dec. 9, 2004.
Continuation-in-part of application No. 11/012,965, filed on Dec. 15, 2004.
Continuation-in-part of application No. 10/616,097, filed on Jul. 8, 2003.

(60) Provisional application No. 60/621,173, filed on Oct. 21, 2004. Provisional application No. 60/579,129, filed on Jun. 10, 2004. Provisional application No. 60/579,129, filed on Jun. 10, 2004. Provisional application No. 60/621,215, filed on Oct. 21, 2004.

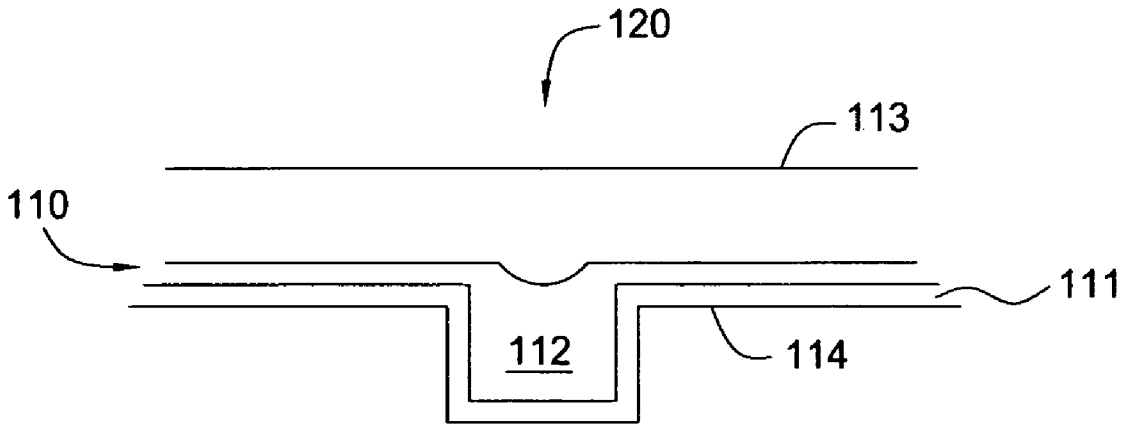
Publication Classification

(51) **Int. Cl.**
C25D 5/34 (2006.01)
C25D 3/38 (2006.01)

(52) **U.S. Cl.** **205/205**; 205/291

(57) **ABSTRACT**

The present invention teaches a method for depositing a copper seed layer onto a substrate surface, generally onto a barrier layer. The barrier layer may include a refractory metal and/or a group 8, 9 or 10 metal. The method includes cathodically pre-treating the substrate in an acid-containing solution. The substrate is then placed into a copper solution (pH≧7.0) that includes complexed copper ions and a current or bias is applied across the substrate surface. The complexed copper ions are reduced to deposit a copper seed layer onto the barrier layer. In one aspect, a complex alkaline bath is then used to electrochemically plate a gapfill layer on the substrate surface, followed by overfill in the same bath. In another aspect, an acidic bath ECP gapfill process and overfill process follow the alkaline seed layer process.



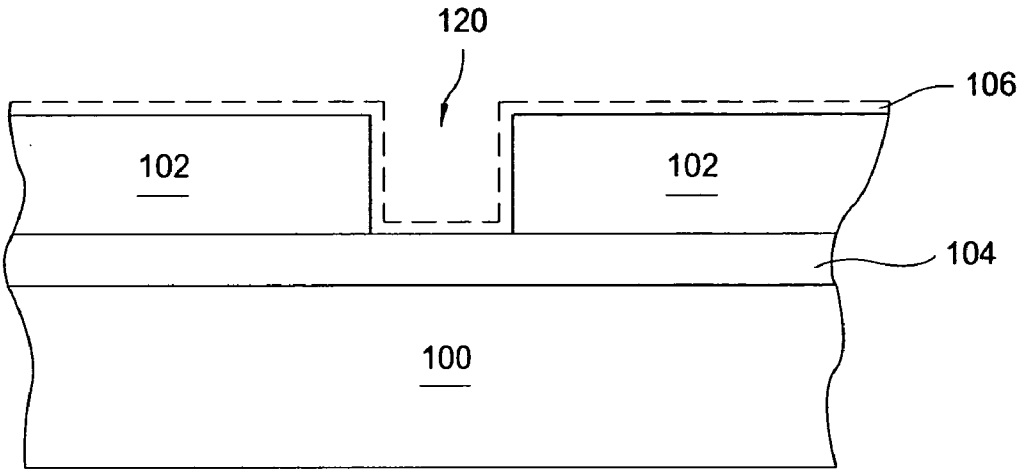


FIG. 1A

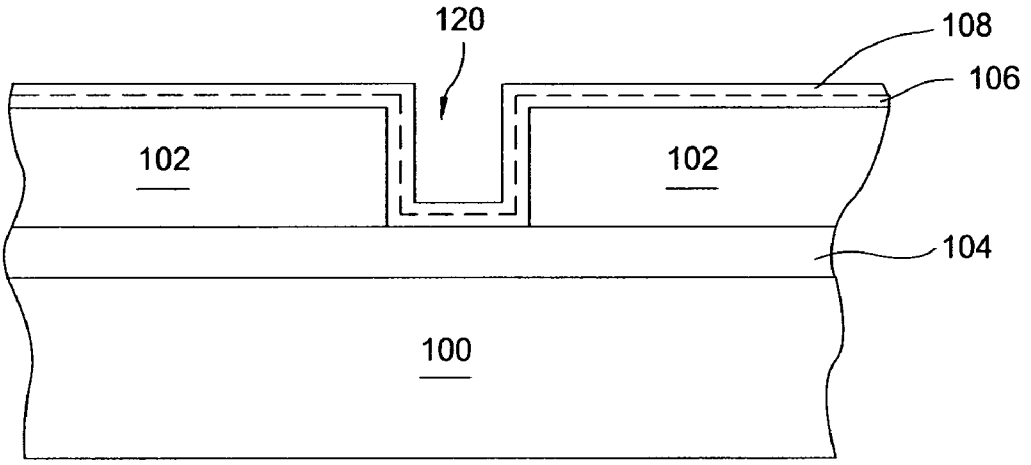


FIG. 1B

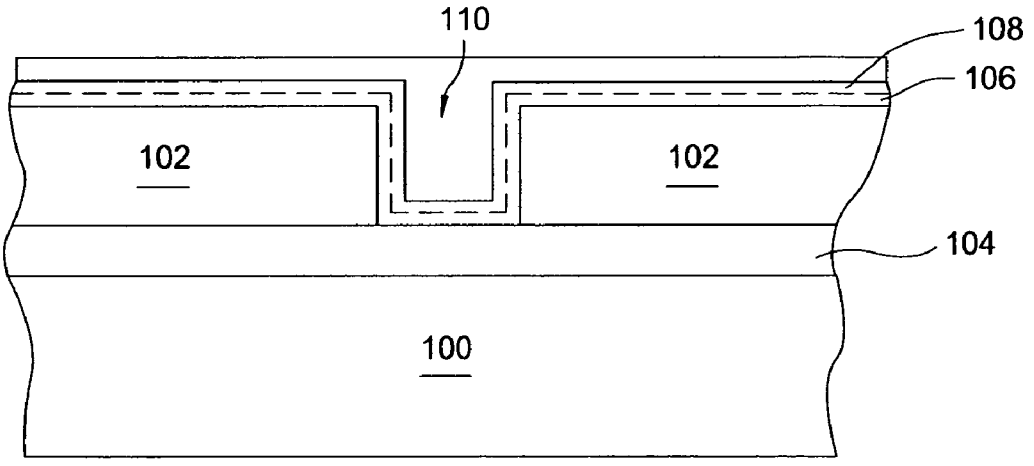


FIG. 1C

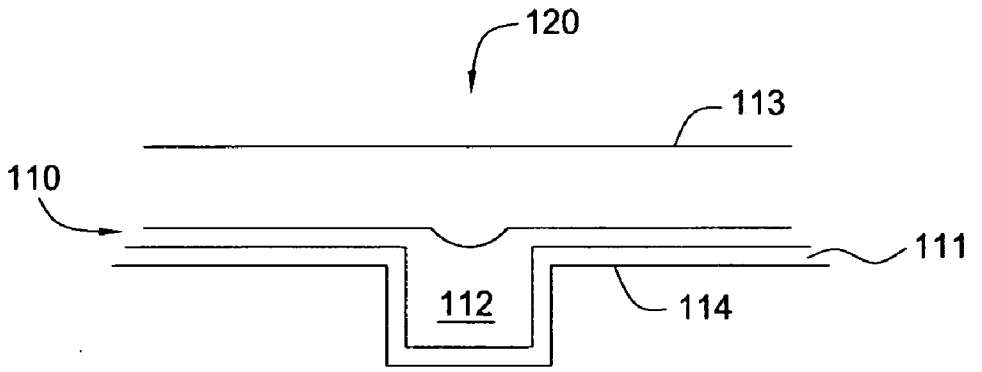

120
113
110
111
112
114

FIG. 2

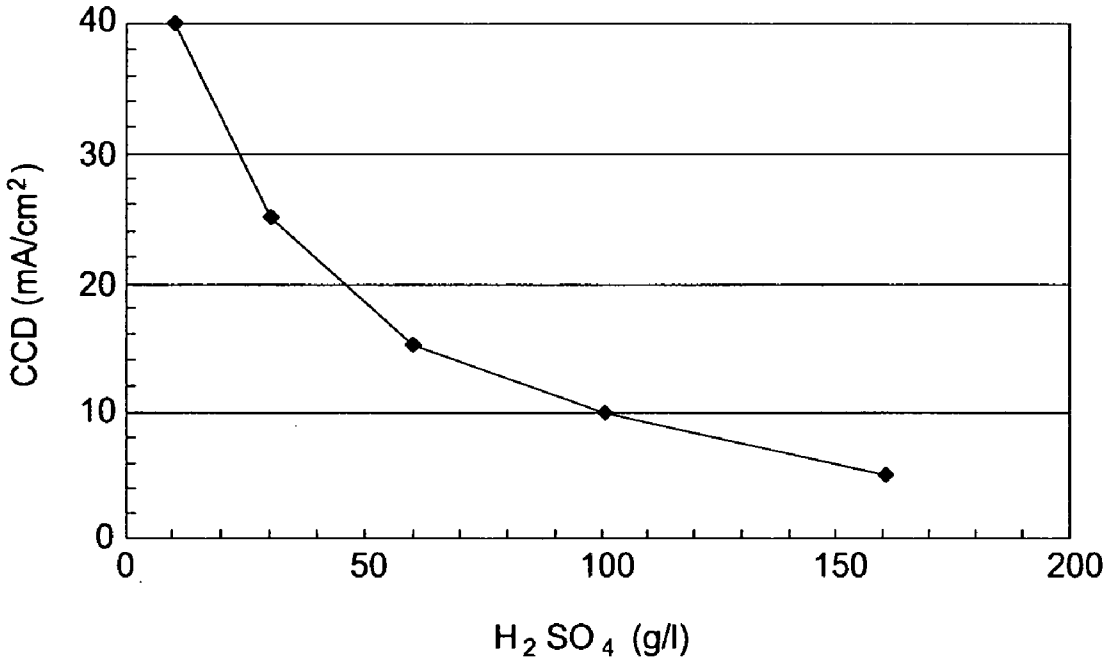
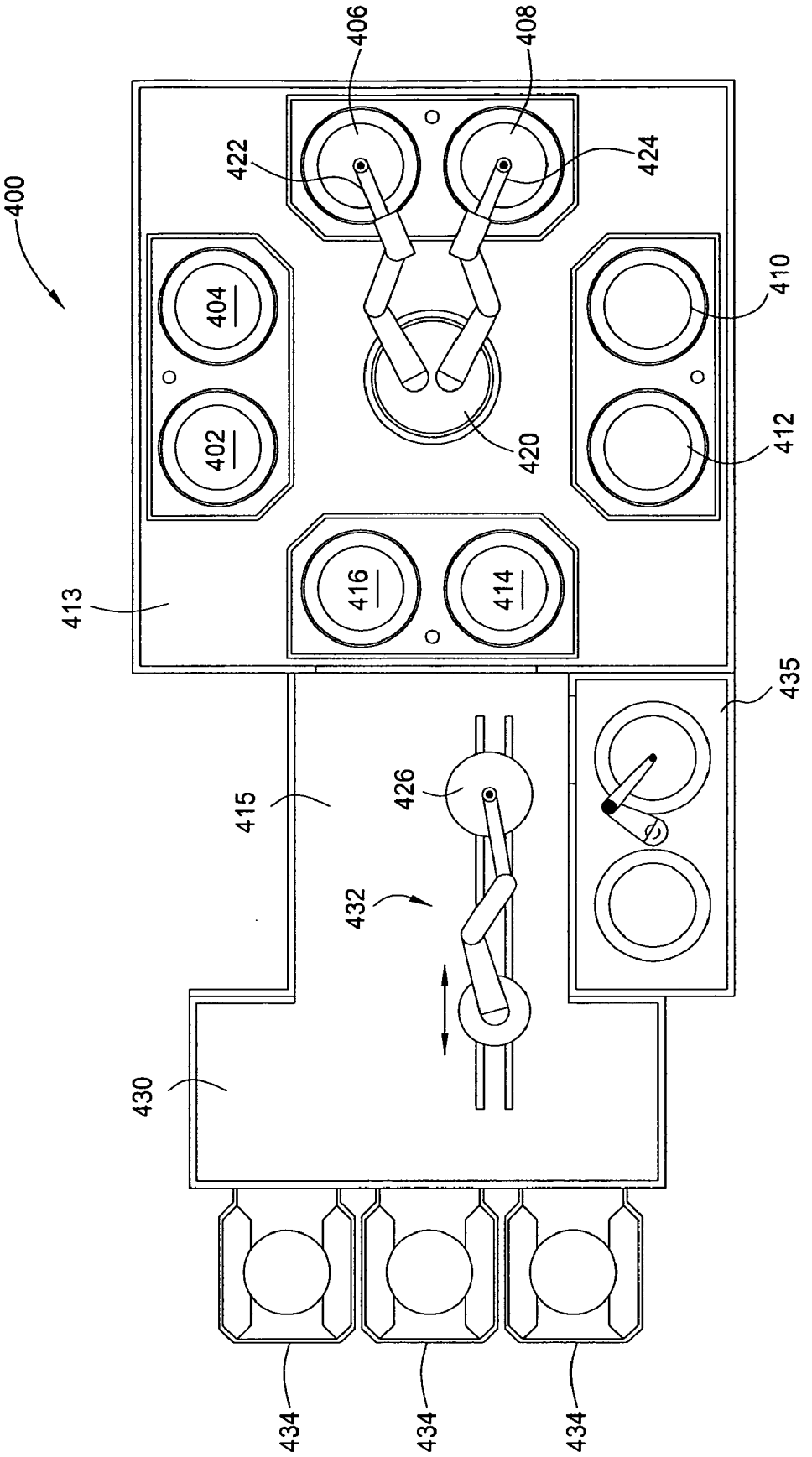

40
30
20
10
0
CCD (mA/cm2)
0
50
100
150
200
H2 SO4 (g/l)

FIG. 3


400
406
408
422
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434

FIG. 4

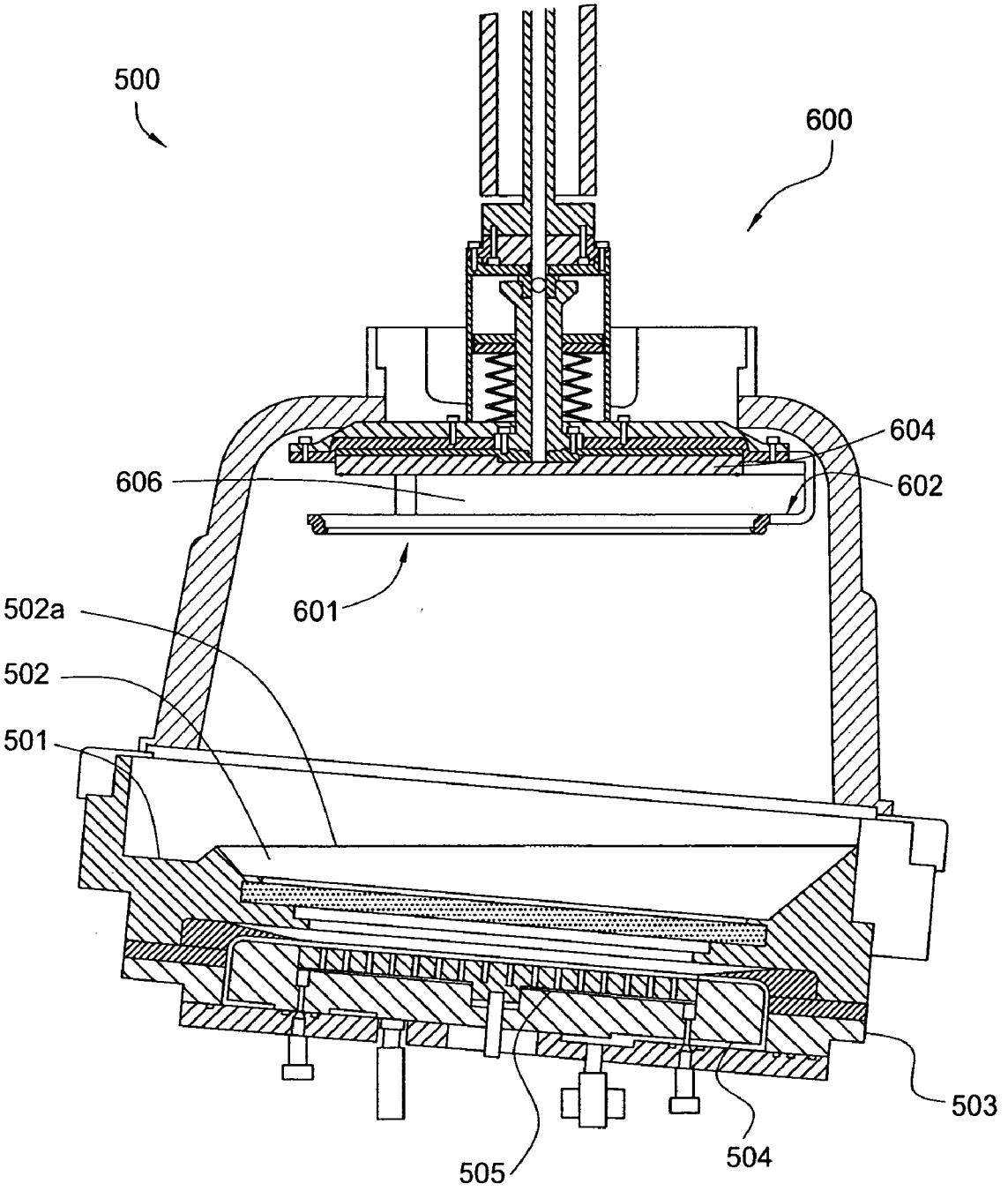

FIG. 5

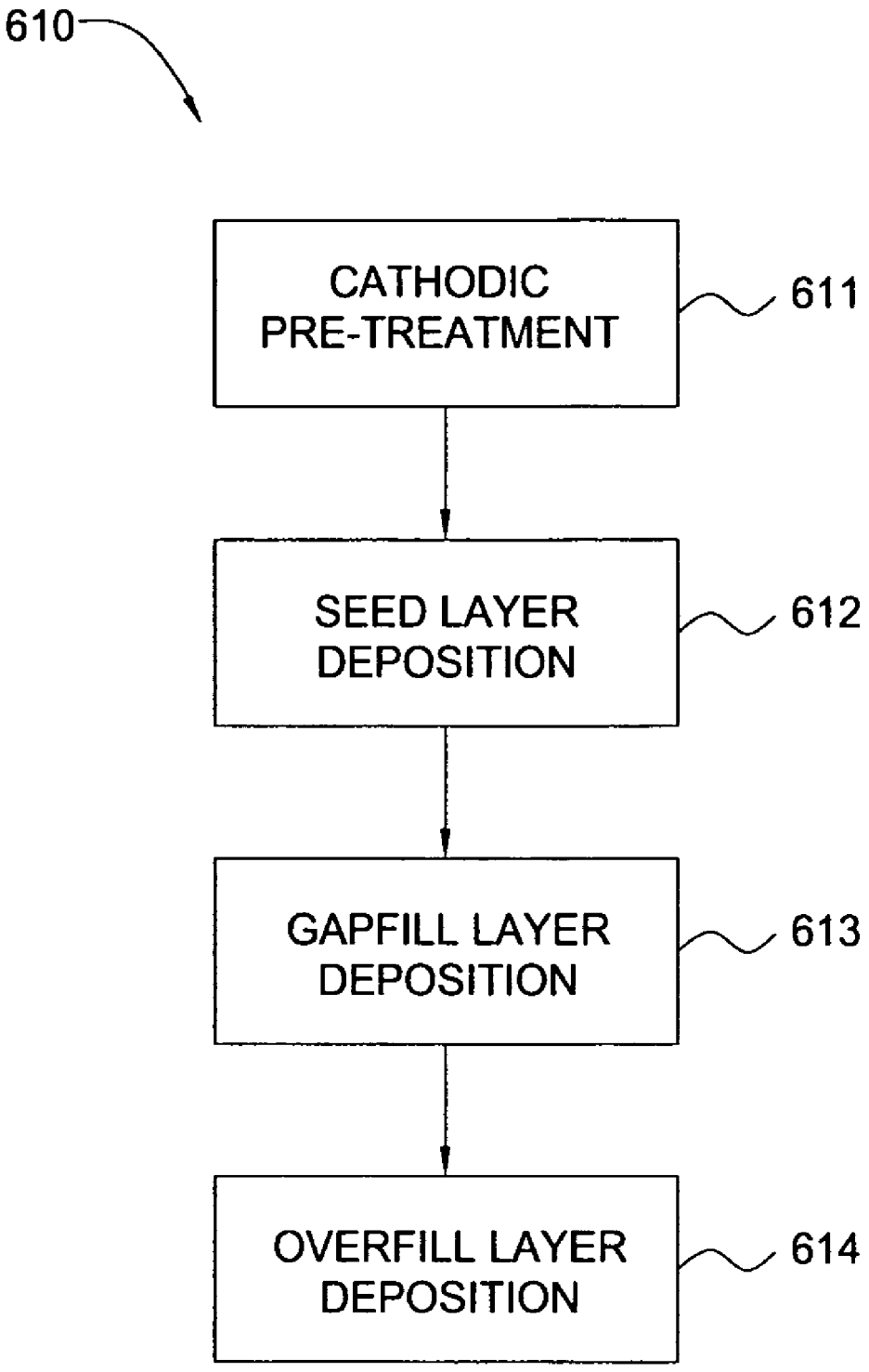
610
CATHODIC PRE-TREATMENT
611
SEED LAYER DEPOSITION
612
GAPFILL LAYER DEPOSITION
613
OVERFILL LAYER DEPOSITION
614

FIG. 6

METHOD OF DIRECT PLATING OF COPPER ON A SUBSTRATE STRUCTURE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims benefit of U.S. provisional patent application Ser. No. 60/621,173 [APPM 9762L], filed Oct. 21, 2004, which is herein incorporated by reference.

[0002] This application is a continuation-in-part of co-pending U.S. patent application Ser. No. 11/007,857 [APPM 9200], filed Dec. 9, 2004, which claims benefit of U.S. Provisional Patent Application Ser. No. 60/579,129, filed Jun. 10, 2004. This application is also a continuation-in-part of co-pending U.S. patent application Ser. No. 11/012,965 [APPM 9201], filed Dec. 15, 2004, which claims benefit of U.S. Provisional Patent Application Ser. No. 60/579,129, filed Jun. 10, 2004, and U.S. Provisional Patent Application Ser. No. 60/621,215, filed Oct. 21, 2004. This application is also a continuation-in-part of co-pending U.S. patent application Ser. No. 10/616,097 [APPM 8241], filed Jul. 8, 2003. Each of the aforementioned related patent applications is herein incorporated by reference.

BACKGROUND OF THE INVENTION

[0003] 1. Field of the Invention

[0004] Embodiments of the present invention generally relate to a method to deposit a metal layer with electrochemical plating and more particularly, to the direct plating of a copper layer onto a barrier or adhesion layer.

[0005] 2. Description of the Related Art

[0006] Metallization for sub-quarter micron sized features is a foundational technology for present and future generations of integrated circuit manufacturing processes. In devices such as ultra large scale integration-type devices, i.e., devices having integrated circuits with more than a million logic gates, the multilevel interconnects that lie at the heart of these devices are generally formed by filling high aspect ratio interconnect features with a conductive material (e.g., copper or aluminum). Conventionally, deposition techniques such as chemical vapor deposition (CVD) and physical vapor deposition (PVD) have been used to fill these interconnect features. However, as interconnect sizes decrease and aspect ratios of device features increase, void-free filling of interconnect features via conventional metallization techniques becomes increasingly difficult. As a result, plating techniques, such as electrochemical plating (ECP) and electroless plating have emerged as viable processes for filling sub-quarter micron sized, high aspect ratio interconnect features in integrated circuit manufacturing processes.

[0007] In an ECP process, sub-quarter micron sized high aspect ratio features formed into the surface of a substrate may be efficiently filled with a conductive material, such as copper. Most ECP processes are generally two stage processes, wherein a seed layer is first formed over the surface features of the substrate (this process may be performed in a separate system), and then the substrate surface features are exposed to an electrolyte solution while an electrical bias is simultaneously applied between the substrate and an anode positioned within the electrolyte solution. The electrolyte solution is generally rich in ions to be plated onto the surface of the substrate. Therefore, the application of the electrical bias drives a reductive reaction to reduce the metal ions and precipitate the respective metal. Upon precipitating, the metal plates onto the seed layer to form a film.

[0008] The process requirements for copper interconnects are becoming more stringent, as the critical dimensions for modern microelectronic devices shrink to 0.1 μm or less. As a result thereof, conventional plating processes will likely be inadequate to support the demands of future interconnect technologies. Conventional plating practices include depositing a copper seed layer via physical vapor deposition (PVD), chemical vapor deposition (CVD) or atomic layer deposition (ALD) onto a diffusion barrier layer (e.g., tantalum or tantalum nitride). However, it is extremely difficult to have adequate seed step coverage with PVD techniques, as discontinuous islands of copper agglomerates are often obtained close to the feature bottom in high aspect ratio features with PVD techniques. For PVD techniques, a thick copper layer (e.g., >200 Å) over the field is generally needed to have continuous sidewall coverage throughout the depth of the features, which often causes the throat of the feature to close before the feature sidewalls are covered. For CVD processes, copper purity is generally questionable due to difficult complete precursor-ligand removal. ALD techniques, though capable of giving generally conformal deposition with good adhesion to the barrier layer, suffer from very low deposition rates for depositing a continuous copper film on the sidewalls of adequate thickness to serve as a seed layer

[0009] Direct electroplating on barrier materials, such as tantalum or tantalum nitride, is difficult, since these traditional barrier materials generally have insulating native oxides across the surface. Also during electroplating, conductive barrier materials (e.g., cobalt) generally will oxidize near the reductive potential of free copper ions. Therefore, the integrity of the barrier layer may be compromised during the electroplating of a copper layer.

[0010] PVD has been a preferred technique to deposit a copper seed layer and electroless plating techniques for depositing a seed layer onto a barrier layer of tantalum or tantalum nitride are known. However, these techniques have suffered from several problems, such as adhesion failure between the copper seed layer and the barrier layer, as well as the added complexity of a complete electroless deposition system and the associated difficulties of process control. In addition, for interconnect features as small as 32 to 45 nm, it is beneficial to perform the seed layer deposition and the gapfill deposition uninterrupted to prevent formation of oxide or other contamination of the seed layer. Furthermore, a well-adhered seed layer has several benefits, such as protecting the barrier layer from the acidic solutions utilized during the electroplating of the bulk copper layer. Also, the copper seed supports the subsequently deposited bulk copper and minimizes peeling from the barrier layer.

[0011] Therefore, there is a need for a process for depositing a copper seed layer onto a barrier or adhesion layer. The process should deposit the copper seed layer with a strong adhesion to the underlying layer and with good uniformity over the entire substrate surface. Also, the process should be applicable for a range of barrier/adhesion layer materials, including cobalt, tungsten, tungsten nitride, titanium, titanium nitride, Ti—W alloy, tantalum, tantalum nitride, ruthe-

nium, Ru—Ta alloy, rhodium, palladium, osmium, iridium and platinum. Further, the barrier or adhesion layer should be maintained with little or no oxidation during seed layer deposition and also should not be chemically reduced during the deposition process. Finally, the process should allow the deposition of a seed layer and a gapfill layer sequentially in the same plating bath.

SUMMARY OF THE INVENTION

[0012] The present invention teaches a method for depositing a copper seed layer onto a substrate surface, generally onto a barrier layer or an adhesion layer. The barrier or adhesion layer may include a refractory metal and/or a group VIII metal. The method includes cathodically pre-treating the substrate surface in an acid-containing solution that is free of copper ions. The substrate is then placed into a neutral or alkaline (pH≧7.0) copper solution that includes complexed copper ions and a current or bias is applied across the substrate surface. The complexed copper ions include a carboxylate ligand, such as oxalate or tartrate, or ethylenediamine (ED), EDTA and/or acetate. The complexed copper ions are reduced to deposit a copper seed layer onto the barrier or adhesion layer. In one aspect, a complex alkaline bath is then used to electrochemically plate a gapfill layer on the substrate surface, followed by overfill in the same bath. In this aspect, the ECP deposition of the seed layer, the gap fill layer and the overfill layer may be performed in the same processing chamber. In another aspect, an acidic bath ECP gapfill process is performed on the substrate surface, followed by ECP overfill, also in an acidic plating bath. The copper plating solutions in all embodiments may also contain one or more additive compounds, including suppressors, levelers, brighteners and stabilizers.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] So that the manner in which the above recited features of the present invention can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0014] FIGS. **1**A-**1**C illustrate cross-sectional views of a substrate at different stages of a copper interconnect fabrication sequence.

[0015] FIG. **2** illustrates a copper layer formed on a substrate that may be comprised of multiple copper layers deposited by different electrochemical plating processes.

[0016] FIG. **3** is a graph depicting the relationship of critical current density on a substrate surface during plating versus sulfuric acid concentration in the plating bath.

[0017] FIG. **4** is a top plan view of an electrochemical processing system capable of implementing the methodology of the present invention.

[0018] FIG. **5** illustrates a sectional view of an exemplary plating cell and plating head assembly capable of implementing the methodology of the present invention.

[0019] FIG. **6** is a flow chart of a substrate process sequence for embodiments of the invention.

[0020] For clarity, identical reference numerals have been used, where applicable, to designate identical elements that are common between figures.

DETAILED DESCRIPTION

[0021] The present invention teaches a method for depositing a copper layer onto a substrate surface, generally onto a barrier or adhesion layer. The barrier layer may include a refractory metal and/or a group VIII metal. The term group VIII metals (e.g., old CAS system notation) is generally intended to describe group 8, 9 and 10 elements, such as ruthenium (Ru), rhodium (Rh), palladium (Pd), cobalt (Co), nickel (Ni), osmium (Os), iridium (Ir), and platinum (Pt). The method includes cathodically pre-treating the substrate surface in an acid-containing solution that is free of copper ions. This pre-treatment reduces the critical current density (CCD) required for forming a continuous and void-free seed layer on the barrier or adhesion layer via an ECP process. The substrate is then placed into a neutral or alkaline (pH≧7.0) complex copper solution that includes complexed copper ions and a current or bias is applied across the substrate surface. A "complex bath" or "complex solution", as used herein, is defined as a plating solution containing at least one complexing, or chelating, compound and a metal ion source, wherein the metal ion source comprises the metal to be plated on the substrate, e.g. copper. "Alkaline," as used herein, is defined as pH≧7.0. The complexed copper ions are reduced to deposit a continuous, void-free copper seed layer onto the barrier or adhesion layer. In one aspect, a complex alkaline bath is then used to electrochemically plate a gapfill layer onto the seed layer, followed by electrochemical plating of an overfill layer using an acid plating bath. In this aspect, the ECP deposition of the seed layer and the gap fill layer may be performed in the same processing chamber and preferably with the same plating solution. In another aspect, an acid bath ECP gap fill process is performed on the substrate surface, followed by ECP overfill, also in an acid bath.

[0022] Ruthenium (Ru) thin films, deposited by CVD, ALD or PVD, can be a potential candidate for a seedless interlayer between intermetal dielectric (IMD) and copper interconnect for ≦45 nm technology. "Interlayer", as used herein, is defined as a layer deposited between a dielectric layer and a subsequently deposited metal layer. Examples of an interlayer include a copper barrier layer, an adhesion layer, and a combined barrier/adhesion layer. Ruthenium is a group VIII metal that has a relatively low electrical resistivity (resistivity ~7 μΩ-cm) and high thermal stability (high melting point ~2300° C.). It is relatively stable even in the presence of oxygen and water at ambient temperature. The thermal and electrical conductivities of ruthenium are twice those of Tantalum (Ta). Ruthenium also does not form an alloy with copper below 900° C. and shows good adhesion to copper. Therefore, the semiconductor industry has shown an interest in using Ru as an interlayer layer or adhesion layer. The low resistivity of ruthenium can be an advantage when trying to fill ruthenium-coated features with copper without a seed layer. However, because ruthenium layers are often very thin (10-100 Å) and have over three times the electrical resistivity of copper, ruthenium layers still exhibit high sheet resistances, e.g. >20 ohm/square for

100 Å thick ruthenium films. The terminal effect associated with trying to plate a material on materials that have a high sheet resistance can make obtaining uniform, void-free copper films on 200 and 300 mm substrates problematic.

[0023] FIGS. **1**A-**1**C illustrate cross-sectional views of a substrate at different stages of a copper interconnect fabrication sequence incorporating a group VIII metal layer. FIG. **1**A illustrates a cross-sectional view of a substrate **100** having metal contacts **104** and a dielectric layer **102** formed thereon. The substrate **100** may comprise a semiconductor material such as, for example, silicon, germanium, or gallium arsenide. The dielectric layer **102** may comprise an insulating material such as, silicon dioxide, silicon nitride, silicon oxynitride and/or carbon-doped silicon oxides, such as SiO_xC_y, for example, BLACK DIAMOND™ low-k dielectric, available from Applied Materials, Inc., located in Santa Clara, Calif. The metal contacts **104** may comprise, for example, copper, among others. Apertures **120** may be defined in the dielectric layer **102** to provide openings over the metal contacts **104**. The apertures **120** may be defined in the dielectric layer **102** using conventional lithography and etching techniques. The width of apertures **120** may be as large as about 900 Å and as small as about 400 Å. The thickness of dielectric layer **102** could be in the range between about 1000 Å to about 10000 Å.

[0024] A barrier layer **106** may be formed in the apertures **120** defined in the dielectric layer **102**. The barrier layer **106** may include one or more refractory metal-containing layers used as a copper-barrier material such as, for example, cobalt, titanium, titanium nitride, titanium silicon nitride, tantalum, tantalum nitride, tantalum silicon nitride, tungsten, tungsten nitride and Ti—W alloy, among others. The barrier layer **106** may be formed using a suitable deposition process, such as ALD, chemical vapor deposition (CVD) or physical vapor deposition (PVD). The thickness of the barrier layer is between about 5 **521** to about 150 Å and preferably less than 100 Å.

[0025] As noted above, the barrier layer **106** may instead comprise a thin film of group VIII metal, such as ruthenium (Ru), a ruthenium-tantalum alloy, rhodium (Rh), palladium (Pd), osmium (Os), iridium (Ir), and platinum (Pt). Such group VIII metal, which is resistant to corrosion and oxidation, may provide a surface upon which a copper layer is subsequently deposited using an electrochemical plating (ECP) process. The group VIII metal may act as a copper-barrier layer. Alternately, the group VIII metal may be deposited on the conventional barrier layer, such as Ta (tantalum) and/or TaN (tantalum nitride), to serve as an adhesion layer or other interlayer between the conventional barrier layer and subsequently deposited copper layers. The group VIII metal is typically deposited using a chemical vapor deposition (CVD) process, atomic layer deposition (ALD) or a physical vapor deposition (PVD) process. Referring to FIG. **1**B, a group VIII metal interlayer **108**, such as ruthenium (Ru), is formed on the substrate, and in this example on the barrier layer **106**. The thickness for the group VIII metal interlayer **108** often depends on the device structure to be fabricated. Typically, the thickness of the group VIII metal interlayer **108**, such as ruthenium, is less than about 1,000 Å, preferably between about 5 Å to about 200 Å.

[0026] It has been found that the process of directly plating a metal layer (e.g., copper layer **110**) on a barrier **106** that contains pure tantalum (Ta), or tantalum nitride (TaN), will not give good process results. One of the problems of plating a metal layer on a pure Ta, or TaN, barrier layer is due to tantalum's high affinity for oxygen, which causes a thermodynamically stable oxide layer to form on the Ta, or TaN, surface, which thus prevents good adhesion between the directly plated metal layer and the Ta, or TaN, barrier layer **106**. The adhesion problem is typically found during the direct plating process since the deposited layer easily separates, or de-bonds, from the surface of the barrier layer **106**. Conventional processing steps that are adapted to remove the surface oxides on the Ta and TaN, such as aqueous, thermal or plasma processes, which are intended to reduce the formed oxides, are generally ineffective due to rapid re-oxidation of the freshly exposed surfaces.

[0027] A Ru—Ta alloy, when used as a group VIII metal interlayer **108** as shown in FIGS. **1**A-**1**C, has the combined benefits of blocking copper diffusion as effectively as conventional tantalum barrier layers and providing a suitable surface for direct plating of a copper seed layer but does not suffer from the same adhesion problems as found with conventional Ta and TaN barrier layers. Therefore, in one aspect of the invention, the barrier layer **106** contains a Ru—Ta alloy that contains between about 70 atomic % and about 95 atomic % of ruthenium and the balance tantalum. In another aspect, the barrier layer preferably contains a Ru—Ta alloy that contains between about 70 atomic % and about 90 atomic % of ruthenium and the balance tantalum. In yet another aspect, the barrier layer more preferably contains a Ru—Ta alloy that contains between about 80 atomic % and about 90 atomic % of ruthenium and the balance tantalum. In one aspect, it may be desirable to select a Ru—Ta alloy that does not contain regions of pure ruthenium and/or pure tantalum on the surface.

[0028] In some cases, group VIII metal interlayer **108** may also comprise a discontinuous copper layer, for example a very thin (<100 Å) layer of PVD copper. Such a copper layer may not be electrically conductive, but may provide additional nucleation sites for subsequently deposited copper layers, essentially lowering the effective CCD of the group VIII metal interlayer.

[0029] Referring to FIG. **1**C, the apertures **120** may thereafter be filled with copper layer **110** via one or more direct electroplating processes to complete the copper interconnect. Direct plating of copper may be performed onto a barrier layer **106** or a group VIII metal interlayer **108**. However, because it may be beneficial to reduce the critical current density (CCD) required to plate copper onto the substrate surface, i.e. onto barrier layer **106** or group VIII metal interlayer **108**, embodiments of the invention contemplate the application of a cathodic pre-treatment process prior to the deposition of copper layer **110**. Critical current density and cathodic pre-treatment are described below in conjunction with FIG. **3**. Embodiments of the invention further contemplate different electroplating methods for the deposition of copper layer **110**.

[0030] Referring to FIG. **2**, copper layer **110** may be comprised of multiple copper layers deposited by different electrochemical plating processes. For clarity, layers deposited on the substrate prior to copper deposition, such as dielectric layer **102**, metal contacts **104**, barrier layer **106** and group VIII metal interlayer **108**, are illustrated together

in FIG. **2** as conductive substrate surface **114**. Copper layer **110** may include a thin, substantially conformal, continuous, void-free layer, hereinafter referred to as a seed layer **111**, a gap fill layer **112** and an overfill layer **113**.

[**0031**] In one embodiment, after cathodic pre-treatment of the substrate surface, a seed layer **110** is electrochemically plated onto conductive substrate surface **114** using a complex alkaline bath and plating process described below in conjunction with FIGS. **3**, **5** and **6**. Gap fill layer **112** is then electrochemically plated onto seed layer **110** using either a complex alkaline bath gapfill process, described below in conjunction with FIGS. **3**, **5** and **6** or a conventional acid bath gapfill process, described below in conjunction with FIGS. **5** and **6**. In one aspect, an overfill layer **113** is then deposited onto gap fill layer **112** with an acid bath ECP process, described below in conjunction with FIGS. **5** and **6**. An example of an electrochemical plating (ECP) system and an exemplary plating cell are described below in conjunction with FIGS. **4**, **5** and **6**.

Electrochemical Processes

Cathodic Pre-Treatment of Barrier Layer

[**0032**] Embodiments of the invention contemplate a cathodic pre-treatment of a substrate surface prior to electrochemical plating of copper onto the surface.

[**0033**] The plating current for a typical ECP process onto a copper seed layer is typically in the range from about 2 mA/cm^2 to about 10 mA/cm^2 for filling copper into submicron trench and/or via structures, such as apertures **120** (shown in FIGS. **1**A-**1**C). However, it has been found that a plating current density of 2-10 mA/cm^2 will not provide deposition of a continuous copper film on a ruthenium layer, creating voids. A continuous copper film is formed on Ru when the plating current density is increased and/or the electrolyte resistivity is reduced beyond the values used in conventional copper plating. A minimum or critical current density, or CCD, has been determined wherein plating current densities equal to or above this value will form a thin continuous copper film on a Ru layer and current densities below this value will not form a thin continuous film on the Ru layer. The magnitude of the CCD is strongly dependent on the resitivity of the plating solution.

[**0034**] FIG. **3** illustrates an example of the CCD versus sulfuric acid (H_2SO_4) concentration. The CCD, as shown in FIG. **3**, is defined as the minimum current density required to form a 1000 Å continuous copper film on a ruthenium surface. Below the CCD, no visually shiny continuous copper film will be deposited at the center regions of the substrate. The magnitude of CCD is shown to strongly depend on the acidity level of the plating bath.

[**0035**] It is well known that the kinetics of nucleation and crystal growth for electro-deposition is intimately related to the local electrochemical over-potential at the nucleation/growth sites as well as the condition of the surface whereon crystal growth takes place. Over-potential is defined as the difference between the actual potential and the zero-current (open-circuit) potential. A high over-potential favors new crystal nucleation by lowering the critical nucleus size and increasing the density of nuclei, while a low electrochemical over-potential favors growth on existing crystallites. Since the plating current density depends on the electrochemical over-potential for a given bath, the copper deposit structure/morphology is therefore affected by the plating current density. Further, nucleation is also dependent on the "activity" of the substrate surface, i.e., the concentration of "active sites" on the substrate. Any kind of surface imperfection, such as a crystal dislocation, crystal boundary or incorporated alien atom may serve as the active site. At the same overvoltage, or at the same applied current density, the amount of nuclei formed will be much higher if the barrier layer is free from unwanted deposits, such as ruthenium oxides and some organic compounds, that block the active sites and, hence, inhibit nucleation.

[**0036**] As predicted by theory and confirmed by scanning electron microscopic (SEM) images, a substrate with a copper film plated on a 100 Å Ru film in a 10 g/l sulfuric acid containing plating solution with a plating current of 3 mA/cm^2 had large crystallites and poor film deposition in the center region of the substrate. Measured at the edge of the substrate, the thickness of the copper plated film was 1000 Å. According to the results shown in FIG. **3**, the CCD is about 40 mA/cm^2 when the sulfuric acid concentration is 10 g/l. The current density of 3 mA/cm^2 is much lower than the 40 mA/cm^2 CCD shown in FIG. **3** and, as expected, a non-continuous layer was formed. It is believed that under this plating condition, only a few crystallites are stable enough to serve as the nucleation center for further crystal growth, and thus the energy from the plating current is primarily used in growing these crystals, with the help of fast copper adatom surface diffusion. Therefore, the SEM shows large crystallites and copper island deposition in the center region of the substrate. To form a continuous copper film across the entire substrate under this condition, the deposited layer would have to be very thick and the deposited layer would likely contain voids, which would make it unsuitable for Cu interconnect applications. Such poor deposition has been found even when the plating current density is only slightly lower than the CCD. For example, a substrate that has a 5000 Å thick continuous copper film can be formed on a 100 Å Ru film (deposited by PVD), using a plating solution containing 60 g/l of H_2SO_4 and a plating current density of about 10 mA/cm^2 (slightly lower than the CCD of 15 mA/cm^2). In agreement with theory, however, there were large voids at the Cu/Ru interface.

[**0037**] Simply increasing plating current density to allow plating of a void-free, continuous film onto a ruthenium interlayer also has disadvantages; generally, a high plating current density tends to result in poor gap fill. Plating current densities of less than about 10 mA/cm^2 have been found to encourage bottom-up deposition of trenches and vias, such as apertures **120**, with a gap fill layer **112**, shown in FIGS. **1**A-**1**C. In order to reduce the plating current density to the range suitable for bottom-up gap fill, the ion concentration of the plating bath may be increased. For example, it has been shown that a continuous 1000 Å copper film may be deposited on a 100 Å Ru film on a substrate using a plating bath with a H_2SO_4 concentration of 160 g/l and a plating current of 5 mA/cm^2. Referring to FIG. **3**, 5 mA/cm^2 is equal to the CCD for this particular acidic concentration. However, cross-section SEM pictures show that voids were formed at the Cu/Ru interface. When the plating current was raised to 10 mA/cm^2 (2 times CCD of 5 mA/cm^2) and the same plating bath was used, a continuous 5000 Å copper film was formed on a 100 Å Ru layer with no voids at the copper/Ru interface.

[0038] One of the reasons for the CCD dependence on bath acidity is related to the local electrochemical overpotential discussed above. In addition, higher acidity plating solutions may remove unwanted deposits from the surface and increase the activity of the plating surface. Increasing acid concentration to lower the CCD introduces other problems, however. Because the intention of direct plating is to form a uniform, conformal metal layer on a barrier layer, electrical conductivity of the bath should be reduced as much as is practicable. A more conductive plating bath, such as a bath containing a high concentration of acid, degrades the uniformity of the resultant film.

[0039] Recent research presented by Chyan, et al. from University of North Texas in American Chemical Society National Meeting in New Orleans, La., held in Mar. 23 to Mar. 27, 2003, shows that ruthenium oxide (RuO_2) has a metal-like conductivity, and copper also plates and adheres strongly to ruthenium oxide. The high CCD's observed on a ruthenium surface could be the result of unwanted deposits on the ruthenium surface. "Unwanted deposits", as used herein, is defined to include unwanted oxidation of a deposited surface as well as organic contaminants that accumulate on the fresh metallic surface after deposition. A "pure" ruthenium surface is believed to be more active for Cu nucleation. Hence, removing the unwanted deposits by a pre-treatment process before copper plating may greatly reduce the plating current and the plating bath acidity required to form a continuous copper layer and avoid voids at the Cu/Ru interface. Embodiments of the invention contemplate a pre-treatment process that includes a cathodic pre-treatment of the barrier or barrier/adhesion layer, such as barrier layer **106** or group VIII metal interlayer **108**, as shown in FIGS. **1**A-**1**C.

[0040] The cathodic treatment mentioned above is an electrochemical treatment of a substrate surface in a copper-ion-free acid solution. An oxidized metallic surface, particularly a RuO_x surface that has formed on a freshly deposited ruthenium barrier/adhesion layer on a substrate, may be cathodically reduced. Additionally, weakly-bound organic surface contaminants may be expelled from the surface by the cathodic polarization. The removal of these unwanted deposits on the substrate surface prior to electrochemical plating has been demonstrated to reduce the CCD of the barrier/adhesion layer. One possible reduction reaction is shown in equation (1):

$$RuO_2+4H^*+4\ e^- \rightarrow Ru+2H_2O \quad (1)$$

[0041] The cathodic treatment may be performed in an electrochemical plating cell similar to the copper plating cell described below in association with FIG. **5**, or in a treatment cell separated from the copper plating system. The cathodic treatment cell requires an anode, a cathode and a copper-ion-free acid bath. The acidic concentration range should be in the range between about 10 g/l to about 100 g/l, and preferably in the range between about 10 g/l to about 50 g/l. A preferred acid is H_2SO_4, but other types of acidic solutions, such as organic sulfonic acid solutions (e.g. methylsulfonic acid), may also be used. The acidic bath needs to be free of copper ions to prevent copper deposition on the surface during the cathodic treatment. Such deposition would be in the form of poorly nucleated copper islands, leading to poor adhesion and/or voids.

[0042] The cathodic treatment can be realized through potential control or current control. With the potential control approach, a reference electrode is needed to monitor the wafer potential, in addition to the working electrodes, which are the thin as-deposited Ru film on the wafer surface, and an anode. Potential control can be realized through a potentiostat. The controlled ruthenium electrode potential, with respect to the reference electrode, is in the range of about 0 volt to about −0.5 volt. In addition to RuO_x reduction to ruthenium, H_2 evolution may occur on the Ru film surface, hence, it is important to avoid applying a reduction potential to the substrate that is too high. With the current control approach, a cathodic current will be passed between the substrate, coated with a ruthenium film for example, and an anode. The current density should be in the range of about 0.05 mA/cm^2 to about 1 mA/cm^2. The treatment time should be in the range of about 2 seconds to about 30 minutes. However, in the interest of maintaining adequate throughput during large-scale processing of substrates, the treatment is preferably kept below 5 minutes.

[0043] Another benefit of cathodically pre-treating a barrier or barrier/adhesion layer on a substrate, particularly when the layer is a group VIII metal interlayer **108**, is the improved adhesion between copper and the adhesion layer. Experimental results have shown that the adhesion is better between copper and a pre-treated, clean, and possibly oxide-free ruthenium surface due to a high-integrity Cu/Ru interface free of voids. Good interface integrity between the Cu and the Ru layers can be an important aspect in forming a reliable semiconductor device. Hence, having a pre-treated ruthenium surface is critical to achieve high quality copper deposition on ruthenium films. Additionally, cathodically pre-treating a ruthenium surface prior to copper plating may improve the substrate surface's hydrophilicity. The step coverage of copper plating on substrate features, such as apertures **120**, may be improved, since the treated surface is more hydrophilic and, hence, more able to draw the plating solution deep into the features.

[0044] The experimental results and discussion related to Ru are merely used as examples. The inventive concept may also be applied to other group VIII metals, such as rhodium (Rh), osmium (Os) and iridium (Ir) and barrier materials, such as cobalt, titanium, titanium nitride, titanium silicon nitride, tantalum, tantalum nitride, tantalum silicon nitride, tungsten, tungsten nitride, a Ti—W alloy, and a ruthenium-tantalum alloy.

Direct Plating on a Barrier Layer with a Complex Alkaline Electrolyte

[0045] Embodiments of the invention teach the use of complexed copper sources contained within an alkaline plating solution for the direct plating of copper layers on barrier and/or barrier/adhesion layers. "Direct plating", as used herein, is defined as the method of electrochemically plating a more conductive metal layer, such as seed layer **111** in FIG. **2**, onto a substantially less conductive layer, such as conductive substrate surface **114**, to facilitate the subsequent uniform, void-free deposition of a gapfill layer **112** and/or an overfill layer **113**. This process may be performed in a plating cell similar to the electrochemical processing cell described below in conjunction with FIG. **5**.

[0046] A plating solution containing complexed copper sources has a significantly more negative deposition potential than does a plating solution containing free copper ions. Generally, complexed copper ions have a deposition poten-

tial from about −1.1 V to about −0.5 V, depending on the particular complexing agent. Free copper ions have deposition potentials in the range from about −0.3 V to about −0.1 V, when referenced to Ag/AgCl (1 M KCl), which has a potential of 0.235 V verses a standard hydrogen electrode. For example:

$$Cu_2(C_6H_4O_7)+2H_2O \rightarrow 2Cu^0+C_6H_8O_7+O_2 \quad \Delta\epsilon=-0.7\ V$$

$$Cu^{+2}+2e^- \rightarrow Cu^0 \quad \Delta\epsilon=-0.2\ V.$$

Further, the current dependence on potential for the complex bath is substantially reduced when compared to a bath with free copper ions. Therefore, the local current density variation across the substrate surface will be improved, even in the presence of a large potential gradient across the substrate surface due to the low electrical conductivity of thin barrier metals. This leads to better deposition uniformity across the substrate surface. A more detailed description of electrochemical polarization of copper complex baths may be found in commonly U.S. patent application Ser. No. 10/616,097 [APPM 8241], filed Jul. 8, 2003, which is hereby incorporated by reference in its entirety to the extent not inconsistent with the claimed invention.

[0047] Suitable plating solutions that may be used with the processes described herein to plate copper may include at least one copper source compound, at least one chelating or complexing compound, optional wetting agents or suppressors, optional pH adjusting agents and a solvent.

[0048] Plating solutions contain at least one copper source compound complexed or chelated with at least one of a variety of ligands. Complexed copper includes a copper atom in the nucleus and surrounded by ligands, functional groups, molecules or ions with a strong affinity to the copper, as opposed to free copper ions with very low affinity, if any, to a ligand (e.g., water). Complexed copper sources are either chelated before being added to the plating solution or are formed in situ by combining a free copper ion source with a complexing agent. The copper atom may be in any oxidation state, such as 0, 1 or 2, before, during or after complexing with a ligand. Therefore, throughout the disclosure, the use of the word copper or elemental symbol Cu includes the use of copper metal (Cu^0), cupric (Cu^{+1}) or cuprous (Cu^{+2}), unless otherwise distinguished or noted.

[0049] Examples of suitable copper source compounds include copper citrate, copper ED, copper EDTA, among others. A particular copper source compound may have ligated varieties. For example, copper citrate may include at least one cupric atom, cuprous atom or combinations thereof and at least one citrate ligand and include $Cu(C_6H_7O_7)$, $Cu_2(C_6H_4O_7)$, $Cu_3(C_6H_5O_7)$ or $Cu(C_6H_7O_7)_2$. In another example, copper EDTA may include at least one cupric atom, cuprous atom or combinations thereof and at least one EDTA ligand and include $Cu(C_{10}H_{15}O_8N_2)$, $Cu_2(C_{10}H_{14}O_8N_2)$, $Cu_3(C_{10}H_{13}O_8N_2)$, $Cu_4(C_{10}H_{12}O_8N_2)$ or $Cu_2(C_{10}H_{12}O_8N_2)$. Examples of suitable copper source compounds include copper sulfate, copper pyrophosphate and copper fluoroborate.

[0050] The plating solution contains one or more chelating or complexing compounds that include compounds having one or more functional groups selected from the group of carboxylate groups, hydroxyl groups, alkoxyl, oxo acids groups, mixture of hydroxyl and carboxylate groups and combinations thereof. Further examples of suitable chelating compounds include compounds having one or more amine and amide functional groups, such as ethylenediamine (ED), diethylenetriamine, diethylenetriamine derivatives, hexadiamine, amino acids, ethylenediaminetetraacetic acid (EDTA), methylformamide or combinations thereof. The plating solution may include one or more chelating agents at a concentration in the range from about 0.02 M to about 1.6 M.

[0051] The one or more chelating compounds may also include salts of the chelating compounds described herein, such as lithium, sodium, potassium, cesium, calcium, magnesium, ammonium and combinations thereof. The salts of chelating compounds may completely or only partially contain the aforementioned cations (e.g., sodium) as well as acidic protons, such as $Na_x(C_6H_{8-x}O_7)$ or Na_xEDTA, whereas X=1-4. Such salt combines with a copper source to produce $NaCu(C_6H_5O_7)$. Examples of suitable inorganic or organic acid salts include ammonium and potassium salts or organic acids, such as ammonium oxalate, ammonium citrate, ammonium succinate, monobasic potassium citrate, dibasic potassium citrate, tribasic potassium citrate, potassium tartrate, ammonium tartrate, potassium succinate, potassium oxalate, and combinations thereof. The one or more chelating compounds may also include complexed salts, such as hydrates (e.g., sodium citrate dihydrate).

[0052] Wetting agents or suppressors may be added to the solution in a range from about 10 ppm to about 2,000 ppm, preferably in a range from about 50 ppm to about 1,000 ppm. Suppressors include polyacrylamide, polyacrylic acid polymers, polycarboxylate copolymers, polyethers or polyesters of ethylene oxide and/or propylene oxide (EO/PO), coconut diethanolamide, oleic diethanolamide, ethanolamide derivatives or combinations thereof.

[0053] One or more pH-adjusting agents are optionally added to the plating solution to achieve a pH≧7.0, preferably between about 7.0 and about 9.5. The amount of pH adjusting agent can vary as the concentration of the other components is varied in different formulations. Different compounds may provide different pH levels for a given concentration, for example, the composition may include between about 0.1% and about 10% by volume of a base, such as potassium hydroxide, ammonium hydroxide or combinations thereof, to provide the desired pH level. The one or more pH adjusting agents may also include acids, including carboxylic acids, such as acetic acid, citric acid, oxalic acid, phosphate-containing components including phosphoric acid, ammonium phosphates, potassium phosphates, inorganic acids, such as sulfuric acid, nitric acid, hydrochloric acid and combinations thereof.

[0054] In an exemplary direct plating process using a Cu-ED alkaline electrolyte, a constant cathodic current is applied to the substrate resulting in a constant current density which may be in a range between about 1 mA/cm^2 to about 10 mA/cm^2 for a time period between about 0.1 seconds and 5.0 seconds. This results in the formation of a copper seed layer between about 50 Å and about 300 Å thick on the barrier layer.

[0055] Alternately, in order to ensure that a uniform, void-free seed layer is formed on a substrate during the above-described direct plating process, a "nucleation spike" or "nucleation pulse" may be used when the substrate surface is first brought in contact with the plating solution.

"Nucleation spike" or "nucleation pulse," as used herein, is defined as an initial higher plating current level intended to help the nucleation of the copper deposition on the substrate surface, wherein the initial plating current is at least equal to, or ideally greater than, the CCD. This plating current may exceed the maximum plating current that typically allows for bottom-up gapfill of substrate features and therefore is only applied for a short time. For example, in the case of plating a copper seed layer onto a ruthenium barrier layer, a constant plating current in the range of about 5 mA/cm^2 to about 20 mA/cm^2 is applied to the barrier layer during the nucleation pulse for about 0.1 to about 5 seconds. This allows the formation of a conformal, uniform and void-free layer on the substrate, such as seed layer **111**, as shown in FIG. **2**.

Plating on Copper Seed with a Complex Alkaline Electrolyte

[**0056**] Aspects of the invention teach the use of a complex alkaline electrolyte for plating a gapfill layer, such as gapfill layer **112** (see FIG. **2**), onto a seed layer, such as seed layer **111**, that has been directly deposited on a barrier layer via an alkaline solution ECP process. This process may be performed in an electrochemical plating cell similar to the electrochemical processing cell described below in conjunction with FIG. **5**.

[**0057**] This process is similar to that described above for direct plating on a barrier layer with a complex alkaline electrolyte. Process parameters are believed to enhance the bottom-up gapfill process, however, including plating current and deposition time. Generally, higher deposition rates and, hence, plating current densities, may be utilized for this process.

[**0058**] The bath used for this process is also similar to that used for direct plating. The complex alkaline bath for gapfill contains at least one copper source compound and at least one complexing compounds, as detailed previously. The one or more complexing compounds may also include salts of the chelating compounds, listed above. The bath also may contain wetting agents and one or more pH-adjusting agents (see above). Concentrations of the bath's components are believed to enhance the bottom-up gapfill process.

[**0059**] Additionally, the use of a nucleation pulse is unnecessary for the formation of a uniform, void-free metal layer to be formed on the seed layer.

Plating on Copper Seed with an Acidic Electrolyte

[**0060**] Aspects of the invention teach the use of a conventional acid electrolyte for plating a gap fill layer onto a seed layer that has been directly deposited on a barrier layer via an alkaline solution ECP process. ECP gapfill deposition of copper onto a copper seed layer using an acidic plating solution is well known in the art and may be performed in an electrochemical plating cell similar to the copper plating cell described below in conjunction with FIGS. **4** and **5**. This process may also be used for depositing a copper overfill layer on a substrate, such as overfill layer **113**, in FIG. **2**.

[**0061**] A conventional, i.e., non-complex, electrochemical plating solution for ECP generally includes a copper source, an acid source, a chlorine ion source, and at least one plating solution additive, i.e., levelers, suppressors, accelerators, antifoaming agents, etc. For example, the plating solution may contain between about 30 g/l and about 60 g/l of copper, between about 10 g/l to about 50 g/l of sulfuric acid, between about 20 and about 100 ppm of chlorine ions, between about 5 and about 30 ppm of an additive accelerator, between about 100 and about 1000 ppm of an additive suppressor, and between about 1 and about 6 ml/l of an additive leveler. The plating current may be in the range from about 2 mA/cm^2 to about 10 mA/cm^2 for filling about 300 Å to about 3000 Å copper into the submicron trench and/or via structure. A substantially similar process is used for an overfill plating process, in which an additional 5000 Å to 10,000 Å of copper is plated on to a substrate to complete a copper interconnect layer. Examples of copper plating chemistries and processes can be found in commonly assigned U.S. patent application Ser. No. 10/616,097, titled "Multiple-Step Electrodeposition Process For Direct Copper Plating On Barrier Metals", filed on Jul. 8, 2003, and U.S. patent application NO. 60/510,190, titled "Methods And Chemistry For Providing Initial Conformal Electrochemical Deposition Of Copper In Sub-Micron Features", filed on Oct. 10, 2003.

Exemplary Plating Apparatus

Electrochemical Processing System

[**0062**] FIG. **4** is a top plan view of an embodiment of an electrochemical processing system (ECPS) **400** capable of implementing the methodology of the present invention. The ECPS **400** generally includes a processing base **413** having a robot **420** centrally positioned thereon. The robot **420** generally includes one or more robot arms **422** and **424** configured to support substrates thereon. Additionally, the robot **420** and the robot arms **422** and **424** are generally configured to extend, rotate and vertically move so that the robot **420** may insert and remove substrates to and from a plurality of processing locations **402**, **404**, **406**, **408**, **410**, **412**, **414** and **416** positioned on the base **413**. Processing locations may be configured as electroless plating cells, electrochemical processing cells, substrate rinsing and/or drying cells, substrate bevel clean cells, substrate surface clean or preclean cells and/or other processing cells that are advantageous to plating processes. Preferably, embodiments of the present invention are conducted within at least one of the processing locations **402**, **404**, **406**, **408**, **410** and **412**.

[**0063**] The ECPS **400** further includes a factory interface, or FI **430**. The FI **430** generally includes at least one FI robot **432** positioned adjacent one side of the FI **430** that is adjacent to the processing base **413**. The FI robot **432** is positioned to access a substrate **426** from substrate cassettes **434**. The FI robot **432** delivers the substrate **426** to one of processing locations **414** and **416** to initiate a processing sequence. Similarly, FI robot **432** may be used to retrieve substrates from one of the processing locations **414** and **416** after a substrate processing sequence is complete. In this situation FI robot **432** may deliver the substrate **426** back to one of the cassettes **434** for removal from the system **400**. Further, robot **432** also extends into a link tunnel **415** that connects factory interface **430** to processing mainframe or platform **413**. Additionally, FI robot **432** is configured to access an anneal chamber **435** positioned in communication with the FI **430**.

Electrochemical Plating Cell

[**0064**] FIG. **5** illustrates a partial perspective and sectional view of an exemplary electrochemical processing cell, hereinafter referred to as plating cell **500**, that may be imple-

mented in processing locations **402**, **404**, **406**, **408**, **410**, **412**, **414**, **416** of FIG. **4**. The plating cell **500** generally includes a plating head assembly **600**, a frame member **503**, an outer basin **501** and an inner basin **502** positioned within outer basin **501**.

[**0065**] The plating head assembly **600** includes a receiving member **601**for supporting and rotating a substrate during immersion into the electrochemical processing solution and during electrochemical processing. In this example, receiving member **601** includes a contact ring **602** and a thrust plate assembly **604** that are separated by a loading space **606**. The contact ring **602** may be adapted to make electrical contact around the periphery of the substrate so that the necessary electrical bias may be applied to the substrate. The contact ring **602** may be further adapted to include a reference electrode that is located close to the substrate surface. A more detailed description of the contact ring **602** and thrust plate assembly **604** may be found in commonly assigned U.S. patent application Ser. No. 10/278,527, filed on Oct. 22, 2002 and entitled "Plating Uniformity Control By Contact Ring Shaping", and commonly assigned U.S. Pat. No. 6,251,236 entitled Cathode Contact Ring for Electrochemical Deposition, both of which are hereby incorporated by reference in their entirety to the extent not inconsistent with the present invention.

[**0066**] The frame member **503** of plating cell **500** supports an annular base member **504** on an upper portion thereof. Since frame member **503** is elevated on one side, the upper surface of base member **504** is generally tilted from the horizontal at an angle that corresponds to the tilt angle of frame member **503** relative to a horizontal position. Base member **504** includes a disk-shaped anode **505**. Plating cell **500** may be positioned at a tilt angle, i.e., the frame portion **503** of plating cell **500** may be elevated on one side such that the components of plating cell **500** are tilted between about 3° and about 30°.

[**0067**] Inner basin **502** is generally configured to contain a processing solution, such as a plating solution or a cathodic pre-treatment solution, during electrochemical processing of substrates. During processing, the processing solution is generally continuously supplied to inner basin **502**, and therefore, the processing solution continually overflows the uppermost point **502***a*, generally termed a "weir", of inner basin **502** and is collected by outer basin **501** and drained therefrom for chemical management and recirculation. The exemplary electrochemical processing cell is further illustrated in commonly assigned U.S. patent application Ser. No. 10/268,284, filed on Oct. 9, 2002, and entitled "Electrochemical Processing Cell", claiming priority to U.S. Provisional Application Ser. No. 60/398,345, which was filed on Jul. 24, 2002, both of which are incorporated herein by reference in their entireties.

[**0068**] In an exemplary electrochemical process, such as substrate process sequence **610**, described below in conjunction with FIG. **6**, a substrate may be transferred into an electrochemical processing cell, such as plating cell **500** for example, and positioned face-down on contact ring **602**. Thrust plate assembly **604** holds the substrate in place during processing. The substrate is then immersed in the electrolyte solution filling inner basin **502**, typically while being rotated by the contact ring **602** between about 5 rpm and about 60 rpm. The electrolyte solution may comprise an acidic, copper free solution, a complexed-copper alkaline solution, or a conventional acidic copper-containing solution, depending on the process being performed on the substrate. The substrate may be rotated between about 10 rpm and about 100 rpm during processing step by contact ring **602**. The time required for processing is dependent on each particular process, such as cathodic pre-treatment, seed layer deposition, seed layer and gapfill layer deposition, etc. Once the processing step is complete, the bias is then removed and the substrate is positioned above the electrolyte solution and uppermost point **502***a* of inner basin **502** for removal from plating cell **500**. Prior to removal from plating cell **500**, the substrate may be rotated between about 100 and 1000 rpm for between about 1 second and about 10 seconds in order to remove excess solution from the substrate.

[**0069**] FIG. **6** is a flow chart of a substrate process sequence **610**. Embodiments include a method for depositing a metal layer onto a barrier and/or adhesion layer on a substrate that includes:

[**0070**] A cathodic pre-treatment **611** of the barrier or adhesion layer in an acid-containing bath.

[**0071**] Seed layer deposition **612** of a continuous, void-free seed layer onto the cathodically pre-treated layer.

[**0072**] Gapfill layer deposition **613** of a gapfill layer on the seed layer.

[**0073**] Optional overfill deposition **614** of an ECP overfill layer.

[**0074**] In one embodiment, a cathodic pre-treatment **611** of a substrate surface, such as conductive substrate surface **114** in FIG. **2**, is performed. As noted above, the cathodic pre-treatment **611** may reduce the critical current density required to form a uniform, void-free, conformal metal layer on a barrier layer.

[**0075**] Next, seed layer deposition **612** takes place on the substrate, wherein a seed layer, such as seed layer **111** in FIG. **2**, is directly plated onto conductive substrate surface **114** using an electrochemical process with a complex alkaline bath. In one aspect, a nucleation pulse is used to improve the quality of the seed layer. In one aspect, the cathodic pre-treatment **611** and seed layer deposition **612** are performed on the same electrochemical processing system, such as ECPS 400, described above in conjunction with FIG. **4**, reducing the exposure time of the cathodically treated surface to oxygen and ambient contamination to minutes or even seconds. This minimizes the formation of unwanted deposits on the treated barrier layer surface prior to seed layer deposition.

[**0076**] Gapfill layer deposition **613** then takes place on the substrate, wherein a gapfill layer, such as gapfill layer **112** in FIG. **2**, is plated onto seed layer **111** using the electrochemical gapfill process with a complex alkaline bath described above. In one aspect, the seed layer deposition **612** and the gapfill layer deposition **613** are performed sequentially in the same plating cell using the same plating solution. This is especially useful for gapfill of interconnect features smaller than 65 nm; such small interconnect features are particularly sensitive to the formation of voids during gapfill as well as the presence of unwanted deposits at the interface between the seed layer and the gapfill layer. Because a single bath is used for both process steps, the surface of the seed layer is

never exposed to atmosphere prior to gapfill layer deposition **613**, eliminating the possibility of unwanted oxidation. Further, there is virtually no time for organic contaminants to accumulate on the seed layer surface since the seed layer deposition **612** may be followed immediately by the gapfill layer deposition **613**.

[**0077**] An overfill deposition **614** then may be performed on the substrate, wherein an ECP overfill layer, such as overfill layer **113**, may be deposited to complete formation of an interconnect layer. In one aspect, the overfill deposition **614** is performed sequentially in the same plating cell as gapfill deposition **613**, using the same plating solution. This avoids oxidation and organic contamination of the gapfill layer prior to overfill deposition **614**. In another aspect, the overfill deposition **614** is performed via a conventional acidic electrolyte ECP process. In this aspect, an additional rinsing step is performed on the substrate between the gapfill layer deposition **613** and the overfill deposition **614** to prevent cross-contamination of the plating solution used for ECP overfill. The additional rinsing step may be performed in a dedicated rinsing chamber, preferably located on the same electrochemical processing system wherein the substrate process sequence **610** may be performed. The substrate is rinsed with an aqueous solution while rotating at a rate from about 20 to about 400 rpm and subsequently dried via gas flow and/or spin-drying. Due to the inherent incompatibility of acidic and basic solutions, as well as the serious problems associated with cross-contamination of organic additives between plating solutions, rigorous cleaning of the plating cell would have to be performed between the gapfill layer deposition **613** and the overfill deposition **614** for each substrate processed therein. Instead, it is preferred that two separate ECP cells are used to complete the formation of copper layer **110** in apertures **120** on a substrate: one cell dedicated to an alkaline-based plating process, i.e., the seed layer deposition **612** and the gapfill layer deposition **613**, and one cell dedicated to acid-based plating processes, i.e., the overfill deposition **614**. To minimize waiting time and the associated oxidation and contamination of the gapfill layer prior to the overfill deposition **614**, both ECP cells are preferably situated on the same substrate processing platform, such as the exemplary plating system described below in conjunction with FIG. **4**. The overfill deposition **614** is particularly beneficial when there is a need to fill large and small interconnect features on a substrate surface at the same time; the small or high aspect ratio interconnect features are filled during the gapfill layer deposition **613** and the larger, low aspect ratio features are filled with the higher deposition rate ECP overfill process.

[**0078**] In another embodiment, a cathodic pre-treatment **611** is performed on a substrate surface, such as conductive substrate surface **114** in FIG. **2**. As stated above in the previous embodiment, the cathodic pre-treatment **611** reduces the critical current density.

[**0079**] Next, the seed layer deposition **612** takes place on the substrate, wherein a seed layer is directly plated onto conductive substrate surface **114** using an electrochemical process with a complex alkaline bath. In one aspect, a nucleation pulse is used to improve the quality of the seed layer. In one aspect, the cathodic pre-treatment **611** and the seed layer deposition **612** are performed on the same electrochemical processing system. In another aspect, the smallest interconnect features on a substrate are completely filled during the seed layer deposition **612**, whereas only a conformal seed layer is formed on the surfaces of larger interconnect features. As described above in the seed layer deposition **612** of the previous embodiment, it is beneficial for the cathodic pre-treatment **611** and the seed layer deposition **612** to be performed on the same electrochemical processing system to minimize the formation of unwanted deposits on the treated barrier layer surface prior to seed layer deposition.

[**0080**] In gapfill layer deposition **613**, a gapfill layer is plated onto seed layer **111** using an electrochemical gapfill process with a conventional acid bath as described above. No complexing agents are necessary in this plating process. Preferably, gapfill layer deposition **613** is performed in a different electrochemical processing cell than the seed layer deposition **612** to isolate acid-based and alkaline-based processes. In one aspect, an additional rinsing step is performed on the substrate between the seed layer deposition **612** and the gapfill deposition **613** to prevent cross-contamination of the plating solution used for gapfill. The additional rinsing step is substantially similar to that described above in overfill deposition **614** of the previous embodiment.

[**0081**] In overfill deposition **614** an ECP overfill layer may be deposited to complete formation of an interconnect layer. In one aspect, overfill deposition **614** is performed via a conventional acidic electrolyte ECP process. Overfill deposition **614** may be performed in the same electrochemical processing cell as gapfill layer deposition **613** to prevent oxidation and other surface contaminants form forming at the interface between the gapfill layer and the overfill layer. In another aspect, overfill deposition **614** is performed on the same electrochemical processing system as gapfill layer deposition **613**, but in a different electrochemical processing cell.

[**0082**] This embodiment allows for gapfill of the smallest features on a substrate during cathodic pre-treatment **611**, wherein the seed layer is deposited for larger interconnect features. Subsequently, gapfill of the larger features as well as overfill deposition of the interconnect layer may be performed on a substrate in a single ECP cell. This method increases the productivity of electrochemical processing systems by combining two process steps into a single plating cell.

[**0083**] Although several preferred embodiments which incorporate the teachings of the present invention have been shown and described in detail, those skilled in the art can readily devise many other varied embodiments that still incorporate these teachings.

[**0084**] While the foregoing is directed to embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

1. A method for depositing copper onto a substrate surface, wherein the substrate surface comprises an interlayer, comprising:

depositing an interlayer on a substrate surface;

pre-treating the substrate surface to remove unwanted deposits from the surface of the interlayer by a cathodic

treatment in an acid-containing bath to reduce a critical current density during plating; and

depositing a first copper layer onto the interlayer, wherein the first copper layer is a continuous copper layer and wherein the process of depositing the first copper layer onto the interlayer comprises:

placing the substrate surface into contact with a copper solution, wherein the copper solution comprises complexed copper ions, a complexing agent and a pH equal to or greater than 7.0; and

applying a first plating bias to the substrate surface.

2. The method of claim 1, wherein the interlayer is selected from the group consisting of cobalt, titanium, titanium nitride, titanium silicon nitride, tantalum, tantalum nitride, tantalum silicon nitride, tungsten, tungsten nitride, a Ti—W alloy, ruthenium, a ruthenium-tantalum alloy, rhodium, osmium or iridium.

3. The method of claim 1, wherein the complexed copper ions are selected from the group consisting of copper ED, copper EDTA, copper citrate and combinations thereof.

4. The method of claim 1, wherein the acid-containing bath is positioned on the same copper plating system as the copper solution.

5. The method of claim 1, wherein the cathodic treatment is performed at a potential in the range of about 0 volt to about −1.0 volt.

6. The method of claim 1, wherein the cathodic treatment is performed at a current density in the range of about 0.05 mA/cm^2 to about 5 mA/cm^2.

7. The method of claim 1, wherein the acid-containing bath contains sulfuric acid, wherein the concentration of the sulfuric acid is in the range between about 10 g/l to about 50 g/l.

8. The method of claim 1, wherein the process of applying a first plating bias comprises plating copper onto the interlayer with a plating current that is at least equal to a critical current density.

9. The method of claim 8, wherein the critical current density is less than 10 mA/cm^2.

10. The method of claim 1, further comprising depositing a second copper layer onto the first copper layer, wherein the process of depositing the second copper layer comprises:

placing the substrate surface into a second copper solution, wherein the second copper solution is acidic and includes free-copper ions; and

applying a second plating bias to the substrate surface.

11. The method of claim 10, further comprising:

applying a third plating bias to the substrate surface while in contact with the second copper solution to deposit a third copper layer onto the second copper layer.

12. The method of claim 1, further comprising:

applying a second plating bias to the substrate surface while in contact with the copper solution to deposit a second copper layer onto the first copper layer.

13. The method of claim 1, further comprising:

applying a nucleation bias to the substrate surface after placing the substrate surface into the copper solution and prior to applying a first plating bias to the substrate surface, the nucleation bias being configured to generate a first current density across the substrate surface greater than a critical current density.

14. The method of claim 2, wherein the interlayer is an interlayer on which a discontinuous copper film has been deposited.

15. A method for depositing copper onto a substrate surface, wherein the substrate surface comprises an interlayer, comprising:

depositing an interlayer on a substrate surface;

pre-treating the substrate surface to remove unwanted deposits from the surface of the interlayer by a cathodic treatment in an acid-containing bath to reduce a critical current density during plating;

depositing a first copper layer onto the interlayer, wherein the first copper layer is a continuous copper layer and wherein the process of depositing the first copper layer onto the interlayer comprises:

placing the substrate surface into contact with a copper solution, wherein the copper solution comprises complexed copper ions, a complexing agent and a pH equal to or greater than 7; and

applying a first plating bias to the substrate surface; and

applying a second plating bias to the substrate surface while in contact with the copper solution to deposit a second copper layer onto the first copper layer.

16. The method of claim 15, wherein the interlayer is selected from the group consisting of cobalt, titanium, titanium nitride, titanium silicon nitride, tantalum, tantalum nitride, tantalum silicon nitride, tungsten, tungsten nitride, a Ti—W alloy, ruthenium, a ruthenium-tantalum alloy, rhodium, osmium and iridium.

17. The method of claim 15, wherein the complexed copper ions are selected from the group consisting of copper ED, copper EDTA, copper citrate and combinations thereof.

18. The method of claim 15, further comprising:

applying a third plating bias to the substrate surface while in contact with the copper solution to deposit a third copper layer onto the second copper layer.

19. A method for depositing copper onto a substrate surface, wherein the substrate surface comprises a ruthenium-tantalum alloy, comprising:

depositing a ruthenium-tantalum alloy on a substrate surface; and

depositing a first copper layer onto the ruthenium-tantalum alloy, wherein the first copper layer is a continuous copper layer and wherein the process of depositing the first copper layer onto the ruthenium-tantalum alloy comprises:

placing the substrate surface into contact with a copper solution, wherein the copper solution comprises complexed copper ions, a complexing agent and a pH equal to or greater than 7.0; and

applying a first plating bias to the substrate surface.

20. The method of claim 19, wherein the ruthenium-tantalum alloy contains between about 70 atomic % and about 95 atomic % of ruthenium and the balance tantalum.

21. The method of claim 20, wherein the thickness of the ruthenium-tantalum alloy is between about 5 Å to about 200 Å.

22. The method of claim 19, wherein the complexed copper ions are selected from the group consisting of copper ED, copper EDTA, copper citrate and combinations thereof.

23. The method of claim 19, further comprising depositing a second copper layer onto the first copper layer wherein the process of depositing the second copper layer comprises:

applying a second plating bias to the substrate surface while in contact with the copper solution to deposit a second copper layer onto the first copper layer.

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