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(54) Title: LOW DROP-OUT DC VOLTAGE REGULATOR

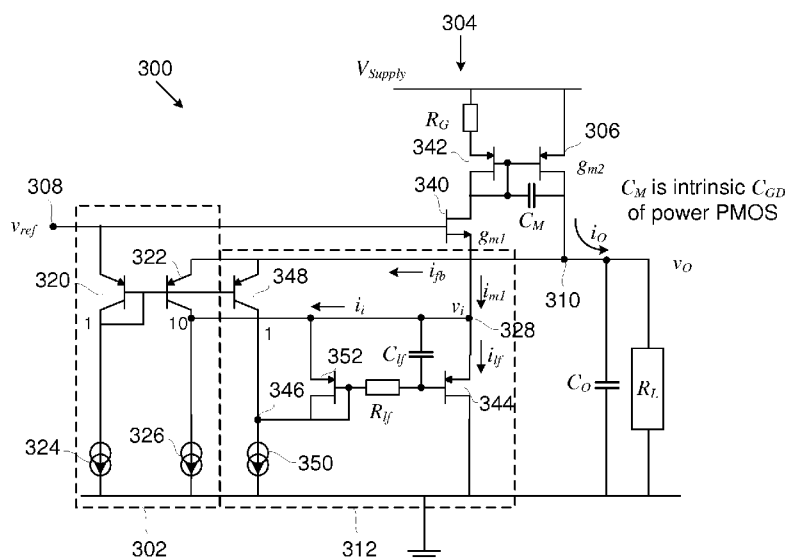


Fig. 3

(57) Abstract: A low drop-out DC voltage regulator comprising an output pass element (306) for controlling an output voltage (v) of power supplied from a power supply through the output pass element to a load (R), a source of a reference voltage (v), and a feedback loop for providing to the output pass element a control signal tending to correct error in the output voltage. The feedback loop includes a differential module (302) responsive to relative values of the output voltage (v) and the reference voltage (v) and an intermediate module (304) driven by the differential module for providing the control signal. The differential module (302) presents the widest bandwidth of the modules of the regulator and the differential module presents a frequency pole (500) that is higher than the cut-off frequency (502) of the regulator, at which its regulation gain becomes less than one.

Title : LOW DROP-OUT DC VOLTAGE REGULATOR**Description**Field of the invention

This invention relates to low drop-out (LDO) DC voltage regulators.

5 Background of the invention

A low drop-out DC voltage regulator is a regulator circuit that provides a controlled and stable DC voltage relative to a reference voltage. The operation of the circuit is based on feeding back an amplified error signal which is used to control output current flow of a pass device, such as a power field-effect transistor ('FET') driving a load. The drop-out voltage is the difference between the supply
10 voltage and the output voltage below which regulation is lost. The minimum voltage drop required across the LDO regulator to maintain regulation is just the voltage across the pass device.

The low drop-out nature of the regulator makes it appropriate (over other
15 types of regulators such as DC-DC converters and switching regulators) for use in many applications such as automotive, portable, and industrial applications. In the automotive industry, the low drop-out voltage is necessary for example during cold-crank conditions where an automobile's battery voltage can be below 6V. LDO voltage regulators are also widely used in mobile products with battery power
20 supplies (such as cellular phones, personal digital assistants, cameras and laptop computers), where the LDO voltage regulator typically needs to regulate under low supply voltage conditions.

The main components of a simple LDO DC linear voltage regulator are a power amplifier such as an FET forming the pass device and a differential
25 amplifier (error amplifier). One input of the differential amplifier monitors a percentage of the output, as determined for example by the ratio of a resistive voltage divider across the output. The second input to the differential amplifier is from a stable voltage reference (such as a bandgap reference voltage source). If the output voltage rises too high relative to the reference voltage, the drive to the

power FET changes so as to maintain a constant output voltage. These elements constitute a DC regulation loop which provides voltage regulation.

In a typical LDO voltage regulator, the first stage (the error amplifier) presents a high impedance node. This high impedance node creates a frequency pole. The power amplifier, the output (including the load) and the first stage pole would give instability, which is avoided by using the output pole as the dominant pole to get stability. Generally this type of driver is still unstable when the load capacitance is 0. Accordingly, the output capacitance has to be specified, as does a minimum and maximum Equivalent Series Resistance ('ESR'). As the load is part of the regulation loop, it is still possible for instability to be caused by such indeterminate factors as parasitic capacitance.

US patent specification 6 373 233 describes a LDO voltage regulator including a capacitor connected in a compensation circuit element between control and output terminals of an output transistor. The voltage characteristics of the capacitor must be compatible with the usage specification and for a high voltage application, such as a 40 volt maximum output voltage, for example, the capacitor cannot be integrated in the manufacturing process of the voltage regulator using some metal-oxide-Silicon manufacturing techniques.

Transient load regulation is another important parameter of a LDO voltage regulator but US patent specification 6 373 233 gives no information on how adequate performance in this respect could be achieved.

Summary of the invention

The present invention provides a low drop-out DC voltage regulator as described in the accompanying claims.

Brief description of the drawings

Figure 1 is a schematic circuit diagram of a known low drop-out DC voltage regulator,

Figure 2 is a graph of voltage gain against frequency for the LDO regulator of Figure 1,

Figure 3 is a schematic circuit diagram of a low drop-out DC voltage regulator in accordance with one embodiment of the invention, given by way of example,

Figure 4 is a representation of a configuration of the LDO regulator of Figure 3 for the purposes of open feedback loop analysis, without a frequency and phase
5 compensation module,

Figure 5 is a graph of open-loop voltage gain against frequency for the LDO regulator configuration of Figure 5,

Figure 6 is a representation of a configuration of the LDO regulator of Figure 3, with the frequency and phase compensation module, for the purposes of open
10 feedback loop analysis,

Figure 7 shows graphs of open-loop voltage gain against frequency for the LDO regulator of Figures 4 and 6 by way of comparison,

Figures 8 and 9 show graphs of open-loop voltage gain against frequency for the LDO regulator of Figure 5 for two different load capacitances,

Figure 10 is a representation of the LDO regulator of Figure 3 in closed loop configuration but without the frequency compensation module, and
15

Figure 11 is a graph of output voltage against time for the LDO regulators of Figures 3 and 10, illustrating their comparative transient responses.

Detailed description of the preferred embodiments

Figure 1 shows a known LDO voltage regulator 100 powered by a voltage
20 V_{supply} from a power supply (not shown) such as a battery, and which comprises a differential field effect transistor ('FET') pair module T1-T4, receiving a reference voltage v_{ref} from a source (not shown) such as a bandgap circuit on one input and a feedback voltage v_{fb} on another input. The differential transistor pair module T1-
25 T4 provides an output corresponding to the difference between the reference voltage v_{ref} and the feedback voltage v_{fb} to an intermediate buffer stage comprising FETs T5-T6 in series between the supply voltage v_{supply} and ground, the buffer stage driving an FET pass device T7 coupled to a load comprising in parallel a resistive component R_L and a capacitor C_L having an equivalent series resistance
30 ESR. The output voltage is applied to a voltage divider comprising resistors R_1

and R2, which generate the feedback voltage v_{fb} with a proportionality that may be varied to choose the relation between the regulated output voltage and the reference voltage. These elements constitute a DC regulation loop which provides low drop-out voltage regulation.

5 Figure 2 shows the open loop gain A_{vo} of the voltage regulation loop, that is to say the gain V_O/V_{fb} with V_{ref} fixed (DC voltage) and the feedback loop opened between the gate of T2 and the common point between R1 and R2, as a function of frequency f . The system has a dominant low frequency pole FP_{OUT} created by the output capacitance CL, a zero Z_{ESR} created by the ESR of the output
10 capacitance CL, a further sub-dominant pole FP_{DIFF} created by the differential pair module T1-T4 and a further sub-dominant pole FP_{INT} created by the intermediate buffer stage T5-T6. The dominant low frequency pole FP_{OUT} created by the output capacitance CL is at a frequency much lower than the cut-off frequency at which the regulation gain of the regulator becomes less than one (zero dB).

15 It will be understood that the use in the intermediate buffer stage of device T5 alone produces the plot shown in full and chain-dotted lines in Figure 2, and that the use additionally of device T6 allows the pole FP_{OUT} to track the displacement of the pole FP_{OUT} as shown by the dashed line in the drawing. The open loop DC gain of the output stage varies as a function of output current since it is
20 proportional to:

$$g_{m7} \cdot (r_{DS7} // R_L) \propto \frac{1}{\sqrt{I_L}} \dots \dots \dots \text{Equation 1}$$

where g_{m7} is the transconductance of the pass device T7 itself, r_{DS7} is the output resistance presented by the pass device T7 with the voltage divider R1-R2 and $(r_{DS7} // R_L)$ is the resistance presented by the parallel combination of the resistances
25 r_{DS7} and R_L .

The frequency of the pole of the output stage is given by:

$$f_{OUT} = \frac{1}{2\pi C_L (r_{DS7} // R_L)} \dots \dots \dots \text{Equation 2}$$

and also varies as a function of output current since:

$$r_{DS7} // R_L \propto \frac{1}{I_L} \dots \dots \dots \text{Equation 3}$$

It follows that an increase in the load current results in the pole frequencies of the output and buffer stages increasing faster with output current than the gain diminishes, resulting in more gain at higher frequencies before reaching the cut-off frequency of the regulator.

The output pass device T7 is a PMOS FET, which allows a regulated low drop-out voltage to be obtained between supply and output voltages, but since the output is made with the drain of the PMOS device T7, the output is high impedance and the load and hence the load capacitor are part of the loop. Since the load capacitance C_L appears in the main loop of the regulator, a strict specification is imposed on its value and on its ESR, which may still require the use of a large external bypass external capacitor in addition in order to ensure the stability of the loop.

Figure 3 shows a low drop-out DC voltage regulator 300 in accordance with an embodiment of the present invention, given by way of example, which is stable independently of the load capacitance and whose use is not limited to a range of minimum and maximum load ESR, especially for high voltage applications, but also for other applications.

The low drop-out DC voltage regulator 300 is powered by a voltage v_{supply} from a power supply (not shown) such as a battery, and which comprises a differential amplifier module 302, an intermediate buffer stage 304, and an output FET pass device 306. The differential amplifier module 302 receives a reference voltage v_{ref} at an input terminal 308 from a source (not shown) such as a bandgap circuit on one input and a feedback voltage on another input equal to the output voltage v_O appearing at an output terminal 310. The load, shown as comprising a resistive component R_L and a capacitive component C_O , is connected between the output terminal 310 and ground. The differential amplifier module 302 and the intermediate buffer stage 304 form a feedback loop for providing to the output FET pass device 306 a control signal tending to correct error in the output voltage. A frequency and phase compensation module 312 between the differential amplifier

input stage 302 and the intermediate buffer stage 304 provides gain and phase compensation as a function of frequency.

In more detail, the differential amplifier input stage 302 comprises pnp transistors 320 and 322 connected with common bases. The transistor 322 is arranged to have a current-carrying capacity substantially greater than the transistor 320. In this example, it is ten times greater than the transistor 320 but in other embodiments of the invention the current-carrying capacity of the transistor 322 is between five and fifteen times the current-carrying capacity of the transistor 320. The emitter of the transistor 320 is connected to receive the reference voltage v_{ref} from the input terminal 308 and its collector is connected to its base and through a current source 324 to ground. The emitter of the transistor 322 is connected to receive the feedback voltage v_o from the output terminal 310 and its collector is connected through a current source 326 to ground and to a node 328 in the buffer stage 304.

The output pass device 306 is a p-type power FET, which has its source connected to receive the voltage v_{supply} from the power supply and its drain connected to the output terminal 310. The only significant capacitive element C_M presented by the regulator 300 at the output terminal 310 is constituted by the intrinsic gate-drain capacitance C_{GD} of the FET 306 itself. No external capacitance is utilised and would be unnecessary for the stable functioning of the regulator.

The buffer stage 312 comprises an n-type FET 340, whose source is connected to the node 328, whose gate is connected to the reference terminal 308 and whose drain is connected to the gate of the output pass FET 306. Pole tracking is provided by a p-type FET 342, whose source is connected to receive the voltage V_{supply} from the power supply through a resistor R_G , whose drain is connected to the drain of the FET 340 and whose gate is connected to the gate of the output pass FET 306 and to the drain of the FET 340.

The frequency and phase compensation module 312 comprises a p-type FET 344 whose source is connected to the node 328, whose drain is connected to ground and whose gate is connected through a capacitor C_{If} to the node 328 and through a resistor R_{If} to a node 346. The node 346 is connected to the collector of a pnp transistor 348, whose emitter is connected to the output terminal 310 and

which has its base connected in common with the transistors 318 and 320. The node 346 is also connected through a current source 350 to ground and to the drain and gate of a p-type FET 352, whose source is connected to the output terminal 310.

5 In operation, ignoring initially the effect of the frequency and phase compensation module 312, the transistor 320 establishes across the current source 324 a voltage equal to reference voltage v_{ref} diminished by a small voltage drop between the emitter and collector of the transistor 320 and applies the same voltage to the base of the transistor 322. The transistor 322 establishes across the
 10 current source 326 an error voltage v_i proportional to output voltage v_O diminished by a voltage drop between the emitter and collector of the transistor 322 and applies the same voltage to the node 328, the voltage drop across the emitter and collector path of the transistor 322 being a function of the difference between the output voltage v_O and the voltage at the collector of the transistor 320. Normally,
 15 the output voltage v_O applied to the emitter of the transistor 322 (and the emitter of the transistor 348 when the frequency and phase compensation module 312 is added) will be slightly less than the reference voltage v_{ref} and the gate-source voltage applied to the FET 340 by the terminal 308 and the node 328 will cause the FETs 340 and 342 of the buffer stage to conduct a current i_{m1} that is a function
 20 of the difference between the output voltage v_O and the reference voltage v_{ref} and of the resistor R_G , with a transconductance of the buffer stage of g_{m1} . The corresponding voltage applied to the gate of the pass FET 306 is a control signal tending to cause the FET 306 to correct error in the output voltage v_O with a transconductance of g_{m2} .

25 The differential module 302 (with the transistor 348), and hence the output 310 present low impedances to the feedback current i_{fb} , whose values in this embodiment of the invention are of the order of 260 ohms for a bias current of 100 μ A, for example, and the low impedance of this emitter-follower stage is in parallel with the drain of the FET 306. The differential module 302 presents the widest
 30 bandwidth of the modules of the regulator and the differential module 302 presents a frequency pole that is higher than the cut-off frequency of the regulator because the frequency pole of the differential module 302 is inversely proportional only to

the parasitic capacitance at this stage. In a specific implementation of the regulator of Figure 3, the resistance r_L presented to the output terminal 310 by the regulator was 140 ohms, the DC gain (at 0 Hertz) with a power supply current of 200 mA was 63dB for high load resistance and 48dB for load resistance R_L of 25 ohms.

- 5 The cut-off frequency was 20 MHz. The frequency pole of the differential module 302 was higher than the cut-off frequency and would have been over 30 MHz. More generally, the closed loop gain of the regulator is given by:

$$v_o/v_i = g_{m1} R_G g_{m2} (R_L // r_L) \bullet \frac{g_{m1}}{j C_M \omega} \dots \dots \dots \text{Equation 4}$$

- 10 where v_i is the voltage at the node 328. This gain is higher the lower the resistance r_L and the capacitance C_M presented to the output terminal 310 by the regulator. In this embodiment of the invention, the capacitance C_M is reduced to the intrinsic gate-drain capacitance C_{GD} of the FET 306 itself.

- 15 The DC gain is $v_o/v_i = g_{m1} R_G g_{m2} (R_L // r_L)$ and the difference between the DC gains at high load impedance and at low (25 ohm) load impedance is only 15dB in the implementation example referred to above.

- Figure 4 represents a theoretical configuration of the regulator of Figure 3 for open-loop analysis, with an interruption in the feedback loop between the output terminal 310 and an input 400 for the differential amplifier input stage 302, the frequency and phase compensation module 312 being omitted initially. Figure 5 shows the overall open loop gain v_o/v_{fb} of the regulator for the implementation referred to above, where v_{fb} is the voltage at the input 400, and the curve v_i/v_{fb} shows that the frequency pole 500 of the differential amplifier module 302 does not appear before a frequency over 30MHz, higher than the cut-off frequency 502 at $\frac{g_{m1}}{2\pi \cdot C_M}$, which is 20MHz in this implementation.

- 25 An effect of the addition of the frequency and phase compensation module 312 is illustrated by comparison with Figure 6, which is a theoretical open loop configuration of the regulator similar to Figure 4 but including the frequency and phase compensation module 312. Figure 7 shows the open loop gain v_i/v_{fb} of the differential amplifier input stage 302 alone in curve 700 and with the phase

compensation module 312 included in curve 702. It will be seen that without the phase compensation module 312 the gain of the stages is 10 dB in the implementation referred to above, substantially independent of frequency until the frequency pole, at over 30MHz. In the phase compensation module 312, the FET 344 is part of a current amplifier, driven by the transistor 348, which has a current carrying area $1/10^{\text{th}}$ of the transistor 322 in this example, and by the FET 352 through the resistance R_{if} . At low frequencies, below 733 Hz for example, the phase compensation module 312 increases the gain v_i/v_{fb} of the two stages to nearly 30dB but the gain reduces to 10dB at higher frequencies, due to the capacitor C_{if} between the gate and source of the FET 344. The high frequency gain is sufficient to drive the maximum transient output current in the load R_L .

Analysis shows that the LDO regulator 300 is stable whatever the values of the load resistance and capacitance, as measured by the phase margin, that is to say the margin from a phase shift in the regulator loop of 180° at which the feedback would be positive instead of negative and oscillation would occur. When the load capacitance C_O is large, for example 100 μ F, the dominant pole is given by C_O and the phase margin for the implementation referred to above is 85° , so that the regulator is stable.

As shown in Figure 8, when the load capacitance C_O is zero, the dominant pole is internal to the regulator and the phase margin for the implementation referred to above is 31° .

Analysis shows that, for the implementation referred to above, the worst case occurs for a value of the load capacitance C_O of 100nF, which is shown in Figure 9, and for which the phase margin is 12° , which is still sufficient to ensure stability.

Analysis also shows that, in the absence of the capacitor C_{if} of the intermediate module, the regulator would be unstable, with a negative phase margin for load capacitances of the order of 1 μ F to 10 μ F.

Figure 10 shows a theoretical closed-loop configuration 800 of the regulator of Figure 4 without the frequency and phase compensation module 312 for the purpose of comparison of the transient response with the complete regulator 300 of Figure 3. In Figure 11, the curve 900 shows the response as a function of time of the configuration 500 of Figure 10 to a step change in load resistance from

open-circuit to a finite value conducting a current i_O of 200 mA and the curve 902 shows the comparable response of the complete regulator 300. The transistor 320 and current source 324 carry a substantially constant current of 10 μ As.

For both configurations 300 and 800, at time 0 shown at point 504 where the
 5 load is open-circuit, the load current i_O is 0 mAs and the offset between the output voltage v_O and the reference voltage v_{ref} is zero. The feedback current i_{fb} from the node 310 to the modules 302 and 312 is 100 μ As and flows through the transistor 322 and the current source 326 to ground.

When the load assumes its finite value, the load current i_O rises to its
 10 maximum value, in this example 200 mAs, and the offset between the output voltage v_O and the reference voltage v_{ref} rises to 60 mV, as shown at point 906 in Figure 11. In the case of the configuration 800 of Figure 10, the feedback current i_{fb} from the node 310 to the module 302 is reduced to 10 μ As and is added with a current i_i of 90 μ As from the node 328 of the buffer stage 304 to flow through the
 15 current source 326 to ground. Consequently, the voltage difference between the gate (v_{ref}) and the source (node 328) of the FET 340 remains reduced and the offset between the output voltage v_O and the reference voltage v_{ref} remains at 60 mV, as shown at 908.

In the case of the configuration 300 of Figure 3, at the point 906, the
 20 feedback current i_{fb} from the node 310 to the module 302 is again reduced to 10 μ As and flows through the transistor 322, being added with a current i_i of 90 μ As from the node 328 of the buffer stage 304 to flow through the current source 326 to ground. A current i_{lf} of 80 μ As also flows through the FET 344, which is biased by the capacitor C_{lf} , previously charged by the voltage v_{ref} through the FET 340.
 25 Consequently, the voltage difference between the gate (v_{ref}) and the source (v_i) of the FET 340 increases rapidly and the offset between the output voltage v_O and the reference voltage v_{ref} reduces rapidly from 60 mV to 4mV at point 910 in Figure 11, the capacitor C_{lf} progressively discharging due to a current of 10 μ As also flowing through the resistor R_{lf} and the current source 350 to ground.

Claims

1. A low drop-out DC voltage regulator comprising an output pass element (306) for controlling an output voltage (v_O) of power supplied from a power supply through the output pass element to a load (R_L), a source of a reference voltage (v_{ref}), and a feedback loop for providing to said output pass element a control signal tending to correct error in the output voltage, said feedback loop including a differential module (302) responsive to relative values of said output voltage (v_O) and said reference voltage (v_{ref}) and an intermediate module (304) driven by said differential module for providing said control signal, the regulator presenting a cut-off frequency at which its regulation gain becomes less than one,

characterised in that said differential module (302) presents the widest bandwidth of the modules of the regulator and said differential module presents a frequency pole (500) that is higher than said cut-off frequency (502).
2. A low drop-out DC voltage regulator as claimed in claim 1, wherein said feedback loop presents a gain at high frequencies sufficient to drive the transient output current in said load (R_L) and a higher gain at low frequencies.
3. A low drop-out DC voltage regulator as claimed in claim 1 or 2, wherein said differential module (302) includes a differential amplifier (320-326), and said feedback loop includes a further amplifier element (312) comprising a capacitive element (C_{lf}) such as to increase gain of said differential module at low frequencies.
4. A low drop-out DC voltage regulator as claimed in claim 3 wherein said differential amplifier (320-326) comprises a differential pair of transistors (320, 322) connected in common base configuration for providing an error voltage (v_i) that is responsive to relative values of said output voltage (v_O) and said reference voltage (v_{ref}), and said further amplifier element (312) comprises a further transistor (348) connected in common base configuration with said

differential pair (320, 322) and connected to drive a current amplifier (344) including said capacitive element.

5. A low drop-out DC voltage regulator as claimed in any preceding claim, wherein said intermediate module (304) comprises the series combination of a first control element (340) driven by said differential module and a second control element (342) connected in a current mirror configuration with said output pass element (306).

AMENDED CLAIMS

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(02.02.2009)

1. A low drop-out DC voltage regulator (300) comprising an output pass element (306) for controlling an output voltage (v_o) of power supplied from a power supply through the output pass element to a load (R_L), a source of a reference voltage (v_{ref}), and a feedback loop for providing to said output pass element a control signal tending to correct error in the output voltage, said feedback loop including a differential module (302) including a differential amplifier (320-326) responsive to relative values of said output voltage (v_o) and said reference voltage (v_{ref}) and an intermediate module (304) driven by said differential module for providing said control signal, the regulator presenting a cut-off frequency at which its regulation gain becomes less than one,

wherein said differential module (302) presents the widest bandwidth of the modules of the regulator and said differential module presents a frequency pole (500) that is higher than said cut-off frequency (502), and said feedback loop includes a further amplifier element (312) comprising a capacitive element (C_{lf}) such as to increase gain of said differential module at low frequencies, the low drop-out DC voltage regulator (300) being stable as measured by the phase margin whatever the values of the load resistance and capacitance.
2. A low drop-out DC voltage regulator as claimed in claim 1, wherein said feedback loop presents a gain at high frequencies sufficient to drive the transient output current in said load (R_L) and a higher gain at low frequencies.
3. A low drop-out DC voltage regulator as claimed in claim 1 or 2 wherein said differential amplifier (320-326) comprises a differential pair of transistors (320, 322) having bases connected in common for providing an error voltage (v_i) that is responsive to relative values of said output voltage (v_o) and said reference voltage (v_{ref}), and said further amplifier element (312) comprises a further transistor (348) having a base connected in common with the bases of said differential pair (320, 322) and connected to drive a current amplifier (344) including said capacitive element.

4. A low drop-out DC voltage regulator as claimed in any preceding claim, wherein said intermediate module (304) comprises the series combination of a first control element (340) driven by said differential module and a second control element (342) connected in a current mirror configuration with said output pass element (306).

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PRIOR ART

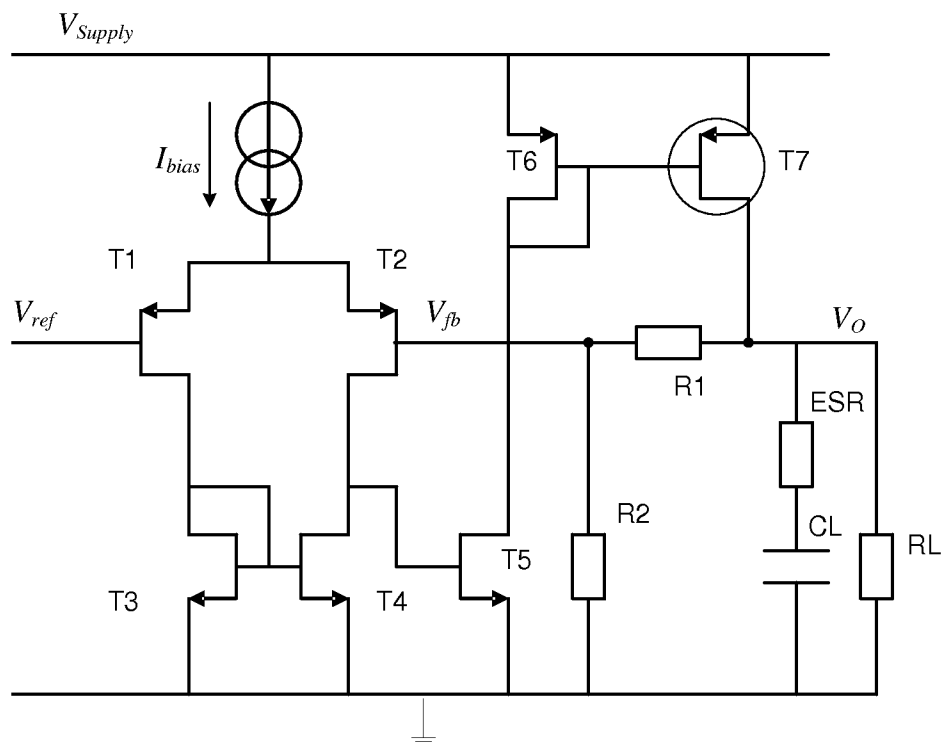


Fig. 1

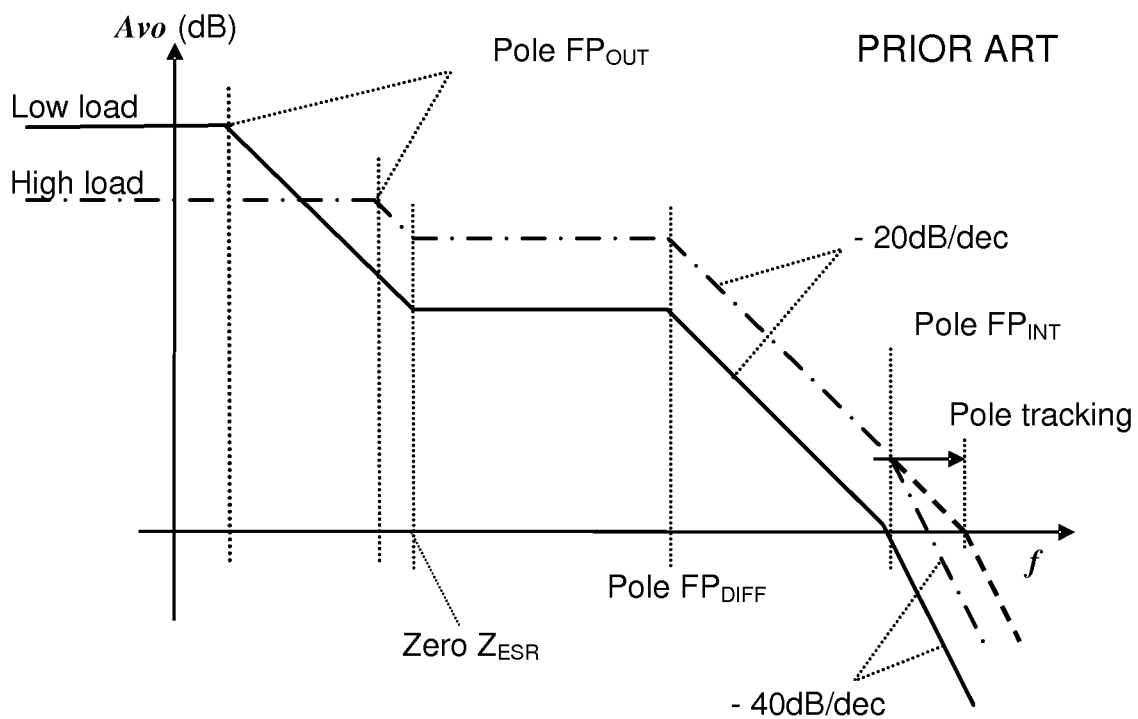


Fig. 2

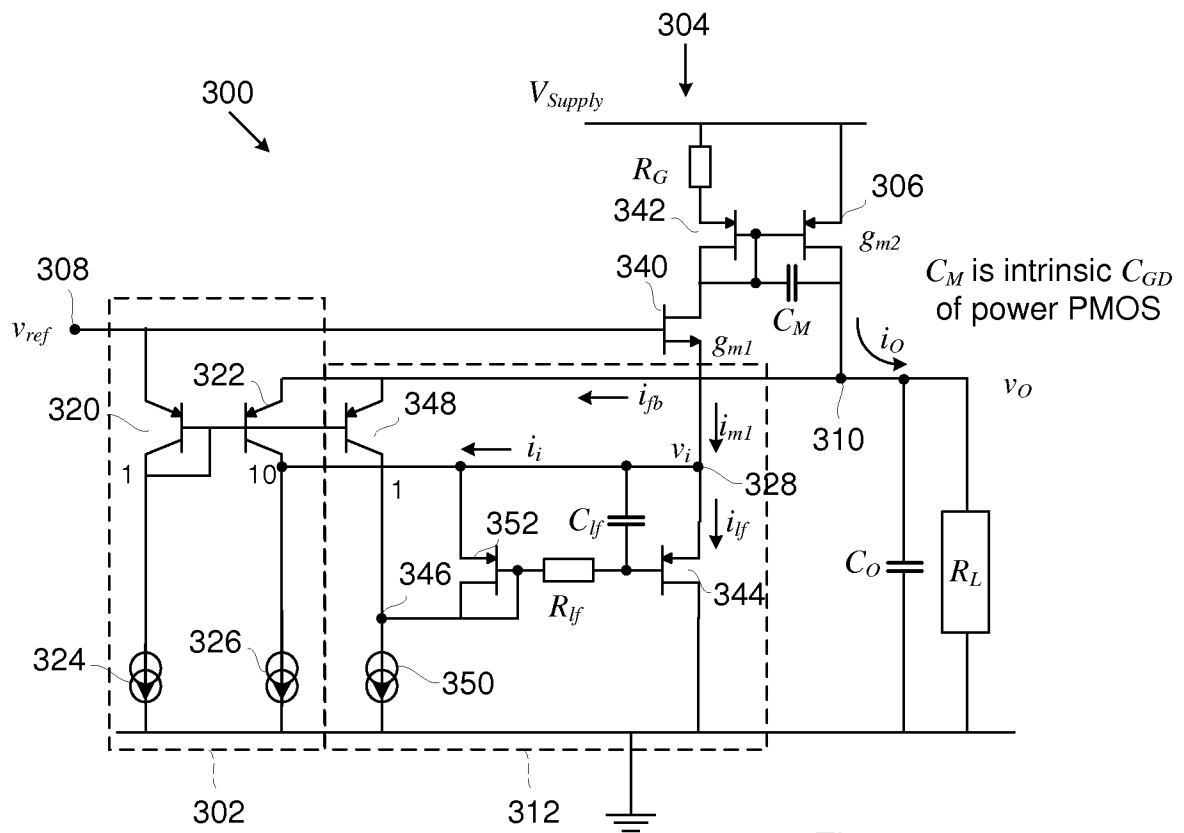


Fig. 3

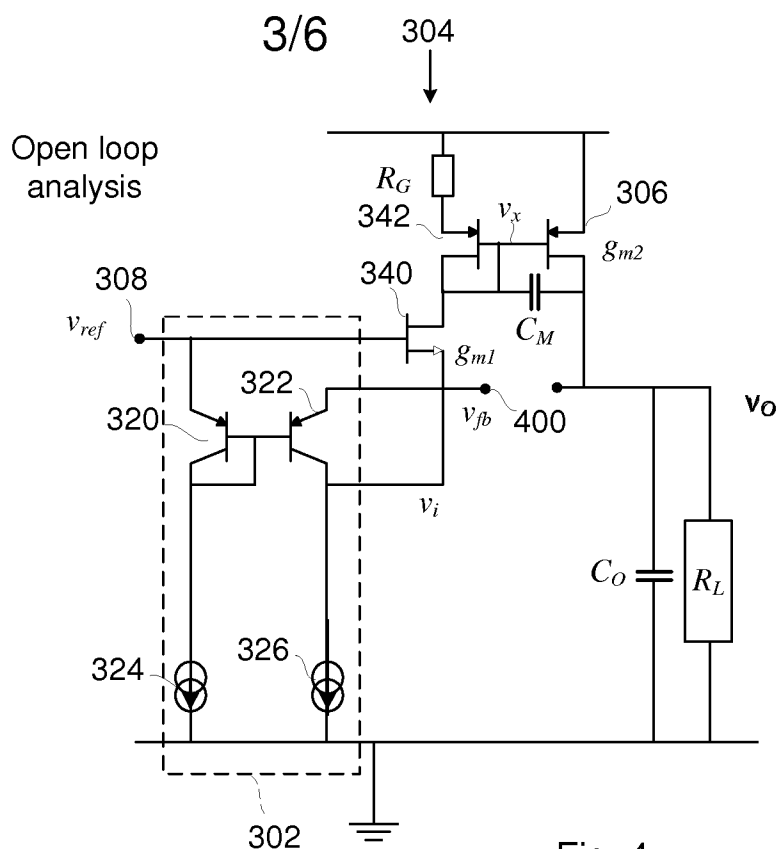


Fig. 4

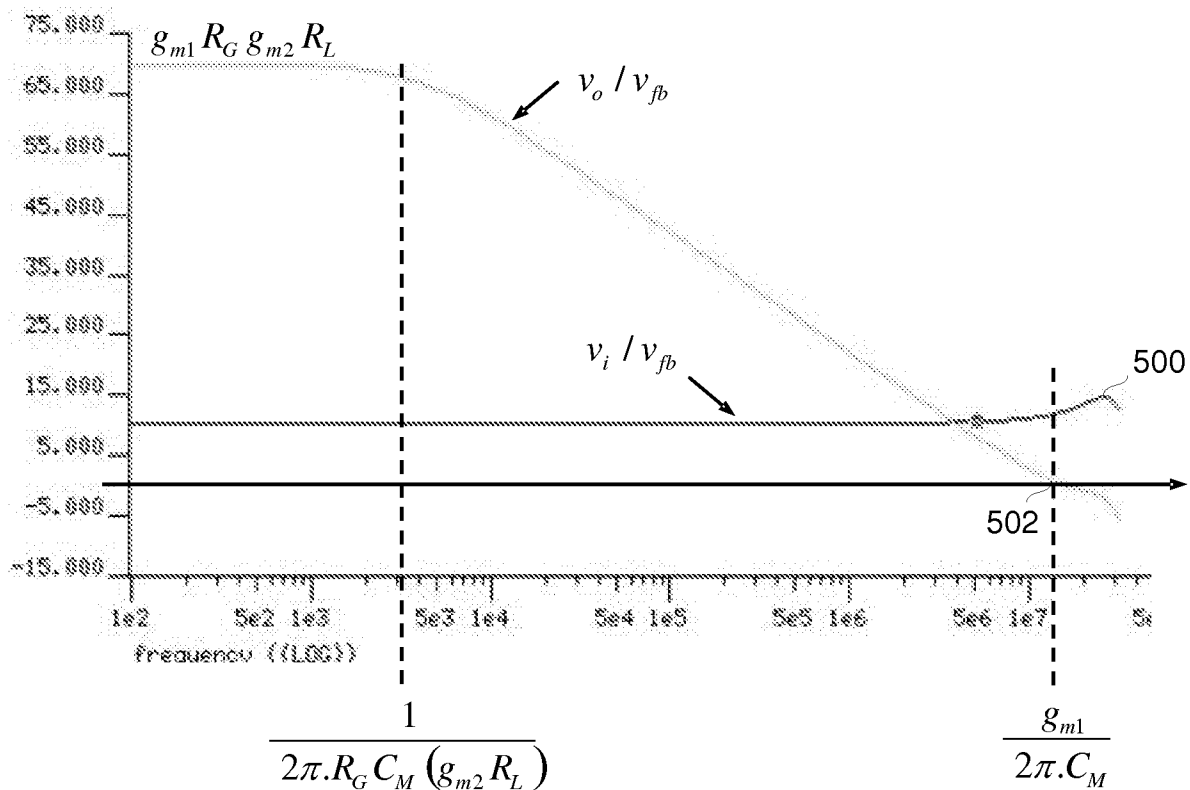


Fig. 5

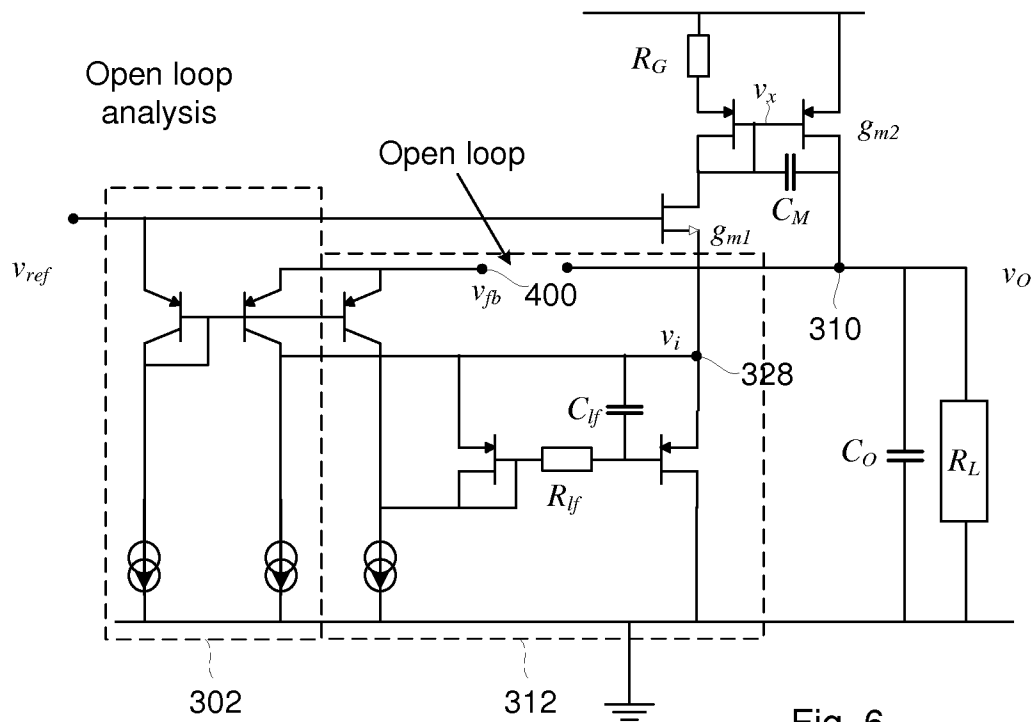


Fig. 6

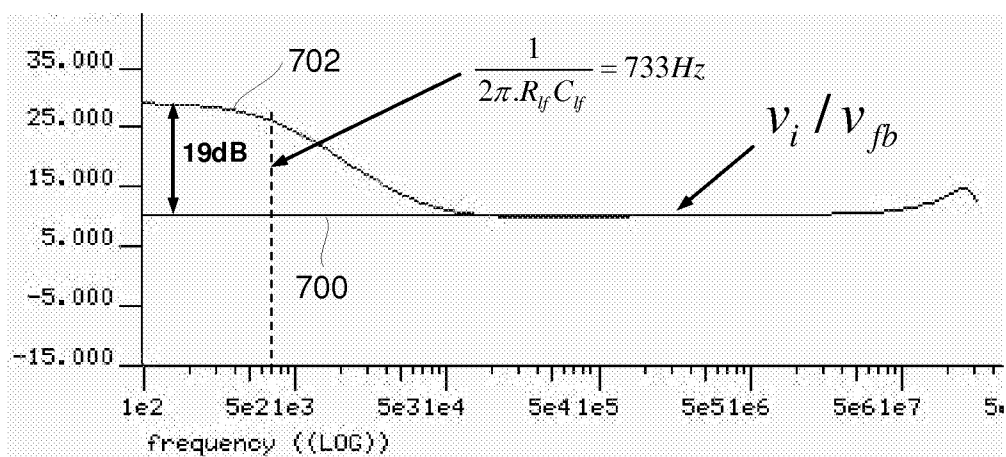


Fig. 7

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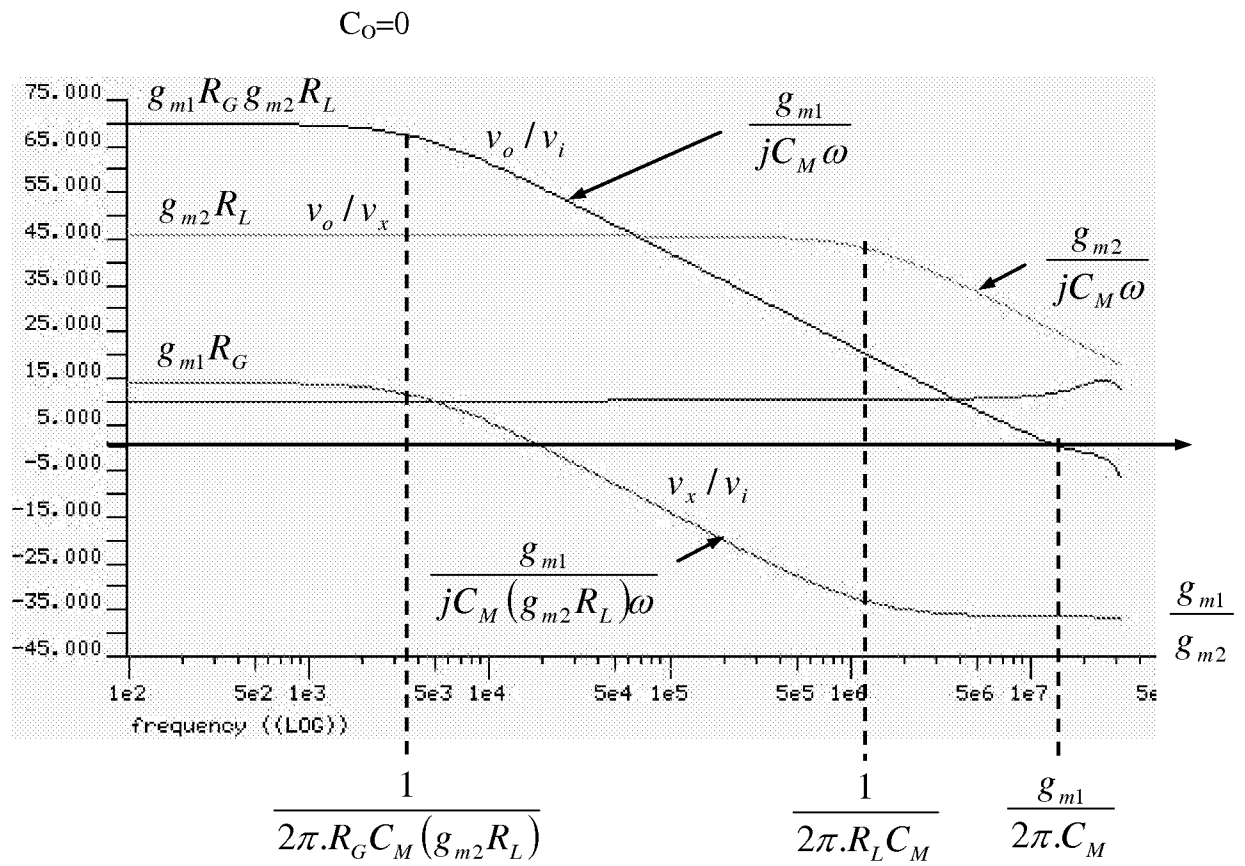


Fig. 8

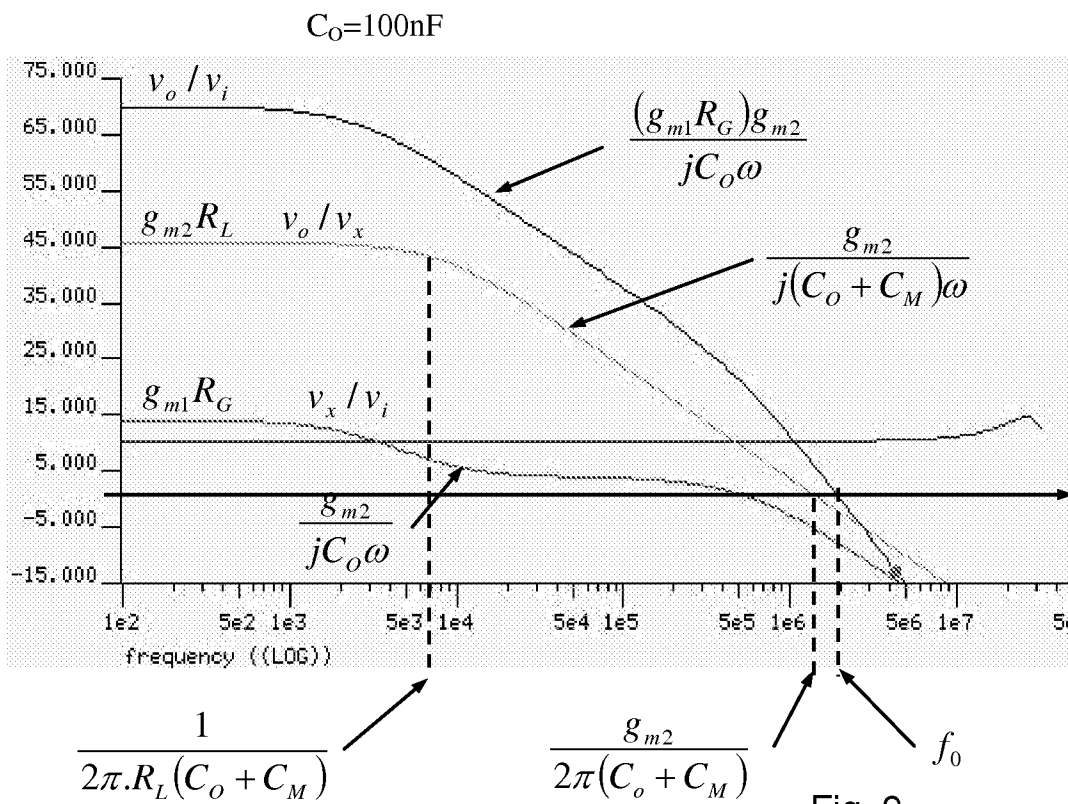


Fig. 9

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Transient analysis

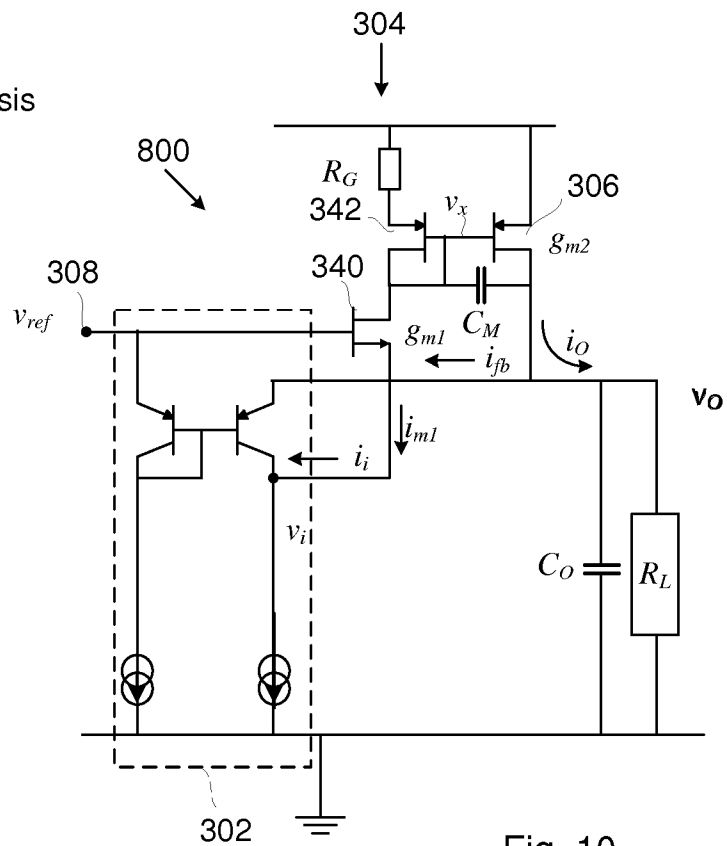


Fig. 10

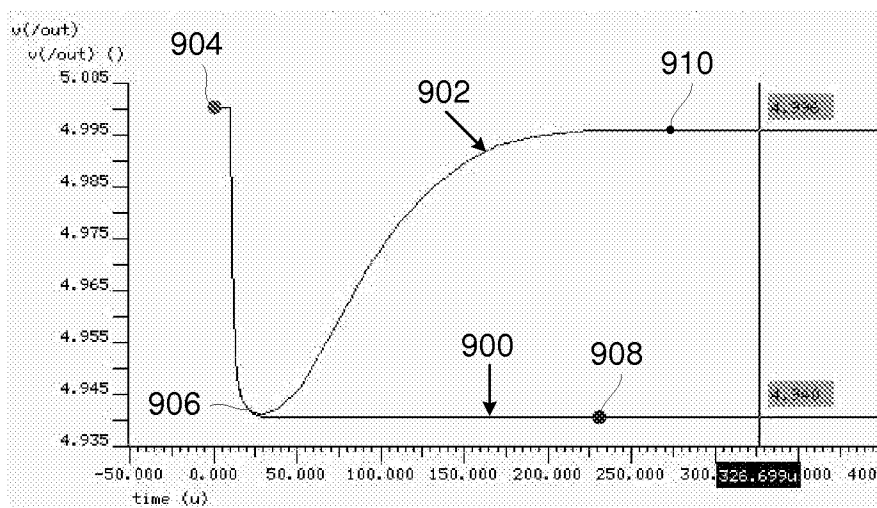


Fig. 11

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2008/051769

A. CLASSIFICATION OF SUBJECT MATTER
INV. G05F1/56

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G05F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2006 318204 A (FUJI ELEC DEVICE TECH CO LTD) 24 November 2006 (2006-11-24) paragraphs [0004] - [0011]; figures 1,2,11,12	1-5
A	US 2004/164789 A1 (LEUNG KA NANG [HK] ET AL) 26 August 2004 (2004-08-26) columns 1-6; figures 1-4	1-5
A	US 5 909 109 A (PHILLIPS TIMOTHY A [US]) 1 June 1999 (1999-06-01) columns 1-6; figures 1-4	1-5
A	US 2003/235058 A1 (TOYOSHIMA HIROSHI [JP] ET AL) 25 December 2003 (2003-12-25) paragraphs [0058] - [0079]; figures 1-9	1-5



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/IB2008/051769

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
JP 2006318204	A	24-11-2006	NONE	
US 2004164789	A1	26-08-2004	NONE	
US 5909109	A	01-06-1999	NONE	
US 2003235058	A1	25-12-2003	JP 3993473 B2	17-10-2007
			JP 2004021871 A	22-01-2004
			US 2007176580 A1	02-08-2007