(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
1 November 2012 (01.11.2012)

WIPO | PCT

(10) International Publication Number
WO 2012/149123 A1

(51) International Patent Classification:
H04L 27/08 (2006.01)

(21) International Application Number:
PCT/US2012/035148

(22) International Filing Date:
26 April 2012 (26.04.2012)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
13/094,485 26 April 2011 (26.04.2011) US

(71) Applicant *(for all designated States except US)*: **ANALOG DEVICES, INC.** [US/US]; One Technology Way, Norwood, MA 02062-9106 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **ALAVI, Reza** [US/US]; 234 Monroe Ave., Belle Mead, NJ 08502 (US). **AGHTAR, Saeed** [IR/US]; 62 Longfield Dr., Hillsborough, NJ 08844 (US). **STEINBRECHER, Christoph** [DE/US]; 285 Davidson Ave., Somerset, NJ 08873 (US). **SUNDARESAN, Arathi** [IN/US]; 20 River Court, Apt. 1906, Jersey City, NJ 07310 (US).

(74) Agents: **HAILS, Robert, L.** et al.; Kenyon & Kenyon LLP, 1500 K Street, N.W., Washington, DC 20005 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

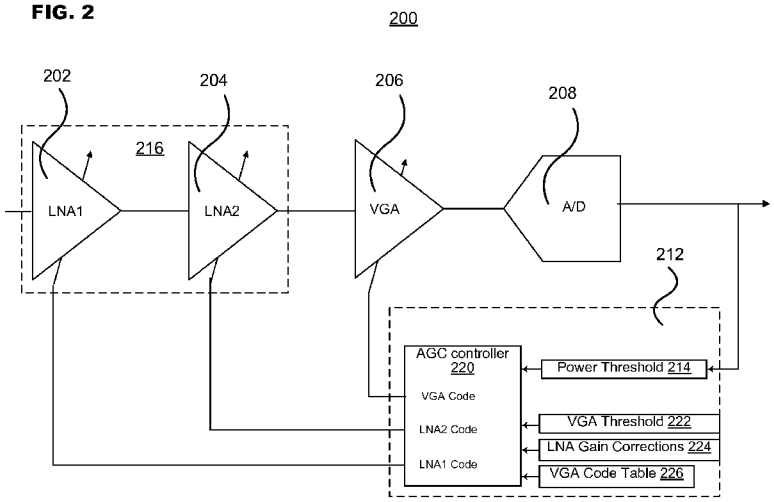
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) **Title**: RF AGC CONTROL

FIG. 2



(57) **Abstract**: Embodiments of the present invention may provide a signal processor with a wide gain range. The signal processor may comprise at least a discrete step gain stage and a continuous variable gain amplifier (VGA) stage. The discrete step gain stage may comprise a programmable gain amplifier (PGA) (e.g., low noise amplifiers 1 and 2 (LNAl and LNA2)). The VGA stage may provide a continuous range to compensate the LNAs gain steps. In one embodiment, the AGC controller enables an inherent hysteresis with the AGC step change if required.

WO 2012/149123 A1

RF AGC CONTROL

FIELD OF INVENTION

The present invention relates to signal processors, and more particularly to a signal receiver that provides a wide range of continuous front end gain.

BACKGROUND

Signal processors sometimes incorporate a front-end gain stage to keep an input signal within the input range of an analog-to-digital converter (ADC). For example, Figure 1 shows a prior art receiver with a front-end gat stage before an ADC. Sometimes, the front-end system contains a mixer to bring the input signals to a frequency band that can be digitized by the ADC.

In a typical application, a gain control algorithm changes the front-end gain according to the signal power at the input or output of the ADC. The specific usage of the signals determines whether the front-end gain changes should be continuous or discrete. A lot of applications require continuous signals and often cannot tolerate jumps in the front-end gain due to large gain steps. However, it is extremely challenging to provide continuous gain variation with a wide gain range and sufficient linearity. Further, continuous gain is difficult to implement in semiconductor processes and special processes are usually required to design such gain stages. For example, complementary metal–oxide–semiconductor (CMOS) technology can only provide gains in steps and thus, is not well suited to implement gain stage with a continuous gain variation. Therefore, there is a need in the art for providing a signal processor that can provide a wide range of continuous front end gain.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a prior art receiver with a front gain stage.

FIG. 2 illustrates a signal processor with a wide range of continuous front end gain according to an exemplary embodiment of the present invention.

FIG. 3 illustrates a low noise amplifier according to an exemplary embodiment of the present invention.

FIG. 4 illustrates a continuous variable gain amplifier (VGA) according to an exemplary embodiment of the present invention.

FIG. 5 illustrates VGA control signal mapping according to an exemplary embodiment of the present invention.

FIG. 6A illustrates an output current mirror circuit according to an exemplary embodiment of the present invention.

FIG. 6B illustrates a circuit generating control signals for the output current mirror circuit of FIG. 6A according to an exemplary embodiment of the present invention.

FIG. 7 illustrates ramp generator waveforms according to an exemplary embodiment of the present invention.

FIG. 8 illustrates gain variations of a signal processor according to an exemplary embodiment of the present invention.

FIG. 9 illustrates a process for a PGA gain calibration procedure according to an exemplary embodiment.

FIG. 10 illustrates a process for mapping the LNA offsets to VGA control offsets according to an exemplary embodiment of the present invention.

FIG. 11 illustrates a process for generating gain distributions among the PGA and VGA according to an exemplary embodiment of the present invention.

FIG. 12 illustrates a process for determining the VGA codes as a function of VGA control signal according to an exemplary embodiment of the present invention.

DETAILED DESCRIPTION

Embodiments of the present invention may provide a signal processor with a wide gain range. The signal processor may comprise at least a discrete step gain stage and a continuous variable gain amplifier (VGA) stage. The discrete step gain stage may comprise a programmable gain amplifier (PGA) (e.g., low noise amplifiers 1 and 2 (LNA1 and LNA2)). The VGA stage may provide a continuous range to compensate the LNAs gain steps. In one embodiment, the AGC controller enables an inherent hysteresis with the AGC step change if required.

Furthermore, the present invention may also provide for a method of calibrating and controlling a signal processing AGC with non-uniform gain steps. The method may comprise measuring offsets of the gain steps with respect to a lowest gain and record the offsets. When the step gain changes, the AGC may provide a continuous gain by looking up the offset and compensate for the offset.

FIG. 2 illustrates a signal processor 200 according to an exemplary embodiment of the present invention. The signal processor 200 may comprise a discreet gain stage 216, a

continuous gain stage 206 (e.g., variable gain amplifier (VGA)), an analog-to-digital converter (ADC) 208, an automatic gain control (AGC) block 212. The discreet gain stage 216 may comprise discreet step amplifiers LNA1 202 and LNA2 204. The two discreet step amplifiers LNA1 and LNA2 may be collectively referred to as the PGA. The overall front end gain to the ADC 208 may be provided by the combination of LNA1, LNA2 and VGA 206. Each of the LNA1 and LNA2 may provide stepwise gains and the VGA 206 may provide continuous gain to supplement the steps (e.g., continuous gain between the steps). Thus, the overall front end gain may be a wide range of continuous gain. This overall front end gain may be controlled by an AGC algorithm and referred to as the AGC gain. The AGC gain may be determined and controlled by the AGC block 212, which may comprise a power threshold block 214, an AGC controller 220, a VGA threshold 222, LNA gain corrections 224 and a VGA code table 226.

In one embodiment, the AGC gain may set based on the root mean square (RMS) power of the ADC output (e.g., output of the ADC 208) with respect to a target value. The AGC block 212 may monitor the input signal strength by comparing the ADC output to a power threshold at the power threshold block 214. If ADC output power is below a lower power threshold, the AGC gain may be increased. And if the ADC output power is above an upper power threshold, the AGC gain may be decreased. The AGC block 212 may include one or more filters that performs post processing on the control decisions to smooth out decision outputs and to control the adaptation rate (e.g., adjust the gain slowly even when the input signal power level needs to be greatly changed). Further, the AGC block 212 may control the timing of when the control signal is applied relative to system timing. The filtered output of the AGC decisions may be referred to as the control signal.

The power threshold block 214 may signify a change in the overall front end gain by changing an AGC control signal. The AGC controller 220 may map the AGC control signal received from the power threshold block 214 to an AGC control code. The AGC control code may be a specific code combination of the VGA code, LNA1 code and LNA2 code. The specific code combination may correspond a collective settings for the VGA, LNA1 and LNA2 to achieve the target overall front end gain. The respective VGA code, LNA1 code and LNA2 code may be determined using the VGA threshold 222, LNA Gain Corrections 224 and VGA code table 226.

The VGA threshold 222 may store programmable upper and lower VGA threshold levels. These upper and lower VGA threshold levels may be used to determine whether the gain change warrants a step change. That is, when the continuous change provided by the VGA 206 may be increased or decreased to the level of a step of the LNA1 or LNA2, this amount of

gain may be provided by the LNA1 or LNA2, and the gain provided by the VGA 206 may be reduced accordingly.

The LNA Gain Corrections 224 may be used to correct system errors of step gains. For example, the LNA gain steps may be non-uniform (e.g., a step of 3dB may be actually 2.99dB or 3.01dB instead of an exact 3dB). System errors of each gain step, which may be referred to as LNA offsets, may be recorded during a calibration process (to be described in detail later) and recorded. The LNA Gain Corrections 224 may store the LNA offsets. The AGC controller 220 may use the LNA offsets to determine the exact LNA gain and compensate with the VGA gain to ensure a smooth step change. The VGA code table 226 may store a plurality of VGA codes mapped to respective gain levels (e.g., smallest unit level controlled by the VGA). The VGA code and mapping will be described later.

In one embodiment, the signal processor 200 may be a broadband front-end receiver and the AGC block 212 may be implemented as a radio frequency (RF) AGC. In one embodiment, the broadband front-end receiver 200 may operate on an input signal having at most a Nyquist bandwidth (BW). For example, the signal processor 200 may operate on input signals up to 1 GHz of BW to accommodate the international telecommunications standard Data Over Cable Service Interface Specification (DOCSIS) cable signaling requirements.

The signal processor 200 may provide a wide gain range with discrete step gain stages using LNA1 and LNA2. FIG. 3 illustrates a low noise amplifier (LNA) 300 according to an embodiment of the present invention. The LNA 300 may comprise a ladder network 302 and a decoder 304. The ladder network 302 may comprise a plurality of resistors R306 chained in series with parallel resistors (e.g., shunt resistors) R308 coupled to each intermediate ladder node and a resistor R310 coupled to the bottom ladder node. The signal amplitude of a particular ladder node may be attenuated by a certain amount (e.g., a step) with respect to the previous ladder node. The tap-to-tap attenuation may be set by the values of the resistors R306, R308, and R310. In one embodiment, each ladder node may be coupled to a switchable transconductance amplifier (e.g., a gm-stage). The decoder 304 may generate a control signal (e.g., one of the control signals gmsel<7:0> may be on and others may be off) (the shorthand notion <n:0> in the specification may refer to the series 0, 1, 2, ...n) to select a particular gm-stage. The output current of the gm-stages may flow into a load resistor RL to generate the output voltage.

In one embodiment, the ladder network 302 may comprise eight (8) ladder nodes (e.g., 8 gm-stages) with each of the eight gm-stages being individually switchable. In this embodiment, the LNA code may be a three bits code and the decoder 304 may map the code

to a control signal to activate one of the eight gm-stages. The gain step change in the LNAs may be have a particular nominal value (e.g., 3 dB steps). In this embodiment, only one gm-stage may be active at any time and the 8 nodes resistor ladder may result in a gain range of 7 times the particular nominal value (e.g., 21dB).

The resistive input ladder network 302 may achieve constant Signal to Noise-plus-Distortion Ratio (SNDR) performance over a wide range of input amplitudes. In addition, the frequency response variation from one ladder node to the next may be small, resulting in a frequency-independent gain-control that progressively attenuates the input signal.

In the signal processor 300, the VGA gain provided by the VGA stage 206 may compensates the LNAs step gain changes in order to provide a continuous variable gain from a system perspective. FIG. 4 illustrates a VGA 400 according to an embodiment of the present invention. The VGA 400 may comprise a feedback amplifier 402 and a ramp generator 404. In one embodiment, the VGA may achieve a continuous gain by changing the value of the input-side resistor R1 of the feedback amplifier 402. R1 may include a plurality of switchable resistors. The plurality of switchable resistors may be controlled by ramps. That is, they may be controlled by soft switches (e.g., switches may be operating in weak inversion (or moderate inversion) regions (e.g., not fully open (strong inversion) or completely closed (sub-threshold) but in a kind of intermediate (leaking) mode)). The ramps may be generated by the ramp generator 404. In one embodiment, the feedback amplifier 402 may be a non-inverting feedback amplifier. In another embodiment, an inverting feedback amplifier could be used as well.

In one embodiment, as shown in FIG. 4, the input-side resistor R1 may comprise a bank of 16 switchable resistors, each controlled by one of the switches MNS_0 to MNS_{15}. The switches MNS_0 to MNS_{15} may be controlled by the ramps ramp<0> ~ ramp <15>, respectively. Each of the switches MNS_0 to MNS_{15} may operate in the weak inversion regions. The values of R10, R11, ..., R115 may be chosen such that the closed-loop gain of the amplifier has a linear-in-dB characteristic. In one embodiment, the non-inverting feedback amplifier 402 may be a current-feedback amplifier (CFA). Therefore, gain-independent loop gain may be achieved. Although the VGA only needs to provide enough continuous range to compensate for maximum LNA steps change, a VGA gain range larger than the LNA step may allow for incorporating hysteresis in the AGC path. In one embodiment, the VGA gain range may be 10dB while the LNA step may be 3dB.

In one embodiment, the VGA code may be a 10-bit control word applied to the VGA 206. The ramp generator 404 may map the 10 bit word to 16 ramp levels. FIG. 5 illustrates a ramp

generator 500 that maps the VGA code to the VGA setting according to an embodiment of the present invention. The ramp generator 500 may comprise a ramp current generator 502, a control voltage generator 504 and output ramp level generator 506. The ramp current generator 502 may comprise a current digital-to-analog converter (IDAC) 508 and an output current mirror 510. The 10-bit word may be input to the 10-bit IDAC 508. The IDAC 508 may generate an output current for each of the 8 most significant bits (MSB) of the 10-bit word and thus, there are 8 MSB output currents: MSB_iout<7:0>. The IDAC 508 may also generate one output current for the 2 least significant bits of the 10-bit word: LSB_iout (e.g., 4 levels). The 9 output currents (e.g., 8 MSB_iout and 1 LSB_iout) may be applied to the output current mirror 510. The IDAC 508 may further generate a plurality of control signals (e.g., four control signal lsbsw<3:0>) from the VGA code. The output current mirror 510 may combine the 9 output currents to generate four ramp currents ramp_curr<3:0> according to the control signals. The details of the output current mirror 510 will be described with respect to FIG. 6A and the generation of the control signals will be described with respect to FIG. 6B below.

The four ramp currents generated by the output current mirror 510 may be provided to the output ramp level generator 506, which may comprise four trans-impedance amplifiers (TIA), TIA0 through TIA3. The four ramp currents may be applied to the four TIAs respectively to generate ramp voltages ramp<0>, ramp<5>, ramp<10> and ramp<15>. As shown in FIG. 5, the remaining ramp voltages (e.g., ramp<1>, ramp<2>, etc.) may be generated by resistively interpolating the outputs of the four TIAs.

The control voltage generator 504 may comprise two voltage generation blocks: a V_{off}-gen block and a V_{on}-gen block. The voltage V_{off} may be a function of the input common-mode voltage VCM_{in}. The voltage V_{on} may be the maximum voltage that complies with the allowable operating voltages of the switches MNS_0 through MNS_{15} in the resistor bank R1 of FIG. 4. The voltage V_{off} may be applied to the positive terminal of the TIAs. The ramp voltages generated by the output ramp level generator 506 may start at a voltage level V_{off}, and the maximum voltage of the ramp voltages may be Imax*Rf, but is no larger than V_{on}.

FIG. 6A illustrates an output current mirror circuit 600 according to an exemplary embodiment of the present invention. The output current mirror circuit 600 may generate a plurality of ramp currents (e.g., ramp_curr<3:0>) from the input currents generated based on the VGA code (e.g., one LSB_iout current and 8 MSB_iout currents). As shown in FIG. 6A, each of the ramp currents ramp_curr<3:0> may be a combination of some of the input currents. The ramp current ramp_curr<0> may be a combination of LSB_iout, MSB_iout<0>, MSB_iout<1>, MSB_iout<2>, MSB_iout<3> and MSB_iout<4>. The ramp_curr<1> may be a

combination of LSB_iout, MSB_iout<1>, MSB_iout<2>, MSB_iout<3>, MSB_iout<4> and MSB_iout<5>. The ramp_curr<2> may be a combination of LSB_iout, MSB_iout<2>, MSB_iout<3>, MSB_iout<4>, MSB_iout<5> and MSB_iout<6>. The ramp_curr<3> may be a combination of LSB_iout, MSB_iout<3>, MSB_iout<4>, MSB_iout<5>, MSB_iout<6> and MSB_iout<7>. Each of the ramp currents ramp_curr<3:0> may be further controlled by one of the control signals lsbsw<3:0>, respectively.

FIG. 6B illustrates a circuit 610 that may generate the control signals lsbsw<3:0> for the output current mirror circuit of FIG. 6A according to an exemplary embodiment of the present invention. The circuit 610 may comprise a bin-to-thermo decoder 612. The bin-to-thermo decoder 612 may take the eight (8) most significant bits of the VGA 10-bit control word and generates 256 signals s<255:0> (e.g., 2^8 = 256). In one embodiment, as shown in FIG. 6B, the control signal lsbsw<0> may be an inversion of the signal s<159>, the control signal lsbsw<1> may be an XOR of the signals s<31> and s<191>, the control signal lsbsw<2> may be an XOR of the signals s<63> and s<223>, and the control signal lsbsw<3> may be the signal s<95>. In one embodiment, the bin-to-thermo decoder 612 may be a part of the IDAC 508.

FIG. 7 illustrates ramp generator waveforms according to an exemplary embodiment of the present invention. As shown in FIG. 7(a), each of the ramp currents ramp_curr<3:0> may be offset by 128 VGA codes and each may span a code-range of 640 codes. Thus, each of the ramp currents may overlap with other ramp currents over certain ranges of the VGA codes. FIG. 7(b) illustrates 16 ramp voltages ramp<15:0> generated according to the ramp currents. As described above with respect to FIG. 4, the 16 ramp voltages may be applied to the switches MNS_0 through MNS_{15} in the resistor bank R1. FIG. 7(c) illustrates the overall VGA gain corresponding the VGA code according to one embodiment. As shown in FIG. 7(c), the overall VGA gain may be a monotonic function of the VGA code. In one embodiment, the minimum VGA gain in dB may be $Avga,min=20*\log_{10}(1+R2/R100)$. The maximum VGA gain may be $Avga,max=20*\log_{10}(1+R2/R1eq)$, where R1eq may be the equivalent parallel resistance of R10, R11, ..., R115 and R100 of R1 of FIG. 4. Between these minimum and maximum values, the VGA gain may increase monotonically and semi-continuous (e.g., still in steps but in much smaller steps). The magnitude of the gain ripple may depend on the value of the feedback resistors R_F of the TIA's. For example, in one embodiment, the resistor RF may set the slope of the ramp voltages ramp<0>, ramp<5>, ramp<10> and ramp<15> (for example, ramp<0> = RF*ramp_curr<0>). A steeper slope may reduce the overlap of adjacent voltage ramps. In other works, the switches MNS_0 through MNS_{15} may be turned on

"harder" when R_F has a small value, which may result in ripples. Overlap between ramps may help to provide a smooth gain-curve.

In one embodiment, any deviation from a linear curve may be mitigated by a gain calibration process of a gain control procedure, and by dividing the range of the VGA gain into M piece-wise linear segments. The number M may determine how small each linear segment may be. For example, M may take on a value of 20, 40 or 80. In one embodiment, the VGA gain range may be 10dB, and, if the M is 20, 40 or 80, the VGA gain may increase or decrease in a linear segment of ½, ¼ or 1/8 dB linear segments respectively. The VGA code corresponding to each start and end linear segment may be recoded in a VGA code table "vgaTable" during a calibration process. Thus, for any specific VGA gain, the corresponding VGA code may be looked up directly from the vgaTable to determine whether it falls on a start or end of a linear segment, or may be interpolated from a start or end of a linear segment covering the specific VGA gain. It should be noted that M can take on any value desirable. A large value may mean that the VGA gain has small linear segments, while a small value may mean that the VGA gain has large linear segments.

FIG. 8 (including FIG. 8(a) and FIG. 8(b)) illustrates gain variations of a signal processor according to an exemplary embodiment of the present invention. As describe above with respect to FIG. 2, the AGC controller 220 may map the control signals to PGA (LNA1 or LNA2) and VGA control codes (e.g., LNA code and VGA code). FIG. 8 shows how LNA and VGA gain may be controlled. When the input signal power is close to its peak, the PGA may have a zero dB gain; and when the input signal power is lower than a certain level, the PGA gain may be started in 3dB increments. However, as shown, a step change in PGA may occur when the VGA gain reaches one of the two preset threshold values, upper limit (UL) and lower limit (LL) thresholds. Thus, a change in the overall gain control may generally map to a change in the VGA gain control until a step change in PGA may occur.

In one embodiment, when the VGA gain goes above the UL, the PGA gain may be increased by 1 step and VGA gain control signal may be reduced such that VGA gain may drop to compensate for the increase in LNA gain. Alternatively, if the VGA gain goes below the LL, the PGA gain may be decreased by 1 step and VGA gain control signal may be increased such that VGA gain may increase to compensate for the gain drop in the PGA. In this manner, the overall gain change of the system may be continuous.

In one embodiment, the VGA gain may generally operate between the preset UL and LL limits. However, if the PGA gain saturates at maximum or minimum, the VGA gain control signal may be allowed to approach maximum or minimum gains, respectively.

In one embodiment, the AGC control code may be a L-bit word in 2's complement. The L-Bit word includes N whole bits and M fractional bits. The whole bits may map to settings for the LNAs. For example, each 8-level LNA may be controlled by 3 bits (e.g., 3-bit LNA code as shown in FIG. 3, in which corresponding to 7 steps)) and two 8-level LNAs may provide totally14 steps and need 4 whole bits. The values of the 4 bits may be mapped into two sets of 3-bit control signal and applied to LNA1 and LNA2. As shown in FIG. 8(a), each step in the discreet step amplifier PGA (LNA1 or LNA2) may be 3dB. If each of LNA1 and LNA2 has 7 steps, then together the PGA may provide a total gain of 42dB. That is, 4 whole bits may be used for a total gain of 42dB and a unit change in the AGC control code may map to a step change in the LNA gain.

The M fractional bits may correspond to a M-bit VGA code (e.g., 10-bit code as shown in FIG. 4) for a gain setting for the VGA. As shown in FIG. 8(b), the VGA may have a 10-dB gain range and with a 10-bit range the gain steps are effectively 0.01dB/LSB, thus effectively allowing for a continuous gain change by the front-end.

Figure 8(b) shows that VGA gain may vary between 0 and 3dB before a step in PGA occurs. However, in general, the VGA gain may vary in a range anywhere within the 10dB window depending on the settings of the UL and LL of the VGA thresholds. The UL and LL may be programmable parameters within the 10 dB range of the VGA. The VGA gain control setting may be kept between LL and UL as long as PGA gain is not saturated at max (42dB) or min (0dB) gain.

It may be difficult to assure that VGA and LNA gains occur exactly at the same time. As a result, fast switching of LNA gain may result in an impulse noise. Thus, the above gain change methodology may incorporate hysteresis into the system gain strategy to reduce the LNA gain switching transitions when a control signal is close to a switching threshold. Hysteresis may be included by the difference between the UL and LL thresholds, and by increasing UL and LL the hysteresis may exceed a LNA gain step. As such, hysteresis does not have to be an integral of a LNA gain step.

In one embodiment, the LNA2 gain may start to increase/decrease first as the input signal power decreases/increases. For example, when the input signal power is decreasing, the LNA2 gain may be the first LNA to decrease till it reaches its minimum. Then, LNA1 gain may start to reduce its gain until its gain drops to its minimum value.

As described above, due to non-idealities, the PGA (e.g., LNA1 and LNA2) gain steps may deviate from the nominal step values (e.g., 2.9dB or 3.1 dB instead of 3dB). Further, as shown in FIG. 7(c), the VGA gain vs. gain control signal variation (e.g., VGA code) may not be

linear and can also vary from part to part. Thus, in one or more embodiments, calibration may be performed. FIG. 9 illustrates a process 900 for a PGA gain calibration procedure according to an exemplary embodiment. The process 900 may start at block 902. At block 904, the PGA may be set to the lowest gain (e.g., 0 dB). At block 906, the received signal strength indicator RSSI(0) may be measured at the lowest gain setting. At block 908, the PGA gain setting may be adjusted to increase one step (e.g., LNA1 or LNA 2 increase one step of 3dB). At block 910, the RSSI(n) corresponding to the current step n may be measured. At block 912, the offset for the current step n may be recorded. For example, the offset with respect to the lowest gain may be calculated by an equation of $[10*\log_{10}(RSSI(n)/RSSI(0))-n*3]/3$. At block 914, the process 900 may determine whether it has reached the maximum PGA gain. If yes, the process 900 may proceed to block 916 and stop. If no, the process 900 may go back to block 908 to increase another step for the discreet step gain.

In one embodiment, the PGA gain calibration may use 15 registers (16 bit word each) to store the LNA gain offsets and compensations values for the LNA1 and LNA2 gains steps. These 15 registers may correspond to the storage of the LNA Gain Corrections 224 shown in FIG. 2.

The LNA switching point may occur when the VGA gain reaches UL or LL depending on the direction of signal strength variation. At each transition point (e.g., increase or decrease a LNA step), a new offset word may be recalled from storage and applied to the VGA at the same time as the LNA1 or LNA2 gain changes so a smooth transition may be provided during LNA gain switch. FIG. 10 illustrates a process 1000 for mapping the LNA offsets to VGA control offsets according to an exemplary embodiment of the present invention. The process 1000 may start at block 1002. At block 1004, the VGA code may be set as zero and the initial signal strength RSSI(0) at step 0 may be measured and recorded. At block 1006, the VGA code may be incremented by a predetermined amount, for example, the amount may be determined based on how much accuracy is desired in calibration, and in what region of the VGA gain curve the increase lies. At block 1008, the signal strength RSSI(n) at the current step n may be measured. At block 1010, the value of the increased gain may be determined by the equation of $gainInc = 10*\log_{10}(RSSI(n)/RSSI(0))-n*vgaGaininc$, in which the vgaGaininc may be the resolution for the linearization process (e.g., the linearization process may occur in 1/4, 1/2, or 1dB increments). At block 1012, the process 1000 may determine whether the gainInc is greater than zero. If no, the process 1000 may return to the block 1006 to increment VGA code by the predetermined amount and repeat the blocks 1008, 1010 and 1012 again. If yes, the process 1000 may determine whether the gainInc is greater than zero. If no, the process 1000 may proceed to the block 1014 to increment the step from n to

n+1 and record the VGA code. Then at the block 1016, the process 1000 may determine whether the step number n is still less than a maximum number N. If yes, the process 1000 may proceed to block 1018 and stop. If no, the process 1000 may proceed to block 1006 and the repeat the blocks thereafter.

Accordingly, at each step of the LNA1 and LNA2 gain change, the correct VGA gain control signal offset may be determined. The correct VGA control signal may correspond to the VGA gain that accurately compensates the corresponding discrete gain step so the overall gain may stay constant.

FIG. 11 illustrate a process 1100 for generating gain distributions among the PGA and VGA according to an exemplary embodiment of the present invention. The process 1100 may allow corrections for the LNA gain variation using a one-to-one mapping between the control signal and the AGC gain setting. The process 1100 may start at block 1102 and proceed to block 1104. At block 1104, the control signal "cntlSig" may be limited based on the overall gain and nominal step value. For example, if the PGA (e.g., LNA1 and LNA2) has a total gain of 42dB, the VGA has a gain range of 10dB and the step has a nominal value of 3dB, the control signal may be limited to between 0 and 52/3. At block 1106, the process 1100 may determine whether this is an initialization process. If yes, the process 1100 may proceed to block 1108, at which the step gain "lnaGains" and an offset "lnaOffset" associated with the step gain may be determined. For example, the initial lnaGains may be determined by the control signal subtracting the initial VGA control signal. In one embodiment, the lnaGains may be limited to an integer number between 0 and 14, the LNA1 code may be set as the lesser value between 7 and lnaGains (e.g., MIN(7, lnaGains)), the LNA2 code may be set as larger value between 0 and lnaGains-7 (e.g., MAX(0, lnaGains-7)). The lnaOffset may be looked up from the storage that stores the result of a PGA calibration.

In one embodiment, the control signal may take priority and the initial VGA control signal may be over-written. The VGA control signal may determine the overall gain setting, and its value may determine the PGA and VGA gains based upon the UL and LL thresholds. Therefore, even if an VGA INIT gain is requested, it may be overwritten by the process that determines the PGA and VGA gain settings.

If the check returns no at block 1106, and also from block 1108, the process 1100 may proceed to block 1110. At block 1110, the VGA control signal "vgaCntl" may be determined. In one embodiment, the vgaCntl may be determined by the equation of vgaCntl = cntlSig – lnaOffset – lnaGains, and may be limited in a range of 0 to 10/3. At block 1112, vgaCntl may be compared to the upper threshold UL. If vgaCntl>UL, the process 1100 may proceed to

block 1114, at which lnaGains may be incremented by 1; if not, the process 1100 may proceed from the block 1112 to block 1116 to compare the vgaCntl to the lower threshold LL. If vgaCntl<UL, the process 1100 may proceed to block 1118, at which lnaGains may be decremented by 1. From blocks 1114 and 1118, and if comparison at the block 1116 is false, the process 1100 may proceed to block 1120.

At block 1120, the vgaCntl may be adjusted if necessary. In general, the VGA control may be limited to between 0 and 10/3 and to be adjusted to account for the step gain in LNAs. In one embodiment, the VGA control may not be adjusted when the LNA gains are max or min. That is, when even if vgaCntl exceeds UL or drops below LL, the LNA gain would not change. If lnaGains is changed (e.g., incremented or decremented), the lnaOffset and LNA codes may need to be updated. In one embodiment, as describe above, at a calibration process, the gain differential between the cumulative gains of the LNAs relative to their nominal values may be measured, and may be converted to VGA control signal offset. These values may be stored in a lookup table for the different LNA combinations. The location adhering to 0dB of LNA gain may be zero. In normal operation mode, the VGA control signal may be modified by the stored offsets for the selected LNA gain resulting in a continuous operation of the AGC at the presence of a PGA gain change. At block 1122, the process 1100 may map the vgaCntl to an VGA control code. A block 1124, the process 1100 may stop.

The VGA gain/control signal variation vs. VGA control code can have any shape as long as it is monotonic as shown in FIG. 7(c). As described with respect to FIG. 7(c), this may allow for a construction of a piece-wise linear model of the VGA gain versus the VGA control code (e.g., 10-bit word). FIG. 12 illustrates a process 1200 for determining the VGA codes as a function of VGA control signal according to an exemplary embodiment of the present invention. The process 1200 may start at block 1202. At block 1204, the process 1200 may determine the determine VGA gain "vgaGain". The VGA gain may be determined based on the VGA control signal vgaCntl (e.g., according to the process 1100). In one embodiment, the vgaGain may be determined by multiplying the vgaCntl by the nominal value of the step gain of PGA. For example, for a 10 dB span of the VGA gain, the VGA control signal values may be between 0 and 10/3 corresponding to the minimum and the maximum VGA gain control signal values, respectively. Thus, the vgaGain may be obtained by vgaCntl times three.

At block 1206, the process 1200 may determine start and end VGA code addresses for a linear segment covering the VGA gain. As described above with respect to FIG. 7, the VGA gain may be implemented in a piece-wise linear model. The piece-wise linear model of the VGA gain may be developed by incrementing the gain at measuring the VGA code at predetermined VGA increments. For instance, for a ½ dB gain increments, a 21 entry look up

table for the 10 dB VGA range may be needed. Thus, based on vgaGain, a segment covering the vgaGain may be determined and the start and end VGA codes of a corresponding segment may be obtained. In one embodiment, the start code address may be determined by vgaCodeAdd = vgaGain * gain2Add and the end code address may be determined by nextCodeAdd = vgaCodeAdd + 1. The gain2Add may be reciprocal of the gain increment setting. In one embodiment, the table may be in either one of 1/8, ¼, ½, or 1 dB increments. Hence, the piecewise address of VGA gain table may be determined from product of the VGA gain and the gain2Add. For example, if the VGA gain is 4.3dB, the VGA code for the VGA gain may be a value between the 9^{th} and 10^{th} address in ½ db increments (assuming the first address is for 0dB).

At block 1208, the start and end VGA codes of the corresponding segment covering the vgaGain may be looked up from a lookup table vgaTable. For example, startCode = vgaTable[vgaCodeAdd] and endCode = vgaTable[nextCodeAdd]. Next, at block 1210, the vgaCode corresponding to the gain value may be linearly interpolated by utilizing the piece-wise linear model of the VGA gain. For example, the fraction of the VGA gain within the segment may be determined by fracVgaGain = vgaGain - vgaCodeAdd*gainInc. gainInc may represent the steps of the piece-wise linear model (e.g., ½, ¼, or 1/8 of a dB when M may be 20, 40 and 80 for a span of 10dB). The VGA code may be interpolated by vgaCode = startCode +(endCode -startCode) * fracVgaGain. In one embodiment, the piece-wise linear model of the VGA may allow for an accurate correction of LNA step change.

Several embodiments of the present invention are specifically illustrated and described herein. However, it will be appreciated that modifications and variations of the present invention are covered by the above teachings and within the purview of the appended claims without departing from the spirit and intended scope of the invention.

It should be understood that there exist implementations of other variations and modifications of the invention and its various aspects, as may be readily apparent to those of ordinary skill in the art, and that the invention is not limited by specific embodiments described herein. Features and embodiments described above may be combined. It is therefore contemplated to cover any and all modifications, variations, combinations or equivalents that fall within the scope of the basic underlying principals disclosed and claimed herein.

WE CLAIM

1. A signal processing circuit, comprising:

a discreet step gain amplifier stage;

a variable gain amplifier (VGA);

an analog-to-digital converter (ADC); and

an automatic gain control (AGC) unit to compare an output of the ADC to a power threshold and adjust a control signal, the control signal controlling an overall front end gain provided by a combination of gains of the discreet step gain amplifier stage and VGA stage.

2. The signal processing circuit of claim 1, wherein the AGC unit comprises an AGC controller to map the control signal to an AGC control code, the AGC control code includes bits for controlling the discreet step gain amplifier stage and a VGA control code for controlling the VGA.

3. The signal processing circuit of claim 2, wherein the discreet step gain amplifier stage comprises a plurality of low noise amplifiers (LNAs).

4. The signal processing circuit of claim 3, wherein the AGC controller maps the bits for controlling the discreet step gain amplifier stage to LNA codes for each LNA.

5. The signal processing circuit of claim 3, wherein the AGC unit further comprises lookup tables storing VGA codes for a plurality of measured VGA gains, gain step offsets for each step of the LNAs, and VGA thresholds.

6. The signal processing circuit of claim 5, wherein the VGA thresholds include a lower limit (LL) threshold and an upper limit (UL) threshold.

7. The signal processing circuit of claim 6, wherein a change in the LNAs occurs when the VGA reaches one of the thresholds.

8. The signal processing circuit of claim 7, wherein all changes in the LNAs occur in one respective LNA before the respective LNA reaches its limit.

9. The signal processing circuit of claim 1, wherein the overall front end gain is determined based on the root mean square (RMS) power of the ADC output.

10. The signal processing circuit of claim 1, the AGC unit includes one or more filters that performs post processing on control decisions to smooth out decision outputs and to control an adaptation rate.

11. A method to control a front end gain of a signal processor, comprising:

comparing an output of the signal processor to a power threshold; and

adjusting a control signal based on the comparison, wherein the control signal is mapped to an automatic gain control (AGC) control code, the AGC control code includes a control code for a discreet step gain amplifier stage and a variable gain amplifier (VGA) control code for a variable gain, the bits of control code for the discreet step gain amplifier stage determines step gains and the VGA control code determines a VGA gain, the VGA gain provides a continuous part of the front end gain between the steps.

12. The method of claim 11, wherein each gain step deviates from a nominal value by an offset and all offsets are recorded during a calibration process.

13. The method of claim 12, further comprising looking up an offset for a gain step and compensating for the offset.

14. The method of claim 11, wherein the VGA gain is a monotonic curve with respect to the VGA control code.

15. The method of claim 11, wherein a discreet step gain amplifier stage comprises a plurality of noise amplifiers (LNAs) and the control code for the discreet step gain amplifier stage are mapped to control codes for each of the LNAs respectively.

16. The method of claim 15, wherein the discreet step gain amplifier stage changes the steps by one when the VGA gain change reaches an upper or lower threshold, and the VGA gain is changed to compensate the step change to ensure a smooth gain change.

17. The method of claim 16, wherein all step changes in the LNAs occur in one respective LNA before the respective LNA reaches its limit.

18. The method of claim 11, wherein the overall front end gain is determined based on the root mean square (RMS) power of the output of the signal processor.

19. The method of claim 11, further comprising filtering a control decision to smooth out a decision output and to control an adaptation rate.

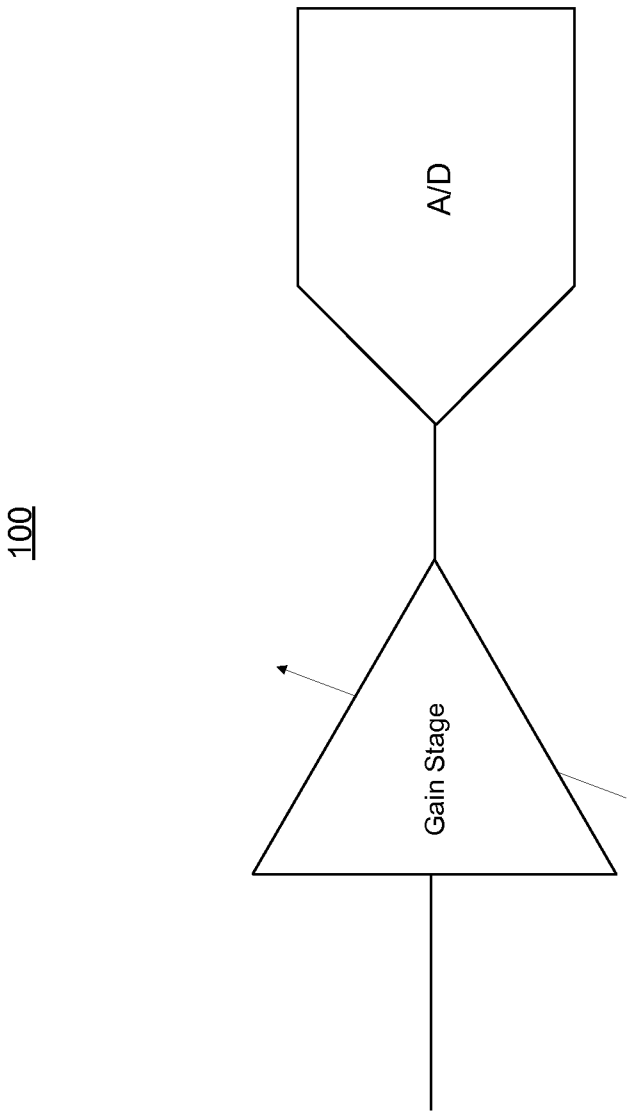


FIG. 1 (PRIOR ART)

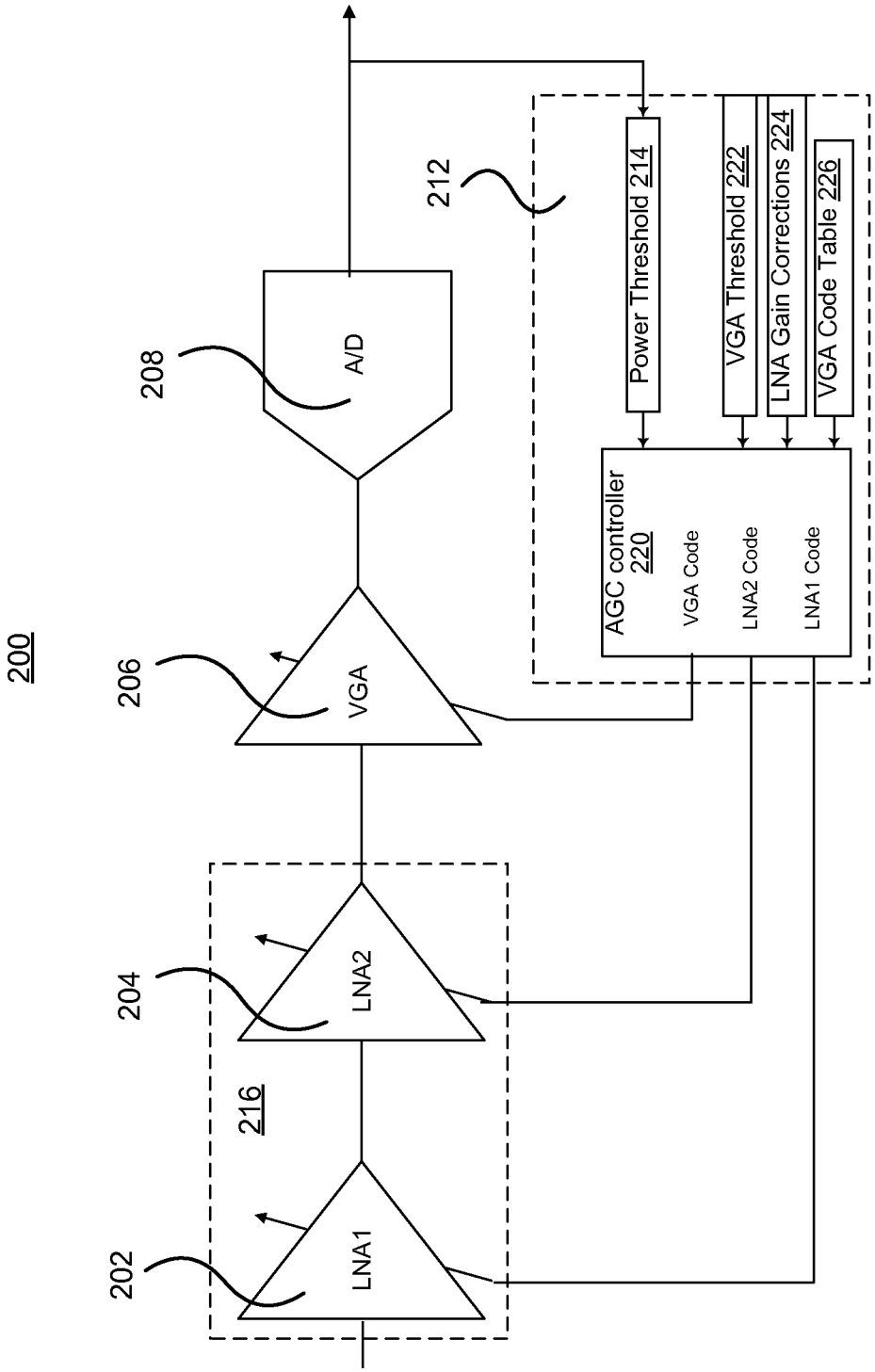

200
202
LNA1
204
LNA2
216
206
VGA
208
A/D
212
AGC controller
220
VGA Code
LNA2 Code
LNA1 Code
Power Threshold 214
VGA Threshold 222
LNA Gain Corrections 224
VGA Code Table 226

FIG. 2

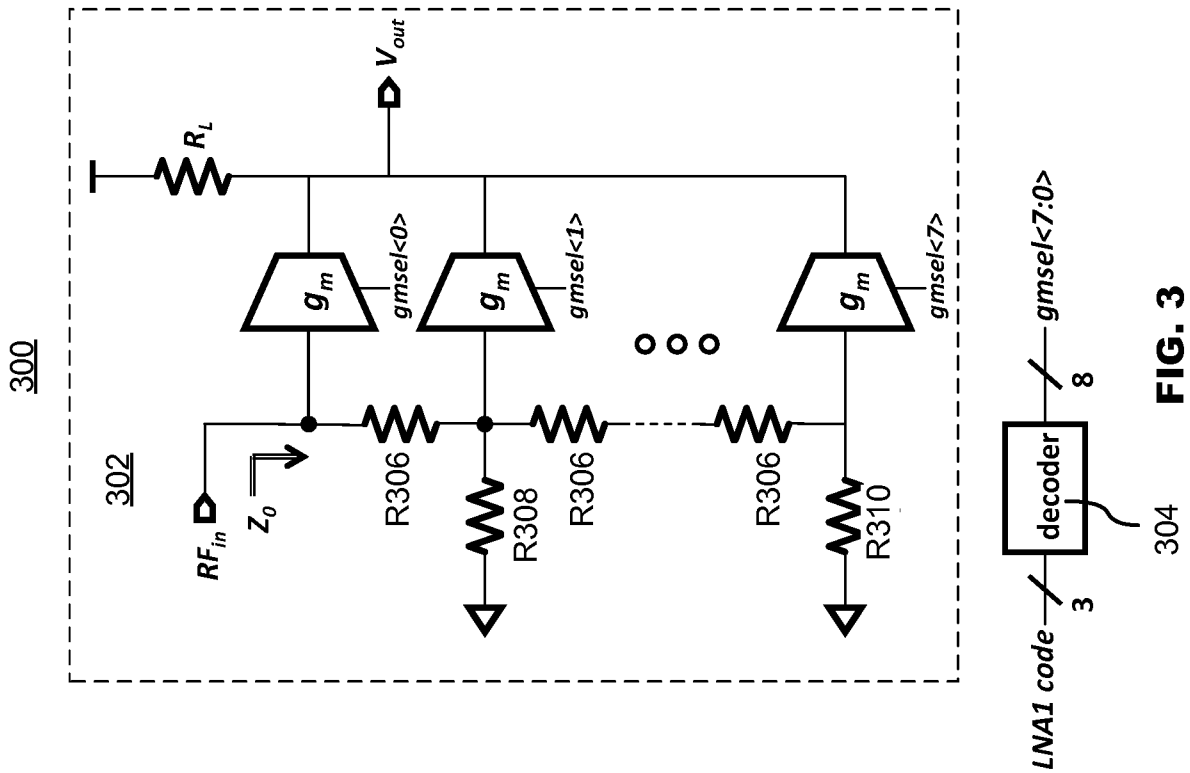

300
302
V_{out}
R_L
g_m
gmsel<0>
gmsel<1>
gmsel<7>
RF_{in}
Z_0
R306
R308
R306
R306
R310
decoder
gmsel<7:0>
8
304
LNA1 code
3

FIG. 3

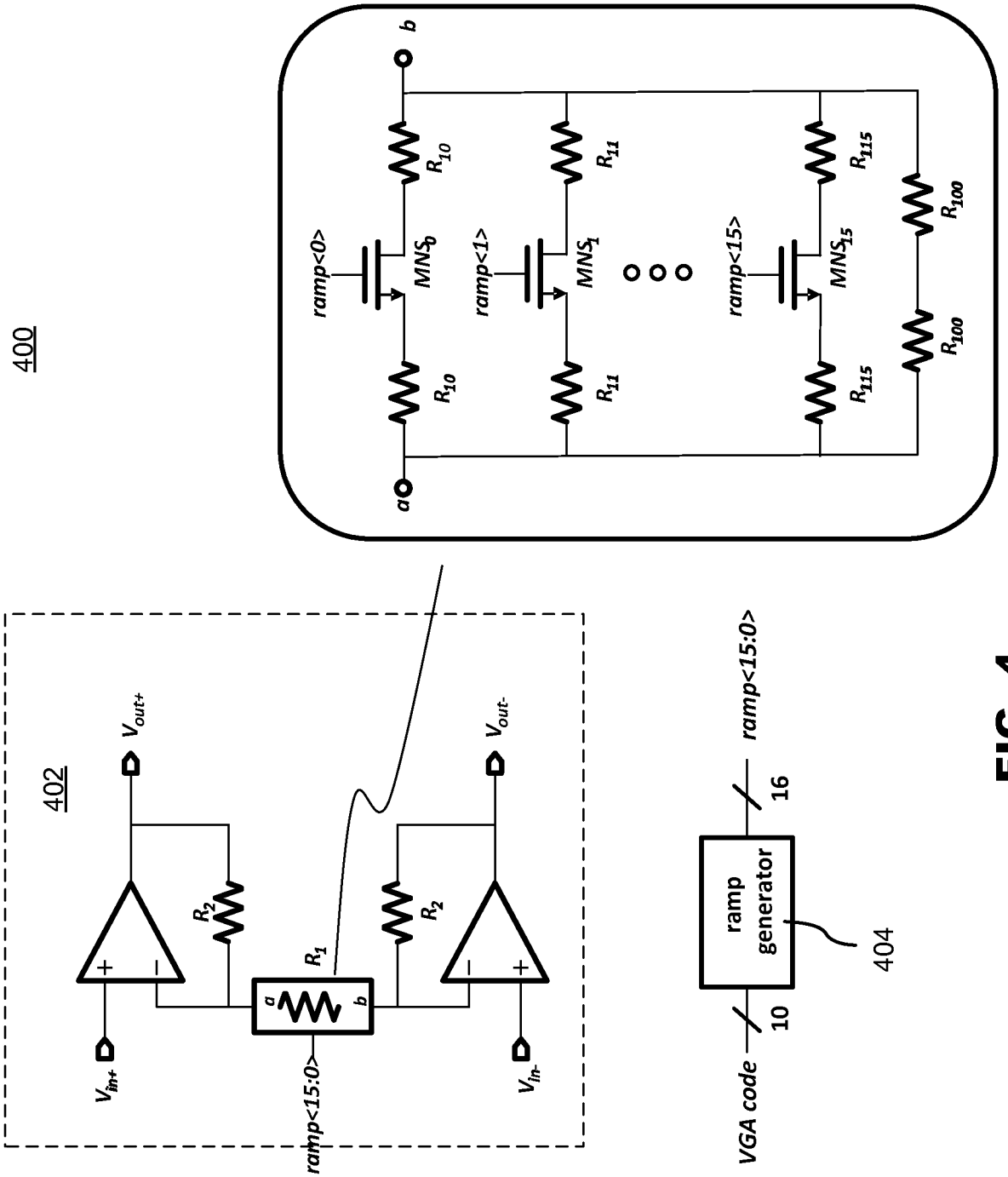

400
402
404
V_{out+}
V_{out-}
V_{in+}
V_{in-}
R_1
R_2
R_2
a
b
ramp<15:0>
ramp generator
16
10
ramp<15:0>
VGA code
ramp<0>
ramp<1>
ramp<15>
MNS_0
MNS_1
MNS_{15}
R_{10}
R_{11}
R_{115}
R_{100}

FIG. 4

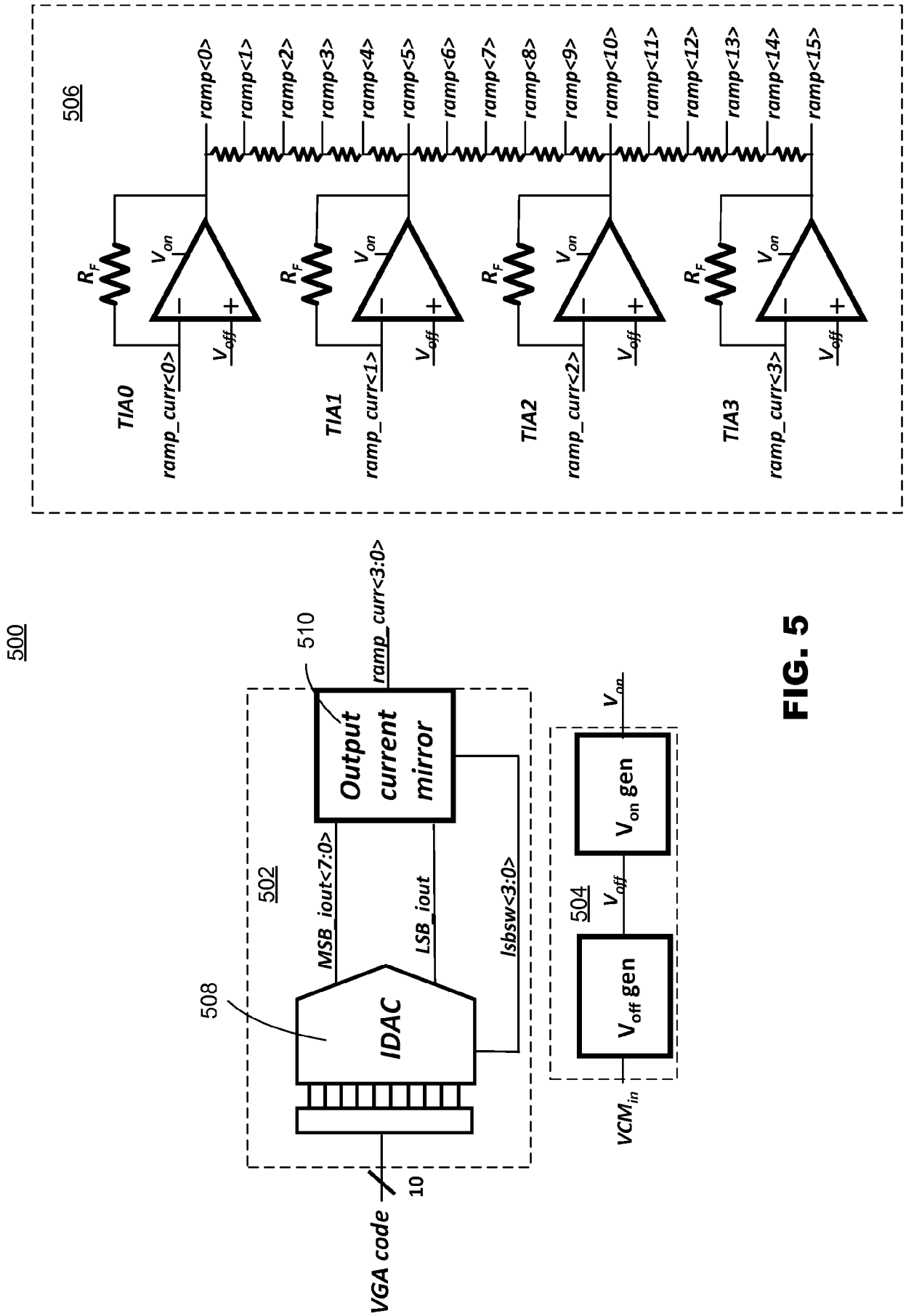

500
510
Output current mirror
ramp_curr<3:0>
502
MSB_iout<7:0>
LSB_iout
lsbsw<3:0>
508
IDAC
VGA code
10
504
V_{on} gen
V_{off} gen
V_{on}
V_{off}
VCM_{in}
506
ramp<0>
ramp<1>
ramp<2>
ramp<3>
ramp<4>
ramp<5>
ramp<6>
ramp<7>
ramp<8>
ramp<9>
ramp<10>
ramp<11>
ramp<12>
ramp<13>
ramp<14>
ramp<15>
R_F
V_{on}
V_{off}
TIA0
TIA1
TIA2
TIA3
ramp_curr<0>
ramp_curr<1>
ramp_curr<2>
ramp_curr<3>

FIG. 5

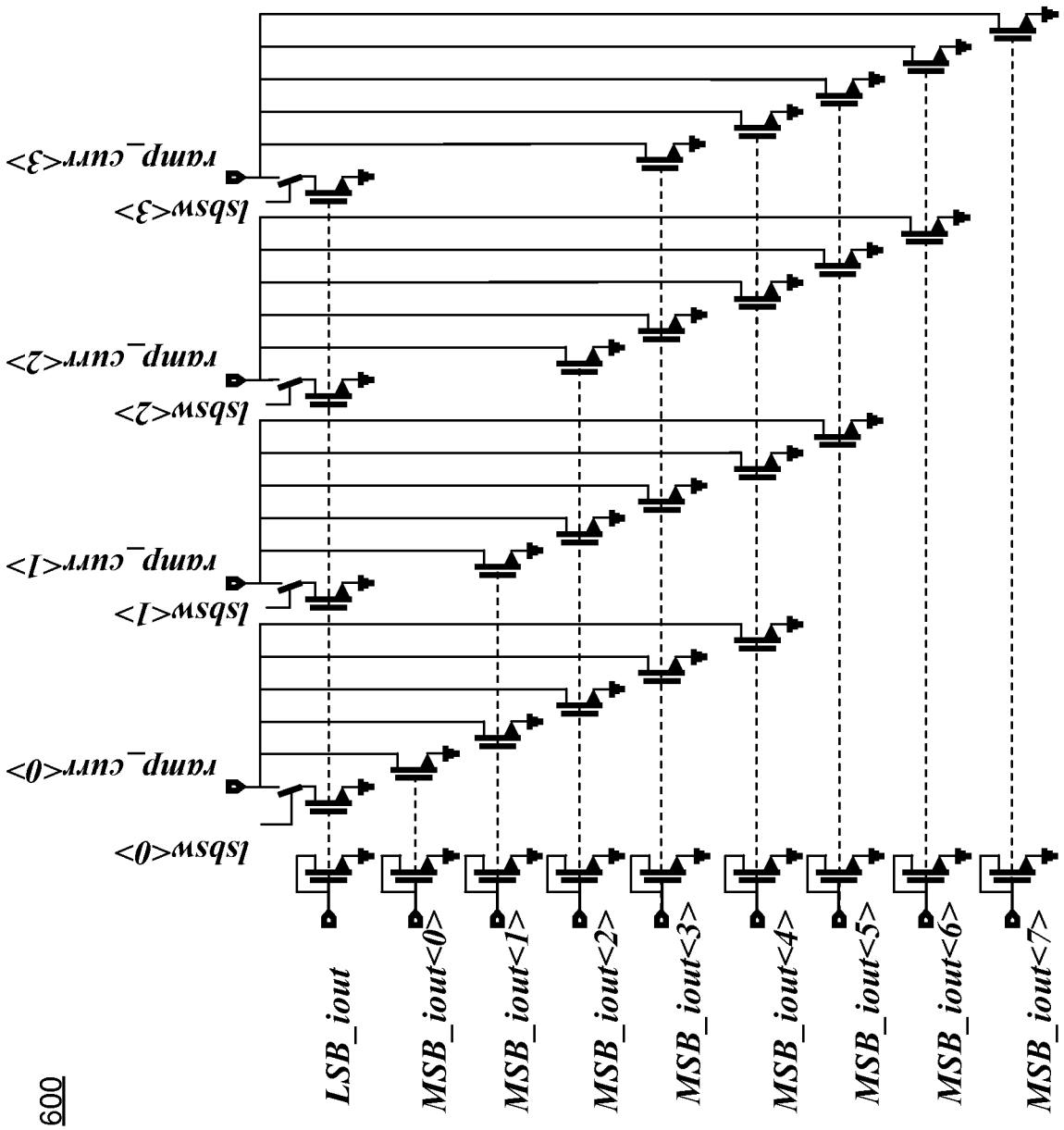

600
LSB_iout
MSB_iout<0>
MSB_iout<1>
MSB_iout<2>
MSB_iout<3>
MSB_iout<4>
MSB_iout<5>
MSB_iout<6>
MSB_iout<7>
lsbsw<0>
ramp_curr<0>
lsbsw<1>
ramp_curr<1>
lsbsw<2>
ramp_curr<2>
lsbsw<3>
ramp_curr<3>

FIG. 6A

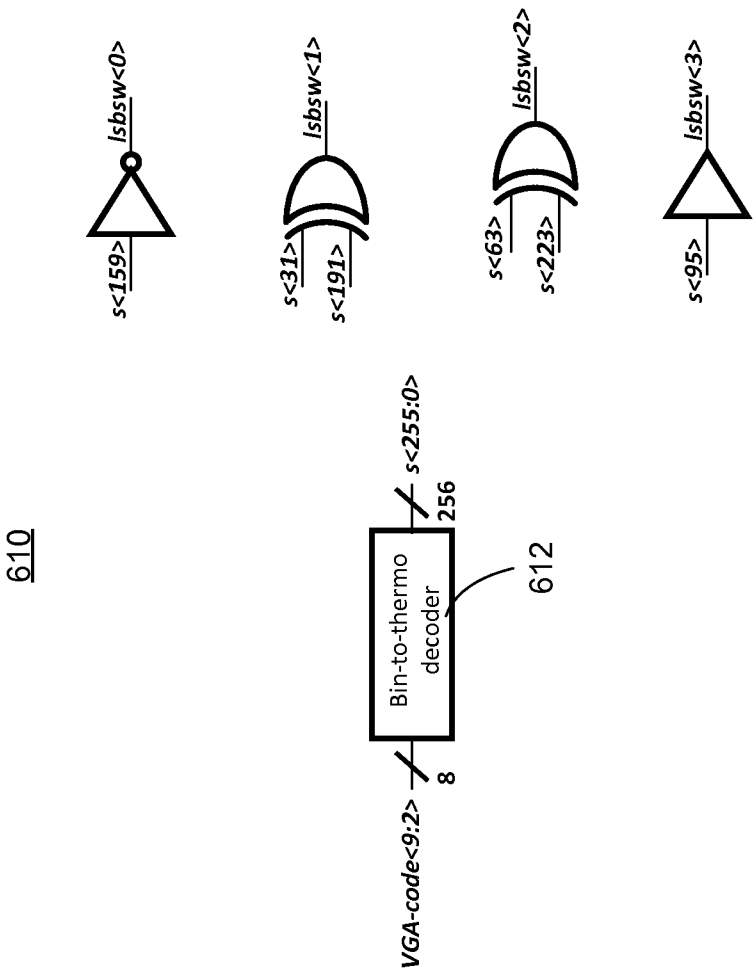

610
lsbsw<0>
s<159>
lsbsw<1>
s<31>
s<191>
lsbsw<2>
s<63>
s<223>
lsbsw<3>
s<95>
s<255:0>
256
Bin-to-thermo decoder
612
8
VGA-code<9:2>

FIG. 6B

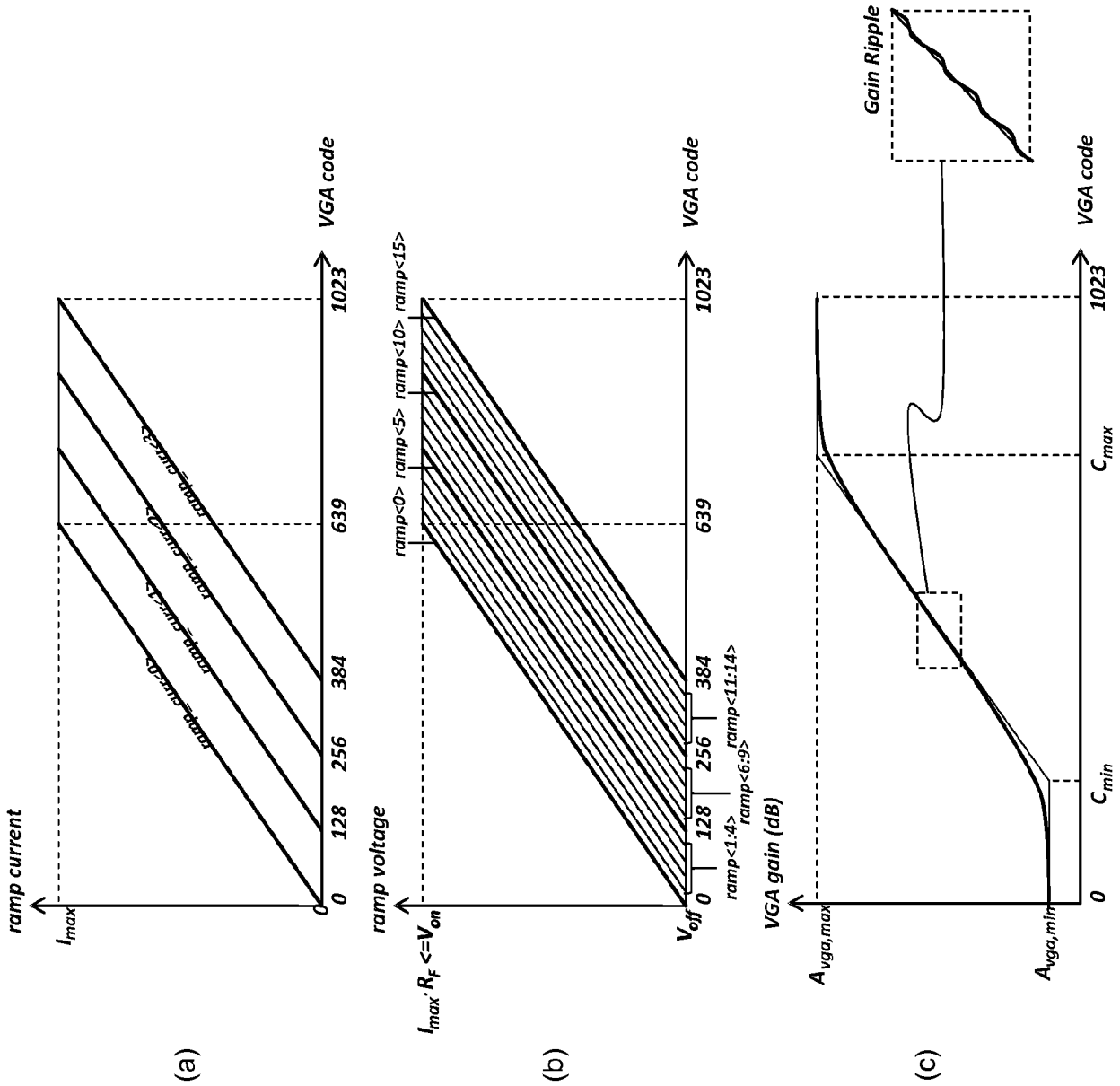

ramp current
I_{max}
0
128
256
384
639
1023
VGA code
ramp<0>
ramp<5>
ramp<10>
ramp<15>
(a)
ramp voltage
$I_{max} \cdot R_F <= V_{on}$
V_{off}
ramp<1:4>
ramp<6:9>
ramp<11:14>
(b)
VGA gain (dB)
$A_{vga,max}$
$A_{vga,min}$
C_{min}
C_{max}
Gain Ripple
(c)

FIG. 7

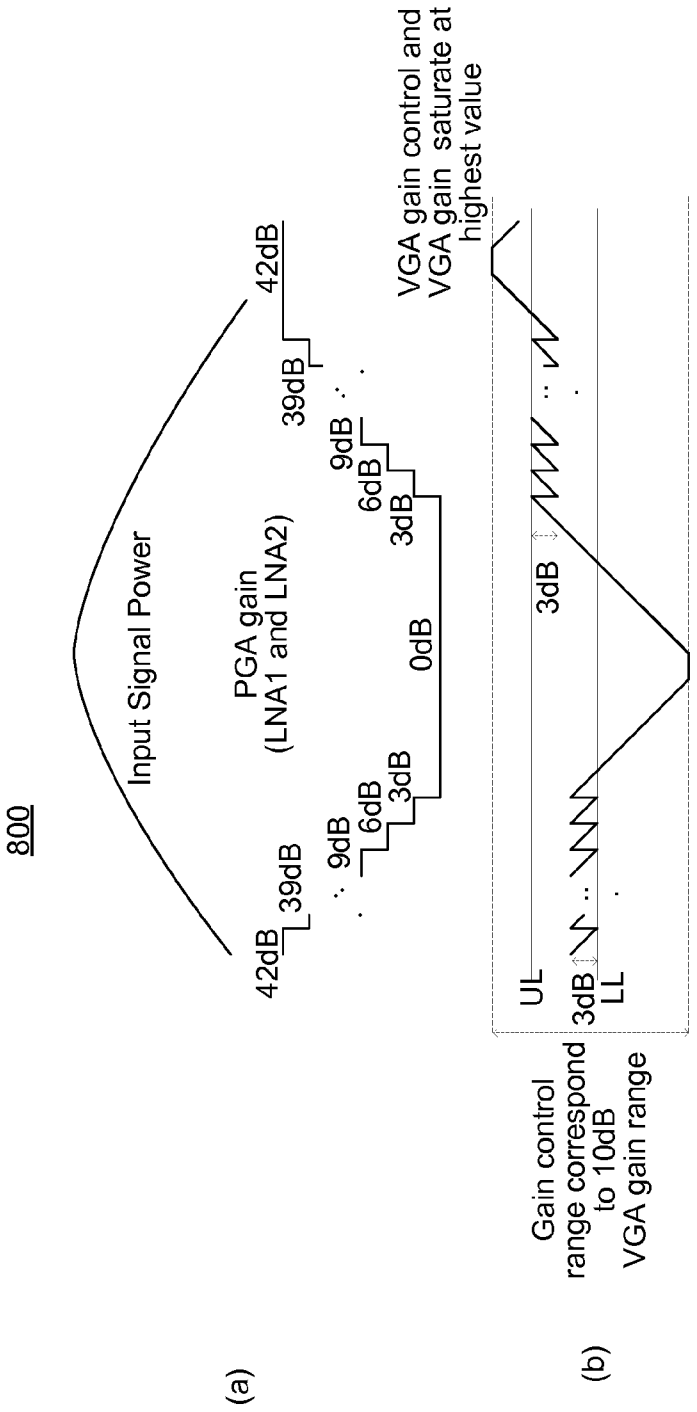

800
(a)
Input Signal Power
PGA gain
(LNA1 and LNA2)
42dB
39dB
9dB
6dB
3dB
0dB
VGA gain control and
VGA gain saturate at
highest value
(b)
UL
LL
3dB
3dB
Gain control
range correspond
to 10dB
VGA gain range
VGA gain control
and VGA gain
saturate at lowest
value

FIG. 8

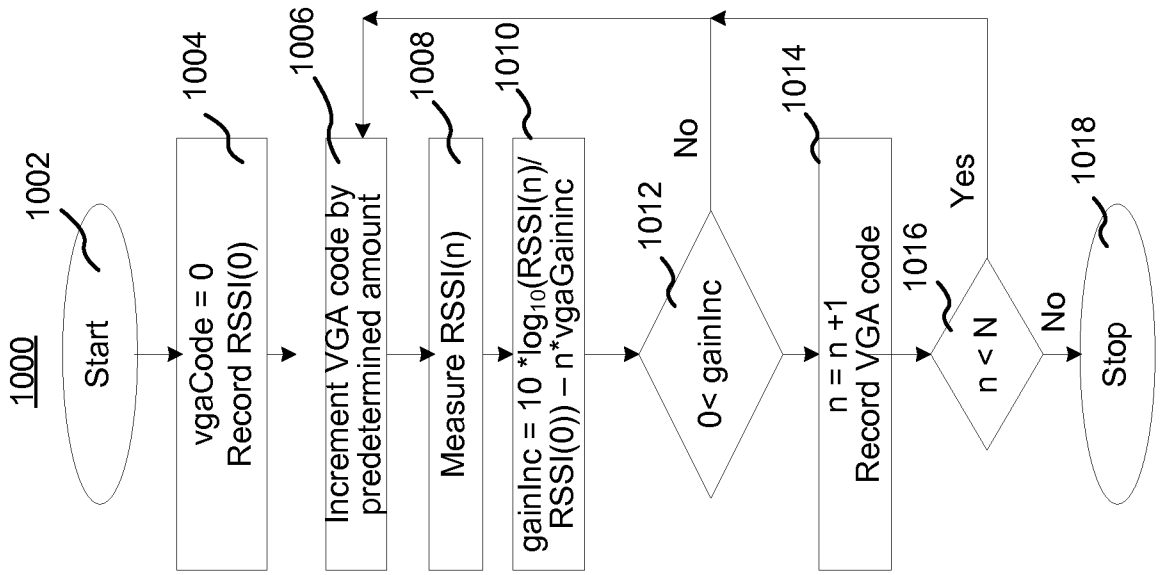

1000
Start
1002
vgaCode = 0
Record RSSI(0)
1004
Increment VGA code by predetermined amount
1006
Measure RSSI(n)
1008
gainInc = 10 *log10(RSSI(n)/ RSSI(0)) – n*vgaGaininc
1010
0< gainInc
1012
No
n = n +1
Record VGA code
1014
n < N
1016
Yes
No
Stop
1018

FIG. 10

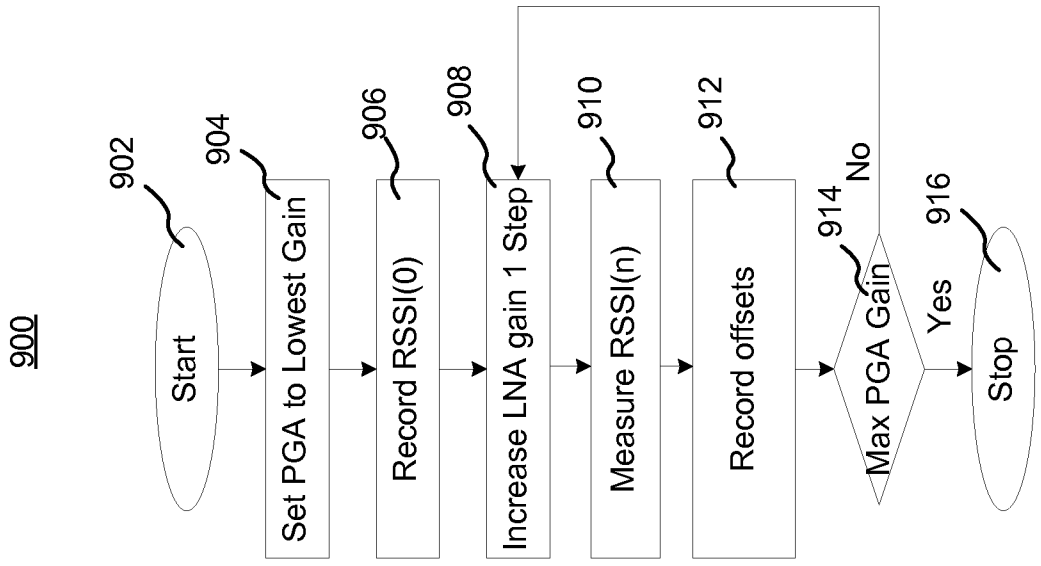

900
Start
902
Set PGA to Lowest Gain
904
Record RSSI(0)
906
Increase LNA gain 1 Step
908
Measure RSSI(n)
910
Record offsets
912
Max PGA Gain
914
No
Yes
916
Stop

FIG. 9

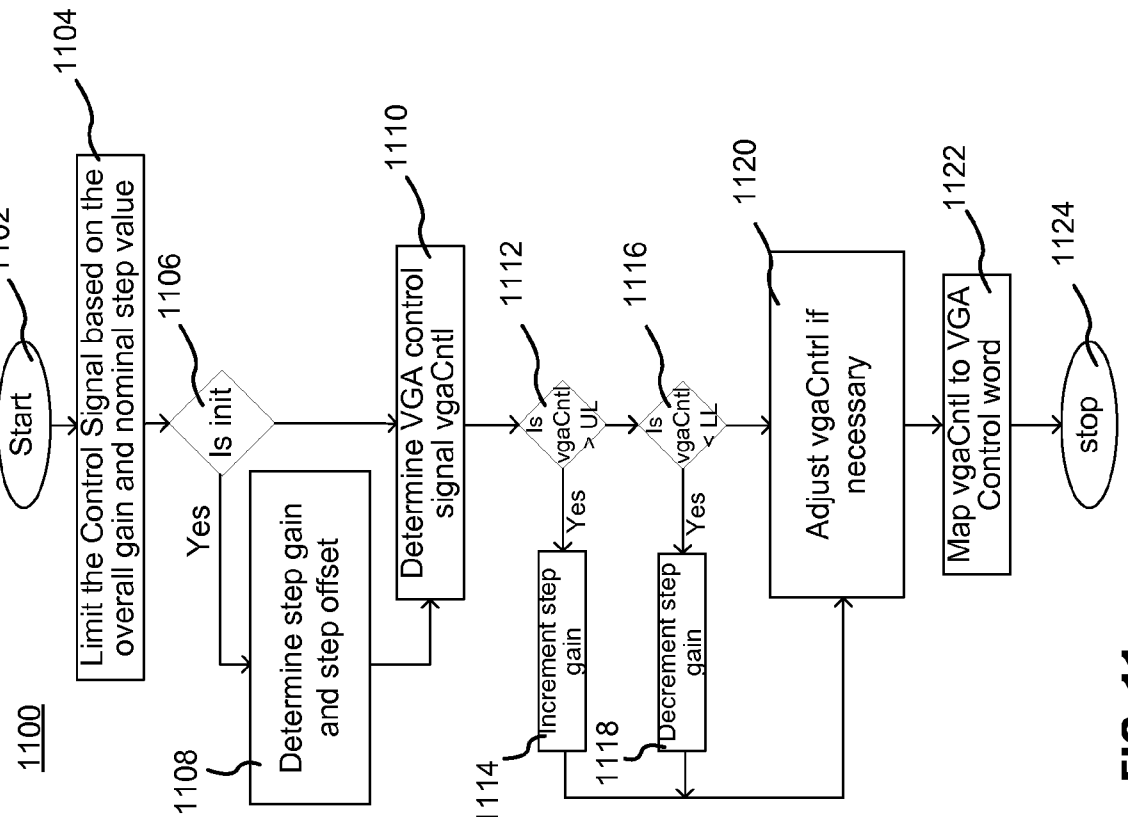

1100
1102
Start
1104
Limit the Control Signal based on the overall gain and nominal step value
1106
Is init
Yes
1108
Determine step gain and step offset
1110
Determine VGA control signal vgaCntl
1112
Is vgaCntl > UL
Yes
1114
Increment step gain
1116
Is vgaCntl < LL
Yes
1118
Decrement step gain
1120
Adjust vgaCntrl if necessary
1122
Map vgaCntl to VGA Control word
1124
stop

FIG. 11

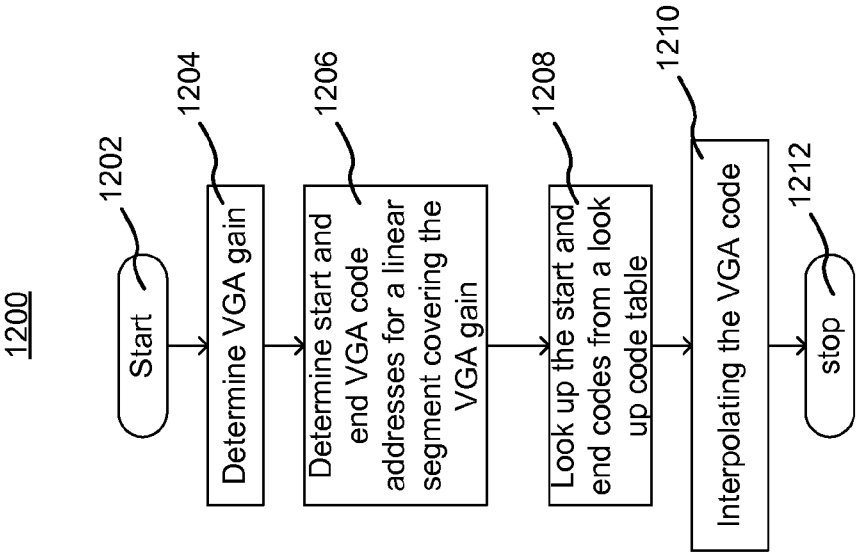

1200
1202
Start
1204
Determine VGA gain
1206
Determine start and end VGA code addresses for a linear segment covering the VGA gain
1208
Look up the start and end codes from a look up code table
1210
Interpolating the VGA code
1212
stop

FIG. 12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US12/35148

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H04L 27/08 (2012.01)
USPC - 375/345; 455/240.1, 241.1
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) Classification(s): IPC(8): H04B 1/06; H03M 1/12; H04L 27/08 (2012.01)
USPC Classification(s): 341/139; 375/345; 455/232.1, 234.1, 240.1, 241.1, 245.1, 251.1

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
MicroPatent (US Granted, US Applications, EP-A, EP-B, WO, JP, DE-G, DE-A, DE-T, DE-U, GB-A, FR-A); IEEE, DialogPro, Google; Search Terms Used: variable gain amplifier, low noise amplifier, feedback, gain control, closed loop, look up, table, agc, lna, adc, analog to digital converter, gain

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y	US 7,187,915 B2 (WANG, C. et al.) March 6, 2007, figure 5 and column 4, lines 19-41	1, 2, 11 and 12 ---------- 3-10 and 13-19
Y	US 7,676,206 B2 (RAGAN, L. et al.) March 9, 2010, figure 3 and column 4, lines 14-27	3-8 and 15-17
Y	US 2004/0259511 A1 (LIU, D. et al.) December 23, 2004, paragraph [0024]-[0027]	5-8 and 13
Y	US 2008/0114252 A1 (RANDALL, K., et al.) May 15, 2008, paragraph [0283]	9 and 18
Y	US 2006/0222118 A1 (MURTHY, V., et al.) October 5, 2006, figure 4 and paragraph [0058]	10 and 19
Y	US 5,838,194 A (KHOURY, J.) November 17, 1998, figure 8 and column 9, lines 33-67	14

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 July 2012	06 AUG 2012
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Shane Thomas PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)