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(71) Applicant(s):  
**INCA DIGITAL PRINTERS LIMITED**  
(Incorporated in the United Kingdom)  
511 Coldhams Land, CAMBRIDGE, CB1 3JS,  
United Kingdom

(72) Inventor(s):  
**Hamilton Buchanan Cleare**

(74) Agent and/or Address for Service:  
**Mathys & Squire LLP**  
120 Holborn, LONDON, EC1N 2SQ, United Kingdom

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(54) Title of the Invention: **Inkjet printhead driver circuit and method**  
Abstract Title: **Drive circuit for repetitively energising a print head**

(57) A drive circuit is disclosed for repetitively energising a print head 10 to eject drops of ink. The print head 10 has multiple nozzle channels each having a respective capacitance  $C_{n1}$ ,  $C_{n2}$  etc, with the print head having its own inherent capacitance  $C_{n0}$ . A print head drive terminal 30 connects the nozzle channels to a first power supply connection 40 from the pulse generation circuit 20, while the nozzle channels are connected by a return path 50 to a second power supply connection 60. Each nozzle is connected in series with a respective switching element  $S_{n1}$ ,  $S_{n2}$  etc. controlled by a print data source 70 and a timing data source 80. The drive circuit comprises a control arrangement 90 to drive wave forms for switching elements  $S_1$ ,  $S_2$  etc in the pulse generation circuit 20. The timing is processed by a timer generator 100. The timing is processed by a timer generator 100.

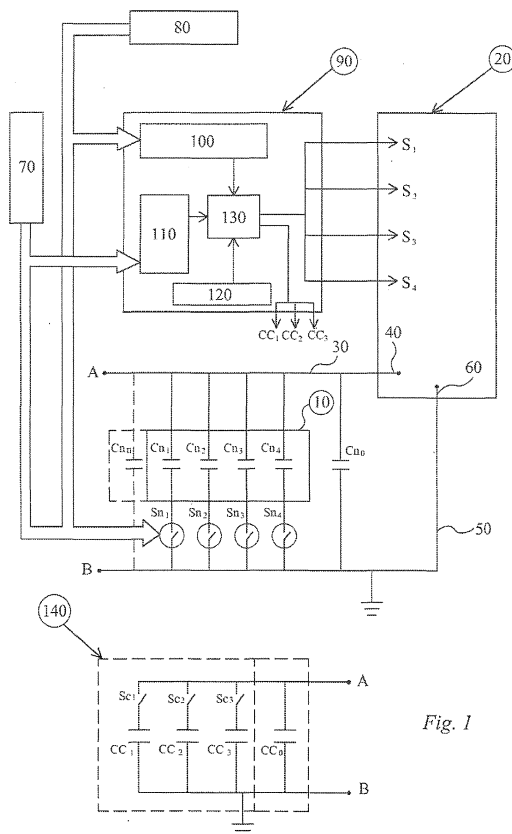
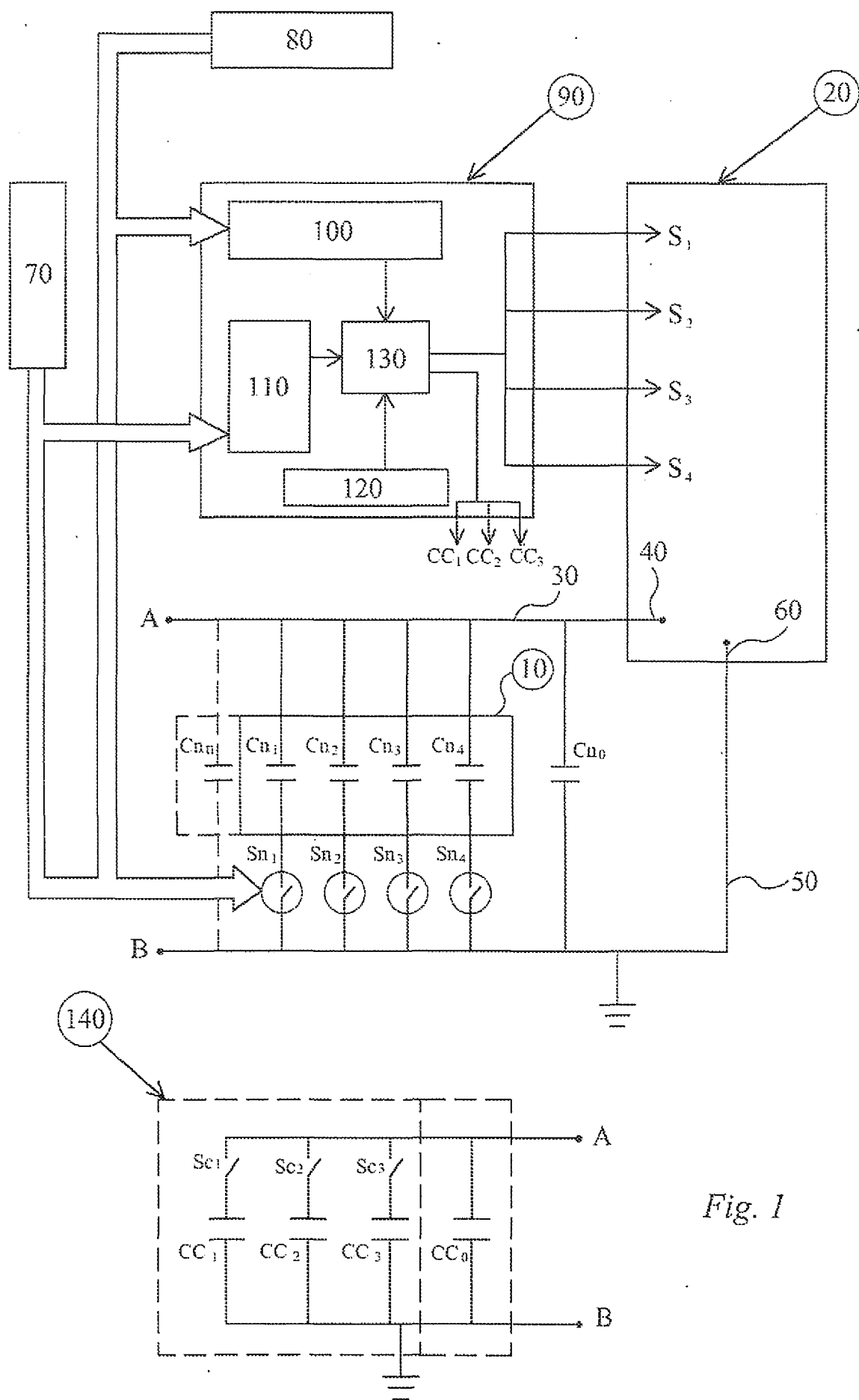


Fig. 1



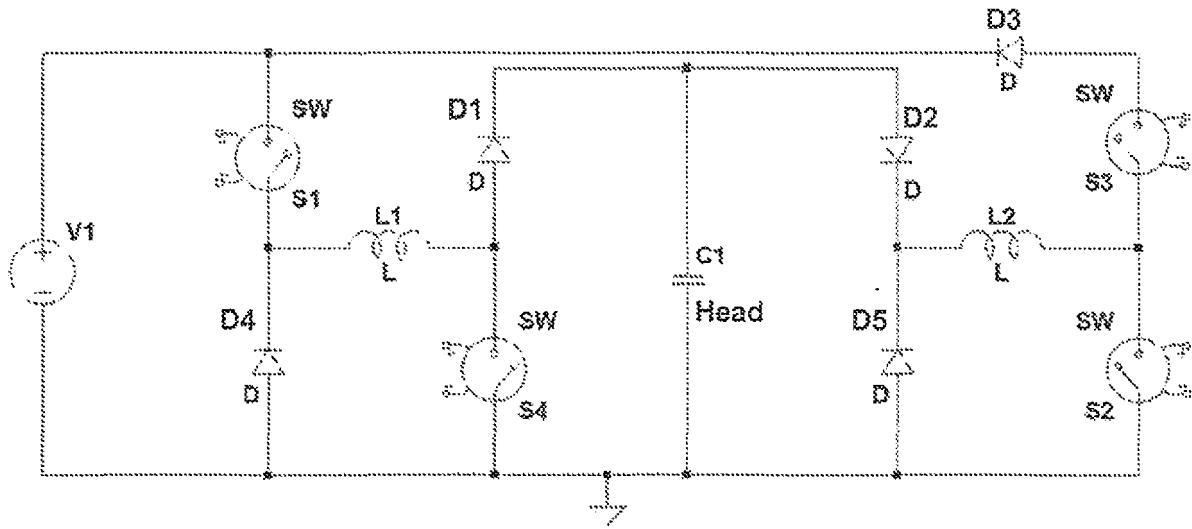


Fig. 2

04 01 13

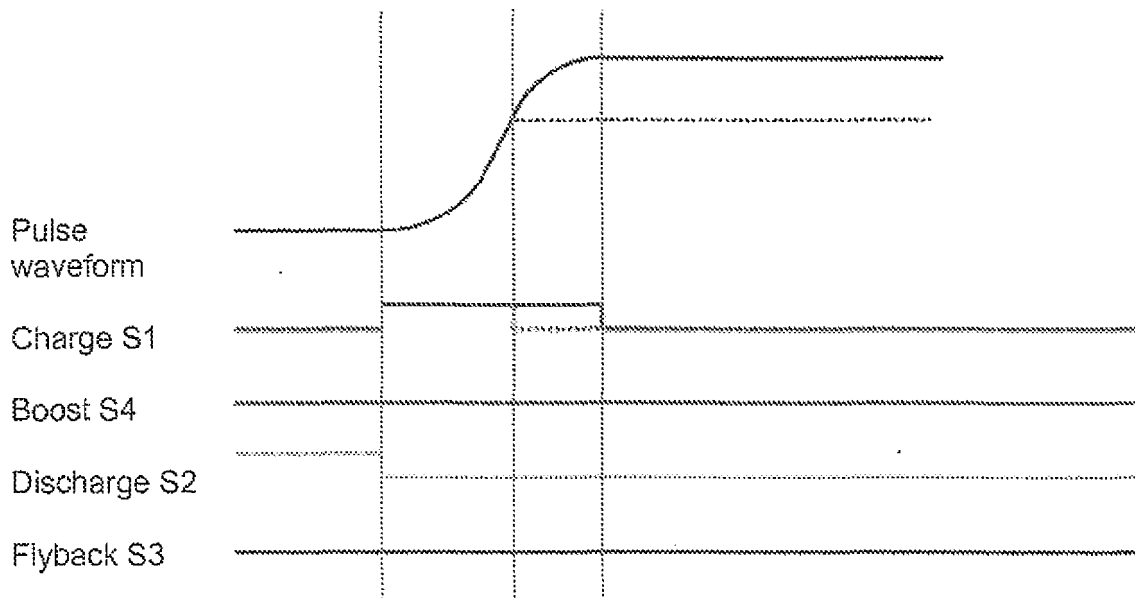


Fig. 3

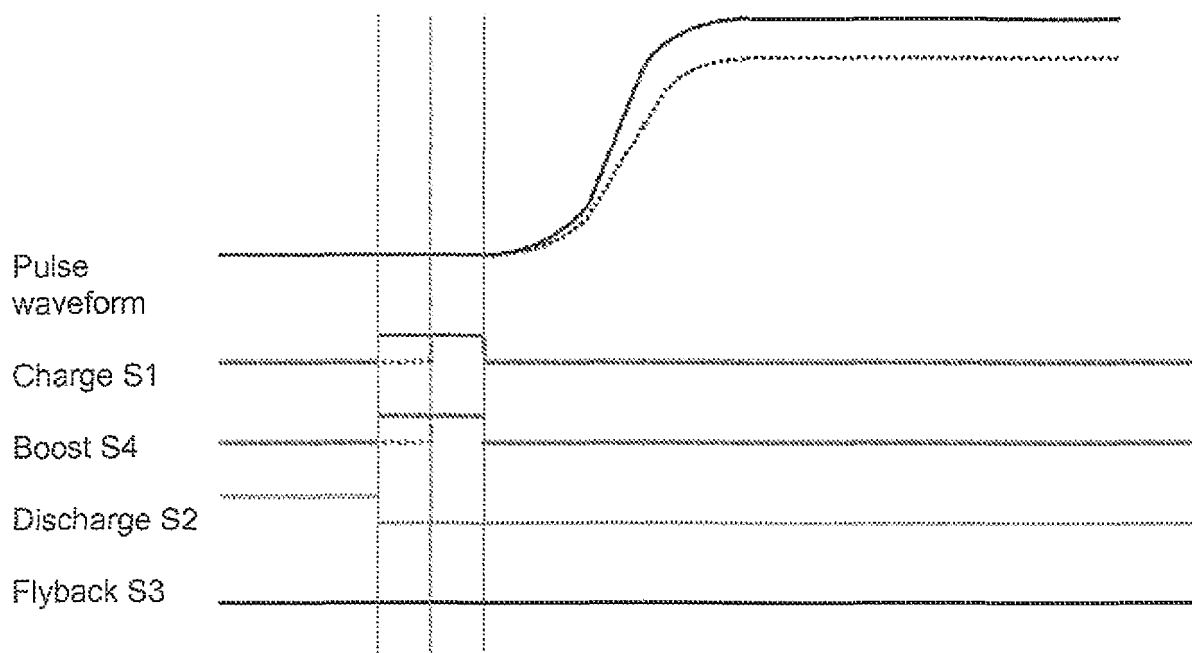


Fig. 4

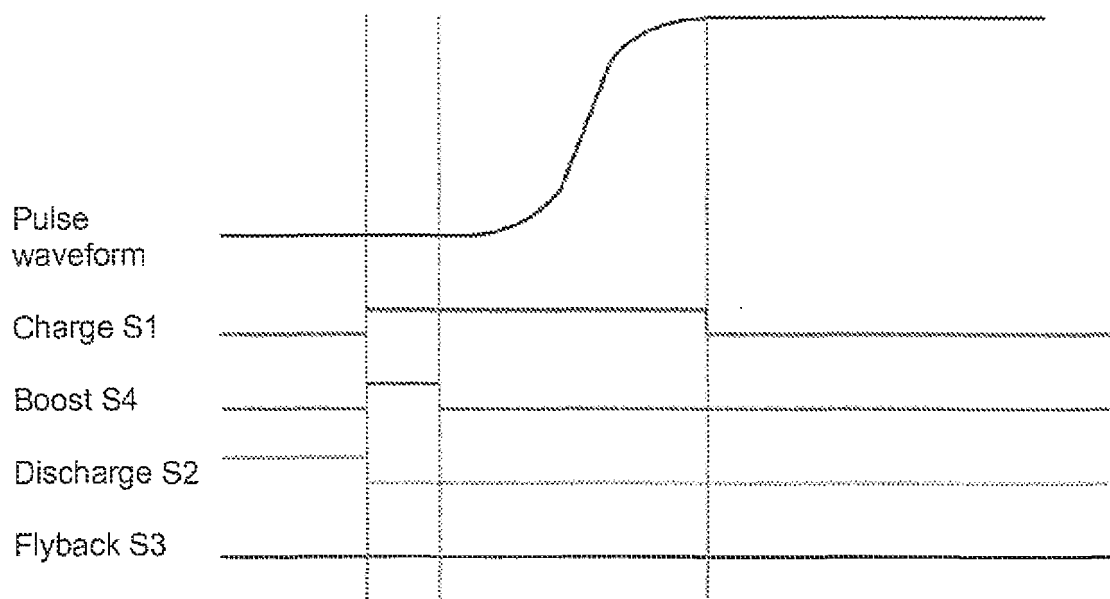


Fig. 5

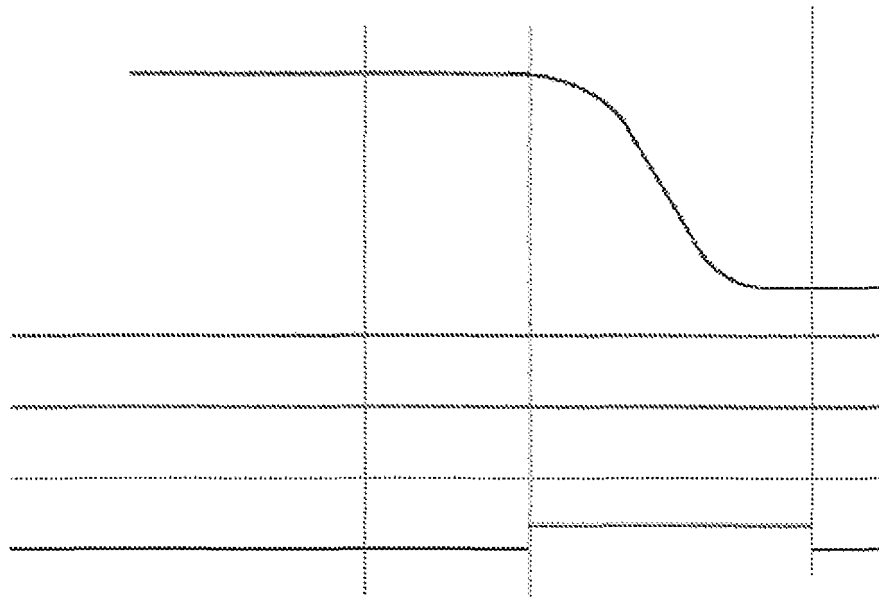
Pulse  
waveform

Charge S1

Boost S4

Discharge S2

Flyback S3



*Fig. 6*

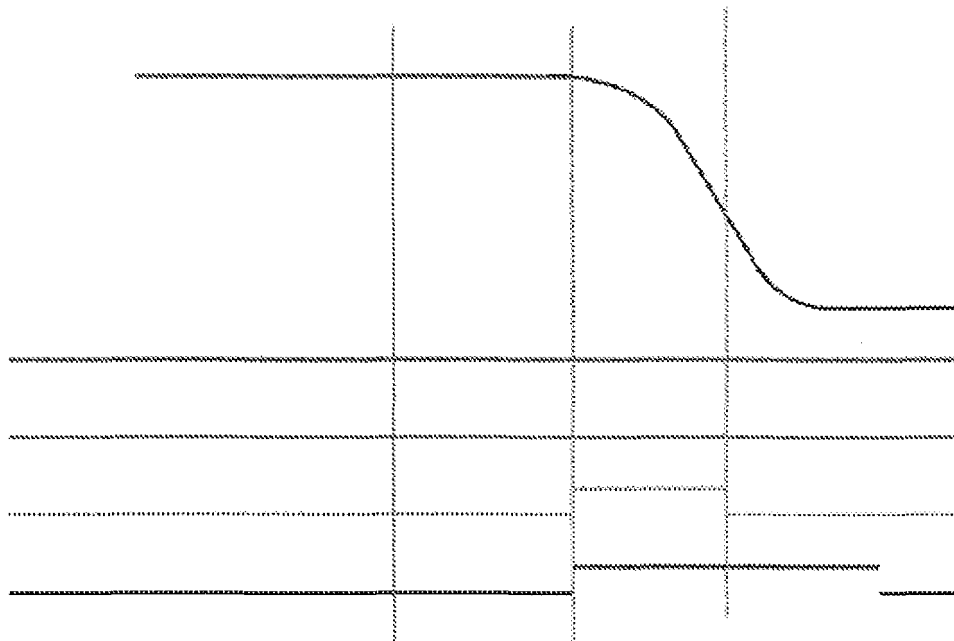
Pulse  
waveform

Charge S1

Boost S4

Discharge S2

Flyback S3



*Fig. 7*

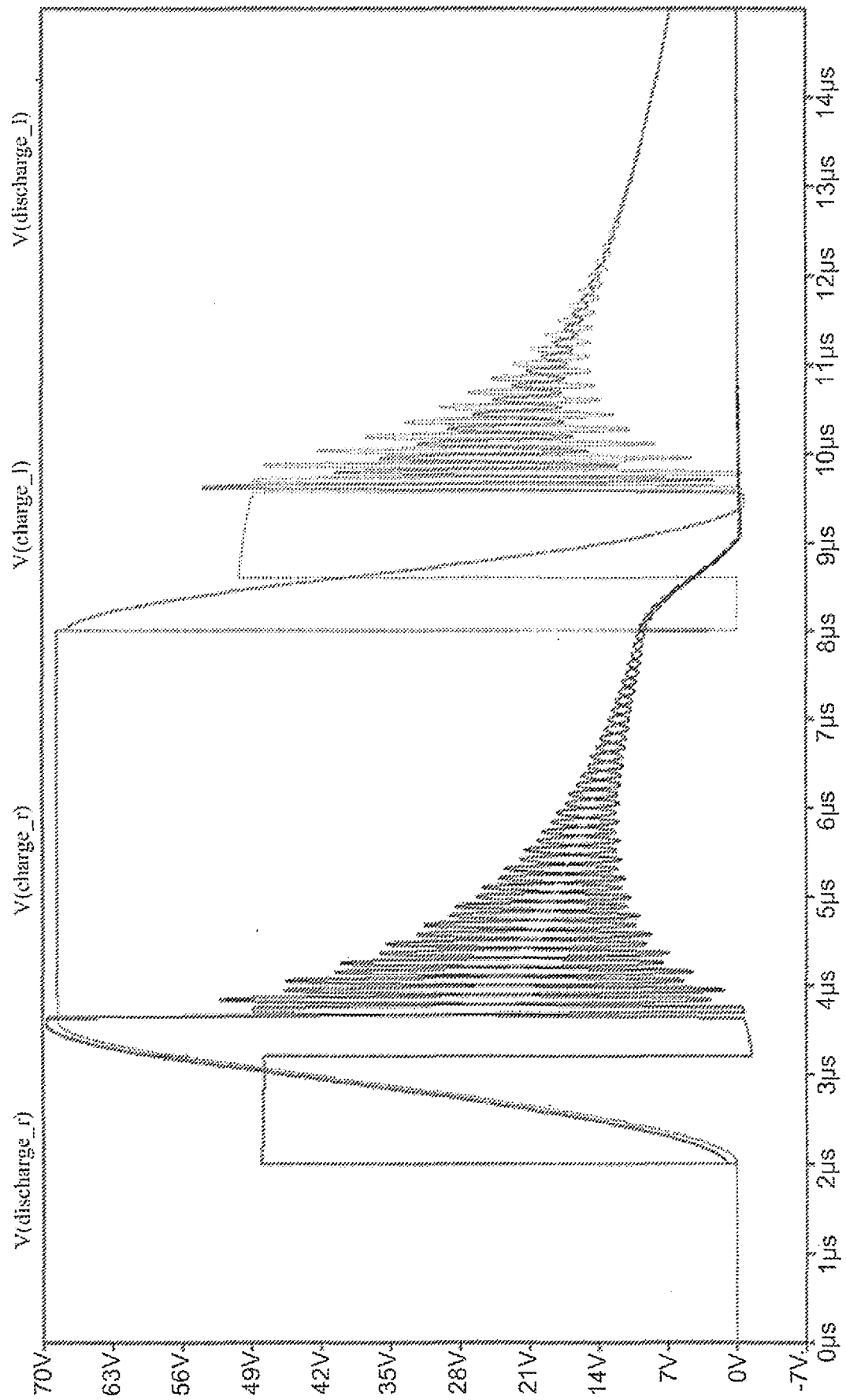


Fig. 8

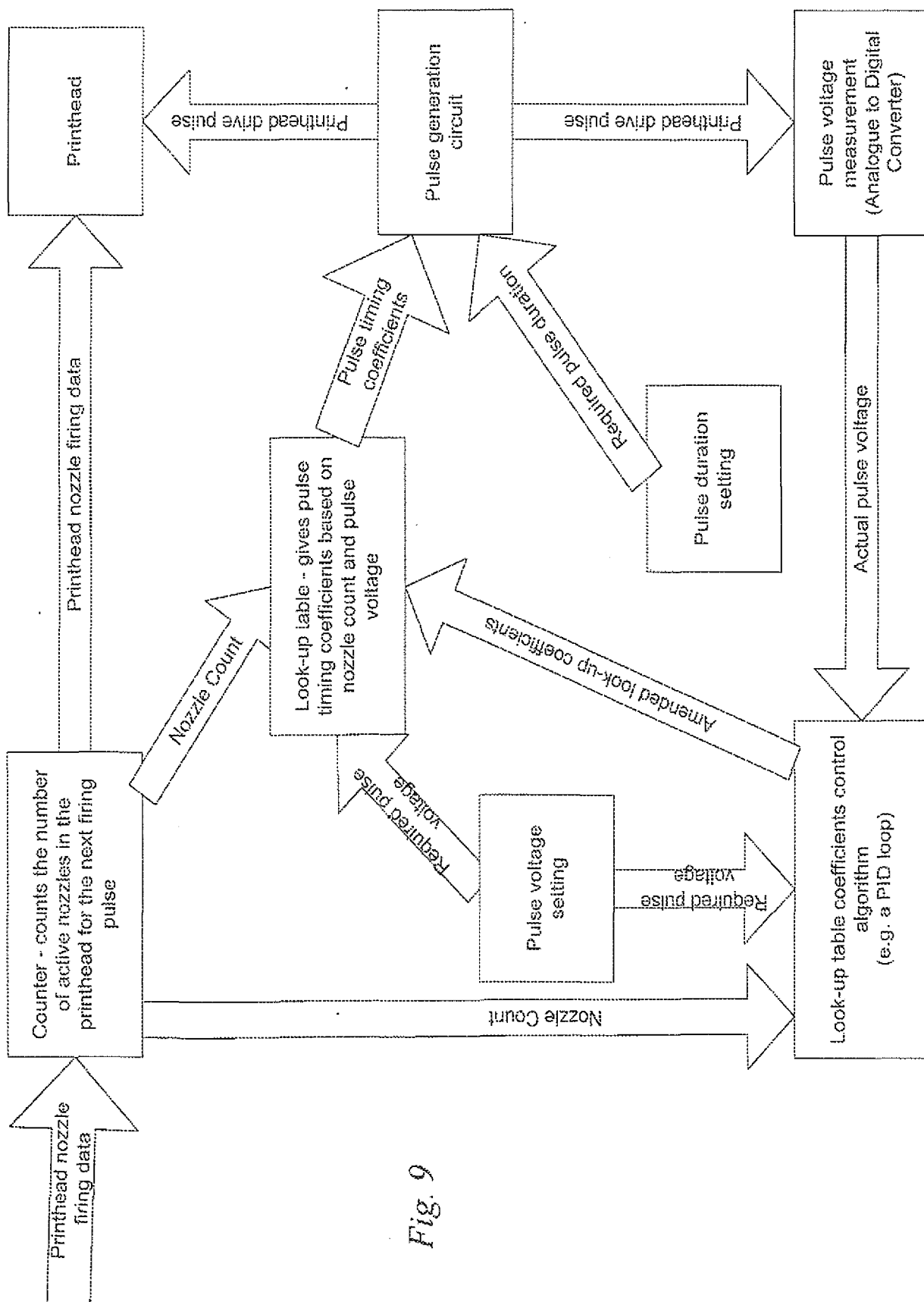


Fig. 9

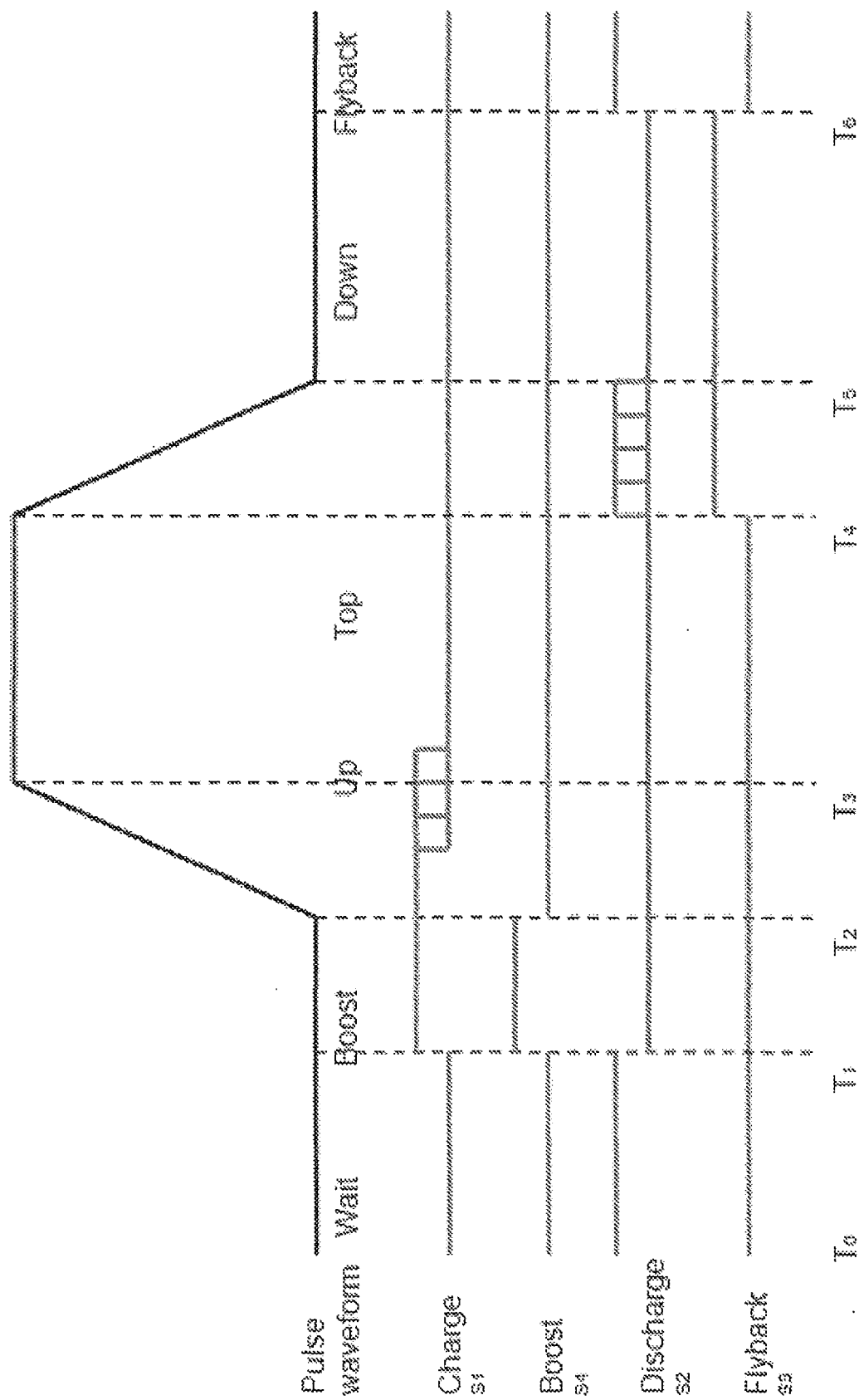


Fig. 10



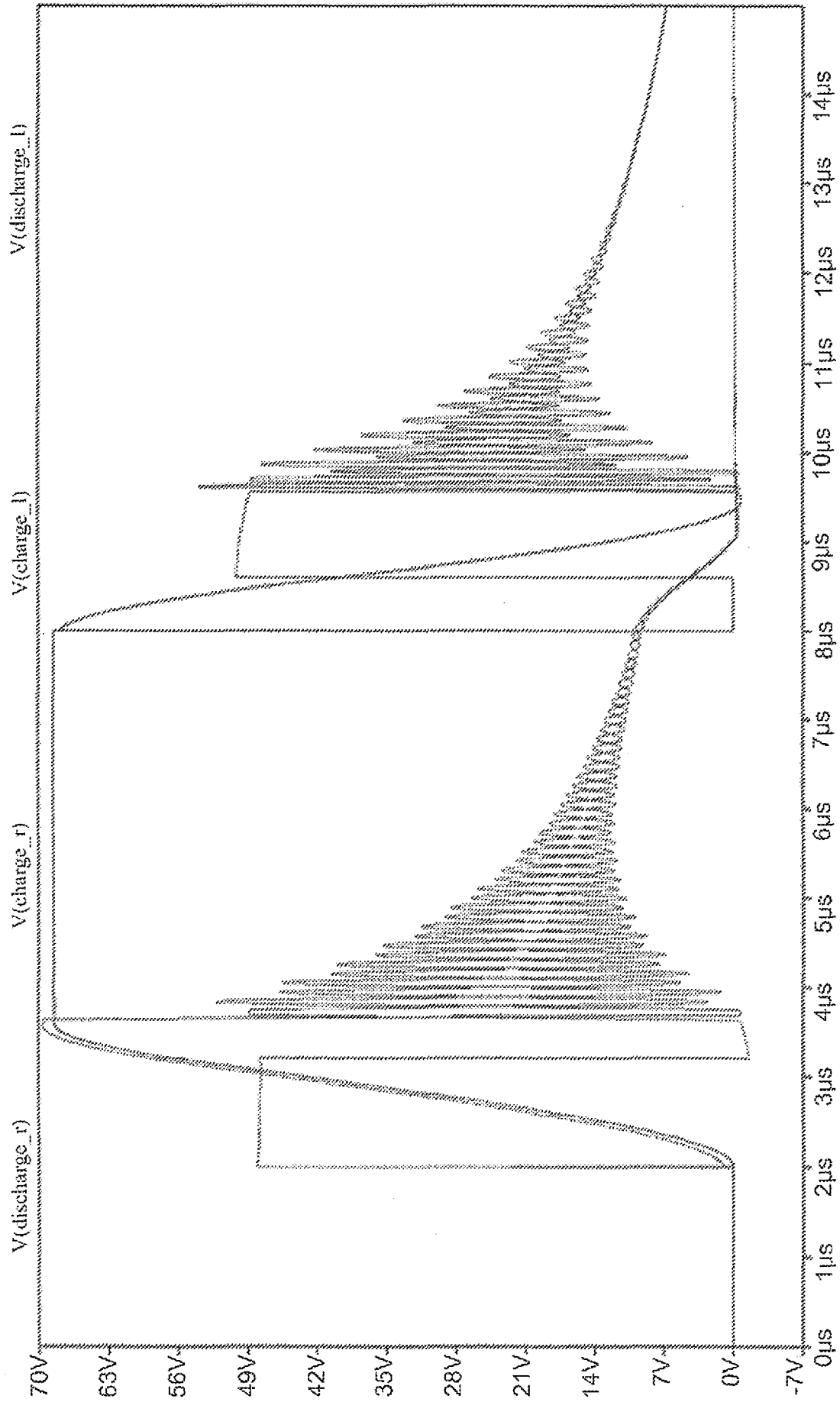


Fig. 11

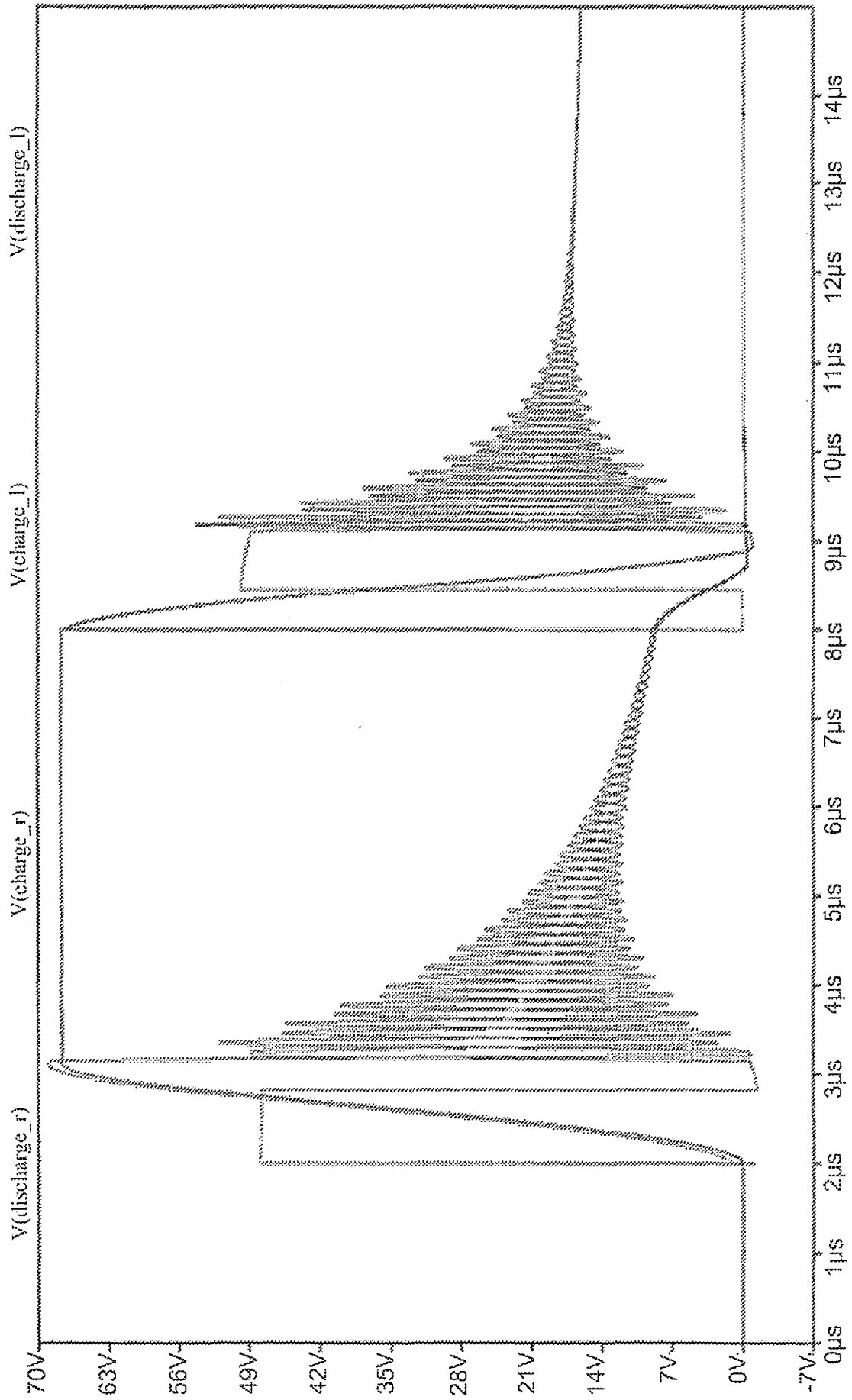


Fig. 12

04 01 13

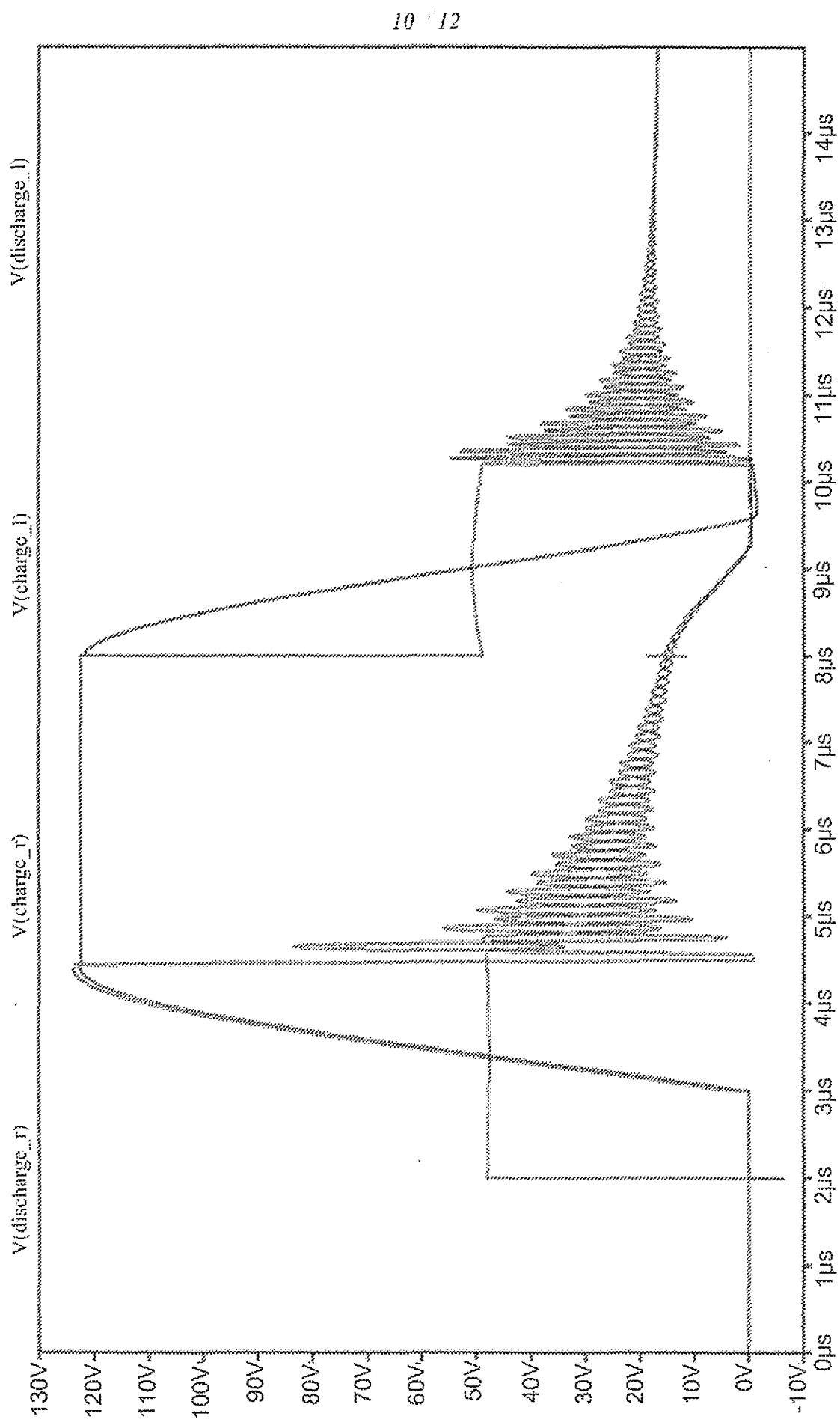


Fig. 13

04 01 13

11/12

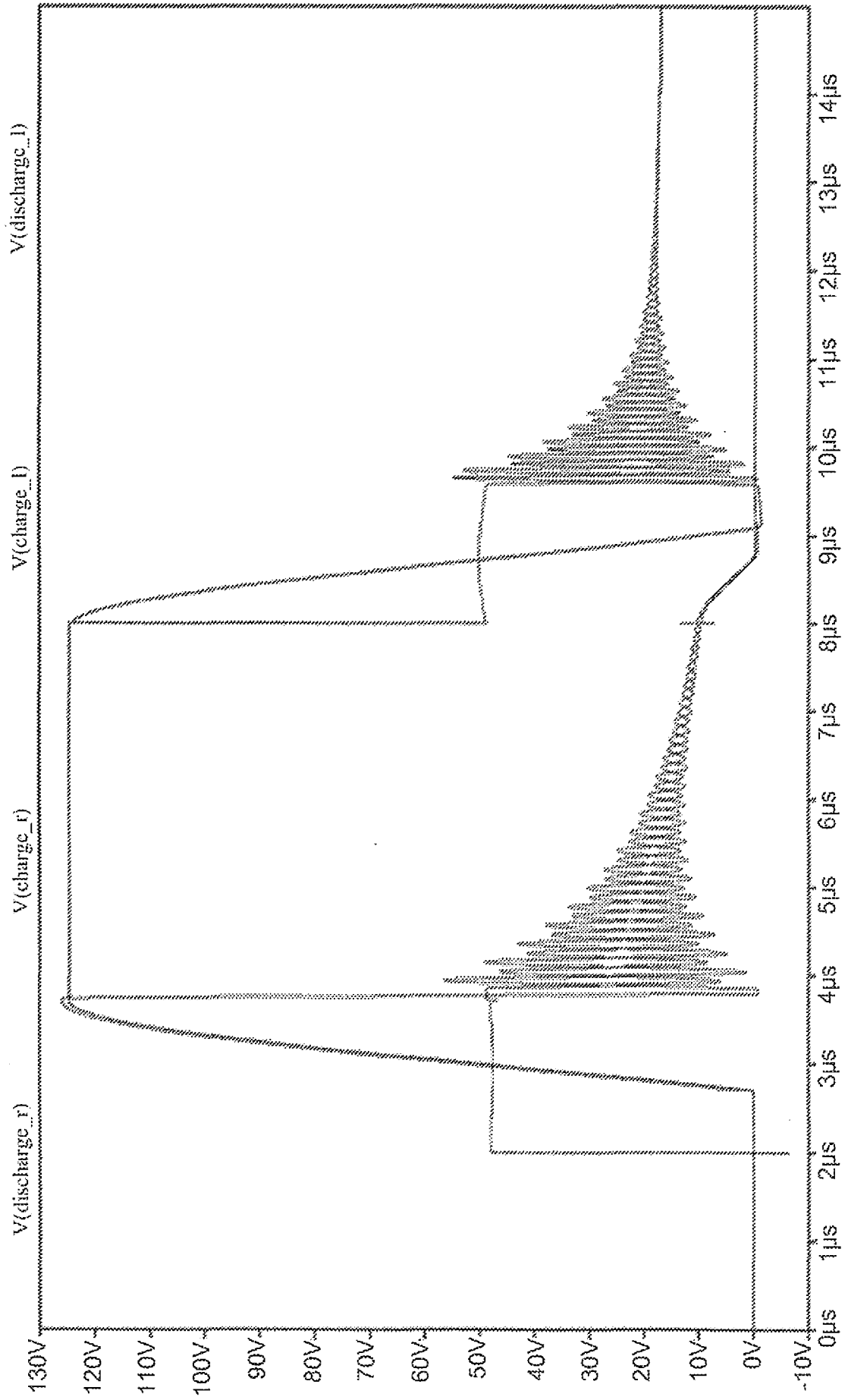


Fig. 14

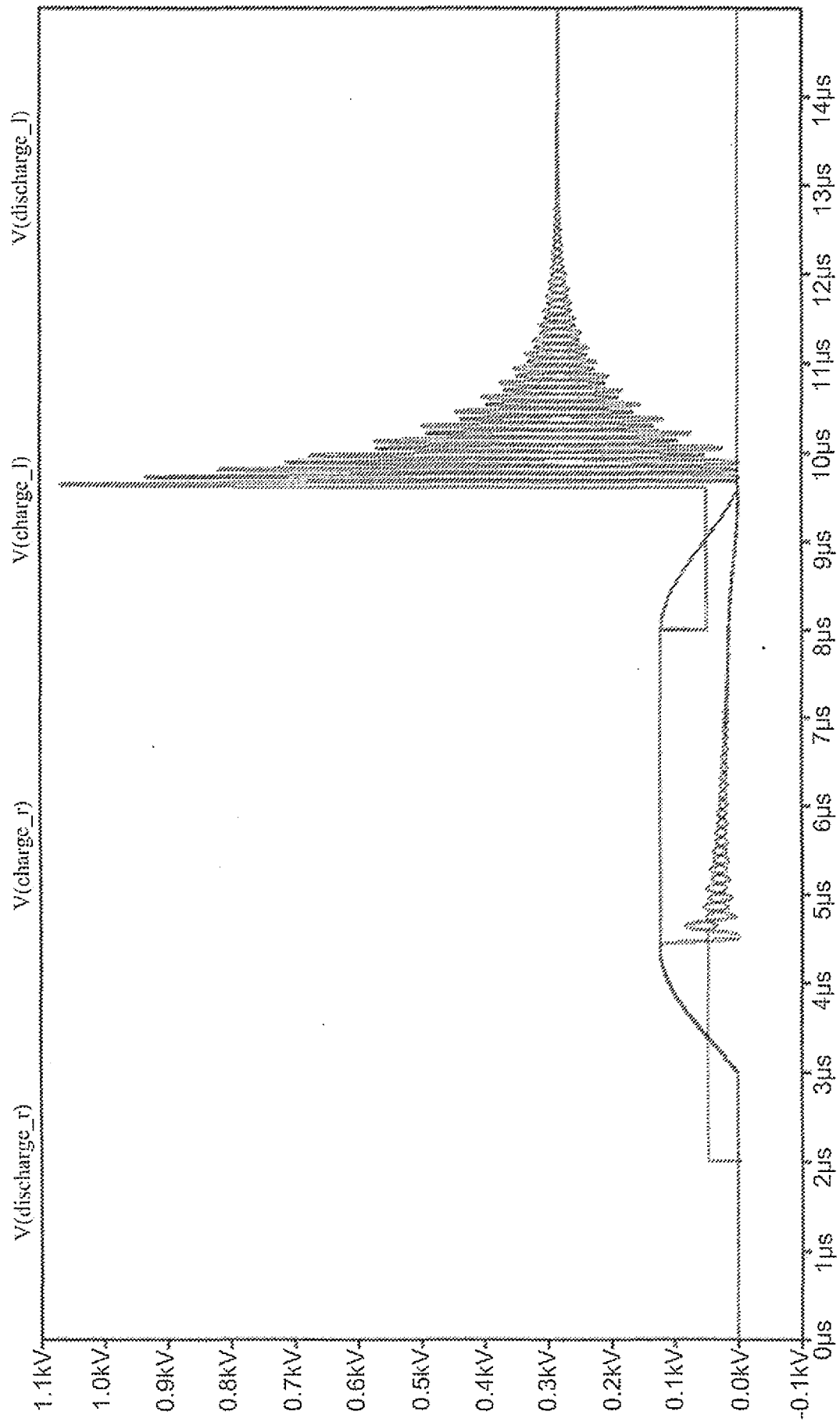


Fig. 15

### **Inkjet Printhead Driver Circuit and Method**

Printheads for ink jet printers are typically piezo electric. Piezo electric elements have capacitance and energy is typically dissipated in rapidly charging and discharging the capacitance to a desired voltage through the intrinsic circuit resistance to eject ink drops. These problems are an issue in high speed high volume printheads where significant power is dissipated, leading both to energy wastage and cooling problems. In systems driving large arrays of printheads, this power dissipation can be significant, requiring large DC power supplies to provide the energy and large heatsinks to dissipate the waste heat.

An inductive energy recovery circuit for driving capacitive loads, such as single piezo actuators, have been described in Efficient Charge Recovery Method for Driving Piezoelectric Actuators with Quasi-Square Waves by Domenico Campolo, Metin Sitti, and Ronald S. Fearing (IEEE Trans. On Ultrasonics, Ferroelectrics, And Frequency Control, Vol. 50, No. 1, January 2003).

It has been proposed to incorporate inductance in a drive circuit for a piezo electric element as energy can be recycled between an inductor (which stores energy as a function of current flowing) and a capacitor, as is well known in electrical theory. However, when theoretical circuits are applied to practical printheads, it is found that issues arise. It is problematic to achieve desired rapid charging and discharging without unwanted ringing and the pulse repetition rate can be adversely affected (which in a printer translates to resolution reduction or printing time increase). Also it is found that a printhead adding an inductor can reduce uniformity of print as printhead voltages may fluctuate.

The present invention provides a drive circuit for repetitively energising a printhead to eject drops of ink, the printhead having multiple nozzle channels each having a respective capacitance, the drive circuit comprising: a first switching element connected to couple a drive connection of the printhead to a first connection of a power supply via a first inductor to provide a charge path for current to charge the capacitance of at least one nozzle channel to a desired operating voltage; and a second switching element connected to couple a drive connection of the printhead to a second connection

of the power supply via a second inductor to provide a discharge path for current to discharge the capacitance of said at least one nozzle channel to a desired inter-pulse voltage.

5 By providing separate switching elements with separate inductors for charge and discharge phases, it has been found that a high pulse repetition rate can be achieved without dissipating energy in resistive losses. The separate inductors can allow the charge and discharge phases to be overlapped and each can be more precisely controlled. It has been found that one cause of variation in a circuit with a single inductor  
10 is that the energy stored may be in an indeterminate state between pulses, partly due to variation in the capacitance of the head. With separate inductors for charge and discharge it is easier to have the charge path in a known state. This use of a pair of inductors offers greater flexibility in the timing of the voltage pulse, allowing higher pulse repetition frequencies to be achieved and permitting more stable operation when  
15 parasitic capacitances are present. As will be apparent, this use of a pair of inductors could be applied to control circuits for other piezo electric devices and benefit from the same advantages.

The inductors may be of differing values to give desired slope times which may be  
20 different for charge and discharge, and may be tailored to physical characteristics of a printhead. Moreover, the interaction of the inductor and the capacitor can allow the capacitor to be charged to a higher voltage than the power supply voltage, as the charge circuit can behave as a voltage doubler; this avoids the need for a separate voltage step-up circuit. By way of example only, a typical print head drive voltage of about 90 volts  
25 may be generated directly from a 48 volt bus voltage.

A circuit element which permits current flow in only one direction, such as a first diode, is preferably connected in series between the first inductor and printhead drive connection to facilitate the voltage doubler operation. The first diode allows current of the  
30 charge path to flow into the capacitance of at least one nozzle channel.

A further circuit element which permits current flow in only one direction, such as a second diode, is preferably connected in series between the second inductor and

printhead drive connection to inhibit reverse current flow from the second inductor. The second diode allows current of the discharge path to flow out from the capacitance of at least one nozzle channel.

5            Preferably the drive circuit further comprises a third switching element connected between the second inductor and the first connection of the power supply. This enables a flyback current pathway for the energy stored in the second inductor, thereby improving efficiency.

10           An additional circuit element which permits current flow in only one direction, such as a third diode, is preferably connected in series between the second inductor and the first power supply connection to facilitate the flyback operation. The third diode allows current of the discharge path to flow back to the first power supply connection.

15           Preferably the drive circuit further comprises a fourth switching element connected between the first inductor and the second connection of the power supply. This can be used to provide a boost by causing (increased) current to flow in the first inductor to store energy, to achieve boost to a voltage higher than double the power supply voltage.

20           A yet further circuit element which permits current flow in only one direction, such as a fourth diode, is preferably connected in series between the first inductor and the second power supply connection to facilitate the boost operation, enabling current to flow when the first switch is open to provide a ground reference (assuming the second  
25 power supply connection is deemed ground, or other potential). The fourth diode allows current to flow from the second power supply connection to the first inductor.

             A still further circuit element which permits current flow in only one direction, such as a fifth diode, is preferably connected in series between the second inductor and  
30 the second power supply connection to facilitate discharge operation from higher voltages, enabling current in the second inductor to flow to the first power supply connection. The fifth diode allows current to flow from the second power supply connection to the second inductor.



The switching elements may be transistors, particularly field effect transistors. Preferably a control arrangement provides drive waveforms for the switching elements to provide switching directly between substantially fully on and fully off, the on and off switching times being selected to provide the desired drive voltage based on the time for 5 which current flows in the first inductor.

Where the fourth switching element is provided, the control arrangement may be arranged to switch between a boost mode in which the fourth switching element is used and a normal mode based on the desired voltage. This may be based on a chosen 10 operating regime; it may be found that although a given voltage is achievable in both modes, it is more efficient to operate in one mode than another.

Preferably the printhead drive terminal is connected to supply power to a plurality of nozzle channels, the nozzle channels being connected to a return path, typically 15 coupled to the second power supply connection, wherein each of the plurality of nozzle channels is connected in series with a respective nozzle switching element. In this way, the power circuit need not be replicated for all nozzle channels and there may be one power circuit for an entire head or even for several heads, the nozzle printing being controlled by the nozzle switching elements. The nozzle switching elements may be 20 smaller and may be arranged to switch only at times when power is not being supplied by the drive connection from the drive circuit to reduce dissipation in the nozzle switching elements.

Preferably the control arrangement is arranged to adjust the drive circuit in 25 dependence on the number of nozzle channels being fired based on information concerning the individual nozzle switching elements or a measure of the number of active nozzle channels for a given drive pulse. This may enable a uniform printing to be achieved unaffected by variations in total capacitance. This feature may be provided independently in a drive circuit for a printhead arranged to supply drive power pulses to a 30 plurality of individually switched nozzle channels characterised by means for adjusting a parameter of the drive circuit based on a measure of the number of nozzle channels active for a given pulse.

Preferably, the drive circuit has at least one inductor in the drive output and wherein the drive circuit has at least one compensating capacitor in parallel across the printhead and drive terminal to reduce the variation in load capacitance with the number of active nozzles. This, in a normal circuit, would be counter-intuitive because it would  
5 merely increase the power needed to drive the print head. However, its presence together with an inductor provides the advantage of stabilizing timing and which outweighs this downside.

In a related aspect, the invention provides determining a measure of the number  
10 of nozzle channels of a printhead expected to be active for a given drive pulse and providing a control parameter to circuitry generating the drive pulse to compensate for variation in nozzle channel capacitance.

In a related aspect, to reduce the dynamic range of adjustment, the invention  
15 provides a compensating circuit for a printhead having a plurality of nozzle channels each having a capacitance and wherein a plurality of nozzle channels are connected to a common drive connection and in series with individual nozzle control switching elements, the circuit comprising a compensating capacitance arrangement connected to the drive connection to reduce the variation in overall capacitance presented to the drive circuit  
20 with variation in the number of active nozzle channels.

The compensating capacitance arrangement may be a fixed capacitor having a capacitance substantially one third the total head capacitance with all nozzle channels active. Additionally or alternatively, the compensating capacitance arrangement may  
25 include one or more additional capacitances coupled via a switching element or via respective switching elements to the drive terminal and control means may be provided for switching additional capacitances to reduce variation in overall capacitance based on the number of active nozzle channels. The additional capacitances may be arranged in binary relation, for example one capacitance of approximately half the difference  
30 between maximum and minimum printhead capacitance, one of a quarter and one of an eighth will reduce the dynamic variation to approximately 12% with only 3 capacitances and a fourth would give approximately 6%.

In a further aspect where a drive circuit for a printhead has an adjustable parameter for controlling pulse voltage, preferably a control arrangement is provided for measuring actual nozzle channel voltages and adjusting the parameter based on measurements. This is most advantageously achieved with the circuit of the first aspect 5 by adjusting timing values based on measured voltages. Most preferably adjustments are made based on both a measure of voltage and a measure of the number of active nozzle channels.

As will be apparent, preferred features of each aspect may be applied with other 10 aspects and method aspects may be provided as corresponding apparatus, for example logic or circuits, and vice versa.

Further features and advantages of the invention will be better understood from the following detailed description, which is given by way of example and in association 15 with the accompanying drawings of which:

Figure 1 shows a schematic diagram of a circuit for energising a printhead;

Figure 2 shows a simplified schematic diagram of a pulse generation circuit; 20

Figure 3 shows the circuit of Figure 2 charging the capacitance of a printhead nozzle channel;

Figure 4 shows the circuit of Figure 2 charging to more than double the supply 25 voltage, relative to ground;

Figure 5 shows the circuit of Figure 2 charging to more than double the supply voltage, relative to supply;

30 Figure 6 shows the circuit of Figure 2 discharging with pulse voltages greater than double the supply;

Figure 7 shows the circuit of Figure 2 discharging with pulse voltages less than double the supply;

Figure 8 shows dissipation of energy from the inductors to avoid “ringing”;

5

Figure 9 shows a flow diagram of a feedback system;

Figure 10 shows switch timing relationships of worked examples of 48 Volt operation of the drive circuit;

10

Figure 11 shows discharge voltage waveforms (less than 2 x HT pulse 10n + 10n load);

Figure 12 shows discharge voltage waveforms (less than 2 x HT pulse 10n 15 load);

Figure 13 shows discharge voltage waveforms (more than 2 x HT pulse, 10n + 10n load);

20 Figure 14 shows discharge voltage waveforms (less than 2 x HT pulse 10n load); and

Figure 15 shows discharge voltage waveforms which occur at premature termination of flyback signal

25

Referring to Figure 1, there is shown a schematic diagram of a control or drive circuit for repetitively energising a printhead 10 to eject drops of ink. The printhead has multiple nozzle channels each with a respective capacitance  $C_{n1}$ ,  $C_{n2}$ ,  $C_{n3}$ ,  $C_{n4}$ ...  $C_{nn}$  which are repetitively energized by the pulse generation circuit 20, as shown in Figure 2, 30 to eject drops of ink. The print head has its own inherent capacitance  $C_{n0}$  indicated in parallel across the nozzle channels. A printhead drive terminal 30 connects the nozzle channels to a first power supply connection 40 from the pulse generation circuit 20. The nozzle channels are connected by a current return path 50 to a second power supply

connection 60 to the pulse generation circuit 20. Each nozzle channel is connected in series with a respective nozzle switching element  $S_{n1}$ ,  $S_{n2}$ ,  $S_{n3}$ ,  $S_{n4}$ ...  $S_{nn}$  controlled by a print data source 70 and a timing data source 80.

- 5        The drive circuit comprises a control arrangement 90 to drive wave forms for switching elements  $S_1$ ,  $S_2$ ,  $S_3$ ,  $S_4$  in the pulse generation circuit 20. The control arrangement receives data from the print data source 70 and the timing data source 80. The timing data is processed by a timing generator 100. The print data is processed by a counter 110 to count the active nozzle channels at any one time based on the print data.
- 10    The control arrangement has a memory chip 120 storing a table of desired power supplies to the nozzle channels. Logic 130 is supplied information from the timing generator 100, counter 110 and look-up memory 120 in order to drive the switching elements  $S_1$ ,  $S_2$ ,  $S_3$ ,  $S_4$  in the pulse generation circuit 20.
- 15        In a development, the drive circuit also comprises a compensating circuit 140 with one or more actively switched compensating capacitors  $C_{c1}$ ,  $C_{c2}$ ,  $C_{c3}$  connected in parallel with a fixed compensating capacitor  $C_{c0}$ . Each compensating capacitor is connected in series with a respective switching element  $S_{c1}$ ,  $S_{c2}$ ,  $S_{c3}$  controlled by the control arrangement 90. The compensating circuit is connected in parallel with the
- 20    printhead 10 via terminals A and B. The fixed compensating capacitor has a capacitance of approximately one third of the total head capacitance with all nozzle channels active. By switching capacitances in dependence on the number of active nozzle channels, the variation in overall capacitance can be reduced. The capacitances may be arranged in binary magnitude, compensating capacitor  $C_{c1}$  may be half
- 25    compensating capacitor  $C_{c0}$ , compensating capacitor  $C_{c2}$  may be half compensating capacitor  $C_{c1}$ , compensating capacitor  $C_{c3}$  may be half compensating capacitor  $C_{c2}$  so that variation may be reduced to about 10%.

The pulse generation circuit operation is discussed with reference to Figures 2 to 9.

Referring to Figure 2 there is shown a simplified schematic diagram of the pulse generation circuit. The switches control the flow of current between the power rail, the printhead capacitance and the inductors.

5        Various switching sequences, resulting in charging or discharging of the printhead capacitance C1, will now be described with reference to Figures 3 to 5,

Referring in particular to Figure 3, closure of first switching element S1 charges printhead capacitance C1 via a first inductor L1 and a first diode D1. Such a circuit can  
10 generate a voltage on the capacitor approaching twice the DC supply voltage, as is shown by the solid line in Figure 3. However, by opening the first switching element S1 before the resonant transfer of energy from the first inductor L1 to printhead capacitance C1 has completed, any voltage up to this voltage can be generated, as is shown by the dashed lines in Figure 3.

15

Referring in particular to Figure 4, there is shown how the circuit charges to more than double the supply voltage, relative to ground potential. First switching element S1 and fourth switching element S4 are closed simultaneously, causing the current through the first inductor L1 to increase linearly with time. The greater the inductor charging time,  
20 the more energy is stored in the inductor's magnetic field. When first and fourth switching elements S1 and S4 are simultaneously open-circuited, there is a partially resonant exchange of energy from the first inductor L1 to the printhead capacitance C1, thus charging it up relative to a ground reference established through a fourth diode D4. The voltage attained will be a multiple of the supply rail voltage, the multiplier factor being  
25 approximately equal to the charging time divided by  $\sqrt{L1 * C1}$ . The effect of a shorter charging time is shown by the dashed lines of Figure 4.

Referring in particular to Figure 5, there is shown how the circuit charges to more than double the supply voltage, relative to ground potential. By keeping first switching  
30 element S1 closed after opening fourth switching element S4, the capacitor is charged in a way similar to the previous description, except the voltage is now established with respect to the supply rail (through first switching element S1) as is shown in Figure 4. Hence a higher voltage than previously is established for the same inductor charging

time: this leads to more efficient operation. In practice, a combination of the above schemes may be used in order to give a wide range of output voltages. Discharging of the printhead capacitance C1 is discussed below with reference to Figures 6 and 7,

5 Referring in particular to Figure 6, there is shown how the circuit discharges with pulse voltages greater than double the supply. When a third switching element S3 is closed, current flows from printhead capacitance C1 through a second diode D2, a second inductor L2 and a third diode D3 to the supply rail. If the initial pulse voltage is sufficiently high, by the time the voltage on the capacitor has been reduced to the supply  
10 rail voltage, the current established in the inductor L2 will be sufficiently high to draw the remaining charge out of the capacitor, reducing the voltage to zero, as is shown in Figure 6. Any current still flowing in the second inductor L2 at this point flows via a fifth diode D5 and a third diode D3 to the supply rail. In a practical circuit, this method works when the pulse voltage is at least 2.7 times greater than the supply voltage.

15

Referring in particular to Figure 7, there is shown how the circuit discharges with pulse voltages less than double the supply. Discharging with Pulse Voltages Less than Double the Supply. When a second switching element S2 is closed (it is convenient to close switching element S3 at this point) current starts to flow from the printhead  
20 capacitance C1 through the second diode D2, the second inductor L2 and second switching element S2 to ground potential. When a sufficient current is flowing in the second inductor L2, the second switching element S2 can be turned off. At this point at this point the current now flows from printhead capacitance C1, through the second diode D2, the second inductor L2, the third switching element S3 and the third diode D3  
25 to the supply rail, until printhead capacitance C1 is fully discharged to 0 volts. Any current still flowing in the second inductor L2 at this point flows via the fifth diode D5 and the third diode D3 to the supply rail, as is shown by Figure 7.

Referring to Figure 8, the benefit of dual inductor topology is discussed. Following  
30 the discharge of an inductor, at the point at which the current becomes zero, there is often a voltage across the inductor and also across any associated stray capacitances (such as inter-winding capacitance in the inductor or capacitance in the semiconductor switches). If the operation of the switches leaves the inductor effectively open circuit

then "ringing" of the voltage across the inductor can occur due to resonant energy transfer between the inductor and the stray capacitance. In order to achieve consistent charging of the inductor, it is helpful if this energy can be fully dissipated before the inductor is next charged. The dual inductor topology allows full current discharge and 5 oscillations in one inductor to decay whilst the other inductor is actively transferring current between the capacitor and supply rail.

A further advantage of the dual inductor topology is that inductor L1 can be charged with current at the same time that inductor L2 is being used to transfer charge 10 from the capacitor C1 to the supply rail. Hence it is possible to charge printhead capacitance C1 from the first inductor L1 shortly after it has been discharged into the second inductor L2 (allowing for the decay of parasitic oscillations). In this manner a very high pulse repetition rate can be achieved, with the limiting waveform appearing approximately sinusoidal.

15

A third advantage is that the pulse rise and fall times are determined by the LC time constants of the circuit components. By using inductors of different values for the charge and discharge inductors, it is possible to set different pulse rise and fall times.

20 In a real printhead, the capacitance presented increases with the number of piezo channels which are firing ink. Hence a more realistic model for the load capacitance when N piezo channels are being fired is:  $C1 = C0 + N \cdot Cn$  [where C0 is a constant capacitance due to the cabling and any fixed capacitor on the drive circuit, and Cn is the capacitance of a single piezo channel].

25

By using an additional load capacitance having a value of approximately one third the capacitance of the printhead when all nozzle channels are active, the dynamic range of loads over which the system must operate is reduced to the range  $[C0, 4 \cdot C0]$ . The extra energy stored in this load capacitance is mostly recovered during the capacitor 30 discharge cycle, so the penalty in terms of extra power dissipation is acceptable. As discussed below, actively switched compensating capacitances reduce variation further and can be used with a secondary drive circuit.



As a consequence of the data-dependant capacitance, the charging times for the pulse generation circuit must be varied depending upon the data being printed in order to achieve a consistent drive voltage. This can be achieved in digital hardware by means of a simple counting circuit and look-up tables for the charging times.

5

Referring to Figure 9, there is shown a flow diagram of a feedback system to achieve a stable pulse voltage. The pulse voltage generated has been shown to be related to the DC rail voltage, the charging inductance, load capacitance and charging times. It is known that these values, particularly the effective load capacitance, can  
10 change over time and may also exhibit some temperature dependence. Hence, in order to achieve a desired pulse voltage, it may be necessary to make fine adjustments to the inductor charging time throughout the operation of the pulse circuit. This may be achieved by measuring the generated voltage and comparing it with the desired voltage. Any error may be used as input to a control algorithm (such as a PID servo loop), which  
15 amends the inductor charging time based on the voltage error.

Values for the circuit components of Figure 2 in this typical, non-limiting, application are as follows:

Inductor (L1 & L2) = typically 10 to 50  $\mu$ H;

20 Capacitor (C1) = of the order of 10nF (No nozzle channels firing) to 40nF (All nozzle channels firing);

Rise and fall times = in the order of 1 $\mu$ s;

Pulse duration = in the range 3 to 6  $\mu$ s;

Pulse to pulse interval = 10 $\mu$ s all the way up to 1ms and beyond;

25 Supply voltage = 24V or 48V although any supply voltage is possible; and

Pulse voltage = typically in the range 60V to 120V although it can be in the lower range of 25V to 35V for some printheads.

Referring to Figures 10 to 14, the following are worked examples of 48 Volt  
30 operation of a typical drive circuit.

Referring in particular to Figure 10, there are shown the switch timing relationships according to the table below.

State	Times	Devices active, Comments
Wait	$T_0 - T_1$	S2 output clamp function
Boost	$T_1 - T_2$	S1 and S4, for pulse voltages $> \approx 1.7 \times HT$ . Can be 0uS.
Up	$T_2 - T_3$	S1 Inductor charge and release whilst driving load
Top	$T_3 - T_4$	This time contributes to the pulse length.
Down	$T_4 - T_5$	S3 and some S2 is required to make sure
Flyback	$T_5 - T_6$	S3 only. S2 must be off otherwise recovered energy is lost and the inductor discharge period is greatly extended. The period $T_4 - T_6$ is typically longer than $T_1 - T_3$ , to ensure that all the energy is returned to the source, otherwise potentially dangerous flyback voltages will arise which will eventually destroy the circuit. Like wise S3 must be on when S2 turns off.
Wait		S2 as output clamp

5

Referring to Figure 11, there is shown the discharge voltage waveforms (less than  $2 \times HT$  pulse  $10n + 10n$  load) according with the switch timings of the table below.

Name	Function	Delay	On	unit s	Comments
S1	Charge L1	2.0	1.2	uS	
S4	Ground L1				Not required
S2	Ground L2	8.0	0.6	uS	To make sure comes back to load goes back to 0 volts
S3	Flyback L2	8.0	>1.6	uS	

10

15

Referring to Figure 12, there is shown the discharge voltage waveforms (less than 2 x HT pulse 10n load) according with the switch timings of the table below.

Name	Function	Delay	On	unit s	Comments
S1	Charge L1	2.0	0.82	uS	
S4	Ground L1				Not required
S2	Ground L2	8.0	0.45	uS	To make sure comes back to load goes back to 0 volts
S3	Flyback L2	8.0	>1.1	uS	

5

Referring to Figure 13, there is shown the discharge voltage waveforms (more than 2 x HT pulse, 10n + 10n load) according with the switch timings of the table below.

Name	Function	delay	On	unit s	Comments
S1	Charge L1	2.0	>2.5	uS	
S4	Ground L1	2.0	1.1	uS	Extra charge in inductor to take over 2x HT
S2	Ground L2				Not required *
S3	Flyback L2	8.0	>2.3	uS	

10

Referring to Figure 14, there is shown the discharge voltage waveforms (less than 2 x HT pulse 10n load) according with the switch timings of the table below.

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Name	Function	delay	On	unit s	Comments
S1	Charge L1	2.0	>1.7	uS	
S4	Ground L1	2.0	0.7	uS	Extra charge in inductor to take over 2x HT
S2	Ground L2				Not required*
S3	Flyback L2	8.0	>1.6	uS	

The above embodiments are to be understood as illustrative examples of the invention. Further embodiments of the invention are envisaged. It is to be

understood that any feature described in relation to any one embodiment may be used alone, or in combination with other features described, and may also be used in combination with one or more features of any other of the embodiments, or any combination of any other of the embodiments. Furthermore, equivalents and  
5 modifications not described above may also be employed without departing from the scope of the invention, which is defined in the accompanying claims.

### Claims

1. A drive circuit for repetitively energising a printhead (10) to eject drops of ink, the printhead having multiple nozzle channels each having a respective capacitance, the  
5 drive circuit comprising:
  - a first switching element (S1) connected to couple a drive connection of the printhead to a first connection of a power supply (V1) via a first inductor (L1) to provide a charge path for current to charge the capacitance of at least one nozzle channel to a desired operating voltage; and
  - 10 a second switching element (S2) connected to couple a drive connection of the printhead to a second connection of the power supply (V1) via a second inductor (L2) to provide a discharge path for current to discharge the capacitance of said at least one nozzle channel to a desired inter-pulse voltage.
- 15 2. A drive circuit as claimed in claim 1, wherein the drive circuit comprises a first circuit element (D1) which permits current flow in only one direction and which is connected in series between the first inductor (L1) and the printhead drive connection.
3. A drive circuit as claimed in either one of claims 1 or 2, wherein the drive circuit  
20 comprises second a circuit element (D2) which permits current flow in only one direction and which is connected in series between the second inductor (L2) and the printhead drive connection.
4. A drive circuit as claimed in any one of the previous claims, wherein the drive  
25 circuit comprises a third switching element (S3) connected between the second inductor (L2) and the first connection of the power supply.
5. A drive circuit as claimed in any one of the previous claims, wherein the drive circuit comprises a third circuit element (D3) which permits current flow in only one  
30 direction and which is connected in series between the second inductor (L2) and the first power supply connection.

6. A drive circuit as claimed in any one of the previous claims, wherein the drive circuit comprises a fourth switching element (S4) connected between the first inductor (L1) and the second connection of the power supply.

5 7. A drive circuit as claimed in any one of the previous claims, wherein the drive circuit comprises a fourth circuit element (D4) which permits current flow in only one direction and which is connected in series between the first inductor (L1) and the second power supply connection.

10 8. A drive circuit as claimed in any one of the previous claims, wherein the drive circuit comprises a fifth circuit element (D5) which permits current flow in only one direction and which is connected in series between the second inductor (L2) and the second power supply connection.

15 9. A drive circuit as claimed in any one of the previous claims, wherein the or each switching element (S1,S2,S3,S4) is a transistor.

10. A drive circuit as claimed in any one of the previous claims, wherein the drive circuit comprises a control arrangement (90) to drive waveforms for the switching  
20 elements (S1,S2,S3,S4) to provide switching directly between substantially fully on and fully off and wherein the on and off switching times being selected to provide the desired drive voltage based on the time for which current flows in the first inductor (L1).

11. A drive circuit as claimed in claim 10 when appended to claim 6, wherein the  
25 control arrangement (90) may be arranged to switch between a boost mode in which the fourth switching element (S4) is used and a normal mode based on the desired voltage.

12. A drive circuit as claimed in any either one of claims 10 or 11, wherein the printhead drive terminal (30) is connected to power supply to a plurality of nozzle  
30 channels and the nozzle channels are connected to a current return path (50), wherein each of the plurality of nozzle channels is connected in series with a respective nozzle switching element (Sn1, Sn2, Sn3, Sn4).

13. A drive circuit as claimed in claim 12, wherein the current return path of the nozzle channels is coupled to the second power supply connection (60).

14. A drive circuit as claimed in either one of claims 12 or 13, wherein the control arrangement is arranged to adjust the drive circuit in dependence on the number of nozzle channels being fired based on information concerning the individual nozzle switching elements or a measure of the number of active nozzle channels for a given drive pulse.

15. A drive circuit as claimed in any one of the previous claims, wherein the drive circuit has at least one inductor in the drive output and wherein the drive circuit has at least one compensating capacitor (Cc1, Cc2, Cc3) in parallel across the printhead (10) and drive terminal to reduce the variation in load capacitance with the number of active nozzle channels.

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16. A drive circuit for a printhead arranged to supply drive power pulses to a plurality of individually switched nozzle channels characterised by means for adjusting a parameter of the drive circuit based on a measure of the number of nozzle channels active for a given pulse.

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17. A method of supplying drive power pulses to a plurality of individually switched nozzle channels, wherein the method comprises the steps of:

a) determining a measure of the number of nozzle channels of a printhead expected to be active for a given drive pulse; and

25 b) providing a control parameter to circuitry generating the drive pulse to compensate for variation in nozzle channel capacitance.

18. A method as claimed in claim 17, further comprising the step:

c) adjusting the timing signals for a drive circuit as claimed in any 1 to 15.

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19. A method as claimed in claim 18, further comprising the step:

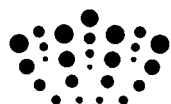
d) adjusting the timing signals on the basis of the measured nozzle channel voltage.

20. A compensating circuit for a printhead having a plurality of nozzle channels each having a capacitance, wherein a plurality of nozzle channels are connected to a common drive connection and in series with individual nozzle control switching elements, wherein  
5 the compensating circuit comprises a compensating capacitance arrangement connected to the drive connection to reduce the variation in overall capacitance presented to the drive circuit with variation in the number of active nozzle channels.
- 10 21. A compensating circuit as claimed in claim 20, wherein the compensating capacitance arrangement comprises a fixed capacitor having a capacitance substantially one third the total head capacitance with all nozzle channels active.
22. A compensating circuit as claimed in either one of claims 20 or 21, wherein the  
15 compensating capacitance arrangement includes:  
one or more additional capacitances coupled via a switching element or via respective switching elements to the drive terminal; and  
control means for switching additional capacitances to reduce variation in overall capacitance based on the number of active nozzle channels.
- 20
23. A drive circuit for a printhead comprising an adjustable parameter for controlling pulse voltage and a control arrangement for measuring actual nozzle channel voltages and adjusting the parameter based on measurements.
- 25 24. A drive circuit for repetitively energising a printhead (C1) to eject drops of ink, the printhead having multiple nozzle channels each having a respective capacitance, the drive circuit comprising:  
a first switching element (S1) connected to couple a drive connection of the printhead to a first connection of a power supply (V1) via a first inductor (L1) to provide a  
30 charge path for current to charge the capacitance of at least one nozzle channel to a desired operating voltage; and  
a second switching element (S2) connected to couple a drive connection of the printhead to a second connection of the power supply (V1) via a second inductor (L2) to



provide a discharge path for current to discharge the capacitance of said at least one nozzle channel to a desired inter-pulse voltage,

wherein the drive circuit comprises a first circuit element (D1) which permits current flow in only one direction and which is connected in series between the first inductor (L1) and the printhead drive connection, wherein the drive circuit comprises a second circuit element (D2) which permits current flow in only one direction and which is connected in series between the second inductor (L2) and the printhead drive connection, wherein the drive circuit comprises a third switching element (S3) connected between the second inductor (L2) and the first connection of the power supply, wherein the drive circuit comprises a third circuit element (D3) which permits current flow in only one direction and which is connected in series between the second inductor (L2) and the first power supply connection, wherein the drive circuit comprises a fourth switching element (S4) connected between the first inductor (L1) and the second connection of the power supply, wherein the drive circuit comprises a fourth circuit element (D4) which permits current flow in only one direction and which is connected in series between the first inductor (L1) and the second power supply connection, wherein the drive circuit comprises a fifth circuit element (D5) which permits current flow in only one direction and which is connected in series between the second inductor (L2) and the second power supply connection.



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**Claims searched:** 1-15, 24

**Date of search:** 22 March 2012

## Patents Act 1977: Search Report under Section 17

### Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance
X	1,9, at least	JP 2000218782 A (SEIKO EPSON CORP); 08.08.2000; see Abstract Accession No. 2000/561065-52, and all figures.
A	-	GB2480822 A (GLOBAL INKJET SYSTEMS LIMITED) see whole document.
A	-	US 6089689 A (SUZUKI) see whole document.
A	-	JP 2004306395 A (SHARP KK); 04.11.2004; see Abstract Accession No. 2004/789108-78.
A	-	JP 2009166292 A (SEIKO EPSON CORP); 30.07.2009; see Abstract Accession No. 2009/L94904-51.

### Categories:

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

### Field of Search:

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC<sup>X</sup>:

Worldwide search of patent documents classified in the following areas of the IPC

B41J; H01L

The following online and other databases have been used in the preparation of this search report

EPODOC, WPI

### International Classification:

Subclass	Subgroup	Valid From
B41J	0002/045	01/01/2006