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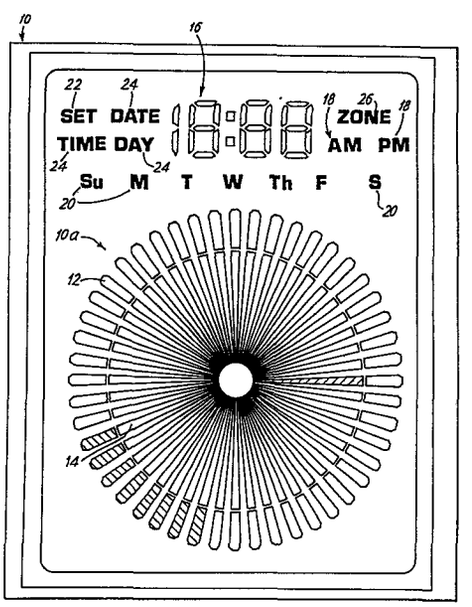
(54) Electronic timeswitch.

(57) The timeswitch comprises a switch actuated in accordance with a pre-set switching program, by microprocessor controlled circuitry, and a display 10 comprising an analogue time display portion 10a. The analogue portion 10a comprises inner and outer concentric circles of actuable indicia 12, 14. In the running mode of the timeswitch, in one configuration, the indicia 14 of the inner circle are sequentially actuated to represent the hour hand of an analogue clock displaying the actual time. The outer indicia 12 are actuated in groups to represent the, switching program «on» times. In the programming mode, the time indicated by the inner indicia 14 may be manually selected, whereafter the state of the switch at that time may be selected. The outer indicia 12 are actuated in sets to represent the switching program being entered. Other configurations of the timeswitch are possible according to the microprocessor software, and some examples are described.



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ELECTRONIC TIMESWITCH

The present invention relates to electronic timeswitches comprising a switch, manually operable input means, control means actuating the switch and storing a switching program, and having a running mode in which the switch is opened and closed at times in accordance with the stored switching program, and a programming mode in which a new switching program may be entered from the input means. Timeswitches of this type may be used, for instance, to turn an industrial heating boiler on and off automatically, at preset times.

Known electronic timeswitches comprise a clock and control circuitry which repeatedly compares the actual time with the stored times for opening and closing the switch, and, at the pre-set switching times, changes the state of the switch. A digital display may be provided which normally displays the actual time but which can be used to display the switching times of the stored program in sequence. The display is also used when entering on and off times. Control is effected by way of an array of push buttons associated with the digits 0 to 9, the days of the week, "ON" and "OFF" and so on. Entering or modifying a timing program or displaying the switching times of the program is rather complex and presents considerable difficulty to a user without a high level of technical awareness.

It is an object of the present invention to provide a timeswitch having an easily readable display which enables the current program to be seen and facilitates reprogramming by clearly showing the program being entered.

A timeswitch according to the present invention is characterised in that it comprises a display having an analogue time display portion controlled by the control means and formed by first and second scales of actuable indicia, and in that, in the running mode, the indicia of the scales are actuated to represent actual time on the first scale and the stored switching program on the second scale, and in that in the programming mode, a time may be manually entered, whereafter the state of the switch at that time may be selected,

and the display represents on one of the scales the program being entered.

One embodiment of the apparatus according to the invention will be described, by way of example, with reference to the accompanying drawings. The embodiment comprises an integrated circuit CPU and may operate in a number of configurations according to the operating program used for the CPU. The apparatus will be described initially when controlling four power circuits, in accordance with respective switching programs.

Subsequently, other modes of operation will be discussed. The embodiment described uses a suitably programmed general purpose CPU but the invention could equally well use a special purpose chip such as those currently available for the specific purpose of time-switching a plurality of circuits.

In the drawings:-

Fig.1 shows the timeswitch display,

Fig.2 is a block diagram of the electronic timeswitch,

Figs.3(a) and 3(b) are a circuit diagram showing the timeswitch in more detail and are assembled as shown in Fig.3,

Fig.4 is the circuit diagram of an array of user input switches, and

Fig.5 is a flow diagram of the CPU software when the timeswitch is in its running mode.

Fig.1 shows the timeswitch display 10 which is a liquid crystal display and has an analogue time display portion 10a comprising two sets of forty-eight display elements 12, 14 which serve as indicia for inner and outer concentric circular scales. Each display element is a partial circular sector, and the two sets of elements 12, 14 are in register. Since there are 48 elements round each scale, they correspond to 1/4 hour incremenets of time.

The display further comprises a digital display portion 16 for displaying the time on the 12-hour clock, and AM and PM symbols 18. Seven symbols 20 are actuable to indicate in which day of the week the displayed time falls. The symbol "SET", 22 is actuable to indicate that the timeswitch is in the mode in which the time may be set, and the symbols 24 are actuable when the date, time or

day has been selected to be set.

The four power circuits are identified as four "zones" and data relating to one selected zone is displayed; the symbol "ZONE", 26 is actuated when a new selection of zone may be made. Four zone annunciators (not shown) indicate to which zone the data displayed relates. The display 10 may be alongside an array of push-button switches whose electrical configuration is described below and the annunciators may be four LED's adjacent symbols "1", "2", "3" and "4" located above the array of switches.

While the timeswitch is running, the sectors 12 provide an analogue display of the switching program of the zone selected for display and sectors 14 show the current time (to the nearest 1/4 hour). Thus the inner sectors 14 are actuated one at a time to act as the hour hand of an analogue clock to display the actual time (in units of a quarter of an hour). The outer sectors 12 display the switching program, being actuated when the zone will be "on", but not when the zone will be "off". Accordingly, the current state of the zone and the stage reached in the program, are clearly displayed. The digital display 16 and the other elements of the display show the actual time more precisely, the day of the week and whether it is AM or PM. A typical display pattern will be an arc of contiguous actuated elements 12 denoting an "ON" period and an arc of non-actuated elements 12 denoting an "OFF" period. Such a pattern and a time of day 3.00 are shown by hatched elements.

During programming, the time indicated by the inner sectors 14 can be manually selected by stepping the hour hand round the display. When an "on" time is entered, the corresponding sector 12 is illuminated, and as the hand is stepped on, successive sectors 12 are actuated, to display the program being entered until an "off" time is selected. Alternative display methods could be used. For instance, the inner sectors 14 could continue to display actual time, while the outer sectors display the selected time by means of a flashing sector and the program being entered, by means of constantly actuated sectors.

A set of switches arranged alongside the display allow the user to perform the following functions:

a) enter a switching program

b) set time of day

c) set day of week

d) review switching program

e) cancel a period of the program in which the switch is closed.

The switches have the following effects. A "SET TIME" switch enables the user, by repeated actuation, to select which item of time data displayed on the digital display portion may be changed when setting time of day. The change is effected by operation of a "TIME ADVANCE" switch which steps on the selected item. The item selected for change flashes. In the solar switch (discussed below) the date and latitude can also be changed.

The day to which a switching program being entered relates is set by a "SET DAY" switch.

A "CANCEL" switch may be operable either to cancel the whole switching program, or a current "on" period of the program.

A "PROGRAM" switch sets the timeswitch into or out of its programming mode, in which a new switching program can be entered.

When in the programming mode, the time displayed by the inner sectors 14 may be advanced by actuation of a "MOVE CURSOR" switch. After selection of a time, a "SET ON/OFF" switch is used to select the start or end of an "on" period, as appropriate. Alternatively, the switch "SET ON/OFF" may be operable in the programming mode for selecting the switch state at each indicated time, rather than to select the start and end of "ON" periods. In this way, every 15 minute period is directly controllable, giving a timeswitch with a quarter-hour switching resolution. Preferably, when the switch is to be used in this way, there is no limit to the number of "ON" periods which may be entered for a day.

Conveniently, a "REPEAT" switch allows the user to program the timeswitch on a selected day with the previous day's program. A "SET ZONE" switch allows the zone displayed to be selected. An "OVERRIDE" switch allows the zone being displayed, if on, to be switched off until the next, programmed switching on time, and vice versa.

Alternatively, the switches "TIME ADVANCE" and "MOVE CURSOR" may be replaced with switches "ADVANCE" and "RETARD" which are used when the timeswitch is running, to increment or decrement time quantities, and in the programming mode to move the cursor in either direction.

Referring to Fig.2, the function of the components of the timeswitch control circuitry will be described. A central processing unit (CPU) 27 provides display data on a data bus BUS1 to two display driver circuits 28 which drive the display 10 by means of buses DBUS1 and DBUS2.

Input means 30 constituted by the switches described above enable the user to control the timeswitch.

The CPU 27 has on-board memory used for storing operating routines. A memory 32 supplements the on-board memory of the CPU and is used for storing switching programs. The memory 32 is connected to the CPU by a two way data and address bus MBUS.

The CPU controls four relays 34. The relays are operated in accordance with the stored switching program to open and close respective power circuit switches 35 corresponding to zones 1 to 4.

Power is supplied to the CPU and other circuits by a power supply unit 37 supplied from the mains and incorporating a battery to ensure program retention in case of mains supply failure. A signal at mains frequency and phase is provided to the CPU by a circuit 36, and pulls the frequency of an oscillator with a crystal 39 into synchronism with the mains.

A counter within the CPU counts mains cycles, or oscillator cycles, and interrupts the CPU when its maximum count is reached. The CPU then updates its actual time clock and resets the counter, in accordance with conventional techniques for handling real time in a microprocessor. A watchdog circuit 38 which is reset by the CPU in each software cycle, interrupts the CPU if the time since it was last reset exceeds a predetermined limit, indicating a malfunction in the CPU or in the operation of the software.

Referring now to Figs. 3(a), 3(b) and 4, the circuitry of the timeswitch will now be described in more detail.

Referring to Fig. 3(a), mains input terminals L and N are connected to the PSU 37 with a fuse FS1 in the live line. Terminal N is also the system earth V_{SS} = OV. The PSU provides a stabilized but non-backed up voltage V_{DD} = 5V and a further stabilized voltage V_{DD1} =5V backed up by a battery B1, which is provided with a charging circuit.

The CPU 27 (IC1) is an 80C49 device whose pins are as follows:-

Pin No.	Name	Description
1	TO	Test Input
2 and 3	XTAL1,2	External crystal connections
4	$\overline{\text{RESET}}$	System reset
5	$\overline{\text{SS}}$	Single step control
6	$\overline{\text{INT}}$	Interrupt request
7	EA	External program memory access
8	$\overline{\text{RD}}$	Data memory read control
9	$\overline{\text{PSEN}}$	External program memory read control
10	$\overline{\text{WR}}$	Data memory write control
11	ALE	External clock
12 - 19	DBO - DB7	Bidirectional port
20	V_{SS}	Earth
21 - 24	P20 - P23	I/O port 2 (low bits)
25	PROG	Control output
26	V_{DD}	+ 5v standby for internal RAM
27 - 34	P10 - P17	I/O port 1
35 - 38	P24 - P27	I/O port 2 (high bits)
39	T1	Event counter input
40	V_{CC}	+ 5v

The description of some pins is rather abbreviated, especially those not used in Fig. 3a. The 80C49 is a member of the 8048 family in which many pins have alternative functions.

These devices are well known in the art and their architecture, signals and instruction set are readily available information (e.g. Osborne "An Introduction to Microcomputers", Vol.2).

DB0 - DB7 is a true bidirectional data bus and I/O port which can also be used as 8 low order address lines. P10 - P17 and P20 - P27 are essentially latched output ports. However a pin at high level can be pulled low to provide data input when the port is read as an input port.

The basic pattern of usage of the three ports is as follows. DB0 - DB7 are provided with pull-up resistors 40 but may be pulled low by the CPU to output data, be pulled low by external signals to input data or be pulled permanently low by links 42 whose function is described below. DB0 - DB3 output or receive four data data RD0 - RD3 to or from the memory 32 (IC2) and receive signals $\overline{KD0}$ - $\overline{KD3}$ from the switches 30. DB7 provides a signal SDI to the display drivers 28 (IC3 and IC4).

P10 to P12 provide keyboard scan signals $\overline{KSCAN0}$ - $\overline{KSCAN2}$ to the switches 30 and also provide signals $\overline{CS0}$ - $\overline{CS1}$ to the drivers 28. Other signals to these drivers are explained below. P20 - P27 provide eight address bits RAM0 - RAM7 to the memory 32 while a ninth bit RAM8 goes to P15. P20 to P23 are furthermore used to output signals $\overline{TRIAC0 - 3}$ for the relays 34 while P24 - P27 output signals DLED0 - 3 for the four annunciator diodes mentioned above.

Line $\overline{SDO}$ provides a serial communication port for the CPU, so that, for instance, another computer can communicate with the timeswitch. In an industrial application, the other computer could be a main computer which controls many different functions in a factory, and which needs to be able to determine the status of the timeswitch and, perhaps, to reprogram the timeswitch. Communication through the port takes place during interrupts in the CPU operating program.

MBUS (Fig.2) comprises RD0 - RD3 and RAM0 - RAM8 in Figs. 3a and 3b.

The memory 32 (IC2) is a 1024 x 4-bit static CMOS RAM, such as the μPD444, whose pins are as follows:-

Pin No.	Name	Description
1 - 7 and 15-17	A_0-A_9	Address inputs
8	$\overline{CS}$	Chip select
9	GND	Earth
10	$\overline{RAMW}$	Write enable
11 - 14	RD0-RD4	Data input/output
18	V_{cc}	+ 5V

This device is well suited for the present application where battery back-up is used to prevent data loss during disruption of the mains supply, because data is retained down to a power supply level of 2V, and if the chip is not selected for a specified length of time, the power requirement is automatically reduced.

The circuit 36 for supplying a mains frequency signal to the CPU comprises a potential divider feeding a signal to the event counter input pin 39 of the CPU 27.

The watchdog circuit 38 described above comprises a capacitor C3 charged through a resistor R_w from the positive supply V_{DD}. A transistor TR3 has its collector connected to the common terminal of the resistor R_w and the capacitor C3, its emitter connected to V_{SS} and its base connected to pin 32 (P15) of the CPU through a coupling capacitor, whereby the CPU may switch on TR3 to discharge C3. This is done once in every normal operating cycle of the CPU software. If a malfunction occurs, and C3 is not discharged within a time set by the values of R_w and C3, the voltage across C3 continues to rise, eventually interrupting the CPU through an inverter 42 (IC5) and diode D5 whose anode is connected to the CPU interrupt pin 6.

For simplicity only one annunciator diode circuit, comprising LED1 (Fig.3b), is shown connected to DLED0 and only a single relay circuit is shown, connected to $\overline{\text{TRIAC0}}$. Like circuits are connected to DLED1 - 3 for LED2 - 4 and are connected to $\overline{\text{TRIAC1 - 3}}$ for the other three relay circuits. The four zone annunciator diodes LED1 - LED4 are used to indicate the zone to which the displayed data relates. The CPU output DLED0 drives LED1 through a pair of inverters 46 providing a signal $\overline{\text{D0}}$.

Bistable relays 34 are used to reduce heat dissipation. Current in the coil of the relay 34 (Fig.3(b)) and hence the state of the relay are controlled by a thyristor SCR1 fired through two inverter circuits IC5 by the CPU output $\overline{\text{TRIAC0}}$ going low. A voltage dependent resistor VD2 may be connected in parallel with the relay coil, but is not necessary if the relay is of the remanence type.

The triacs are always fired at the zero-crossing point of the mains supply to minimise switching currents. The CPU determines the polarity of the mains supply at the time a triac is to be switched on, and waits until the mains crosses zero, before effecting the switching.

When the CPU is addressing the memory 32 (IC2) on RAM0-RAM8, a logic low level on RAM0 would cause spurious triggering of SCR1. To prevent this, the CPU provides a triac holding signal TH at pin 32 when the memory 32 is being addressed. The CPU output TH turns on the transistor TR1 whereby the control terminal of SCR1 is constrained to be at a voltage below the breakdown voltage of the diode D1, since the current which TR1 can sink is greater than that which the inverter IC5 can provide at its output.

BUS1 (Fig.2), through which the CPU communicates to the two display driver circuits 28 is formed by the lines CLK, $\overline{\text{BUSY}}$, $\overline{\text{RESET}}$, $\overline{\text{CS0}}$, $\overline{\text{CS1}}$, CMMD, $\overline{\text{SCLK}}$ and SD1 from the CPU. The drivers are μPD7225 LCD driver/controller integrated circuits described below. Data is sent to the drivers in serial form and each driver 28 incorporates a control unit for directing data flow and decoding high level commands. The drivers are configured by the CPU and

drive the display segments to operate in a duplex mode, that is, the driving signal for an actuated segment has a mark-space ratio of 1:1. This mode of operation places restrictions on the LCD display operating temperature range, but simplifies the display connections. Each driver 28 can drive 32 display segments. One driver also selects one of two back planes in the display, thereby enabling 128 segments to be used.

The pins of the drivers are as follows:-

Pin No.	Name	Description
1	CLK	System clock output
2	$\overline{\text{SYNC}}$	Synchronization port for multichip operation, when all $\overline{\text{SYNC}}$ lines are tied together
3 - 5	V_{LCD1}-V_{LCD3}	LCD bias voltage supply inputs to LCD voltage controller
6	V_{SS}	Earth
7, 33	V_{DD1}	+ 2.7V - 5.5V power supply
8	$\overline{\text{SCLK}}$	Serial clock input
9	SDI	Serial data input (active high) from microprocessor
10	$\overline{\text{CS}}$	Chip select
11	$\overline{\text{BUSY}}$	Busy output. Indicates when circuit ready to receive next data byte
12	CMMD/$\overline{\text{D}}$	Command/data select. Distinguishes input as command or data
13	$\overline{\text{RESET}}$	Reset input
14	NC	No connection
15 - 18	COM_0-COM_3	LCD backplane outputs
19 - 32 34 - 51	S_0 - S_{31}	LCD segment outputs
52	CL_1	System clock input

The commands available allow the CPU to set the driver configuration, to enable or disable a segment decoder, to enable and disable the display, and to cause a segment to blink, for instance. The full set of instructions can be found in data sheets from the manufacturer, NEC Electronics U.S.A. Inc.

The CPU controls the LCD drivers through 6 lines, namely chip select ($\overline{CSO}$, $\overline{CS1}$), command (CMMD/$\overline{D}$), serial clock ($\overline{SCLK}$), serial data input (SDI) and reset ($\overline{RESET}$).

$\overline{RESET}$ is used to initialise the registers of the drivers 28 and to clear their data memories, and to disable the display.

The processor sends data via SDI. Data is clocked in by the rising edge of $\overline{SCLK}$, which is normally high. To simplify the software, the micro is made to do a dummy write to memory, which pulses the $\overline{RAMW}$, i.e. $\overline{SCLK}$ line low, and at the same time, data in the accumulator is output at the BUS port DBO-DB7. Bit 7 (DB7) of the BUS is connected to SDI. Thus only one bit is written to the driver at a time, as required. After each transmission, the accumulator is rotated left once (multiplied by 2), then output to BUS again. In total, this is done 8 times to transmit a data byte (or command byte).

A software routine for the CPU to provide this output to the drivers can be written quite simply, the principle of rotation of data in the accumulator being well known in the microprocessor programming art. Preferably, at each left rotation of the accumulator, the most significant bit is returned to the least significant bit position, so that the original data is returned to the accumulator after eight rotations.

The line CMMD/$\overline{D}$ is used to tell the drivers 28 whether the byte being transmitted is data, which is sent directly to a display memory, or a command, from the available set of commands, which causes appropriate action within the driver.

The lines $\overline{CSO}$ and $\overline{CS1}$ are used to select the driver for which the transmission is intended.

Although two drivers are described controlling a display with two backplanes, the drivers have the facility to drive four planes. Accordingly, a single driver and a display with four back planes could be used.

A transistor TR2, with its associated circuitry, provides reference voltages to the drivers 28 on the driver inpute V_{LCD1}, V_{LCD2} and V_{LCD3} (pins 3, 4 and 5). These reference voltages determine the level of the driving signals applied to the display elements.

The drive characteristics of LCD elements vary with temperature. Accordingly temperature compensation is provided for the reference voltages by the transistor TR2 and a potentiometer POT1. POT1 determines the operating point of the TR2 and hence how much amplification is given to the temperature dependent changes in the base-emitter voltage of TR2, and how the reference voltages change with temperature.

Figs. 3 and 4 indicate how a matrix of switches S1 to S12 is used to provide the manually operable input device 30 for entering a new switch program, for instance. Each of the twelve switches S1 - S12 provides a respective one of the twelve possible connections between one of the lines $\overline{KDO}$, $\overline{KD1}$, $\overline{KD2}$, $\overline{KD3}$ and one of the lines $\overline{KSCAN0}$, $\overline{KSCAN1}$, $\overline{KSCAN2}$.

The switches provide input to the CPU using a well known keyboard scanning technique. $\overline{KSCAN0 - 2}$ are activated in turn and $\overline{KD0 - 3}$ are sensed to ascertain if any switch is closed. The switches are debounced by software in well known manner. When any switch is detected closed, the appropriate software routine is called.

While the timeswitch is running, the CPU repeatedly performs routines with the following functions:

1. Detect input from user.
2. Decode input commands.
3. Transmit data to LCD drivers 28.
4. Service timer counter interrupts and update CPU internal clock.
5. Fetch program data from memory and compare with present time.
6. Fire triacs if appropriate.
7. Retrigger watchdog circuit.

The clock is updated and triacs are fired once every quarter of an hour only.

Fig. 5 is a flow diagram of software suitable for the CPU when the timeswitch is in its running mode.

When the timeswitch is started, the CPU reads the wired links 42 through the bus DB0 - DB7 to determine the timeswitch configuration. The initial values of variables are then set, and any software changes consequent on the configuration are made.

The keyboard is then scanned for the presence of an input which, if present is debounced and decoded. Whether or not data is present, the display is updated.

The CPU then determines whether the state of the switch is to be changed, that is whether the current time is an "ON" or an "OFF" time. If no change of state is required, the CPU reverts to the beginning of the cycle and again scans the keyboard, after retriggering the watchdog. If the status is to be changed, the desired new state is determined and the corresponding triac is fired on the positive or negative mains cycle to turn the relay on or off. The CPU then retriggers the watchdog and returns to scanning the keyboard.

Interrupts are serviced after the display is updated, and return after the operation of determining whether the switch state is to be changed. At an interrupt, the CPU determines whether the interrupt has come from the timer counter or the serial data port.

Dealing with interrupts from the data port forms no part of the invention and the software for doing so is not shown in the flow diagram. When a timer counter interrupt occurs, the timer is stopped, reset to zero and restarted. The stored time values and the display are then updated before returning to the main software routine.

In addition to the mode of operation described above, re-programming of the CPU allows variants of operations. For instance the switch could be used to control a single zone only. Another possibility is a switch which is manufactured to control a number of zones, which number can be increased by connecting a module to the original switch. Naturally, it would be necessary to provide means for alerting the CPU to the presence of the module, so that the CPU operating sequence could be suitably changed. The module may contain additional memory, required for controlling the additional zones.

The timeswitch can be used with mains frequencies of 50 Hz or 60 Hz as a timebase or with a crystal oscillator, in accordance with principles well known in themselves.

The timeswitch could be operated as a solar timeswitch, in which part of the program is related to the time of sunset or sunrise and therefore varies through the year.

For configuring the CPU, each of the resistor links 42 is connected to the collector of a transistor TR3 whose emitter is connected to V_{SS} and whose base is connected to $\overline{\text{RESET}}$. The CPU when turned on, reads the diode links by turning TR3 on and reading the inputs DBO-DB7. Thereafter, TR3 is turned off and the BUS can be used as normal.

In configuring the CPU, one of the links 42 determines whether or not the switch is a solar timeswitch. A second Link determines whether the CPU uses the crystal time base only or locks to mains frequency. A third Link determines whether BST changeover is to occur.

In the solar timeswitch, the remaining five links set the latitude of operation. Thirty-two separate latitudes may be selected.

In a non-solar timeswitch a fourth link sets the time-switch to be a Tariff switch and a fifth link sets the number of zones to be used. The remaining threelinks are not used.

The timeswitch has been described with a 12 hour display, but could be arranged to display the whole 24 hour program all the time. The display described would then have a resolution of only half an hour, but clearly the display could be changed, with concomitant changes in software and, if necessary, the number of LCD driver circuits, to provide a 24 hour display with quarter of an hour resolution.

CLAIMS

1. An electronic timeswitch comprising a switch (35), manually operable input means (30), control means (27,32, 34) actuating the switch (35) and storing a switching program, and having a running mode in which the switch (35) is opened and closed at times in accordance with the stored switching program, and a programming mode in which a new switching program may be entered from the input means (30), characterised in that it comprises a display (10) having an analogue time display portion (10a) controlled by the control means (27,28) and formed by first and second scales (14,12) of actuable indicia, and in that, in the running mode, the indicia of the scales (12,14) are actuated to represent actual time on the first scale (14) and the stored switching program on the second scale (12), and in that in the programming mode, a time may be manually entered, whereafter the state of the switch (35) at that time may be selected, and the display (10) represents on one of the scales (12,14) the program being entered.

2. An electronic timeswitch according to claim 1, characterised in that the scales (12,14) of actuable indicia are arranged in inner and outer concentric circles.

3. An electronic timeswitch according to claim2, characterised in that, in the running mode, the indicia of the first scale (14) are sequentially actuated, to represent the hour hand of an analogue clock face.

4. An electronic timeswitch according to claim 2 or 3, characterised in that, in the running mode, the indicia (12) of the second scale are actuated in groups, to indicate periods of the stored switching program during which the switch (35) is closed.

5. An electronic timeswitch according to claim 2, 3 or 4, characterised in that the first and second scales (14,12) are the inner and outer scales respectively.

6. An electronic timeswitch according to claim 2, characterised in that in the programming mode, the indicia of one scale (14) are actuated to represent the hour hand of an analogue clock face displaying the manually entered time.

7. An electronic timeswitch according to claim 2 or 6, characterised in that, in the programming mode, the indicia of one scale (12) are actuated in groups, to indicate periods of the switching program being entered during which the switch (35) is to be closed.

8. An electronic timeswitch according to claim 6 and 7, characterised in that, in the programming mode, an hour hand is represented by the inner scale (14) and the periods during which the switch (35) is to be closed are represented on the outer scale (12).

9. An electronic timeswitch according to any of the above claims, characterised in that the display (10) further comprises a digital time display device (16).

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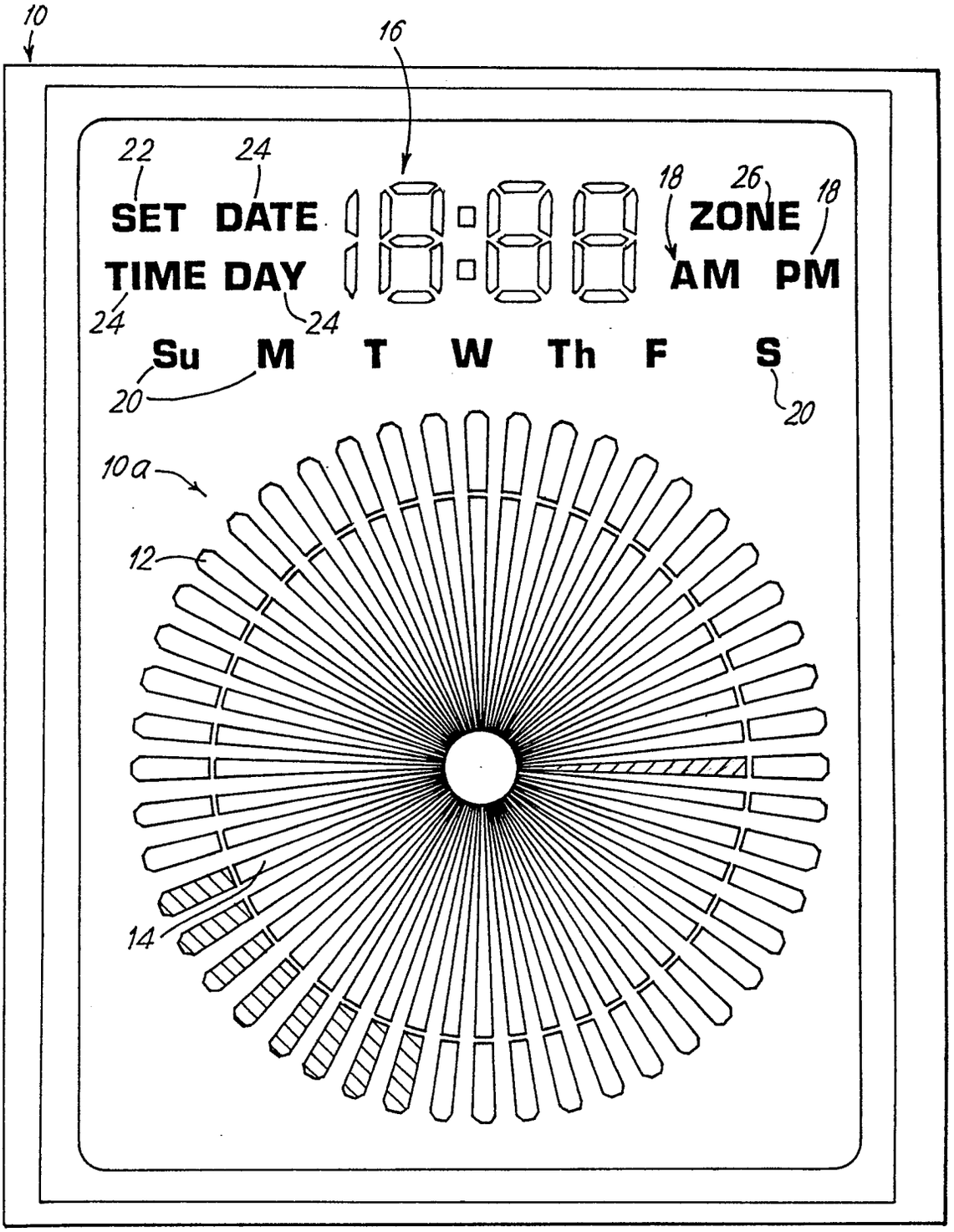

FIG.1

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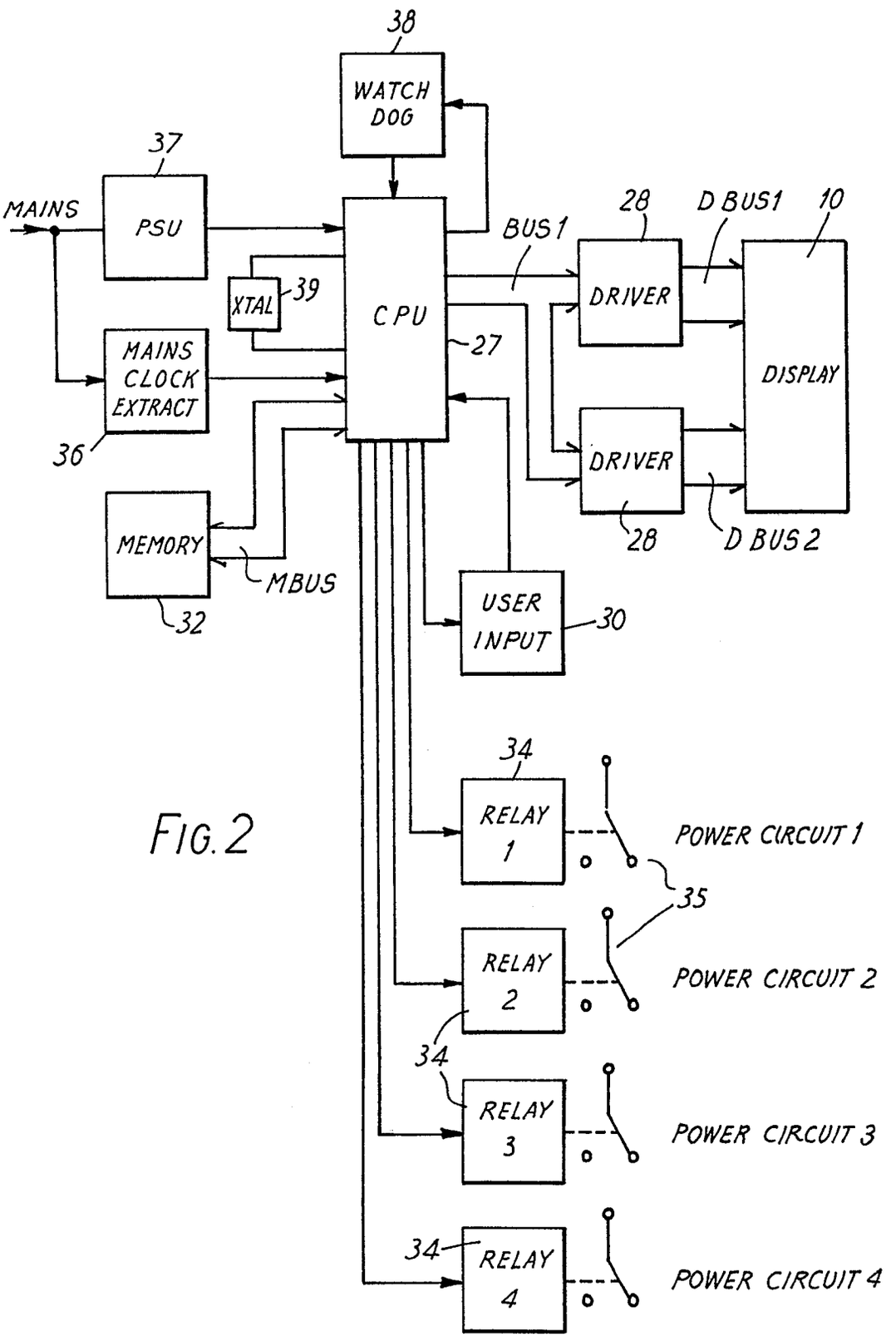

FIG. 2

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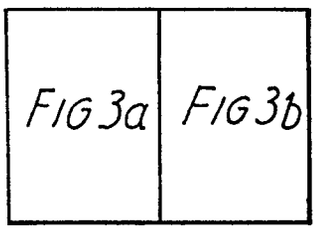

FIG.3

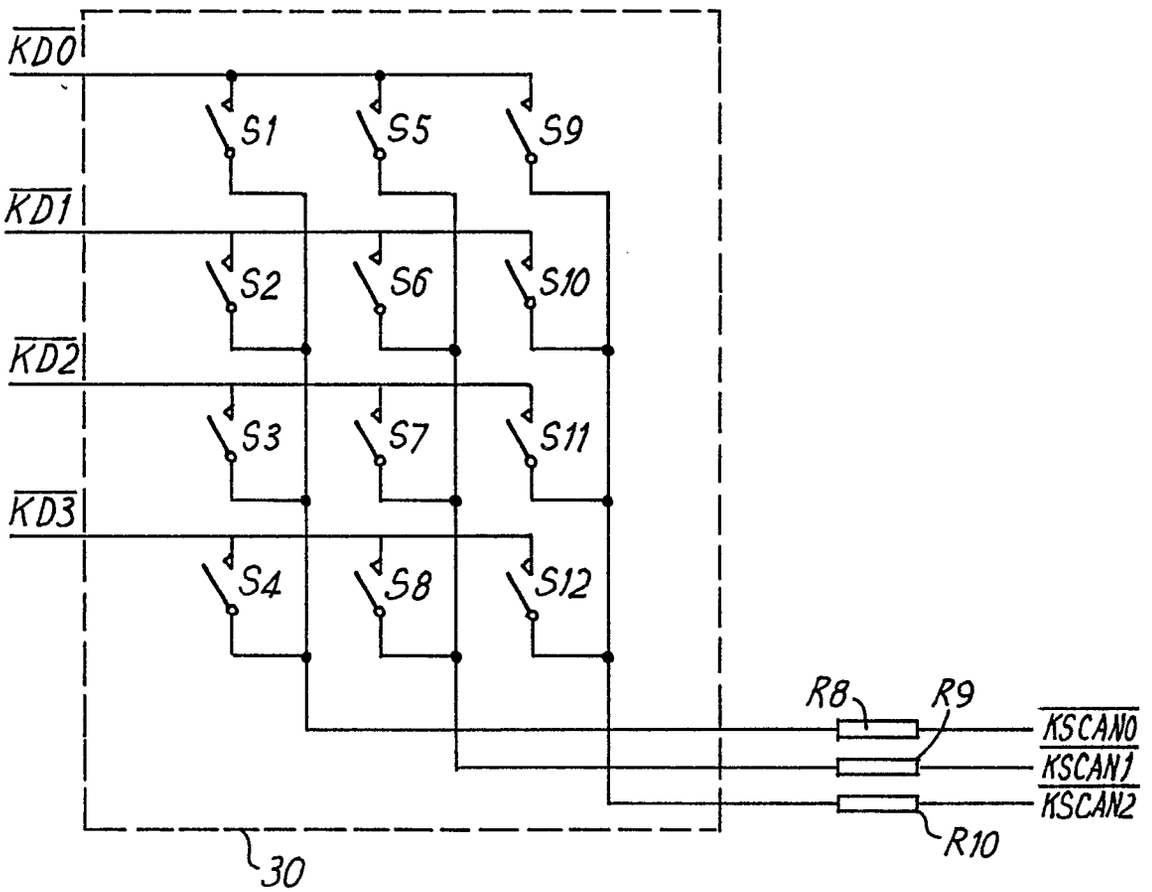

FIG.4

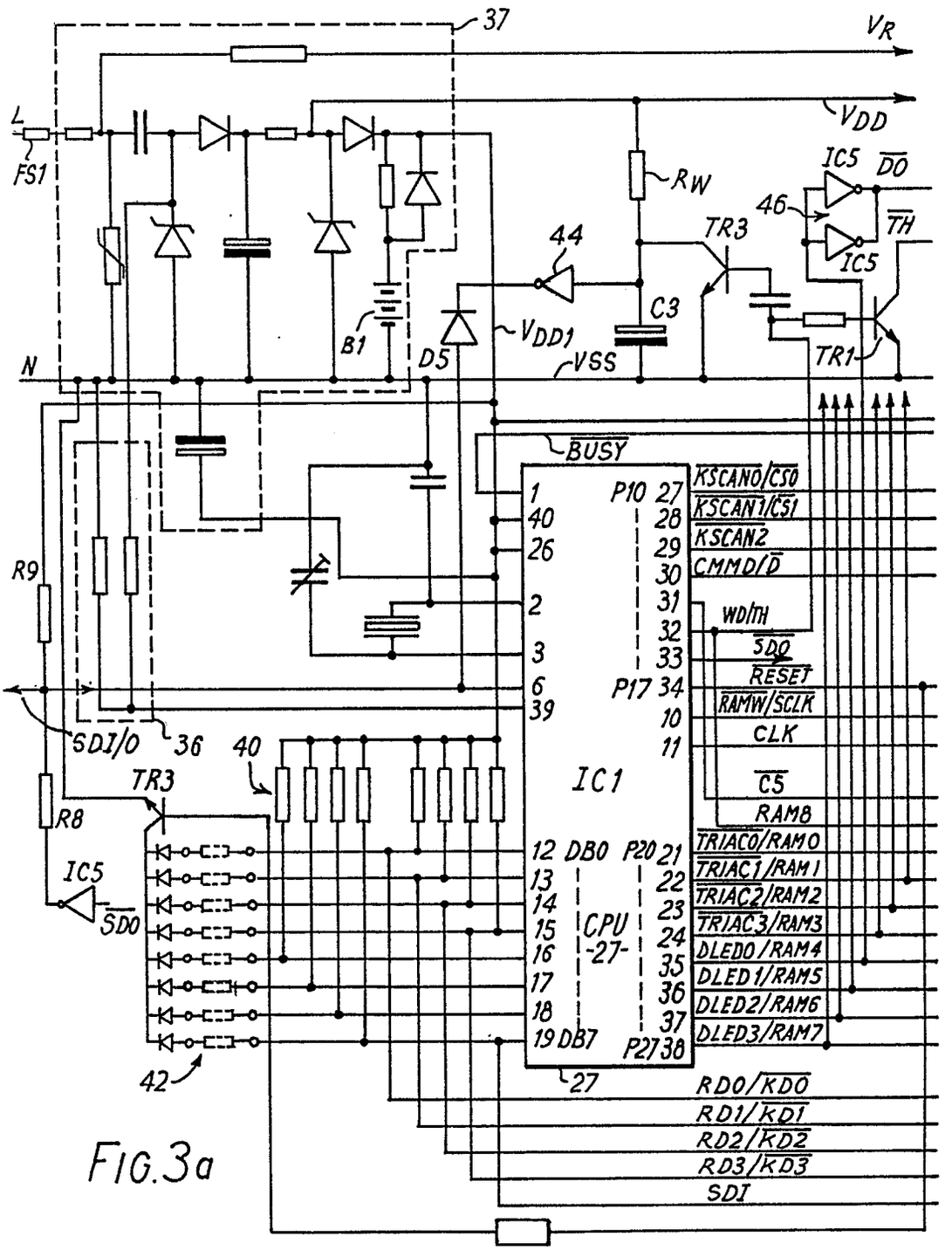
37
VR
L
FS1
VDD
RW
IC5
DO
46
TH
TR3
44
C3
B1
D5
VDD1
VSS
TR1
N
BUSY
R9
SDI/O
36
40
TR3
R8
IC5
SDO
42
IC1
P10
P17
P20
P27
DB0
DB7
CPU
-27-
KSCAN0/CS0
KSCAN1/CS1
KSCAN2
CMMD/D
WDITH
SDO
RESET
RAMW/SCLK
CLK
C5
RAM8
TRIAC0/RAM0
TRIAC1/RAM1
TRIAC2/RAM2
TRIAC3/RAM3
DLED0/RAM4
DLED1/RAM5
DLED2/RAM6
DLED3/RAM7
RD0/KD0
RD1/KD1
RD2/KD2
RD3/KD3
SDI

FIG.3a

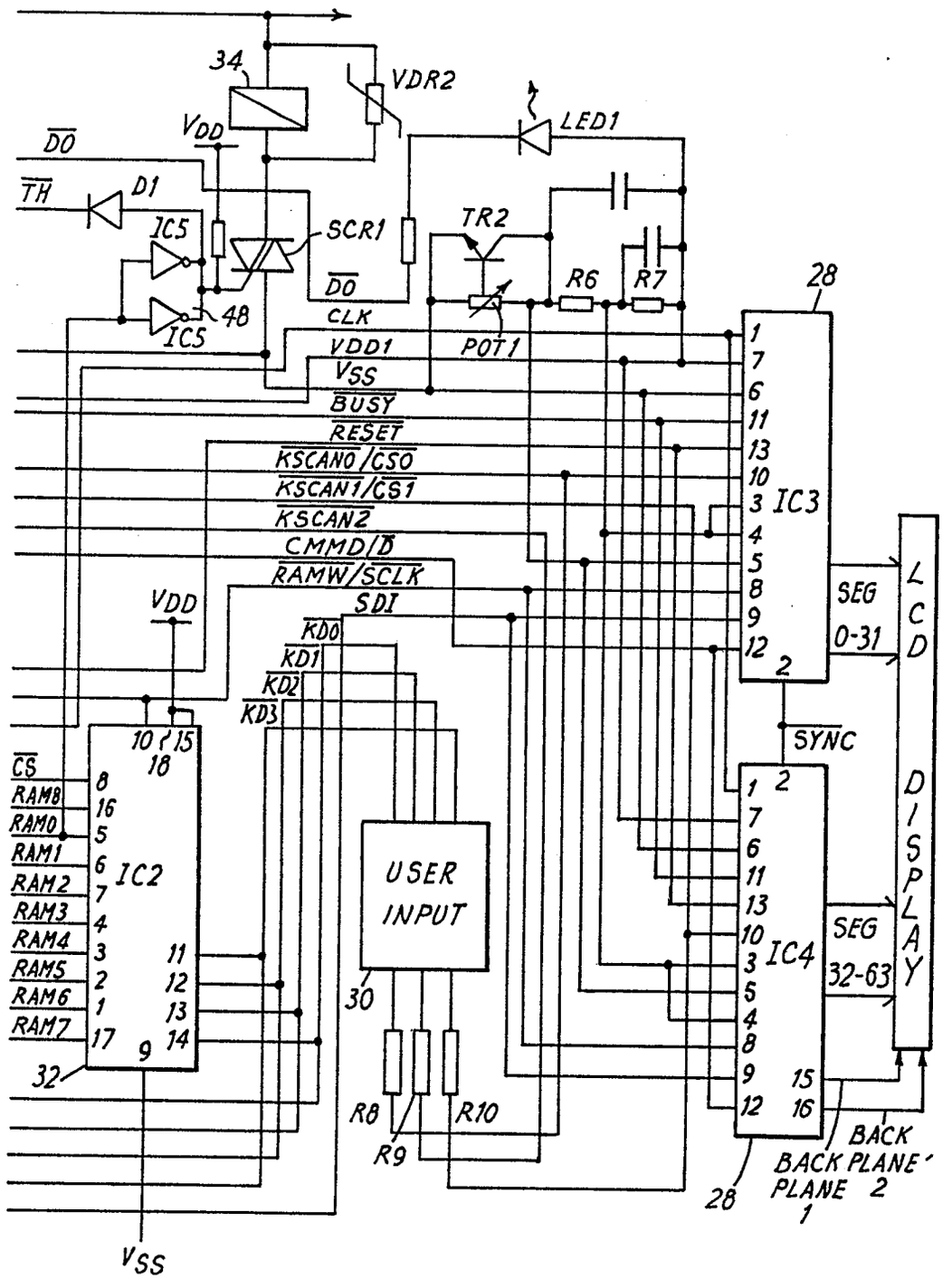
34
VDR2
LED1
VDD
DO
TH
D1
IC5
SCR1
TR2
R6
R7
28
48
CLK
VDD1
POT1
VSS
BUSY
RESET
KSCAN0/CS0
KSCAN1/CS1
KSCAN2
CMMD/D
RAMW/SCLK
SDI
KD0
KD1
KD2
KD3
IC3
SEG
0-31
LCD
SYNC
IC2
CS
RAM8
RAM0
RAM1
RAM2
RAM3
RAM4
RAM5
RAM6
RAM7
USER
INPUT
30
IC4
SEG
32-63
DISPLAY
R8
R9
R10
BACK
PLANE 2
BACK
PLANE 1
32
VSS

FIG. 3b

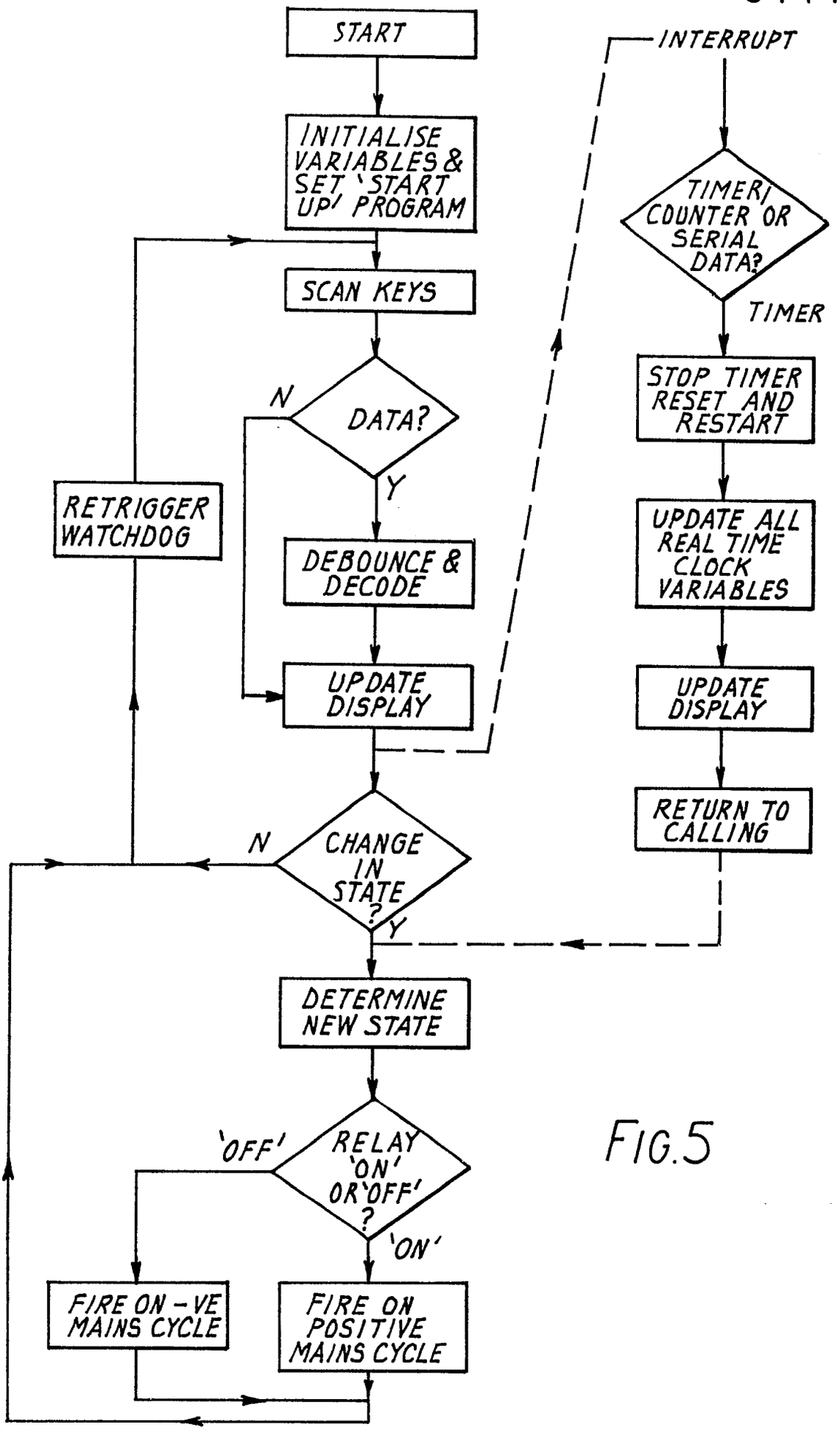
START
INITIALISE VARIABLES & SET 'START UP' PROGRAM
SCAN KEYS
DATA?
N
Y
RETRIGGER WATCHDOG
DEBOUNCE & DECODE
UPDATE DISPLAY
CHANGE IN STATE ?
N
Y
DETERMINE NEW STATE
RELAY 'ON' OR 'OFF' ?
'OFF'
'ON'
FIRE ON -VE MAINS CYCLE
FIRE ON POSITIVE MAINS CYCLE
INTERRUPT
TIMER/ COUNTER OR SERIAL DATA?
TIMER
STOP TIMER RESET AND RESTART
UPDATE ALL REAL TIME CLOCK VARIABLES
UPDATE DISPLAY
RETURN TO CALLING

FIG.5