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ADJUSTABLE COUNTER

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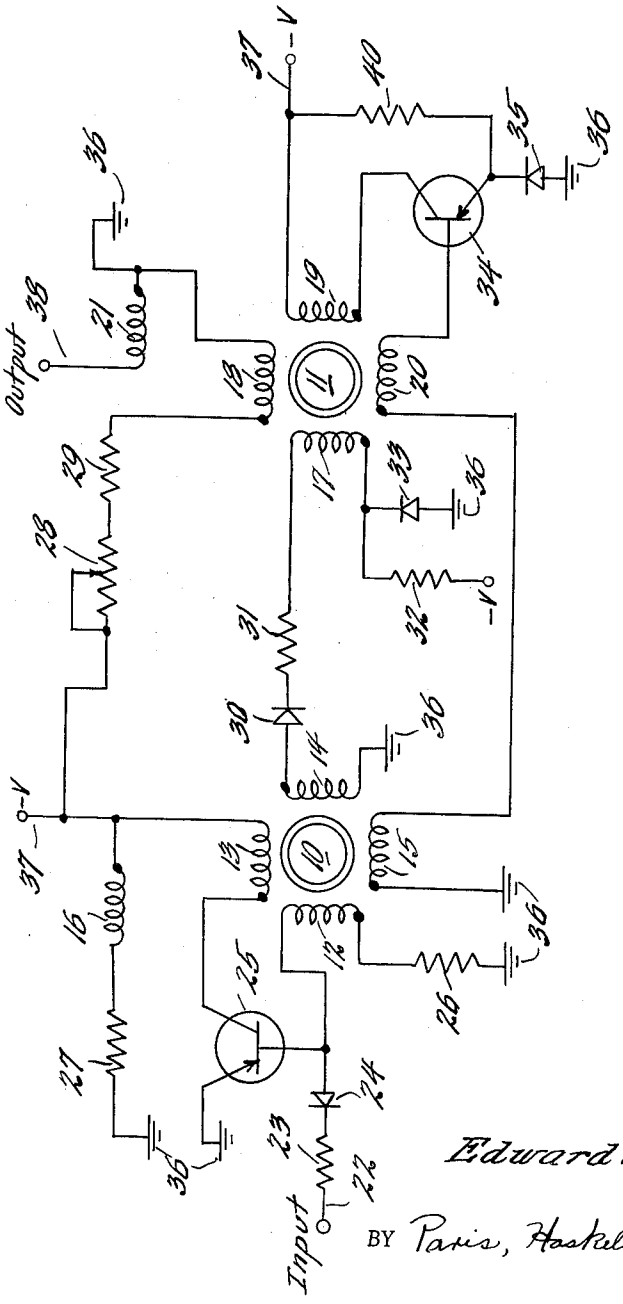

INVENTOR

Edward W. Young,

BY Paris, Haskell and Levine

ATTORNEY

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ADJUSTABLE COUNTER

Edward W. Young, Philadelphia, Pa., assignor, by mesne assignments, to United Aircraft Corporation, a corporation of Delaware

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This invention generally relates to improvements in predetermined counters or adjustable frequency dividers, and is particularly concerned with such devices employing square-loop magnetic cores whose saturation from one condition to the reverse condition may be varied in a discrete number of incremental steps.

Adjustable counters or like circuitry employing magnetic cores that are incrementally saturable in steps by the application of impulses thereto are well known in the art.

With the development of improved core materials having substantially square hysteresis characteristics, such devices have become more accurate and practical with the result that a relatively large number of such circuits are disclosed in the patented and published literature. The availability of transistors, diodes, and other circuit elements in miniature sizes has also provided renewed stimulus to the further development of such magnetic counters and frequency dividers, enabling such counters to be made extremely small and compact and to be variably combined as a series of tiny modules to perform multiple digit pulse counting and like functions.

According to the present invention, there is provided an improved adjustable pulse counter of this type having fewer components and, therefore, being less expensive and smaller in size than prior art devices yet being compatible in performance therewith. In one preferred embodiment, the counter is comprised of a pair of saturable cores, each having a series of energizing and output windings thereon. The first of such cores functions as a pulse quantizer to produce a pair of uniform output impulses in response to each incoming pulse to be counted. One of these output pulses is applied to the second core with a much greater volt-time area than the other and, therefore, serves to increase the degree of saturation of the second core in discrete steps until the core becomes fully saturated in the direction of such pulses after receiving a predetermined number thereof.

The second of such quantized pulses is applied to the core simultaneously with the first pulses but in opposite polarity and, therefore, is dominated by the larger first pulse until such time as the core becomes fully saturated in the direction of the first pulses. Upon the second core becoming fully saturated, the second pulse functions to actuate a resetting means thereby to automatically restore the second core to its initial polarity of saturation and to provide an output or carry over pulse to the next stage. By the use of two such quantizing pulses for each of the input pulses, the circuitry of the present invention provides a savings in the number of components needed, enabling a corresponding reduction in the size, weight, and cost of the adjustable counting unit. To enable the second core to store an adjustable number of impulses, for predetermined counting or frequency dividing purposes, the preferred circuit also provides means for adjustably varying the initial degree of saturation of the second core, whereby it may store a predetermined adjustable number of such pulses before reaching saturation.

It is accordingly a principal object of the present invention to provide an improved magnetic pulse counter of this type having fewer components and, therefore, being less expensive and smaller in size than known prior art devices yet being compatible in performance therewith.

A further object is to provide such a device that is

automatically resettable after storing a predetermined number of pulses and may be easily varied to store different numbers of pulses over a wide range.

Another object is to provide such a device having a minimum number of electrical components whereby the device may be packaged in extremely small individual plug-in modules approximating the size of a match box or smaller, and a number of such tiny modules may be cascaded or otherwise assembled in varying arrangements to provide a multistage predetermined counter or variable frequency divider having a wide range of adjustment.

Other objects and many additional advantages will be more readily understood by those skilled in the art after detailed consideration of the following specification taken with the accompanying drawings, wherein:

FIG. 1 is an electrical schematic drawing illustrating one preferred embodiment of the invention.

Referring now to FIG. 1 for a detailed consideration of one stage of the preferred counter embodiment, there is shown a magnetic circuit comprised of two toroidally shaped miniature magnetic cores **10** and **11**, each being of magnetic material having substantially square hysteresis loop characteristics.

The first core **10** and its associated circuitry function as a quantizer to produce a pair of output impulses of constant volt-time area in response to each incoming impulse to be counted that is received over input line **22**. The first of said quantized output impulses is produced by output winding **14** and the second of such quantized output pulses is produced by output winding **15**. The second toroidal core **11** and its associated circuitry functions as a pulse storage counter in response to each of the quantized pulses to incrementally vary its degree of saturation in a series of discrete steps, whereby after a predetermined number of such pulses are received, the condition of saturation of the core **11** has been reversed from its initial condition and the core becomes fully saturated in the opposite direction.

For coupling the quantized pulses from the first core **10** to the second core **11**, the first series of such pulses being produced by output winding **14** of the first core **10** are directed unidirectionally through diode **30** and current limiting resistor **31** to an input winding **17** on the second core **11**. Each of these pulses produces a flux change in the core **11** thereby incrementally and successively changing the degree of saturation of core **11** along its hysteresis curve.

The second series of quantized pulses being produced at output winding **15** of the first core **10** are simultaneously directed to a winding **20** on the second core **11** and are applied to the core **11** in opposition to the first series of quantizing impulses. The pulses of the second series are also applied with considerably less volt-time area to the core **11** than are the first series. Consequently, assuming that the core **11** has not become fully saturated by the application of the larger quantized pulses of the first series, the flux change being produced in the core **11** by the larger impulses at winding **17** dominates the opposite polarity pulses received at winding **20**. In one preferred manner of winding the coils **17** and **20**, the windings **17** and **20** are both wound on the core **11** in the same direction but the windings **14** and **15** are wound on the quantizer core **10** in the opposite direction, whereby the core **11** is oppositely energized by the two quantized pulses, in the manner as described. As will be evident, as the specification proceeds, other manners of winding the cores may also be employed with the same result.

Thus, in response to each of the incoming impulses being received over input line **22**, which incidentally may be of random waveform and timing, the degree of saturation of the core **11** is uniformly increased by one step or count along its hysteresis curve until such time as the

core 11 becomes fully saturated in a reverse polarity. Upon the core 11 becoming fully saturated after storing a predetermined number of pulses, the next large quantized pulse being received at winding 17 in response to an incoming impulse fails to produce an appreciable flux change in the core 11 due to the fact that the core is now fully saturated in the same direction. As a result, the induced voltage produced across winding 20 is made very small and fails to dominate the opposite polarity quantizing pulse being received from winding 15 which thereupon may pass through the winding 19 and to a switching circuit, including transistor 34.

The switching circuit serves to automatically reset the counting core 11 to its initial condition of saturation and thereby condition the core 11 to again count a predetermined number of cycles or impulses, and additionally, the resetting circuit provides an output pulse over line 38 for transfer to the next succeeding stage (not shown) or to a suitable load circuit (not shown). Returning to the drawing, the resetting circuit comprises a switching transistor 34 having its base electrode being connected to the one terminal of winding 20 and having its collector electrode being connected in series with a reset winding 19 on the core 11 to a negative voltage source of potential, generally indicated at 37. The emitter electrode of switching transistor 34 is connected to ground through a reversely poled diode 35, and it is biased from the negative source of supply 37 through a biasing resistor 40. In operation, after the core 11 has become fully saturated in the direction of the first series of quantizing pulses, the next succeeding quantizing pulses received from the core 10 permits the passage of a negative quantizing pulse through the winding 20 to the base electrode of switching transistor 34. This negative impulse functions to trigger the transistor 34 into operation permitting current flow through the reset winding 19 and thereupon providing an opposite flux change through the core 11. This opposite change of flux through the core 11 induces a feedback voltage in the winding 20 in such direction as to maintain the transistor 34 conducting whereby current flow through the winding 19 is continued until the core 11 becomes fully saturated in the reverse direction to its initial condition thereby resetting the core 11, as desired. Upon the core being reset, a continued current flow through winding 19 does not induce a further sufficient flux change through the core 11 to induce a voltage in winding 20 whereupon the transistor 34 is extinguished to prevent further current flow through winding 19. An additional winding 21 on the core 11 is provided as an output winding whereby during the resetting of the core 11 as described, an output pulse is produced in winding 21 and is directed over line 38 to the next succeeding stage or load (not shown).

Thus, in the manner described, each of the incoming impulses over line 22 produces a discrete pulse that is stored on the counter core 11 thereby to progressively accumulate the counts until the core 11 becomes fully saturated in a reverse direction. Upon the core 11 becoming fully saturated, the next incoming impulses over line 22 initiates the passage of a negative going impulse through winding 20 on the core 11, which negative going impulse triggers the resetting transistor 34 and resetting coil 19 to reset the core 11 to its initial condition of saturation and, in addition, the resetting operation produces an output pulse in winding 21.

For adjusting the number of pulses that may be counted or accumulated on the core 11, the core 11 is provided with a biasing winding 18 having one terminal thereof grounded at 36 and the other terminal thereof connected in series with an adjustable resistor 28 and fixed resistor 29 to the negative source of voltage supply at 37. A variable biasing current is, therefore, directed through the winding 18 in the same direction as the quantized impulses through winding 17 thereby to bias the core 11 upwardly on its saturation curve in the same direction as the quantized impulses received over winding 17. In this manner, the initial condition of the core 11 may be adjustably varied in such manner that the core may count a larger or smaller number of quantized impulses before reaching saturation, thereby to enable adjustment of the number of impulses that may be stored on the core 11.

For producing the quantized impulses, the core 10 is provided with a series of energizing and output windings, together with a switching transistor 25, that function to switch the core from one polarity of saturation to its opposite polarity of saturation upon receiving each of the incoming impulses over input line 22. Referring to the drawing, for a more detailed understanding of this stage, the incoming impulses received over input line 22 are directed through a diode 24 and a current limiting resistor 23 to an energizing coil 12 wound on the core 10. The polarity of each of these impulses is such as to render the switching transistor 25 conducting upon the receipt of each incoming pulse and thereby to permit current flow from the negative source of supply 37 and through a winding 13 and through the emitter-collector electrodes of the switching transistor 25. The current flow through the winding 13 induces a feedback potential in winding 12 in such direction as to maintain the switching transistor 25 conducting, thereby to maintain the switching transistor 25 conducting after the decay of the initial impulse over line 22. The feedback between windings 13 and 12 is progressive such that current continues to flow through winding 13 until the core 10 becomes fully saturated in a reverse direction. Upon reaching saturation, a continued current flow through winding 13 does not produce an appreciable change of flux to induce a feedback voltage in winding 12 whereupon the transistor 25 is extinguished to prevent further current flow through the winding 13. Thus, in response to each of the incoming impulses over line 22, the switching transistor 25 is rendered conducting and functions in conjunction with the feedback windings 12 and 13 in such manner as to reverse the direction of saturation of the core 10. As the core 10 is being saturated in a reverse direction in the manner described, the first output quantizing impulse is induced in winding 14 and directed to the second core 11 in the manner described above, and similarly a second quantized voltage pulse is induced in winding 15 and directed to the core 11 in the manner as described above. For resetting the core 10 to its initial condition after each pair of quantizing impulses have been produced in windings 14 and 15, a reset winding 16 is also provided on the core 10 and is adapted to be continuously energized by a negative source of voltage potential at 37 through a current limiting resistor 27. The current flow through the reset winding 16 is sufficient to restore the core 10 to its initial condition of saturation within a predetermined time interval after the quantizing pulses have been produced, but the magnetizing force produced by winding 16 is considerably less than the magnetizing force being produced by the winding 13 during the production of the saturating impulse. Consequently, the saturation of the core 10 is reversed in the manner as described to produce the quantizing output impulses in windings 14 and 15, and only after the termination of such pulses is the core 10 reset to its initial condition of saturation.

Although but one preferred embodiment of the invention has been illustrated and described, many changes may be made by those skilled in the art without departing from the spirit and scope of this invention. Accordingly, this invention should be considered as being limited only by the following claims appended hereto.

What is claimed is:

1. In an adjustably variable pulse counter, a saturable core having a substantially square hysteresis loop characteristic and a plurality of windings, means for independently and simultaneously applying to said windings first and second impulses producing opposite polarity effects on said core for each of the counts to be accumulated, with each of the first impulses being larger than

those of the second impulses, whereby when said core is not fully saturated, the flux change therein resulting from the first impulse dominates that received from the second impulse, said first impulses each having insufficient volt-time area to fully saturate said core, a switching circuit responsive to the next succeeding second impulse being received after said core has become fully saturated by said first impulses to apply to said core a resetting impulse having the polarity of said second impulses and being sufficient to reset the core to its initial condition, and means for adjustably biasing said core in the first direction.

2. In the variable pulse counter of claim 1, said first and second pulse applying means each including a separate winding adapted to be independently energized by a different one of said first and second impulses responsively to each of the counts to be accumulated, with said first impulses being greater in volt-time area than the second impulses and with said first and second impulses being applied to said core in opposition.

3. In a predetermined impulse counter comprised of two stages, the first stage being responsive to each incoming impulse to be counted to simultaneously produce a pair of quantized output impulses, with one such output impulse being larger than the other, and the second stage comprising a magnetic core adapted to be varied from one polarity of saturation to the opposite polarity of saturation in response to a predetermined number of the larger of said quantized impulses, a pair of windings on said second core, means for simultaneously energizing each of said windings on said second core with a different one of said quantized output impulses from the first core, resetting means in circuit with that one of the windings on the second core receiving the smaller of said quantized impulses for resetting said second core to its initial condition of saturation after said core has become fully saturated by the application of a predetermined number of said larger quantized impulses, and means for adjustably biasing the degree of saturation of the second stage core to adjustably vary the predetermined number of quantized pulses required to saturate the second stage core.

4. In an adjustable counter having a quantizer circuit for simultaneously providing a pair of independent output pulses of constant volt-time area responsive to each input pulse to be counted and a saturable core having a pair of separate windings, each simultaneously receiving a different one of said quantized pulses, said pulses being applied to said core in opposite phase relationship with one being larger than the other but with the larger pulse having insufficient volt-time area to saturate said core, an adjustable biasing means for variably biasing said core in the direction of said larger pulse, and a unidirectional switching means responsive to the other of said quantizing pulses only after said core has been fully saturated in a direction opposite to that of the other pulse to reset said core.

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BERNARD KONICK, *Primary Examiner.*

IRVING L. SRAGOW, *Examiner.*

R. J. McCLOSKEY, M. S. GITTES, *Assistant Examiners.*