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- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

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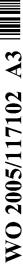
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(54) Title: LOW-VOLTAGE SINGLE-LAYER POLYSILICON EEPROM MEMORY CELL

(57) Abstract: The present invention is an electronic memory cell (200) and a method for the cell's fabrication comprising a first transistor (201) configured to be coupled to a bit line. The first transistor (201) has an essentially zero voltage drop when activated and is configured to control an operation of the memory cell (200). A second transistor (203) is configured to operate as a memory transistor and is coupled to the first transistor (201). The second transistor (203) is further configured to be programmable with a voltage about equal to a voltage on the bit line.



## INTERNATIONAL SEARCH REPORT

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PCT/US05/16267

A. CLAS	SSIFICATION OF SUBJECT MATTER <b>H01L 21/00</b> ( 2006.01), <b>21/8238</b> ( 2006.01), <b>21/8234</b> 2006.01), <b>29/76</b> ( 2006.01), <b>29/788</b> ( 2006.01), <b>29/00</b> (		06.01). <b>21/28</b> (		
USPC: According to	438/164,223,151,157,210,238,323,257,258,574,57 International Patent Classification (IPC) or to both na	75;257/314,315,316,318,501 ational classification and IPC			
B. FIEL	DS SEARCHED				
	cumentation searched (classification system followed 38/164,223,151,157,210,238,323,257,258,574,575;2				
Documentation	on searched other than minimum documentation to the	extent that such documents are included in	n the fields searched		
	ta base consulted during the international search (nam	e of data base and, where practicable, sear	cch terms used)		
	UMENTS CONSIDERED TO BE RELEVANT				
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Y	WOLF, S. Silicon Processing for the VLSI Era, Vol. 1. Lattice Press: Sunset Beach, CA, 2000, pp. 225-226 and 830-831.		3,7,16,18,19		
Further	documents are listed in the continuation of Box C.	See patent family annex.			
* Special categories of cited documents: "T" later document published after the international filing date or pri					
date and not in conflict with the application but cited to understand to document defining the general state of the art which is not considered to be of particular relevance date and not in conflict with the application but cited to understand to principle or theory underlying the invention					
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## INTERNATIONAL SEARCH REPORT

International application No. PCT/US05/16267

tegory *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim N	
Х	US 6,022,770 (HOOK et al) 8 February 2000 (08.02.2000), Figure 1.	16	
Y	WOLF, S. Silicon Processing for the VLSI Era, Vol. 1. Lattice Press: Sunset Beach, CA, 2000, pp. 225-226 and 830-831.	17	
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X	US 6,022,770 (HOOK et al) 8 February 2000 (08.02.2000), Figure 1.	1,4,5,8,20	
Y	US 6,346,457 (KAWANO) 12 February 2002 (12.02.2002), column 3, line 60 to column 4, line 1. —	6	
<b>x</b> ·	US 6,022,770 (HOOK et al) 8 February 2000 (08.02.2000), Figure 1.		
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