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**Declarations under Rule 4.17:**

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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(54) Title: LOW-VOLTAGE SINGLE-LAYER POLYSILICON EEPROM MEMORY CELL

(57) Abstract: The present invention is an electronic memory cell (200) and a method for the cell's fabrication comprising a first transistor (201) configured to be coupled to a bit line. The first transistor (201) has an essentially zero voltage drop when activated and is configured to control an operation of the memory cell (200). A second transistor (203) is configured to operate as a memory transistor and is coupled to the first transistor (201). The second transistor (203) is further configured to be programmable with a voltage about equal to a voltage on the bit line.



WO 2005/117102 A3

# INTERNATIONAL SEARCH REPORT

International application No.

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## A. CLASSIFICATION OF SUBJECT MATTER

IPC: **H01L 21/00**( 2006.01),**21/8238**( 2006.01),**21/8234**( 2006.01),**21/336**( 2006.01),**21/8228**( 2006.01),**21/28**( 2006.01),**29/76**( 2006.01),**29/788**( 2006.01),**29/00**( 2006.01)

USPC: 438/164,223,151,157,210,238,323,257,258,574,575;257/314,315,316,318,501

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/164,223,151,157,210,238,323,257,258,574,575;257/314,315,316,318,501

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6,022,770 (HOOK et al) 8 February 2000 (08.02.2000), Figure 1.	1,4,5,8,20
X	US 6,022,770 (HOOK et al) 8 February 2000 (08.02.2000), Figure 1.	1,4,5,8,20
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Y	US 5,904,524 (SMOLEN) 18 May 1999 (18.05.1999), column 1, lines 48-62.	2
X	US 6,022,770 (HOOK et al) 8 February 2000 (08.02.2000), Figure 1.	1,4,5,8,20
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Y	WOLF, S. Silicon Processing for the VLSI Era, Vol. 1. Lattice Press: Sunset Beach, CA, 2000, pp. 225-226 and 830-831.	3,7,16,18,19

☒ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

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## C. (Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X ---	US 6,022,770 (HOOK et al) 8 February 2000 (08.02.2000), Figure 1.	16 -----
Y	WOLF, S. Silicon Processing for the VLSI Era, Vol. 1. Lattice Press: Sunset Beach, CA, 2000, pp. 225-226 and 830-831.	17
	US 6,346,457 (KAWANO) 12 February 2002 (12.02.2002), column 3, line 60 to column 4, line 1.	
X ---	US 6,022,770 (HOOK et al) 8 February 2000 (08.02.2000), Figure 1.	1,4,5,8,20 -----
Y	US 6,346,457 (KAWANO) 12 February 2002 (12.02.2002), column 3, line 60 to column 4, line 1.	6
X ---	US 6,022,770 (HOOK et al) 8 February 2000 (08.02.2000), Figure 1.	-----
Y	US 2004/0001373 A1 (LIAW et al) 1 January 2004 (01.01.2004), Fig. 1.	9-15