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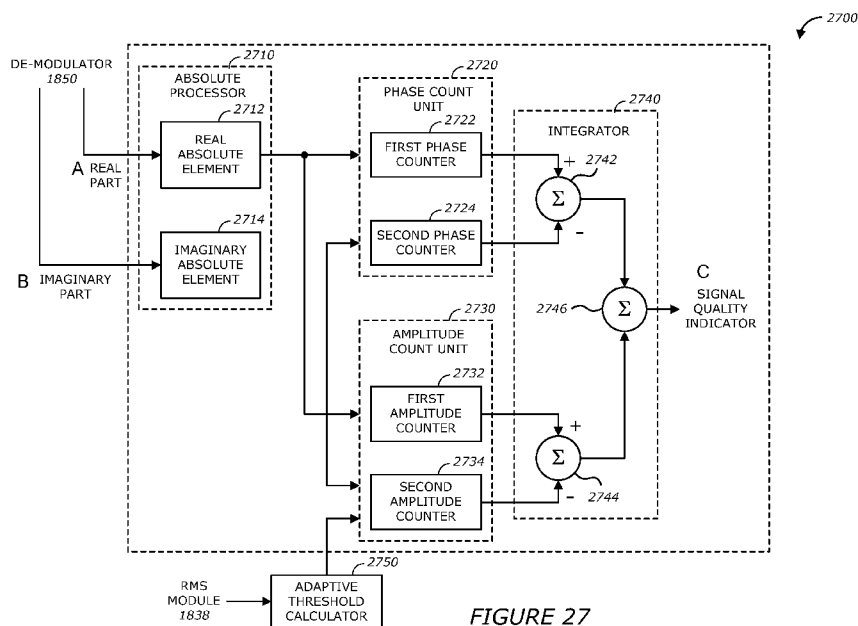


FIGURE 27

(57) Abstract: An embodiment is a method and apparatus to estimate channel quality. An absolute processor computes absolute real and imaginary values of real and imaginary parts, respectively, of output of a demodulator. A phase count unit generates first and second phase counts representing deviations from zero phase noise using the absolute real and imaginary values. An amplitude count unit generates first and second amplitude counts representing attenuation of a received signal using the absolute real and imaginary values. An integrator integrates the first and second phase counts and first and second amplitude counts into a signal quality indicator that represents a measure of quality of channel with respect to noise and fading.

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BLIND CHANNEL QUALITY ESTIMATOR

RELATED APPLICATIONS

[001] This application claims the benefits of the provisional application, filed on June 6, 2008, titled "BLIND CHANNEL QUALITY ESTIMATOR", Serial No. 61/059,715.

TECHNICAL FIELD

[002] The presently disclosed embodiments are directed to the field of communication, and more specifically, to power line communication.

BACKGROUND

[003] Power line communication (PLC) is a communication technology to carry data on electrical media (e.g., wires) that are used for electrical power transmission. Typically, electrical power is transmitted over high voltage transmission lines, distributed over medium voltage, and used inside commercial or residential buildings at lower voltages. Since power line networks transmit data signals over the same electrical grid as that is used for carrying electrical power to commercial or residential buildings, electrical wires and sockets are used simultaneously for electricity and for data transmission, without causing disruption to either.

[004] Broadband technologies provide high speed data transmission. However, currently it is problematic to apply broadband technologies in PLC. Some problems include the ability to efficiently decode signals in noisy channels, achieve time and frequency diversity, remove signal interference, maintain received signals at pre-determined levels, measure channel quality for high transmission rate, provide robustness to wideband and narrow band symbol synchronization.

SUMMARY

[005] One disclosed feature of the embodiments is a method and apparatus to estimate channel quality. An absolute processor computes absolute real and imaginary values of real and imaginary parts, respectively, of output of a demodulator. A phase count unit generates first and second phase counts representing deviations from zero phase noise using the absolute real and imaginary values. An amplitude count unit generates first and second amplitude counts representing attenuation of a received signal using the absolute real and imaginary values. An integrator integrates the first and second phase counts and first and

second amplitude counts into a signal quality indicator that represents a measure of quality of channel with respect to noise and fading.

BRIEF DESCRIPTION OF THE DRAWINGS

[006] Embodiments may best be understood by referring to the following description and accompanying drawings that are used to illustrate various embodiments. In the drawings,

[007] Figure 1 is a diagram illustrating a data frame structure used for data transmission and for the FCC, ARIB and CENELEC A bands according to one embodiment.

[008] Figure 2 is a diagram illustrating a symbol duration for data symbol according to one embodiment.

[009] Figure 3 is a diagram illustrating a data frame structure for data transmission for CENELECs B, C and BC according to one embodiment.

[0010] Figure 4 is a diagram illustrating a symbol duration for data symbol for CENELEC B and C according to one embodiment.

[0011] Figure 5 is a diagram illustrating ACK signal for FCC, ARIB and CENELEC A according to one embodiment.

[0012] Figure 6 is a diagram illustrating ACK signal for CENELEC B, C, and BC according to one embodiment.

[0013] Figure 7 is a diagram illustrating a base-band transmitter according to one embodiment.

[0014] Figure 8 is a diagram illustrating the FEC encoding unit according to one embodiment.

[0015] Figure 9A is a diagram illustrating the data scrambler according to one embodiment.

[0016] Figure 9B is a diagram illustrating the convolutional encoder according to one embodiment.

[0017] Figure 10 is a diagram illustrating the modulator according to one embodiment.

[0018] Figure 11A is a diagram illustrating the DBPSK modulator according to one embodiment.

[0019] Figure 11B is a diagram illustrating the carrier index numbers according to one embodiment.

[0020] Figure 11C is a diagram illustrating the input/output configuration according to one embodiment.

[0021] Figure 12 is a diagram illustrating the PSD shaping module according to one embodiment.

[0022] Figure 13A is a diagram illustrating a raised cosine function according to one embodiment.

[0023] Figure 13B is a diagram illustrating a overlapping and add operation according to one embodiment.

[0024] Figure 14 is a diagram illustrating a preamble signal according to one embodiment.

[0025] Figure 15 is a diagram illustrating the pre-emphasis filter according to one embodiment.

[0026] Figure 16 is a diagram illustrating the pre-emphasis filter according to one embodiment.

[0027] Figure 17A is a diagram illustrating a data scaler on the transmitter data path according to one embodiment.

[0028] Figure 17B is a diagram illustrating a P and M scaler on the transmitter data path according to one embodiment.

[0029] Figure 17C is a diagram illustrating a scaler for frequency-domain P and M signals according to one embodiment.

[0030] Figure 18 is a diagram illustrating a receiver according to one embodiment.

[0031] Figure 19 is a diagram illustrating the demodulator according to one embodiment.

[0032] Figure 20 is a diagram illustrating the FEC decoding unit according to one embodiment.

[0033] Figure 21 is a diagram illustrating timings associated with events in the receiver according to one embodiment.

[0034] Figure 22 is a diagram illustrating the DC blocker according to one embodiment.

[0035] Figure 23 is a diagram illustrating the FFT according to one embodiment.

[0036] Figure 24 is a diagram illustrating the DBPSK demodulator according to one embodiment.

[0037] Figure 25 is a diagram illustrating the ROBO combiner/decoder according to one embodiment.

[0038] Figure 26 is a diagram illustrating the RS decoder according to one embodiment.

[0039] Figure 27 is a diagram illustrating a channel quality estimator according to one embodiment.

[0040] Figure 28A is a diagram illustrating partitioning constellation planes for the phase count unit according to one embodiment.

[0041] Figure 28B is a diagram illustrating partitioning constellation planes for the amplitude count unit using the absolute real value according to one embodiment.

[0042] Figure 29 is a diagram illustrating the adaptive threshold calculator according to one embodiment.

[0043] Figure 30 is a diagram illustrating the RMS module according to one embodiment.

[0044] Figure 31 is a diagram illustrating correspondence between the signal quality indicator and the SNR in the channel according to one embodiment.

DETAILED DESCRIPTION

[0045] One disclosed feature of the embodiments is a method and apparatus to estimate channel quality. An absolute processor computes absolute real and imaginary values of real and imaginary parts, respectively, of output of a demodulator. A phase count unit generates first and second phase counts representing deviations from zero phase noise using the absolute real and imaginary values. An amplitude count unit generates first and second amplitude counts representing attenuation of a received signal using the absolute real and imaginary values. An integrator integrates the first and second phase counts and first and second amplitude counts into a signal quality indicator that represents a measure of quality of channel with respect to noise and fading.

[0046] One disclosed feature of the embodiments may be described as a process which is usually depicted as a flowchart, a flow diagram, a structure diagram, or a block diagram. Although a flowchart may describe the operations as a sequential process, many of the operations can be performed in parallel or concurrently. In addition, the order of the operations may be re-arranged. A process is terminated when its operations are completed. A process may correspond to a method, a program, a procedure, a method of manufacturing or fabrication, etc. One embodiment may be described by a schematic drawing depicting a physical structure. It is understood that the schematic drawing illustrates the basic concept and may not be scaled or depict the structure in exact proportions.

[0047] One disclosed feature of the embodiments is the implementation of a data communication modem for Federal Communication Commission (FCC), Association of Radio Industries and Businesses (ARIB), and European Committee of electrotechnical standardization or Comité Européen de Normalisation Electrotechnique (CENELEC) bands over the power line medium. The system may include a highly integrated PHY (physical layer) and MAC (Media Access Control) digital transceiver and analog front end processing circuits. The system is based on Orthogonal Frequency Division Multiplexing (OFDM).

OFDM has been chosen as the modulation technique because of its inherent adaptability in the presence of frequency selective channels, its resilience to jammer signals, and its robustness to impulsive noise.

[0048] The OFDM system may place N_{carrier} evenly spaced carriers into a specified frequency band such as from DC to 1.2MHz. In one embodiment, $N_{\text{carrier}}=128$. In the following description, the value $N_{\text{carrier}}=128$ will be used for illustrative purposes. It is contemplated that N_{carrier} may be any suitable number. Depending on the band selection, number of carriers participating in transporting data varies. Every carrier may be modulated with Differential Binary Phase Shift Keying (DBPSK). The system may support two modes of operation namely Normal and ROBO (Robust OFDM). The ROBO modulation is robust in the sense that it may provide four times extra redundancy parity bits by mean of repetition code and therefore the system may reliably deliver data under severe channel conditions.

[0049] The system parameters include signal frequency bands, modulation schemes, sampling frequency and physical layer frame structure, etc. The system supports various CELENEC, FCC and ARIB bands. The frequency band associated with each standard is given in Table 1.

	F Low (KHz)	F High (KHz)
FCC	10	480
ARIB	10	450
CELENEC A	9	95
CELENEC B	95	125
CELENEC C	125	140
CELENEC B, C	95	140

Table 1: FCC, ARIB and CENELEC Bands

[0050] An OFDM with DBPSK modulation scheme per carrier may be selected. The OFDM modulation technique is very robust against channel fading, narrowband interference and spike noise. The DBPSK modulation for each carrier may make the receiver design significantly simple since no tracking circuitry is required at the receiver for

coherently detecting the phase of each carrier. In DBPSK demodulator, the phases of carriers in adjacent symbol may be taken as the reference for detecting the phases of the carriers in the current symbol. The phases of corresponding carriers in adjacent OFDM symbols may be expected to be stationary since the channel and the clock frequency variations in time are very slow as compared to the duration of two adjacent symbols.

[0051] Assuming the maximum spectral content of the signal is 480KHz, the sampling frequency at the transmitter and receiver may be selected to be 1.2MHz that is about 240KHz above the Nyquist rate to provide a sufficient margin for signal filtering in the transmitter (for PSD shaping to remove the signal images) and at the receiver (for band selection and signal enhancement).

[0052] The number of frequency bins (FFT points) may be any suitable number. In one embodiment, this number is selected to be $N = 256$. This results in a frequency resolution for the OFDM carriers equal to 4.6875KHz (F_s / N). Note that imperfection such as sampling clock frequency variation may cause Inter Carrier Interference (ICI). In practice, the ICI caused by a typical sampling frequency variation about 2% of frequency resolution is negligible. In other word, considering ± 20 ppm sampling frequency in transmitter and receiver clocks, the drift of the carriers may be approximately equal to 48Hz that is approximately 1.26% of the selected frequency resolution. Considering these selections, the number of usable carriers for each standard may be obtained as given in Table 2.

	Number of Carriers (Ncarr) (KHz)	First Carrier (KHz)	Last Carrier (KHz)
FCC	100	14.063	478.125
ARIB	93	14.0625	445.3125
CELENEC A	19	9.375	93.75
CELENEC B	6	98.4375	121.875
CELENEC C	3	126.5625	135.9375
CELENEC B, C	9	98.4375	135.9375

Table 2: Number of carriers for various bands

[0053] The system may work in two different modes namely Normal and ROBO modes. In Normal mode, the FEC may include a Reed Solomon encoder and a convolutional encoder. The system may also support Reed Solomon code with parity of 8 and 16 Bytes.

[0054] In ROBO mode (robust modulation scheme) the FEC may include Reed Solomon and convolutional encoders followed by a Repetition Code (RC). The RC code may repeat each bit four times making system more robust to channel impairments. This of course may reduce the throughput by a factor of 4. The FEC parameters for RS parity of 8 may be given in Table 3.

	Normal Mode	ROBO Mode
FCC	½ convolutional Code + Reed Solomon (241/249)	½ convolutional Code + Reed Solomon (53/61)+RC (4)
ARIB	½ convolutional Code + Reed Solomon (223/231)	½ convolutional Code + Reed Solomon (49/57) + RC (4)
CENELEC A	½ convolutional Code + Reed Solomon (181/189)	½ convolutional Code + Reed Solomon (38/46) + RC (4)
CENELEC BC	½ convolutional Code + Reed Solomon (171/179)	½ convolutional Code + Reed Solomon (36/44)+RC (4)
CENELEC B	½ convolutional Code + Reed Solomon (111/119)	½ convolutional Code + Reed Solomon (21/29)+RC (4)
CENELEC C	½ convolutional Code + Reed Solomon (111/119)	½ convolutional Code + Reed Solomon (21/29)+RC (4)

Table 3: FEC Parameters

[0055] The number of symbols in each PHY (Physical Layer) frame may be selected based on two parameters, the required data rate and the acceptable delay. Since high bandwidth standard (FCC, ARIB) may be utilized for some delay sensitive applications such as voice transmission, therefore the number of symbols in PHY frame may be selected less than that of low bandwidth standard (CENELEC). The number of symbols and data rate associated with each band may be tabulated in Table 4. To calculate the data rate, the packets may be assumed to be continuously transmitted with no inter frame time gap.

	Data Rate (DBPSK)(kbps)	Data Rate (ROBO)(kbps)	No. of symbols per PHY Frame (Ns)
FCC	170	37	40
ARIB	157	34	40
CELENEC A	37	7.7	160
CELENEC B	9.71	1.84	320
CELENEC C	4.9	0.93	640
CELENEC B, C	14.95	3.15	320

Table 4: Data rate for various standards

[0056] The data rate may be calculated based on the number of symbols per PHY frame (NS), number of carrier per symbol (Ncarr) and number of parity bits added by FEC blocks. As an example, consider the system in the FCC band working in ROBO mode. Total number of bits carried by the whole PHY frame may be equal to:

$$\text{Total_No_Bits} = \text{NS} \times \text{Ncarr} = 40 \times 100 = 4000\text{bits}$$

[0057] The number of bits required at the input of ROBO encoder may be given by:

$$\text{No_Bits_ROBO} = 4000 \times \text{ROBORate} = 4000 \times \frac{1}{4} = 1000\text{bits}$$

[0058] Considering the fact that convolutional encoder may have a rate equal to $\frac{1}{2}$ (CCRate = $\frac{1}{2}$) and also consider adding CCZeroTail = 6bits of zeros to terminate the states of the encoder to all zero states then the maximum number of symbols at the output of Reed Solomon encoder (MAXRSbytes) may be equal to:

$$\text{MAXRSbytes} = \text{floor}((\text{No_Bits_ROBO} \times \text{CCRate} \times \text{CCZeroTail})/8) = \text{floor}((1000 \times \frac{1}{2} - 6)/8) = 61$$

[0059] Symbols: Removing 8 symbols associated with the parity bits, we may obtain:

$$\text{DataLength} = (61 - \text{ParityLength}) \times 8 = 424 \text{ bits}$$

[0060] These 424 bits may be carried within the duration of a PHY frame. The duration of a PHY frame may be calculated by the following formula:

$$T_Frame = ((\text{NS} \times (\text{N_CP} + \text{N} - \text{NO}) + (\text{Npre} \times \text{N}))/\text{Fs})$$

where Npre, N, NO and N_CP are the number of samples in the preamble, FFT length, the number of samples overlapped at each side of one symbol and the number of samples in the

cyclic prefix, respectively. The F_s is the sampling frequency. Typical values for all these parameters for various frequency bands may be given in Table 5.

Number of FFT points	$N = 256$
Number of overlapped samples	$NO = 8$
Number of cyclic Prefix (CENELEC B and C)	$N_{CP} = 89$
Number of cyclic Prefix (FCC, ARIB, CENELEC A)	$N_{CP} = 30$
Sampling frequency	$F_s = 1.2\text{MHz}$

Table 5: Parameters for various frequency bands

[0061] Replacing the above numbers in the equation, T-Frame (PHY frame duration) may be obtained as follows:

$$T_{\text{Frame}} = (40 \times (256 + 22) + (9.5 \times 256)) / 1200000 = 0.0112 \text{ sec.}$$

[0062] Therefore the data rate may be calculated by:

$$\text{Data rate} = 424 / 0.0112 \sim 37\text{kbps}$$

[0063] Signal Types: There are 2 transmission commands to the physical layer as described below.

[0064] Figure 1 is a diagram illustrating a data frame structure 100 used for data transmission and for the FCC, ARIB and CENELEC A bands according to one embodiment. The data frame 100 includes a preamble portion 110 and a data symbol portion 120.

[0065] The preamble 110 may include 8 identical P symbols and 1½ identical M symbols. Each symbol may be 256 samples and may be pre-stored in the transmitter and may be transmitted right before the data symbols. The symbols P may be used for AGC adaptation, symbol synchronization, channel estimation and initial phase reference estimation. For M symbols, two types of symbol may be used. One is the M1 in which all the carriers may be π phase shifted and the other one is M2 in which all the carriers may be $\pi/2$ phase shifted. M1 is used in ROBO mode and M2 may be used in Normal mode. At the receiver, the phase distance between symbol P and symbol M waveforms may be used for frame synchronization purpose. And the distance between the phases of two possible M symbols may be used to detect whether the PHY frame is sent in Normal mode or in ROBO mode.

[0066] Figure 2 is a diagram illustrating a symbol duration for data symbol according to one embodiment. Each symbol may have 8 samples overlapped with adjacent symbols. The last

8 samples (tail) of preamble may also be overlapped with the 8 samples of the first data symbol (head) as shown in the Figure 2. The overlap may be included to smooth the transition between symbols thus reducing the out of band spectral growth.

[0067] Figure 3 is a diagram illustrating a data frame structure 300 for data transmission for CENELECs B, C and BC according to one embodiment. The data frame 300 includes a preamble portion 310 and a data symbol portion 320.

[0068] The preamble 310 for CENELECs B, C & BC bands may include for special symbols labeled as F1F2 symbols, followed by four identical P symbols and 1½ identical M symbols. For CENELEC C, each F1F2 symbol may include three sinewaves whose phases may switch by 180° after 256 samples. Hence, we generate 256 samples of each of the three tones and sum them together, then we add 180° phase shift to each of the three tones and generate another 257 samples, so that the total length of an F1F2 symbol may be 513 samples. For CENELECs B & BC, six tones may be used instead of three, but the length of the F1F2 symbols remains unchanged. The F1F2 symbols may be used for synchronization. Each preamble symbol may contain 513 samples. The reason that we have used a different technique for synchronization is that the allocated bandwidth in CENELECs C, B and BC may be too small, which makes the autocorrelation property of the P symbols not good enough for robust synchronization. As a result, F1F2 symbols may be used. They have much better autocorrelation property. As for the P symbols for narrowband, they may still be used for channel estimation and initial phase reference estimation, same as was the case for wideband. The symbols M1 or M2 proposed for FCC, ARIB and CENELEC standards are also used for narrowband for the same purposes (frame synchronization and mode detection).

[0069] Figure 4 is a diagram illustrating a symbol duration for data symbol for CENELC B and C according to one embodiment. Again, the same approach is used for PHY frame in ROBO mode that is the P and M symbol are exchanged.

ACK/NACK signal

[0070] Figure 5 is a diagram illustrating ACK signal for FCC, ARIB and CENELEC A according to one embodiment. This signal may be used when an acknowledgement is required to confirm whether the data is correctly received (ACK) or it is erroneous (NACK). The same waveform used in preamble with modified M symbol may be used as an ACK signal. The P with 90 degrees shift ($M=jP$) and P with 180 degrees shift ($M=-P$) may

already reserved for normal mode and ROBO mode respectively. The P with 270 degrees shift ($M=-jP$) may be proposed to be used for ACK signaling.

[0071] This may simplify the system, as only one waveform need to be stored in the transmitter and same detection circuit in the receiver as used for preamble detection, is used for ACK signal detection as well. If no signal is received during the specified period, it is interpreted as a NACK signal.

[0072] Figure 6 is a diagram illustrating ACK signal for CENELEC B, C, and BC according to one embodiment. Again the same symbols as used for the preamble for the purpose of synchronization, may also be used for the ACK signal. During the time period that a device is waiting for an acknowledgement, the reception of this signal may be an indication that the data may have been delivered with no error. If the time expires and the ACK signal has not been received, it may be an indication that the data may have been lost or delivered in errors.

[0073] Figure 7 is a diagram illustrating a base-band transmitter 700 according to one embodiment. The base-band transmitter 700 includes a Forward Error Correction (FEC) encoding unit 710, a modulator 720, a power spectral shaping (PSD) module 730, a switch 740, an output formatter 750, and a switch 760.

[0074] The base-band transmitter 700 may receive its input bits in one packet from the Media Access (MAC) Layer. The FEC encoding unit 710 may include a number of FEC encoders. Each FEC encoder may add parity bits to the data and the packet grows as it goes through various blocks in FEC encoding unit 710. At the end of the FEC encoding unit 710, the final packet may be broken down into small packet so that each small packet may be fitted into one OFDM symbol. The size of one small packet depends on the number of carriers used in each OFDM symbol. For example, in FCC band, the packet size becomes equal to 100 bits. In order to understand the size of data as well as signal dimensions at each various points in the transmitter baseband, the calculation method may be described in the following.

[0075] Packet size calculation:

[0076] The total number of bits carried by a PHY frame may be obtained by:

$$N_F = N_G = N_{\text{carr}} \times N_s$$

[0077] The N_F and N_G may represent the size of packet (signal) at nodes (F) and (G), respectively. Where N_{carr} is the number of carriers in each OFDM symbol and N_s is the

number of symbols per PHY frame. Note that the Interleaver does not change the size of packet. The number of bits at point (E) may be given by:

$$N_E = N_F \times R$$

[0078] The value R may be one for Normal mode and 1/4 for ROBO Mode. In order to find M, the number of zeros may need to be padded at the output of convolutional encoder; first we need to calculate the maximum number of RS bytes. The maximum number of RS bytes (MaxRSbytes) at the output of RS encoder may be obtained by the following equation:

$$\text{MaxRSbytes} = \text{floor} ((N_E \times \text{CCRate} - \text{CCZeroTail})/8)$$

[0079] Where CCRate and CCZeroTail are the convolutional code rate (1/2) and the number of zeros to be added to the input of convolutional encoder (to terminate the states to zero state), respectively. And “8” refers to the length of each RS word that is one byte.

Therefore, the value of M may be obtained by:

$$M = N_E - ((\text{MaxRSbytes} \times 8) + 6) \times 2$$

[0080] Table 6 shows the number of zeroes padded after convolutional encoder for various bands.

	ROBO (Bits)	Normal (bits)
FCC	M=12	M=4
ARIB	M=6	M=12
CELENEC A	M=12	M=4
CELENEC B	M=4	M=4
CELENEC C	M=4	M=4
CELENEC B, C	M=4	M=4

Table 6: Number of zeroes padded after convolutional encoder

[0081] The number of bits at point (D), (C) and (B) now may be calculated by:

$$N_D = N_E - M, \quad N_C = N_D / 2, \quad N_B = N_C - 6$$

[0082] Finally, considering the fact the number of parity bytes in RS code may be equal to 8, the packet size delivered by MAC to the physical layer may be given by:

$$N_A = (N_B/8 - 8) \times 8$$

[0083] Table 7 summarizes the input packet to the physical layer for various band and both normal and ROBO modes. It should be noted that CENELEC B and CENELEC C ROBO may not be able to have long header format (48-bit addressing) and RS parity of 16 Bytes at the same time because of the size of the packet limitations.

	ROBO (bits)	Normal (bits)
FCC	424	1928
ARIB	392	1784
CELENEC A	304	1448
CELENEC B	168	888
CELENEC C	168	888
CELENEC B, C	288	1368

Table 7: Packet size delivered by MAC layer to PHY layer

[0084] The packet size at various nodes in the FEC encoding unit 710 for each band (CENELEC (A,B,BC)/FCC/ARIB) may be calculated and summarized in Tables 8A, 8B, 8C, 8D, 8E, and 8F. The nodes A, B, C, D, E, and F are shown in Figure 8.

FEC Node	Normal Mode	ROBO Mode
A	1928	424
B	1992	428
C	1998	494
D	3996	988
E	4000	1000
F	4000	4000

Table 8A: Packet Size at various node of FEC encoder for FCC band

FEC Node	Normal Mode	ROBO Mode
A	1784	392
B	1848	456
C	1854	462
D	3708	924
E	3720	930
F	3720	3720

Table 8B: Packet Size at various node of FEC encoder for ARIB band

FEC Node	Normal Mode	ROBO Mode
A	1448	304
B	1512	368
C	1518	374
D	3036	748
E	3040	760
F	3040	3040

Table 8C: Packet Size at various nodes of FEC encoder for CENELEC A band

FEC Node	Normal Mode	ROBO Mode
A	888	168
B	952	232
C	958	238
D	1916	476
E	1920	480
F	1920	1920

Table 8D: Packet Size at various node of FEC encoder for CENELEC B band

FEC Node	Normal Mode	ROBO Mode
A	888	168
B	952	232
C	958	238
D	1916	476
E	1920	480
F	1920	1920

Table 8E: Packet Size at various node of FEC encoder for CENELEC C band

FEC Node	Normal Mode	ROBO Mode
A	1368	288
B	1432	352
C	1438	358
D	2876	716
E	2880	720
F	2880	2880

Table 8F: Packet Size at various nodes of FEC encoder for CENELEC BC band

[0085] Figure 8 is a diagram illustrating the FEC encoding unit 710 according to one embodiment. The FEC encoding unit 710 includes a data scrambler 810, a Reed-Solomon (RS) encoder 820, a zero padding 830, a convolutional encoder 840, a zero padding 850, a ROBO encoder 860, a switch 870, an interleaver 880, and an un-buffer 890. It is noted that the FEC encoding unit 710 may include more or less than the above elements. In addition, any one of the above elements may be implemented by hardware, software, firmware, or any combination of hardware, software, and firmware.

[0086] The FEC encoders may include Reed Solomon encoder 820 followed by convolutional encoder 840. In ROBO mode, an extra encoder namely Repetition Code (RC) or ROBO encoder 860 may be used after the convolutional encoder 840 that repeats the bits at the output of convolutional encoder 840 four times

[0087] The data scrambler 810 may help give the data a random distribution. Figure 9A is a diagram illustrating the data scrambler 810 according to one embodiment. The data stream

may be XOR-ed with a repeating pseudo random number (PN) sequence using the following generator polynomial: $S(x) = x^7 + x^4 + 1$. The bits in the scrambler are initialized to all ones at the start of processing each PHY frame.

[0088] The RS encoder 820 encodes data from the scrambler 810. The RS encoder 820 may be may be created by shortening RS (255,247, t = 4) and (255,239, t = 8) code. The “RS symbol word length” (i.e., the size of the data words used in the Reed-Solomon block) may be fixed at 8 bits. The value of t (number of word errors that can be corrected) may be either 4 or 8 for different standards. For CENELEC B and C ROBO the RS parity of 8 Bytes (corresponding to t=4) should be used. The number of parity words in a RS-block is thus 2t words. The number of non-parity data words (bytes) in Reed-Solomon encoder 820 may be provided in Table 3. The first bit in time from the data scrambler 810 may become the most significant bit of that symbol. Each RS encoder input block (consisting of 247 symbols) is conceptually formed by one or more fill symbols (“00000000”) followed by the message symbols. Output of the RS encoder (with fill symbols discarded) may proceed in time from first message symbol to last message symbol followed by parity symbols, with each symbol shifted out most significant bit first.

Code Generator Polynomial $g(x) = (x - \alpha^1)(x - \alpha^2)(x - \alpha^3)...(x - \alpha^8)$

Field Generator Polynomial: $p(x) = x^8 + x^4 + x^3 + x^2 + 1$ (435 octal)

	Normal Mode N_A/N_B (Bytes)	ROBO Mode N_A/N_B (Bytes)
FCC	241/249	53/61
ARIB	223/231	49/57
CENELEC A	181/189	38/46
CENELEC BC	171/179	36/44
CENELEC B	111/119	21/29
CENELEC C	111/119	21/29

Table 9: RS encoder input/output packet size

[0089] The representation of α^0 is “00000001”, where the left most bit of this RS symbol is the MSB and is first in time from the scrambler 810 and is the first in time out of the RS encoder 820. The packet size (in Bytes) at the input and output of RS encoder 820 (N_A and N_B) may be given in Table 9.

[0090] The zero padding 830 may pad six zeroes after the RS encoder 820.

[0091] Figure 9B is a diagram illustrating the convolutional encoder 840 according to one embodiment. The convolutional encoder 840 may encode the bit stream at the output of the Reed-Solomon encoder 820 with a standard rate = $\frac{1}{2}$, K=7. The tap connections are defined as $x = 0b1111001$ and $y = 0b1011011$, as shown in Figure 9B.

[0092] When the last bit of data to the convolutional encoder 840 may have been received, the convolutional encoder 840 may insert six tail bits, which may be required to return the convolutional encoder 840 to the "zero state". This may improve the error probability of the convolutional decoder, which relies on future bits when decoding. The tail bits may be defined as six zeros. The number of bits at the input and the output of convolutional encoder may be given in Table 10.

	Normal Mode N_A/N_B (bits)	ROBO Mode N_A/N_B (bits)
FCC	1998/3996	494/988
ARIB	1854/3708	462/924
CENELEC A	1518/3036	374/748
CENELEC BC	1438/2876	358/716
CENELEC B	958/1916	238/476
CENELEC C	958/1916	238/476

Table 10: Convolutional encoder input/output packet sizes

[0093] The zero padding 850 may pad M zeroes after the convolutional encoder 840. M is given in Table 6.

[0094] The ROBO encoder 860 repeats the resulting packet after adding M number of zeros to the packet four times in ROBO mode. The ROBO encoder 860 may be only activated in ROBO mode. The repeat code may be implemented inside the interleaver 880. The switch 870 selects whether to bypass the ROBO encoder 860 or uses the output of the ROBO encoder 860 in ROBO mode.

[0095] The interleaver 880 interleaves the data packet selected from the switch 870. It may be used for both normal mode and ROBO mode. The interleaver 880 may use a linear block

interleaver and may achieve the same performance of a random interleaver using a simpler architecture with less computation.

[0096] The un-buffer 890 breaks down the final packet into small packet so that each small packet may be fitted into one OFDM symbol, as described earlier.

[0097] Figure 10 is a diagram illustrating the modulator 720 according to one embodiment. The modulator 720 includes a DBPSK modulator 1010, a zero padding 1020, an inverse Fast Fourier Transform (IFFT) 1030, and a cyclic prefix (CP) extension 1040. It is noted that the modulator 720 may include more or less than the above elements. In addition, any one of the above elements may be implemented by hardware, software, firmware, or any combination of hardware, software, and firmware.

[0098] Figure 11A is a diagram illustrating the DBPSK modulator 1010 according to one embodiment. The DBPSK modulator 1010 includes a mapper 1110 and a differential modulator 1120.

[0099] The mapper 1110 map data bits for differential modulation. Each phase vector may use its predecessor (same carrier, previous symbol) as phase reference. The mapping function for DBPSK may be given in Table 11.

Input Bit	Output Phase
0	Ψ_k
1	$\Psi_k + \pi$

Table 11: DBPSK Encoding Table of Kth Sub carrier

[00100] The initial phase for the first symbol are the carrier phases of the preamble symbol and are provided in Table 12. Each value in Table 12 may be a multiple integer of $\pi/8$ and may be quantized by 4 bits. The preamble phase reference index in Table 12 may start from 1 and it may refer to the first carrier in the corresponding band as given in Table 13. Note that the carrier index may be numbered from 0 to 127. This may be been illustrated in Figure 11B.

c	F	A	C	C	C	C	c	F	A	c	F	A	c	F	A
	C	R	N	N	N	N		C	R		C	R		C	R
	C	I	L	L	L	L		C	I		C	I		C	I
		B	C	C	C	C			B			B			B
	ϕ_c	ϕ_c	A	B	C	B		ϕ_c	ϕ_c		ϕ_c	ϕ_c		ϕ_c	ϕ_c
			ϕ_c	ϕ_c	ϕ_c	C									
						ϕ_c									
1	14	14	14	X	X	X	26	8	4	51	11	12	76	9	8
2	14	14	13	X	X	X	27	3	15	52	3	3	77	12	11
3	13	13	11	X	X	X	28	15	10	53	10	10	78	15	13
4	13	12	9	X		X	29	10	5	54	1	1	79	3	0
5	12	12	6	X		X	30	5	0	55	9	7	80	6	2
6	11	11	2	X		X	31	0	11	56	15	14	81	9	4
7	10	10	12			X	31	11	5	57	7	4	82	12	6
8	9	8	6			X	33	6	0	58	13	10	83	14	7
9	8	7	14			X	34	0	10	59	4	0	84	0	8
10	6	6	6				35	11	4	60	10	6	85	3	10
11	5	4	12				36	5	14	61	0	11	86	5	10
12	3	2	2				37	15	7	62	6	0	87	7	11
13	1	0	7				38	9	1	63	12	5	88	9	12
14	14	13	10				39	3	10	64	1	10	89	10	13
15	12	11	13				40	12	3	65	7	15	90	11	13
16	9	8	15				41	6	12	66	12	4	91	12	14
17	7	5	0				42	15	5	67	1	8	92	13	14
18	4	2	1				43	8	14	68	7	12	93	14	14
19	1	15	1				44	1	6	69	11	0	94	15	
20	14	11					45	10	14	70	0	4	95	0	
21	10	8					46	3	7	71	5	8	96	0	
22	7	4					47	11	14	72	9	11	97	1	
23	4	0					48	3	6	73	13	15	98	1	
24	0	12					49	11	14	74	1	2	99	1	
25	11	8					50	3	5	75	5	5	100	2	

Table 12: Preamble Phase Vector Definition

	C_{n1}	C_{n2}
FCC	3	102
ARIB	3	95
CELENEC-A	2	20
CELENEC-B	21	26
CELENEC-C	27	29
CELENEC-BC	21	29

Table 13: First and Last Carrier Indexes for each band

[00101] Figure 11B is a diagram illustrating the carrier index numbers according to one embodiment.

[00102] The IFFT 1030 may take the 256-point IFFT of the input vector and may generate the main 256 time domain OFDM words preceded by N_{CP} words of cyclic prefix. In other words, the last N_{CP} samples at the output of the IFFT 1030 may be taken and placed in front of symbol. The useful output may be the real part of the IFFT coefficients. Figure 11C is a diagram illustrating the input/output configuration according to one embodiment. The first carrier C_{n1} and the last carrier index C_{n2} associated with each band may be given in Table 13.

[00103] Figure 12 is a diagram illustrating the PSD shaping module 730 according to one embodiment. The PSD shaping module 730 includes a raised cosine shaping 1210, an overlapping 1220, and a pre-emphasis filter 1230.

[00104] Figure 13A is a diagram illustrating a raised cosine function according to one embodiment. Figure 13B is a diagram illustrating a overlapping and add operation according to one embodiment.

[00105] In order to reduce the out of band emission and to reduce the spectral side lobe, a window function may be applied. In one embodiment, the Raised Cosine shaping 1210 may be applied to all the data symbols. Then the tails and heads of successive symbols may be overlapped and added together by the overlapping 1220. This process is described below. Each side of a symbol may be first shaped by the raised cosine function as shown in Figure 13A.

[00106] The windowing function at each 8-sample boundary may be a Raised Cosine function and its values are given in Table 14. The window function may have a value equal to one at other samples. Then the 8 tail and 8 head shaped samples of the symbol from each side of symbol may be overlapped with the tail and head samples of adjacent symbols as shown in Figure 13B. In other words, In order to construct the n_{th} symbol, firstly its 8 head samples may be overlapped with the 8 tail samples of the $(n-1)_{th}$ symbol and its 8 tail samples may be overlapped with the 8 head samples of the $(n+1)_{th}$ symbol. Finally, the corresponding overlapped parts may be added together. Note that the head of the first symbol is overlapped with the tail of preamble. And the tail of last symbol may be sent out with no overlapping applied.

	Head samples	Tail samples
1	0	0.9619
2	0.0381	0.8536
3	0.1464	0.6913
4	0.3087	0.5000
5	0.5000	0.3087
6	0.6913	0.1464
7	0.8536	0.0381
8	0.9619	0

Table 14: The Raised Cosine Samples

[00107] Figure 14 is a diagram illustrating a preamble signal according to one embodiment.

[00108] Memory locations may need to be allocated in the baseband to store the preamble samples. The preamble samples may be prepared in advance and download into the baseband memory during initialization period by the processor that implements the MAC layer. Each sample of preamble symbol may have an 8-bit length. The preamble signal that may be added to the beginning of each PHY frame may be shown in Figure 14. It may include 8 symbols of type P and 1.5 symbols of type M. The total number of samples may be equal to 2432 samples. The first and the last 8 samples may be shaped according to

Raised Cosine window. Note that the last 8 samples may be overlapped by the first 8 samples of the first data symbol. In practice we only need to store 256 sample of symbol P, 256 samples of symbol M, the first and the last 8 samples. Note that the symbol M may be different in Normal mode from that in the ROBO mode. In the ROBO mode, symbol M may be signed reversed of the P symbol, so there may be no extra storage required to store another symbol M for ROBO mode. In normal mode, the M symbol may have 90° phase shift from the P symbol.

[00109] Figure 15 is a diagram illustrating the pre-emphasis filter 1230 according to one embodiment.

Time-Domain Pre-emphasis Filter:

[00110] A time-domain pre-emphasis filter 1230 may be a linear equalization method where the transmit signal spectrum may be shaped to compensate for amplitude distortion. The purpose of this filter may be to provide frequency shaping to the transmit signal in order to compensate for attenuation introduced to the signal as it goes through the power line.

[00111] The pre-emphasis filter 1230 may be a first order recursive filter with transfer function of $H(z) = 0.5 * [(\text{Gamma} + \text{Beta} * z^{-1}) / (1 - R * z^{-1})]$. It may be specified with below deference equation:

$$y(n) = 0.5 * [\text{Gamma} * x(n) + \text{Beta} * x(n-1) + R * y(n-1)]$$

[00112] As shown, the pre-emphasis filter 1230 may have one zero and one pole. In this implementation Gamma, Beta, and R may be programmable and may be assigned 16-bit registers. The pre-emphasis filter 1230 may be the last block in the transmit path right before the output formatter 750. The pre-emphasis filter may have the following register requirements: an enable/disable bit to enable/bypass the pre-emphasis filter, a Gamma register (signed 16 bits): parameter to control the shape of the pre-emphasis filter, a Beta register (signed 16 bits): parameter to control the shape of the pre-emphasis filter, and an R register (signed 16 bits): parameter to control the shape of the pre-emphasis filter.

Frequency Domain Pre-emphasis Filter:

[00113] Figure 16 is a diagram illustrating the pre-emphasis filter according to one embodiment. The purpose of this block may be to provide frequency shaping to the transmit signal in order to compensate for attenuation introduced to the signal as it goes through the power line.

[00114] The frequency-domain pre-emphasis filter may include of a multiplier that may multiply the complex frequency domain samples of an OFDM symbol with 128 real filter coefficients, then do four right shifts at the output. The filter coefficients may be 5 bits representing unsigned values from 0h to 10h. The filter coefficients may not be allowed to have values larger than 10h. The filter may multiply the first 128 frequency-domain complex samples of an OFDM symbol with the 128 real coefficients of the filter. The rest of the 128 frequency-domain samples of the OFDM symbol may be usually set to zero and may not be multiplied by the filter coefficients. As the block diagram below shows, the input complex samples may be 8 bits each while the filter coefficients may be 5 unsigned bits each. Since the maximum allowed value of any filter coefficients may be 10h, the output of the multiplication may be 12 bits (not 13 bits). The output may then be right shifted by 4 to get a final output of 8 bits that may be used as input to the IFFT.

[00115] The filter coefficient values may vary from 0 to 16, and since we do 4 right shifts at the output, it follows that the filter may provide the following attenuation for any of the 128 carriers:

Scaling factor =====	attenuation in dB =====
16/16	0 dB
15/16	-0.53 dB
14/16	-1.16 dB
13/16	-1.8 dB
12/16	-2.5 dB
11/16	-3.25 dB
10/16	-4 dB
9/16	-5 dB
8/16	-6 dB
7/16	-7.2 dB
6/16	-8.5 dB
5/16	-10.1 dB
4/16	-12 dB
3/16	-14.5 dB
2/16	-18 dB
1/16	-24 dB
0/16	-infinite

[00116] The following registers may be needed to control the frequency-domain pre-emphasis filter: Enable/Disable bit: Allows for enabling/disabling the filter.

Transmitter (TX) P and D Scaler:

[00117] In order to control the transmitted power level of P and M in relation to power level of data two scalers may be implemented in the transmitter: a Data scaler to scale the data, and a P/M scaler to control the levels of the P & M that we are now generating from the frequency domain using the IFFT. Both scalers may be described below. On the receiver path, no scaling may be needed.

[00118] Figure 17A is a diagram illustrating a data scaler on the transmitter data path according to one embodiment. Figure 17B is a diagram illustrating a P and M scaler on the transmitter data path according to one embodiment. Figure 17C is a diagram illustrating a scaler for frequency-domain P and M signals according to one embodiment. Figures 17A and 17B are provided to show how the 4-bit sync reference may be generated and scaled. The P/M scaler is used to scale IFFT output of frequency-domain P and M so that their levels may be as close as possible to original time-domain P & M. Once that is accomplished, the data scaler is used to achieve the desired P/Data RMS ratio. In what follows, the P/M scaler is described first, followed by the data scaler, which may have an identical architecture.

[00119] Figure 17C shows how the IFFT output of frequency-domain P and M may be scaled so that their levels may be as close as possible to original time-domain P & M. This block may be called the "P/M Scaler". The table lists the values for P_scale_factor and P_shift_factor registers for the different wideband and narrowband standards.

[00120] The data scaler may have identical block to the P/M scaler except that P_scale_factor is renamed to Data_scale_factor, and P_shift_factor is renamed to Data_shift_factor, where both may remain 8 bits each. The table shows the default values for the data scalers for the different standards.

[00121] Figure 18 is a diagram illustrating a receiver 1800 according to one embodiment. The receiver 1800 includes a data formatter 1810, a direct current (DC) blocker 1815, an analog automatic gain control (AGC) processor 1820, a processing unit 1830, a digital AGC processor 1840, a demodulator 1850, a symbol synchronizer 1852, a frame synchronizer 1854, a preamble FFT coefficient buffer 1860, a mode detector 1870, and a FEC decoding unit 1880. It is noted that the receiver 1880 may include more or less

than the above elements. In addition, any one of the above elements may be implemented by hardware, software, firmware, or any combination of hardware, software, and firmware.

[00122] Figure 19 is a diagram illustrating the demodulator 1850 according to one embodiment. The demodulator 1850 includes a cyclic prefix (CP) remover 1910, a FFT processor 1920, and a DBPSK demodulator 1930.

[00123] Figure 20 is a diagram illustrating the FEC decoding unit 1880 according to one embodiment. The FEC decoding unit 1880 includes a buffer 2010, a de-interleaver 2020, a ROBO combiner 2030, a zero remover 2040, a Viterbi decoder 2050, a RS decoder 2060, and a descrambler 2070. It is noted that the FEC decoding unit 1880 may include more or less than the above elements. In addition, any one of the above elements may be implemented by hardware, software, firmware, or any combination of hardware, software, and firmware.

[00124] On the receiver side, the PHY layer may receive its input samples from the power line and may hand the demodulated data bits over to the MAC layer. The processing unit 1830 may include a first infinite impulse response (IIR) filter 1832, a second IIR filter 1834, a jammer canceller 1836, and a root mean square (RMS) module 1838. The jammer canceller 1836 removes interference or a jamming signal in the input signal. The symbol synchronizer 1852 and the frame synchronizer 1854 may be used for preamble (ACK signal) detection, symbol and frame synchronization. The frame synchronizer 1854 and the preamble FFT coefficient buffer 1860 may be used to perform the initial preamble phase and the channel estimation, respectively.

[00125] The synchronizers 1852 and 1854 and the jammer canceller 1836 may be ON when the system is in the "Receive" mode. If the jammer or interfering signal may be present in the channel and detected, a switch may be set so that the signal may be taken from the output of the jammer canceller 1836. The jammer detector in the jammer canceller 1836 may do this automatically. The mode detector 1870 detects the mode of operation and sets an ACK flag 1872 or a ROBO flag 1874 as appropriate.

[00126] Two different synchronizer circuits, one for FCC, ARIB and CENELEC bands (Wideband OFDM) and another for CENELEC B, C and BC (Narrow band OFDM), may be used for different bands. The tasks for synchronizers may be the detection of preamble and obtaining the start of preamble symbol (symbol synchronizer) and the start of data symbol (frame synchronizer). As soon as the start of data symbol may be found, a switch may be moved to place the CP remover in the demodulator 1850 (Figure 19) in the

signal path. At the same time a timer 1865 may be enabled to generate the Physical Carrier Sense (PCS) signal. This signal may be high for the entire frame period. It may be at the end of PCS signal that the ACK flag 1872 and the ROBO flag 1874 are reset. Note that same waveforms may be used for ACK signaling and therefore as soon as the preamble is detected the ACK flag 1872 may be set. The value of this flag may be read by the MAC software and may be reset at the end of PCS signal. Note that the frame synchronizer 1854 may also detect if the PHY frame may be in ROBO mode or in Normal mode accordingly set/reset the ROBO flag 1874.

[00127] Once the symbol synchronizer identifies the start of preamble symbols, the initial channel estimator may be activated. At this time a switch may be set since there may be no cyclic prefix extension for preamble symbols. This block may measure the reference phase from the preamble. It may also measure the channel quality at each frequency bin. The channel estimator may also estimate the SNR for each carrier.

[00128] The ROBO flag 1874 may select the position of a switch in the FEC decoding unit 1880. Depending on the preamble waveform, the frame synchronizer 1854 may identify if the frame is in ROBO mode or in Normal Mode and the switch in the FEC decoding unit 1880 is set accordingly.

[00129] Figure 21 is a diagram illustrating timings associated with events in the receiver according to one embodiment.

[00130] The data formatter 1810 may take the data bits from the analog-to-digital converter (ADC) and may perform tasks including, scaling, and mapping to convenient signed value representation. The DC blocker 1815 may be used to remove the DC component of incoming data. Since A/D converters and analog front-end circuitry may not be expected to be totally DC free, this filter may remove the DC residual. Figure 22 is a diagram illustrating the DC blocker 1815 according to one embodiment. The DC blocker 1815 may be a first order recursive filter with transfer function of $H(z) = 1 - z^{-1} / 1 - Az^{-1}$. It may be specified with the difference equation $y(n) = x(n) - x(n-1) + A y(n-1)$. DC blocker may have a zero at DC ($z=1$) and a pole near DC at $z=A$. In order to have the pole and zero cancel each other A may be selected as close as possible to unit circle. In one embodiment, $A = .995 * 2^{15} = 32604$. The DC blocker 1815 may be the first block in receiver path before jammer canceller 1836. An enable/disable register may be allocated for the DC blocker 1815.

[00131] Figure 23 is a diagram illustrating the FFT 1920 according to one embodiment. The same structure as used for the IFFT in the transmitter is used for FFT as well.

[00132] Figure 24 is a diagram illustrating the DBPSK demodulator 1930 according to one embodiment. The phase difference between carriers over successive symbols may be estimated after the FFT of the current symbol may be multiplied by the conjugate values of the FFT of the previous symbol. The size of the signal at each node in Figure 4.15 may be equal to the number of carriers (N_{carr}). The real value of the signal at the output of multiplier may be taken and quantized appropriately by soft detection block. Each bit (carried by each carrier) may be represented by an integer number. The value of this number may depend on the reliability of the bit. The length of this integer number may be provided in fixed-point implementation.

[00133] The bit de-interleaver 2020 may reverse the mappings described in the transmitter section.

[00134] Figure 25 is a diagram illustrating the ROBO combiner/decoder 2030 according to one embodiment. In ROBO mode, the encoded data may be extended 4 times by parity bits. For the repeat code, the soft values for each demodulated carrier are obtained. Then all the four values associated with one data bit may be averaged prior to hard decoding.

[00135] The errors at the output of Viterbi decoder tend to occur in a burst fashion. To correct these burst errors a RS code may be concatenated with convolutional code.

[00136] Figure 26 is a diagram illustrating the RS decoder 2060 according to one embodiment.

[00137] The de-scrambler 2070 may reverse the scrambling action, done on the source information bits in the transmitter.

[00138] Digital communication systems may be configured to support different transmission rates by using different code rates or by different constellation for modulation. The basic trade-off is rate vs. robustness of the system. In order to achieve highest throughput, it is desired that the system use the highest rate resulting in error free transmission as much as possible and to use lower rates when it has to. The blind channel quality estimator may provide a measure that may be used as a solution to the problem of measuring channel quality and choosing the higher rate transmission when possible. The benefits of the blind channel quality estimator may include:

- Using phase and amplitude information to measure the quality of the channel in noisy environment.
- Using the amplitude information to detect frequency selective fading and tones being severely attenuated.
- Using adaptive threshold based on Root Mean Square (RMS) of received signal to compensate for the fluctuation of input signal level due to the AGC.
- Providing a simple technique to estimate the quality of channel without having a known transmit signal reference.
- Providing a means to sense severe attenuation of tones in a fading channel even when noise level is fairly small.

[00139] The blind channel quality estimator may be used in the receiver of a communication system such as the power line communication described above. It may be used in conjunction with the demodulator 1850 and a front-end processing unit to provide a signal quality indicator. The signal quality indicator may correspond to a signal-to-noise ratio (SNR) and may be used in a link adaptation mechanism in the system. The front-end processing module may include the analog AGC processor 1820, the processing unit 1830, the digital AGC processor 1840, and the demodulator 1850 shown in Figure 18. The front end processing module may process an input signal. The analog AGC processor 1820 controls an analog adjustable gain of the input signal using a feedback mechanism and generates a first signal. The processing unit 1830 may include the root mean square (RMS) module 1838 to transform the first signal into a second signal. The digital AGC processor 1840 controls a digital adjustable gain of the second signal using a feed-forward mechanism to generate an output signal. The digital AGC gain value as computed by the digital AGC processor 1840 may be stored a register referred to as the RMS digital AGC output register. The demodulator 1850 demodulates a packet obtained from the output signal.

[00140] Figure 27 is a diagram illustrating a channel quality estimator 2700 according to one embodiment. The channel quality estimator 2700 includes an absolute processor 2710, a phase count unit 2720, an amplitude count unit 2730, an integrator 2740, and an adaptive threshold calculator 2750. It is noted that the channel quality estimator 2700 may include more or less than the above elements. In addition, any one of the above elements may be implemented by hardware, software, firmware, or any combination of hardware, software, and firmware.

[00141] The absolute processor 2710 computes absolute real and imaginary values of real and imaginary parts, respectively, of output of the demodulator 1850. The absolute processor 2710 may include a real absolute element 2712 to compute the absolute real value of the real part of the output of the demodulator 1850, and an imaginary absolute element 2714 to compute the absolute imaginary value of the imaginary part of the output of the demodulator 1850.

[00142] The phase count unit 2720 generates first and second phase counts representing deviations from zero phase noise using the absolute real and imaginary values. The phase count unit 2720 may include a first phase counter 2722 to increment the first phase count if the absolute real value is greater than or equal to the absolute imaginary value, and a second phase counter 2724 to increment the second phase count if the absolute real value is less than the absolute imaginary value. The first phase counter 2722 and the second phase counter 2724 may be implemented by a comparator and a counter. The output of the comparator may be used as a clock to increment the associated counter.

[00143] The amplitude count unit 2730 generates first and second amplitude counts representing attenuation of a received signal using the absolute real and imaginary values. The amplitude count unit 2730 may include a first amplitude counter 2732 to increment the first amplitude count if an amplitude value is greater than or equal to a pre-determined threshold or an adaptive threshold, and a second amplitude counter 2734 to increment the second amplitude count if the amplitude is less than the pre-determined threshold or the adaptive threshold. The first amplitude counter 2732 and the second amplitude counter 2734 may be implemented by a comparator and a counter. The output of the comparator may be used as a clock to increment the associated counter.

[00144] The integrator 2740 integrates, or combines, the first and second phase counts and first and second amplitude counts into a signal quality indicator that represents a measure of quality of channel with respect to noise and fading. The integrator 2740 may include a phase subtractor 2742 to subtract the second phase count from the first phase count to generate a phase quality indicator, an amplitude subtractor 2744 to subtract the second amplitude count from the first amplitude count to generate a channel fading indicator, and an adder 2746 to add the phase quality indicator and the channel fading indicator to provide the signal quality indicator.

[00145] The adaptive threshold calculator 2750 generates the adaptive threshold, the adaptive threshold being used to compensate for level fluctuations of the received signal. In

order to compensate for the fluctuation in the input level, the measured energy of the input signal is used to compensate for the signal level fluctuations. The algorithm may use the data energy measured by the RMS module 1838 and updates the threshold used in amplitude count unit 2730. In order to have more control, a multiplier/scaler is used so a fractional multiple of energy can be used as the new threshold to further fine-tune the threshold chosen. The proposed scheme is able to work in presence of AGC fluctuation and can sense if some of the tones are severely attenuated and switch to a more robust modulation scheme accordingly.

[00146] Figure 28A is a diagram illustrating partitioning constellation planes for the phase count unit 2720 according to one embodiment. The phase count unit 2820 checks the phase information of the received symbol. Noise causes the phase of received symbols to deviate from zero degree. The more the noise, the more is the phase difference.

[00147] Figure 28B is a diagram illustrating partitioning constellation planes for the amplitude count unit using the absolute real value according to one embodiment. The amplitude count unit 2730 looks at the amplitude of the received symbol therefore reflecting the attenuation of the received symbol because of the channel response in certain sub-carrier or noise. It is noted that the amplitude may be computed by using the absolute real value $|R|$ or other schemes such as the sum of the absolute real and imaginary values $|R| + |I|$.

[00148] Figure 29 is a diagram illustrating the adaptive threshold calculator 2750 according to one embodiment. The adaptive threshold calculator 2750 may include a multiplier 2910 to generate a product by multiplying output of the RMS module with a scale factor, a scaler 2920 to scale the product by a pre-determined number of bits, and a clipper 2930 to clip the scaled product by a maximum value. The clipped scaled product represents the adaptive threshold.

[00149] Figure 30 is a diagram illustrating the RMS module 1838 according to one embodiment. The RMS module 1838 may include an input energy processor 3010 to compute energy of the received signal, a scaler 3020 to scale the energy, a register 3030 to latch the scaled energy value, an update counter 3040 to count number of samples for updating the input energy processor 3010; and a gain-adjusted RMS calculator 3050 to generate the RMS output. In general, the RMS module 1838 may be triggered to start its computation whenever it receives the “start of data” signal that indicates that the frame sync has been detected and the system is ready to decode data. Once the trigger signal is received, the RMS module 1838 starts computing the digital AGC input energy over a

predefined number of samples that is programmable by the user. The number of samples may be in the form 2^N where N is an integer, and it may not be greater than the length of one data frame. The RMS module 1838 may then get the proper frozen digital AGC gain value and adjust the computed input energy value. The RMS module 1838 may then clear all its energy registers so that when it gets the next trigger, a new energy value will be computed.

[00150] The input energy processor 3010 may include a multiplier 3012 to square the received signal, an adder 3014 to add the squared received signal, and a register 3016 to store previous sum from the adder 3014. The input energy processor 3010 thus computes accumulated sum of the squared received signal over an update interval which is determined by a number of samples. This number of samples may be determined in advance and programmable by the user. It may be stored in a register denoted by RMS window length.

[00151] The scaler 3020 scales the energy value provided by the input energy processor 3010 by a pre-determined number of bits. The scaling may be performed by shifting right the energy value. In one embodiment, the number of bits to be shifted may range from 12 to 14.

[00152] The register 3030 latches the result from the scaler 3020 to hold or freeze the value during the update interval. It is cleared or unlatched to allow the new value of the scaler 3020 to be stored when the update counter 3040 reaches the end of the update interval. It may be denoted as RMS digital AGC input register.

[00153] The update counter 3040 counts the number of samples and generates an update indicator to signal that a new energy value is computed. This update indicator may be used to clear the register 3016 and to unlatch the register 3030.

[00154] The gain-adjusted RMS calculator 3050 adjusts the RMS value as provided by the scaler 3020 according to the digital AGC gain as determined by the digital AGC processor 1840. A state machine checks if the digital AGC processor 1840 is enabled or disabled. If the digital AGC processor 1840 is disabled, then the computed input energy value should also be copied to the RMS digital AGC output register since input and output energy values may be the same because disabling the digital AGC processor 1840 is equivalent to having unity gain. If the digital AGC processor 1840 is enabled, it is determined if the digital AGC processor 1840 is frozen. If it is frozen, then the proper frozen digital AGC gain value, or the old value that was stored, and multiply it by the

computed input energy value. If it is not frozen, then the digital AGC gain value as computed by the digital AGC processor 1840 is used.

[00155] Figure 31 is a diagram illustrating correspondence between the signal quality indicator and the SNR in the channel according to one embodiment. The SNR estimator with a 2σ gap (2σ range = 95% confidence) is shown in the figure for one illustrative case. It can be seen the estimator value is tightly coupled to the receiver SNR. The estimator value can be used in link adaptation algorithm.

[00156] Elements of one embodiment may be implemented by hardware, firmware, software or any combination thereof. The term hardware generally refers to an element having a physical structure such as electronic, electromagnetic, optical, electro-optical, mechanical, electro-mechanical parts, etc. A hardware implementation may include analog or digital circuits, devices, processors, applications specific integrated circuits (ASICs), programmable logic devices (PLDs), field programmable gate arrays (FPGAs), or any electronic devices. The term software generally refers to a logical structure, a method, a procedure, a program, a routine, a process, an algorithm, a formula, a function, an expression, etc. The term firmware generally refers to a logical structure, a method, a procedure, a program, a routine, a process, an algorithm, a formula, a function, an expression, etc., that is implemented or embodied in a hardware structure (e.g., flash memory, ROM, EPROM). Examples of firmware may include microcode, writable control store, micro-programmed structure. When implemented in software or firmware, the elements of an embodiment are essentially the code segments to perform the necessary tasks. The software/firmware may include the actual code to carry out the operations described in one embodiment, or code that emulates or simulates the operations.

[00157] The program or code segments can be stored in a processor or machine accessible medium. The "processor readable or accessible medium" or "machine readable or accessible medium" may include any medium that may store, transmit, receive, or transfer information. Examples of the processor readable or machine accessible medium that may store include a storage medium, an electronic circuit, a semiconductor memory device, a read only memory (ROM), a flash memory, an erasable programmable ROM (EPROM), a floppy diskette, a compact disk (CD) ROM, an optical disk, a hard disk, etc. The machine accessible medium may be embodied in an article of manufacture. The machine accessible medium may include information or data that, when accessed by a machine, cause the machine to perform the operations or actions described above. The

machine accessible medium may also include program code, instruction or instructions embedded therein. The program code may include machine readable code, instruction or instructions to perform the operations or actions described above. The term “information” or “data” here refers to any type of information that is encoded for machine-readable purposes. Therefore, it may include program, code, data, file, etc.

[00158] All or part of an embodiment may be implemented by various means depending on applications according to particular features, functions. These means may include hardware, software, or firmware, or any combination thereof. A hardware, software, or firmware element may have several modules coupled to one another. A hardware module is coupled to another module by mechanical, electrical, optical, electromagnetic or any physical connections. A software module is coupled to another module by a function, procedure, method, subprogram, or subroutine call, a jump, a link, a parameter, variable, and argument passing, a function return, etc. A software module is coupled to another module to receive variables, parameters, arguments, pointers, etc. and/or to generate or pass results, updated variables, pointers, etc. A firmware module is coupled to another module by any combination of hardware and software coupling methods above. A hardware, software, or firmware module may be coupled to any one of another hardware, software, or firmware module. A module may also be a software driver or interface to interact with the operating system running on the platform. A module may also be a hardware driver to configure, set up, initialize, send and receive data to and from a hardware device. An apparatus may include any combination of hardware, software, and firmware modules.

[00159] It will be appreciated that various of the above-disclosed and other features and functions, or alternatives thereof, may be desirably combined into many other different systems or applications. Various presently unforeseen or unanticipated alternatives, modifications, variations, or improvements therein may be subsequently made by those skilled in the art which are also intended to be encompassed by the following claims.

CLAIMS

What is claimed is:

1. An apparatus comprising:
 - an absolute processor coupled to a demodulator to compute absolute real and imaginary values of real and imaginary parts, respectively, of output of the demodulator;
 - a phase count unit coupled to the absolute processor to generate first and second phase counts representing deviations from zero phase noise using the absolute real and imaginary values;
 - an amplitude count unit coupled to the absolute processor to generate first and second amplitude counts representing attenuation of a received signal using the absolute real and imaginary values; and
 - an integrator coupled to the phase and amplitude count units to integrate the first and second phase counts and first and second amplitude counts into a signal quality indicator that represents a measure of quality of channel with respect to noise and fading.
2. The apparatus of claim 1 wherein the absolute processor comprises:
 - a real absolute element to compute the absolute real value of the real part of the output of the demodulator; and
 - an imaginary absolute element to compute the absolute imaginary value of the imaginary part of the output of the demodulator.
3. The apparatus of claim 1 wherein the phase count unit comprises:
 - a first phase counter to increment the first phase count if the absolute real value is greater than or equal to the absolute imaginary value; and
 - a second phase counter to increment the second phase count if the absolute real value is less than the absolute imaginary value.
4. The apparatus of claim 3 wherein the amplitude count unit comprises:
 - a first amplitude counter to increment the first amplitude count if an amplitude value is greater than or equal to a pre-determined threshold or an adaptive threshold; and
 - a second amplitude counter to increment the second amplitude count if the amplitude is less than the pre-determined threshold or the adaptive threshold.

5. The apparatus of claim 4 wherein the integrator comprises:
a phase subtractor coupled to the first and second phase counters to subtract the second phase count from the first phase count to generate a phase quality indicator;
an amplitude subtractor coupled to the first and second amplitude counters to subtract the second amplitude count from the first amplitude count to generate a channel fading indicator; and
an adder coupled to the phase subtractor and the amplitude subtractor to add the phase quality indicator and the channel fading indicator to provide the signal quality indicator.

6. The apparatus of claim 4 further comprising:
an adaptive threshold calculator coupled to a root mean square (RMS) module to generate the adaptive threshold, the adaptive threshold being used to compensate for level fluctuations of the received signal.

7. The apparatus of claim 6 wherein the adaptive threshold calculator comprises:
a multiplier to generate a product by multiplying output of the RMS module with a scale factor;
a scaler coupled to the multiplier to scale the product by a pre-determined number of bits; and
a clipper coupled to the scaler to clip the scaled product by a maximum value, the clipped scaled product representing the adaptive threshold.

8. A method comprising:
computing absolute real and imaginary values of real and imaginary parts, respectively, of output of a demodulator;
generating first and second phase counts representing deviations from zero phase noise using the absolute real and imaginary values;
generating first and second amplitude counts representing attenuation of a received signal using the absolute real and imaginary values; and
integrating the first and second phase counts and first and second amplitude counts into a signal quality indicator that represents a measure of quality of channel with respect to noise and fading.

9. The method of claim 8 wherein computing absolute real and imaginary values comprises:

computing the absolute real value of the real part of the output of the demodulator;
and

computing the absolute imaginary value of the imaginary part of the output of the demodulator.

10. The method of claim 8 wherein generating first and second phase counts comprises:

incrementing the first phase count if the absolute real value is greater than or equal to the absolute imaginary value; and

incrementing the second phase count if the absolute real value is less than the absolute imaginary value.

11. The method of claim 10 wherein generating first and second amplitude counts comprises:

incrementing the first amplitude count if an amplitude value is greater than or equal to a pre-determined threshold or an adaptive threshold; and

incrementing the second amplitude count if the amplitude is less than the pre-determined threshold or the adaptive threshold.

12. The method of claim 11 wherein integrating comprises:

subtracting the second phase count from the first phase count to generate a phase quality indicator;

subtracting the second amplitude count from the first amplitude count to generate a channel fading indicator; and

adding the phase quality indicator and the channel fading indicator to provide the signal quality indicator.

13. The method of claim 11 further comprising:

generating the adaptive threshold used to compensate for level fluctuations of the received signal using a root mean square (RMS) module.

14. The method of claim 13 wherein generating the adaptive threshold comprises:

generating a product by multiplying output of the RMS module with a scale factor;
scaling the product by a pre-determined number of bits; and
clipping the scaled product by a maximum value, the clipped scaled product
representing the adaptive threshold.

15. A system comprising:
- a front end processing module to process an input signal, the front end processing module comprising:
 - an analog automatic gain control (AGC) processor to control an analog adjustable gain of the input signal using a feedback mechanism, the analog AGC processor generating a first signal,
 - a root mean square (RMS) module coupled to the AGC processor to transform the first signal into a second signal, and
 - a digital AGC processor coupled to the RMS module to control a digital adjustable gain of the second signal using a feed-forward mechanism to generate an output signal;
 - a demodulator coupled to the front end processing module to demodulate a packet obtained from the output signal; and
 - a channel quality estimator coupled to the front end processing module and the demodulator to provide a signal quality indicator, the channel estimator comprising:
 - an absolute processor coupled to a demodulator to compute absolute real and imaginary values of real and imaginary parts, respectively, of output of the demodulator,
 - a phase count unit coupled to the absolute processor to generate first and second phase counts representing deviations from zero phase noise using the absolute real and imaginary values,
 - an amplitude count unit coupled to the absolute processor to generate first and second amplitude counts representing attenuation of a received signal using the absolute real and imaginary values, and
 - an integrator coupled to the phase and amplitude count units to integrate the first and second phase counts and first and second amplitude counts into a signal quality indicator that represents a measure of quality of channel with respect to noise and fading.

16. The system of claim 15 wherein the absolute processor comprises:
a real absolute element to compute the absolute real value of the real part of the output of the demodulator; and

an imaginary absolute element to compute the absolute imaginary value of the imaginary part of the output of the demodulator.

17. The system of claim 15 wherein the phase count unit comprises:
a first phase counter to increment the first phase count if the absolute real value is greater than or equal to the absolute imaginary value; and

a second phase counter to increment the second phase count if the absolute real value is less than the absolute imaginary value.

18. The system of claim 17 wherein the amplitude count unit comprises:
a first amplitude counter to increment the first amplitude count if an amplitude value is greater than or equal to a pre-determined threshold or an adaptive threshold; and

a second amplitude counter to increment the second amplitude count if the amplitude is less than the pre-determined threshold or the adaptive threshold. .

19. The system of claim 18 wherein the integrator comprises:
a phase subtractor coupled to the first and second phase counters to subtract the second phase count from the first phase count to generate a phase quality indicator;

an amplitude subtractor coupled to the first and second amplitude counters to subtract the second amplitude count from the first amplitude count to generate a channel fading indicator; and

an adder coupled to the phase subtractor and the amplitude subtractor to add the phase quality indicator and the channel fading indicator to provide the signal quality indicator.

20. The system of claim 18 further comprising:
an adaptive threshold calculator coupled to a root mean square (RMS) module to generate the adaptive threshold, the adaptive threshold being used to compensate for level fluctuations of the received signal.

21. The system of claim 20 wherein the adaptive threshold calculator comprises:

a multiplier to generate a product by multiplying an RMS output of the RMS module with a scale factor;

a scaler coupled to the multiplier to scale the product by a pre-determined number of bits; and

a clipper coupled to the scaler to clip the scaled product by a maximum value, the clipped scaled product representing the adaptive threshold.

22. The system of claim 21 wherein the RMS module comprises:
an input energy processor to compute energy of the received signal;
a scaler coupled to the input energy processor to scale the energy;
an update counter to count number of samples for updating the input energy processor; and
a gain-adjusted RMS calculator to generate the RMS output.

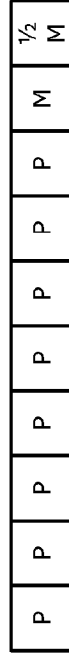
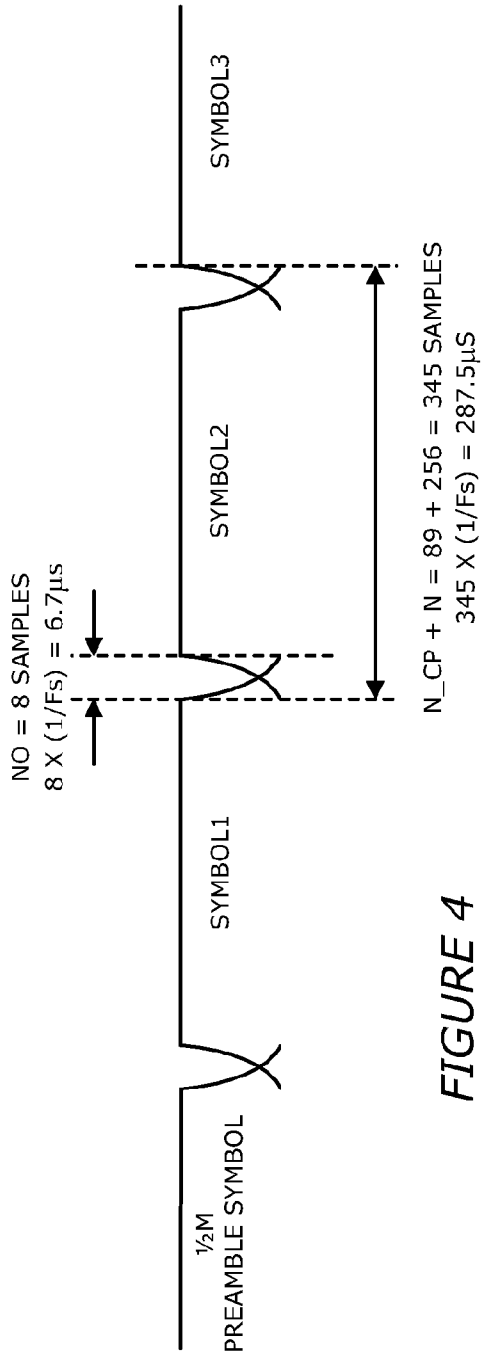


FIGURE 5

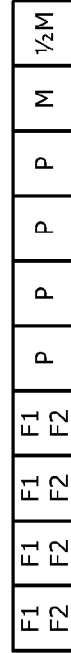
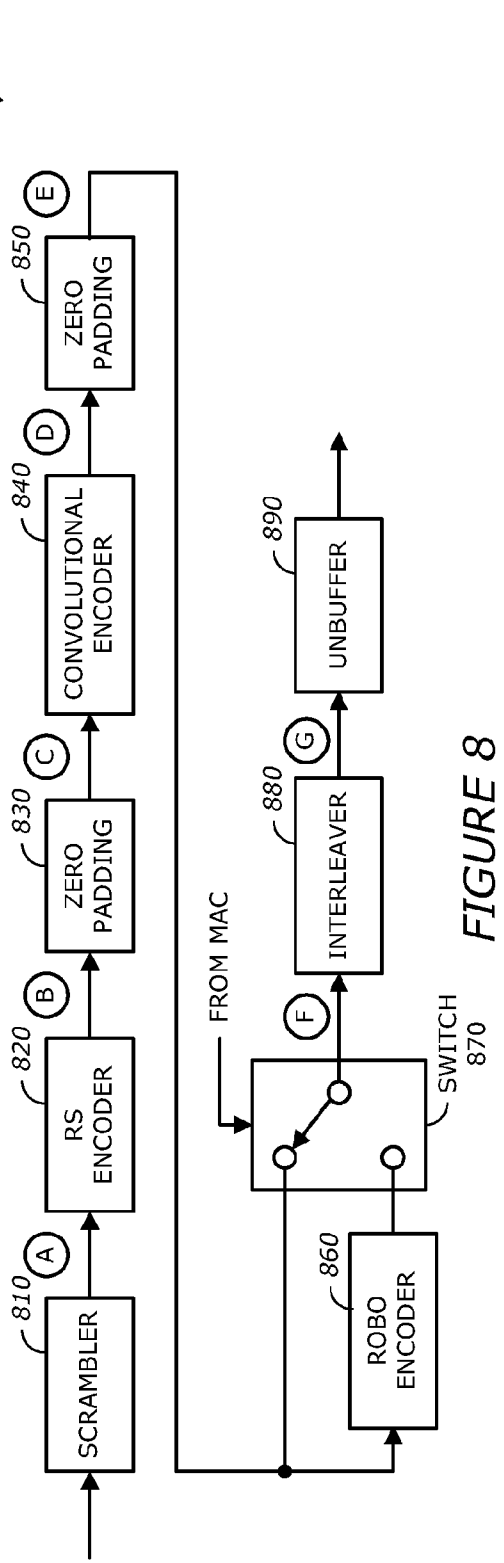
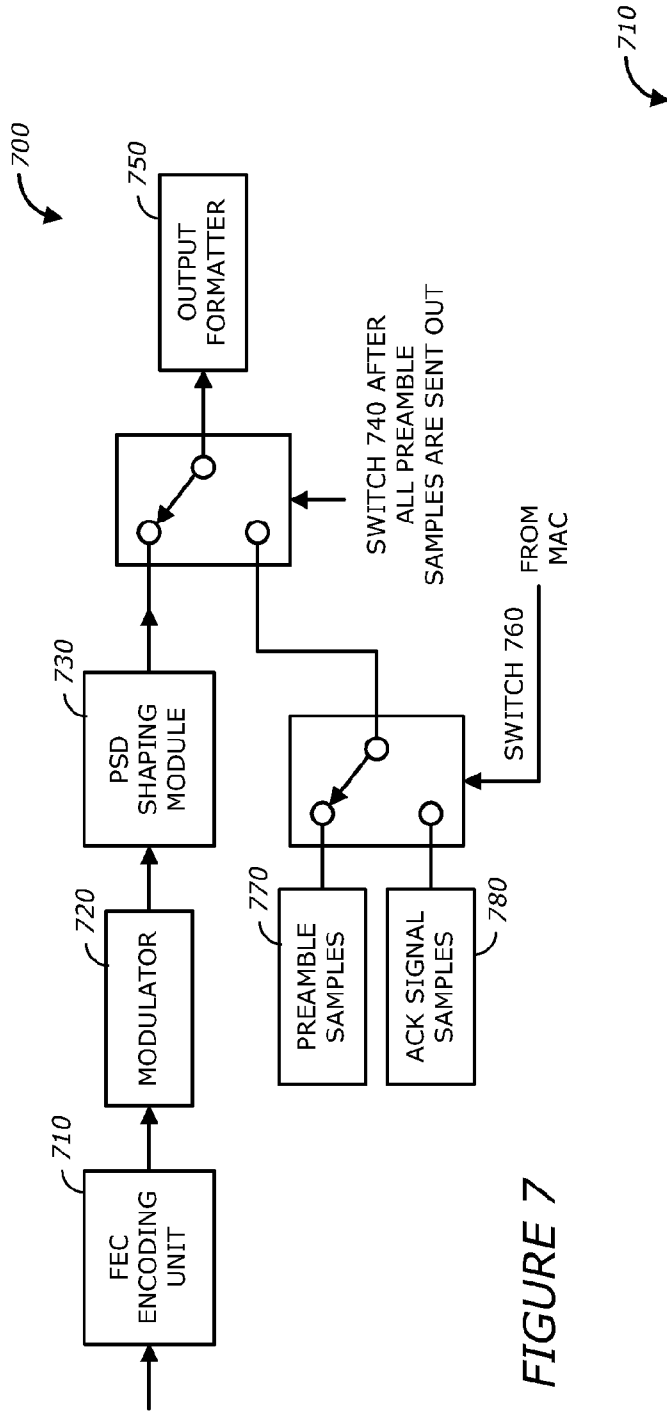


FIGURE 6



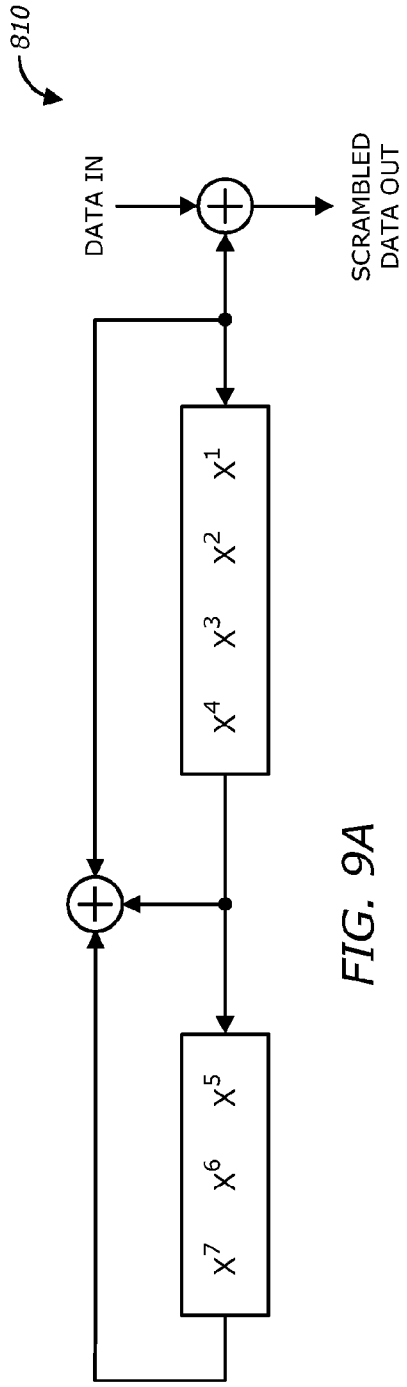


FIG. 9A

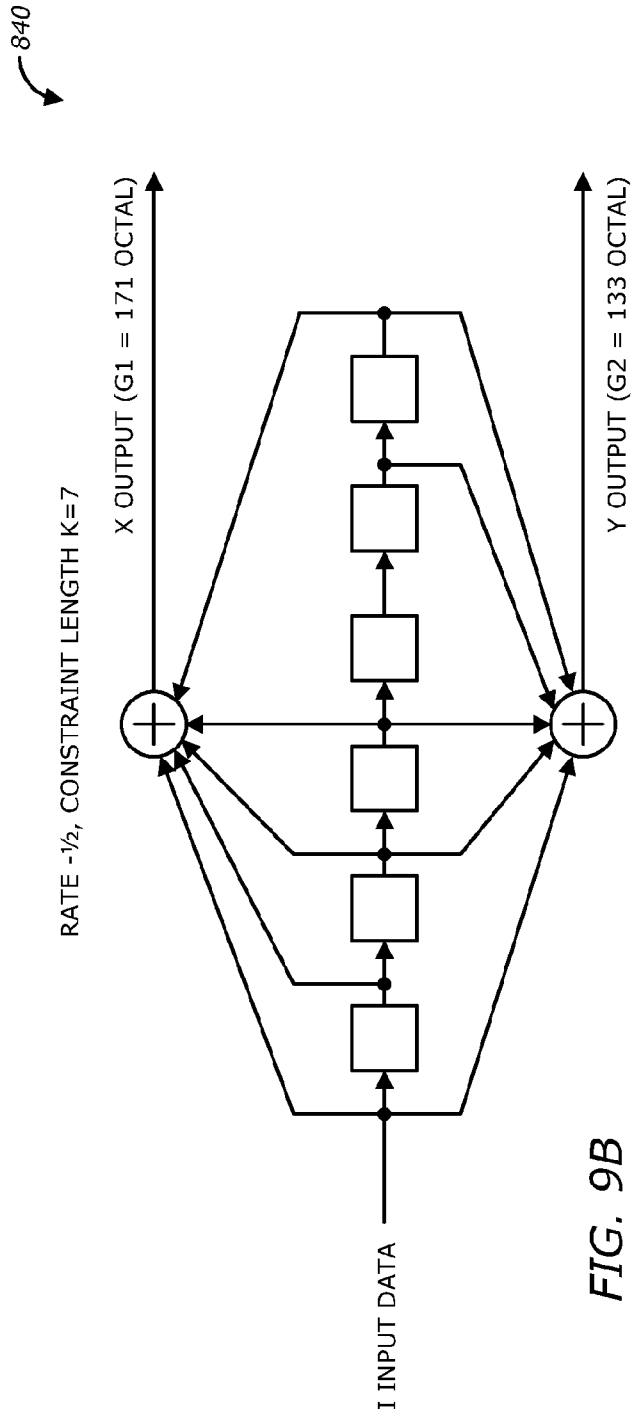


FIG. 9B

810

840

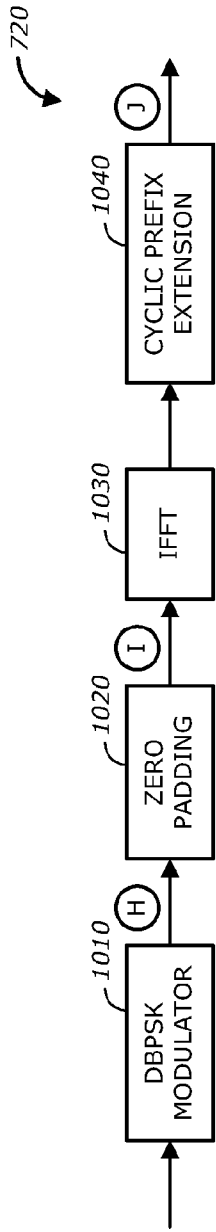


FIGURE 10

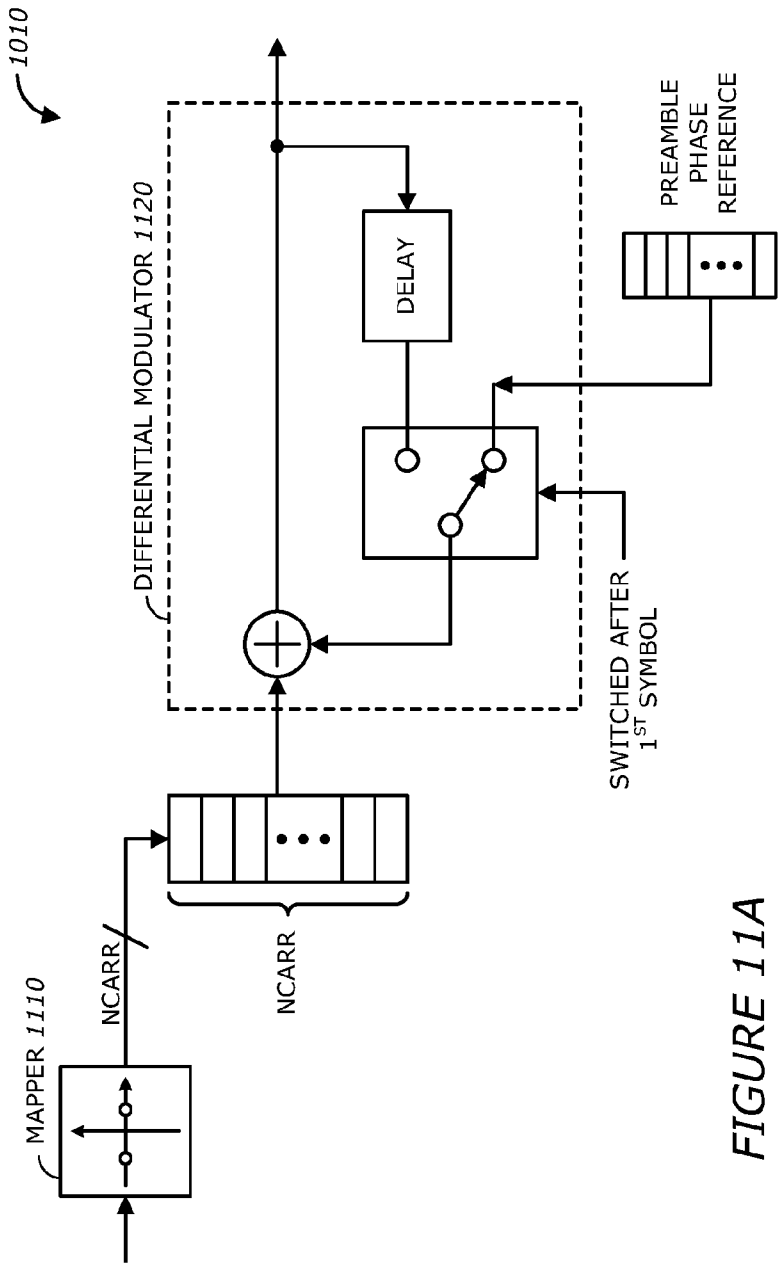


FIGURE 11A

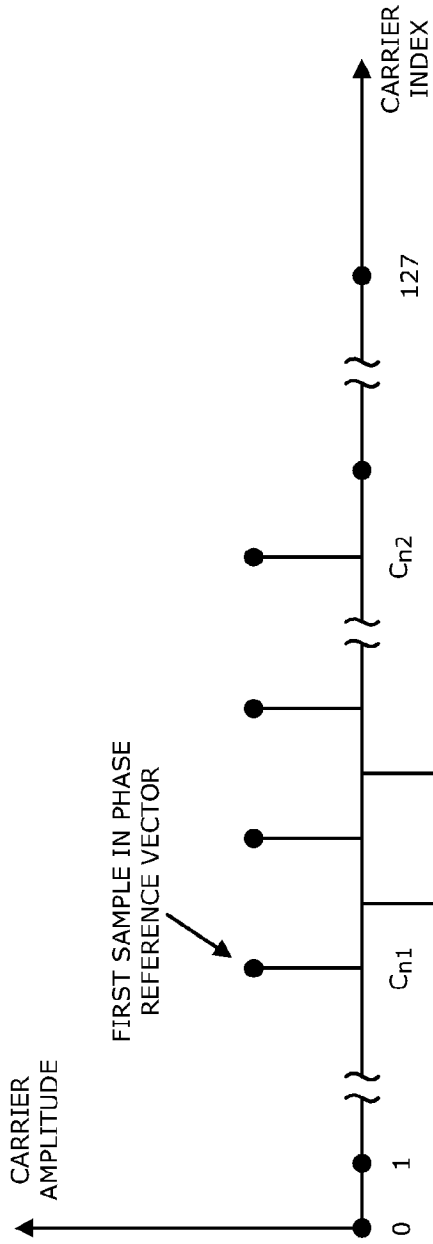


FIGURE 11B

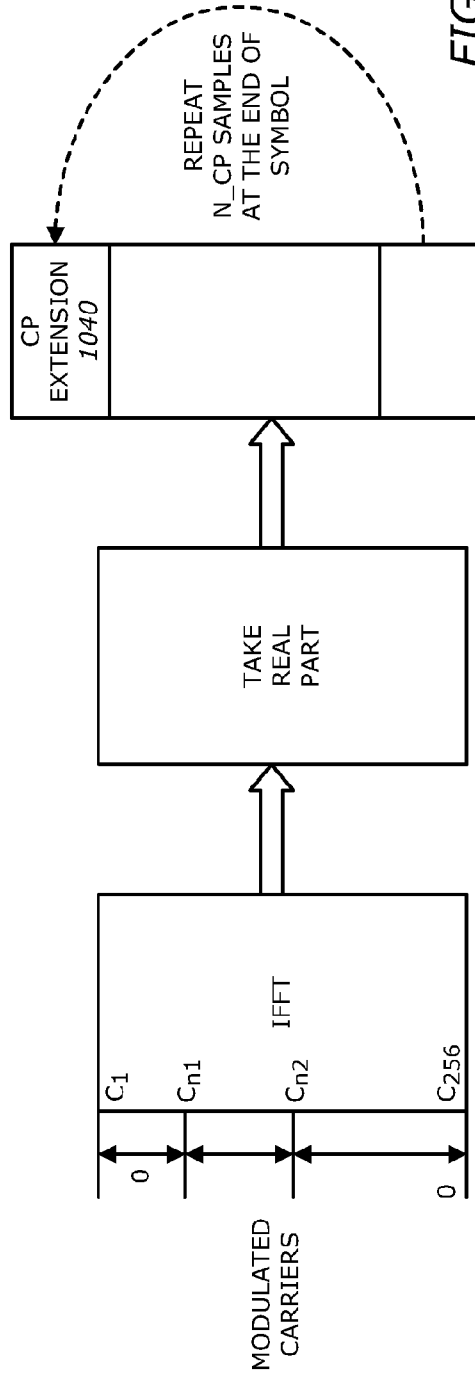


FIGURE 11C

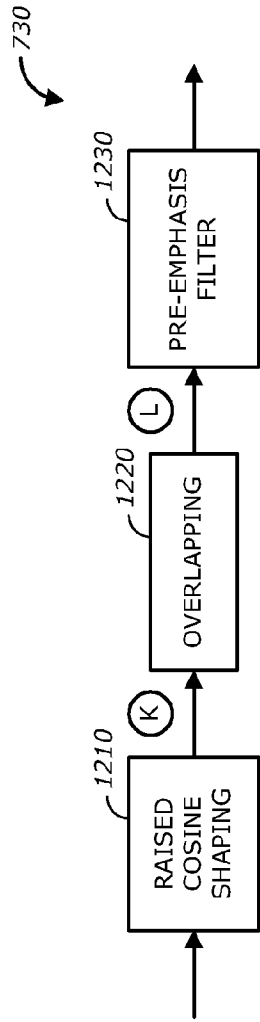


FIGURE 12

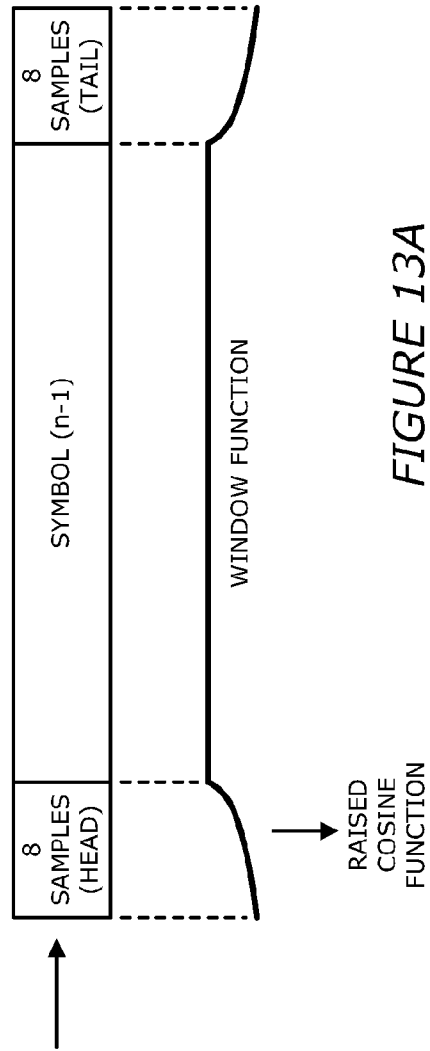


FIGURE 13A

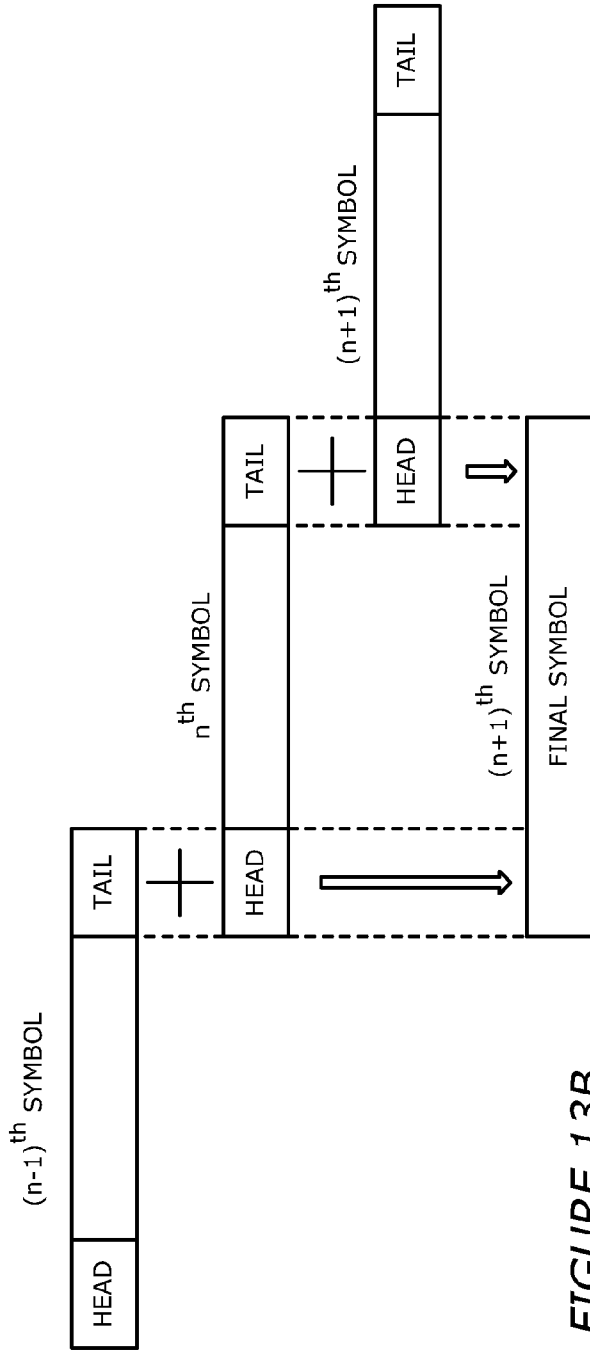


FIGURE 13B

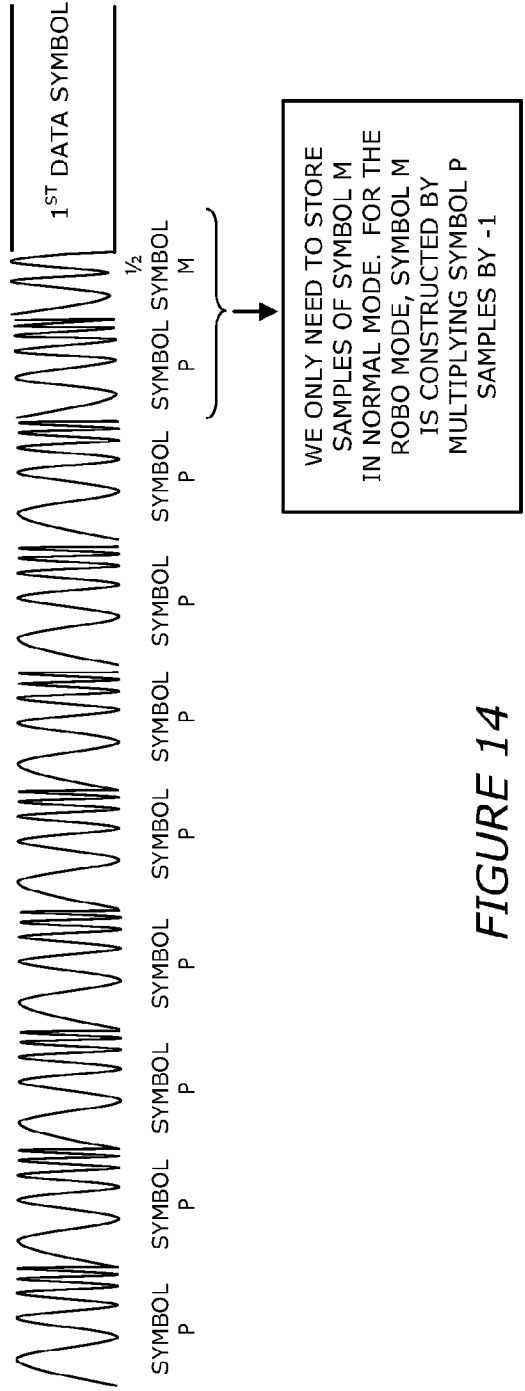


FIGURE 14

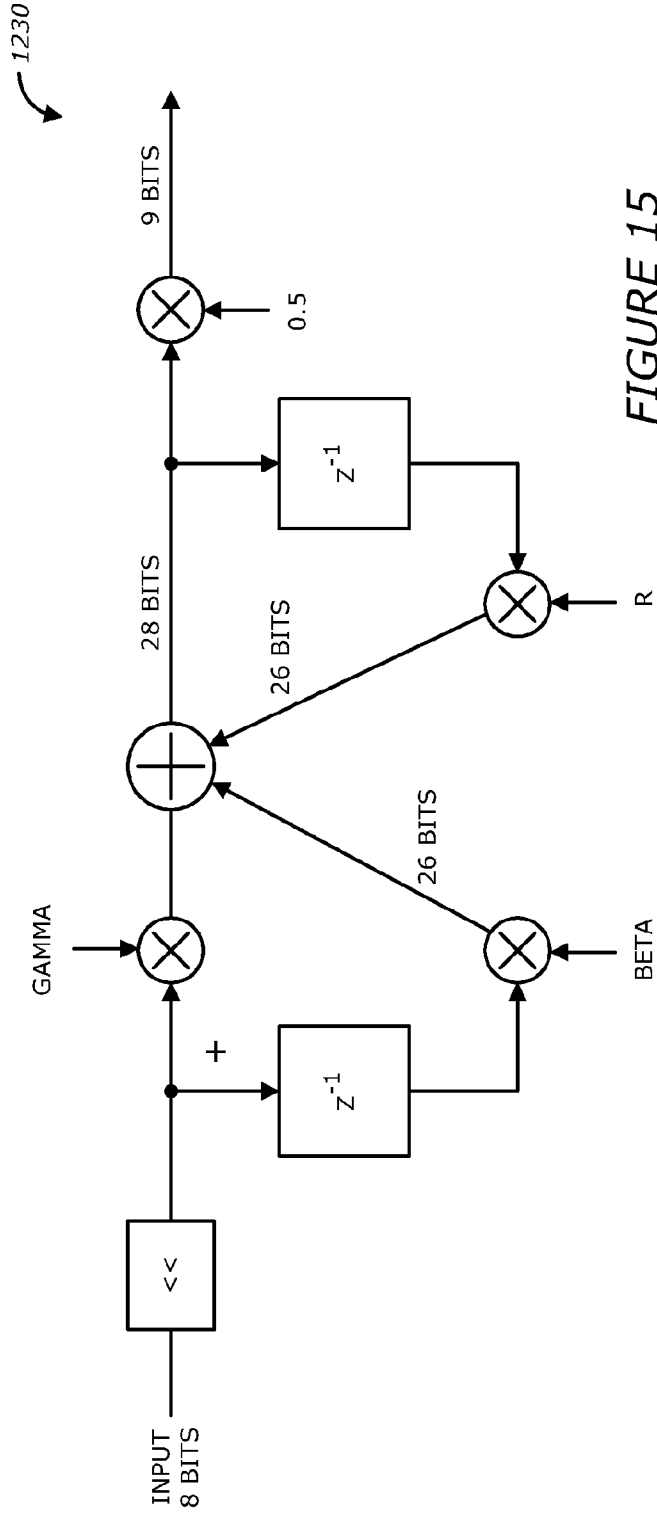


FIGURE 15

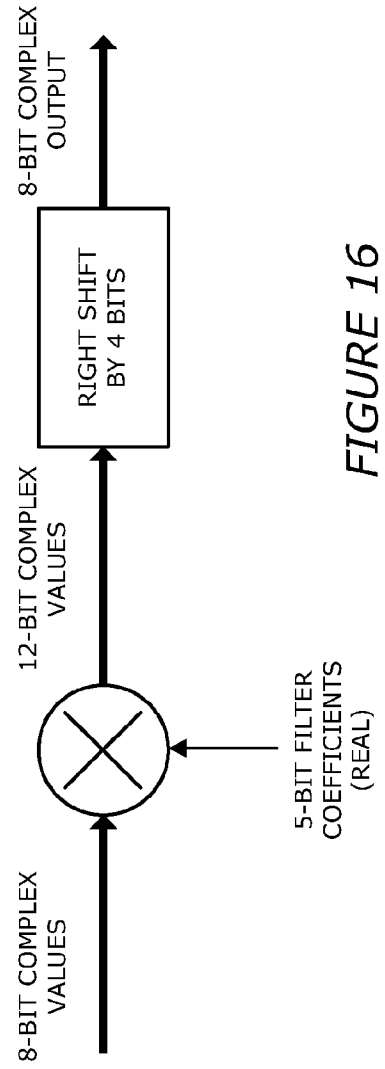


FIGURE 16

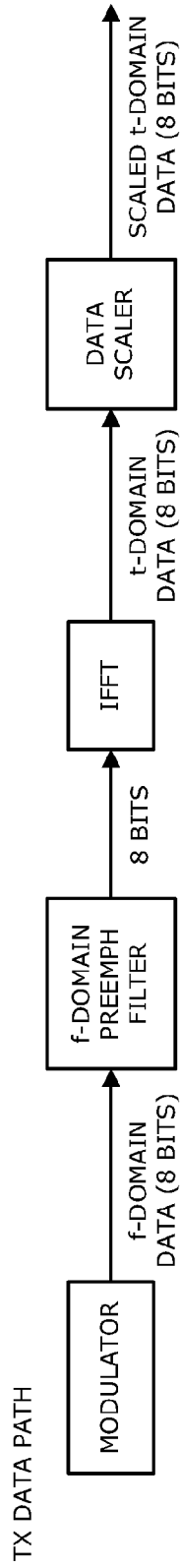


FIGURE 17A

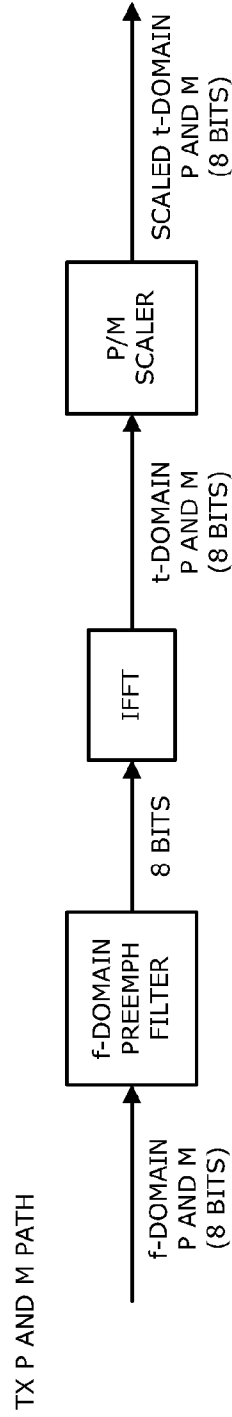


FIGURE 17B

11/20

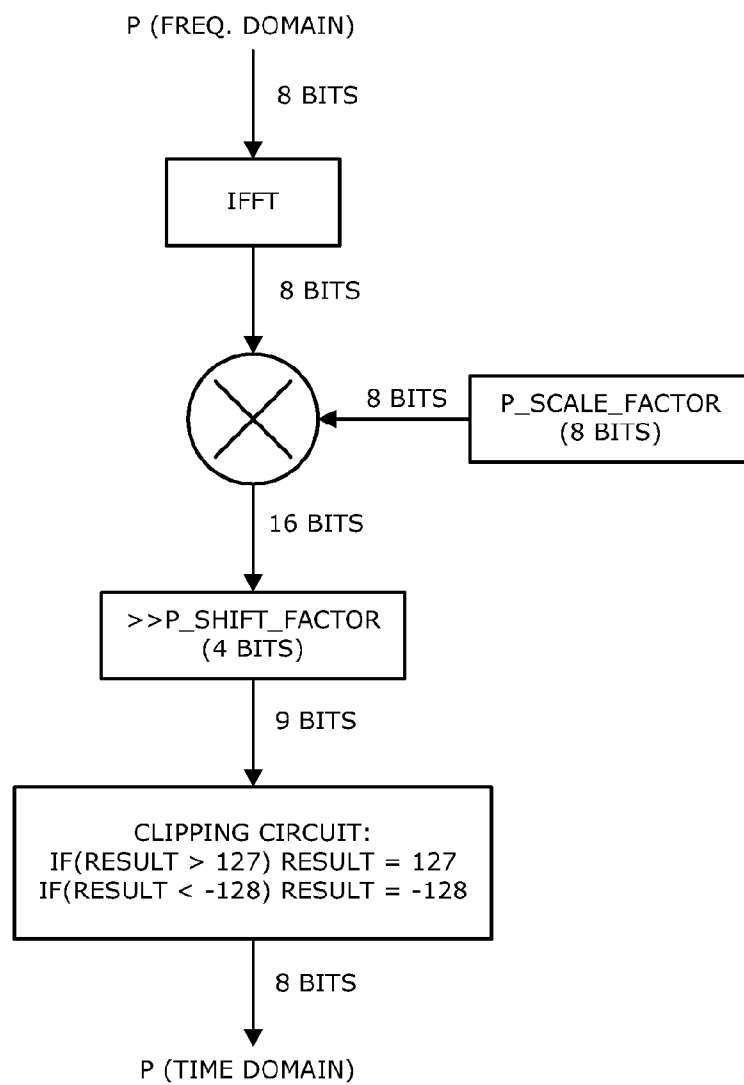


FIGURE 17C

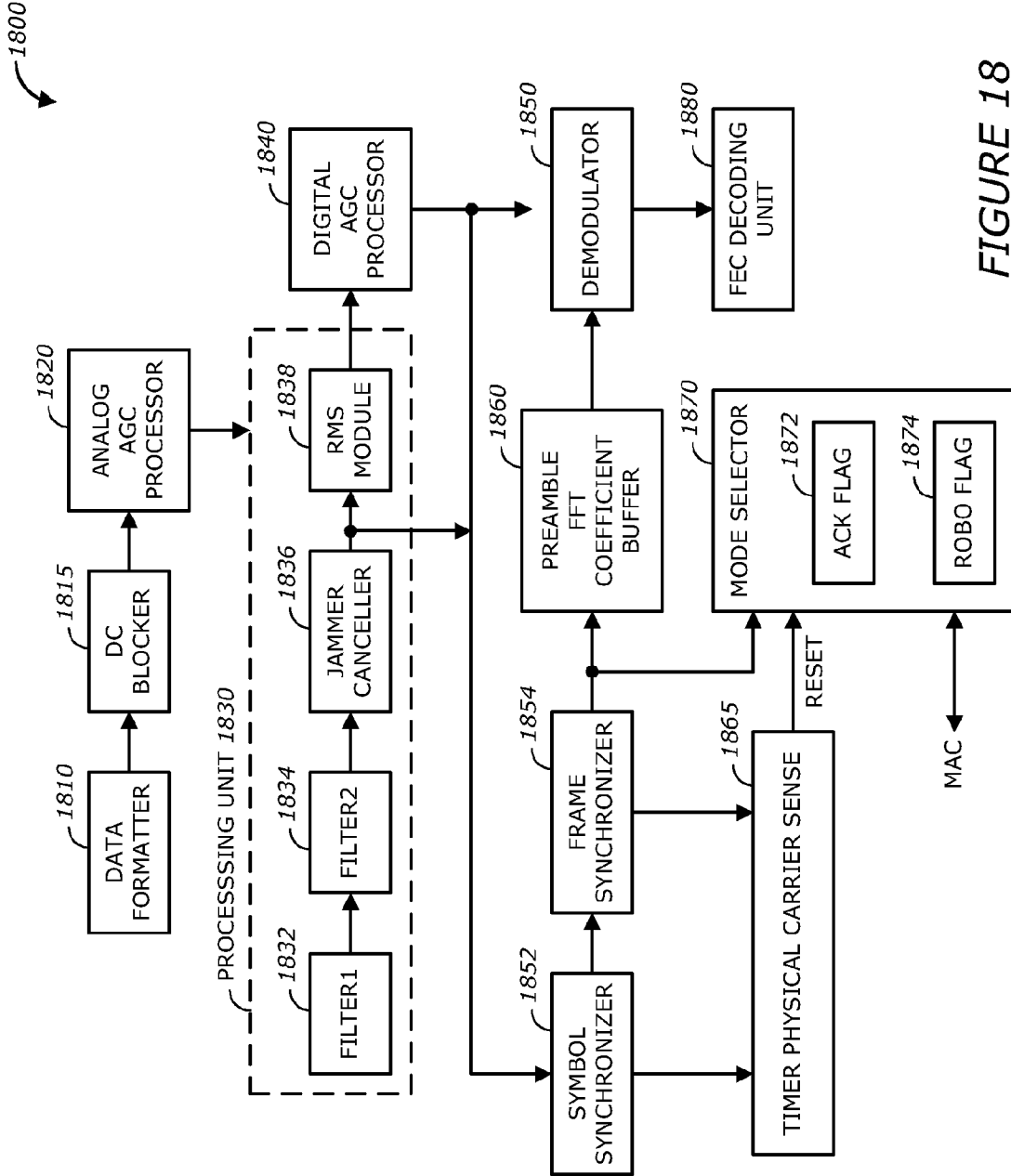


FIGURE 18

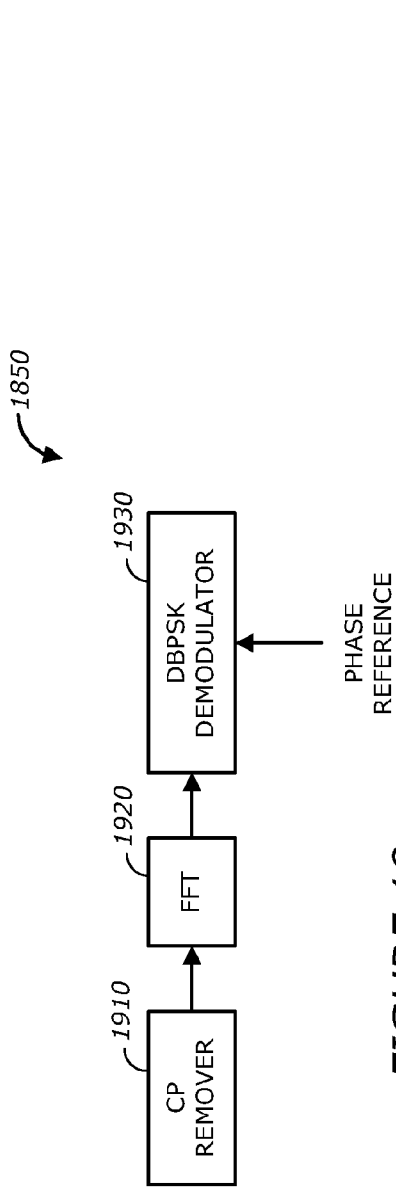


FIGURE 19

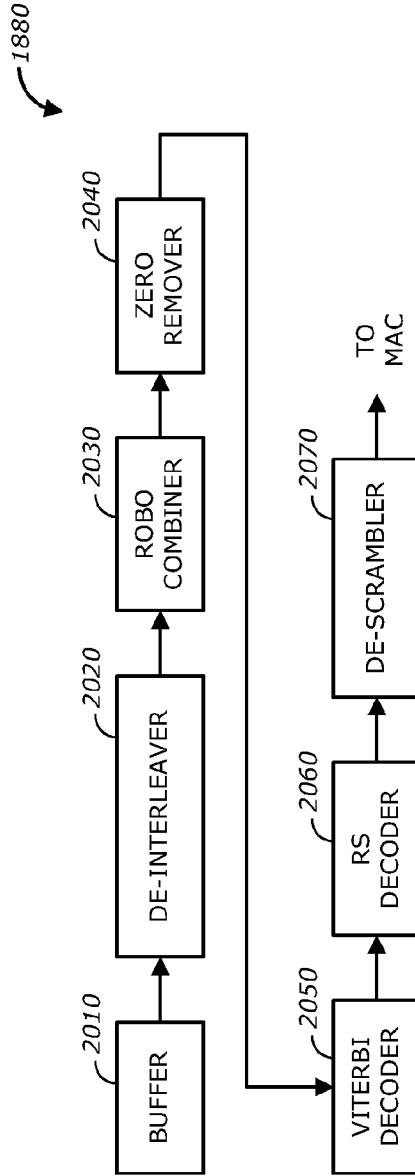


FIGURE 20

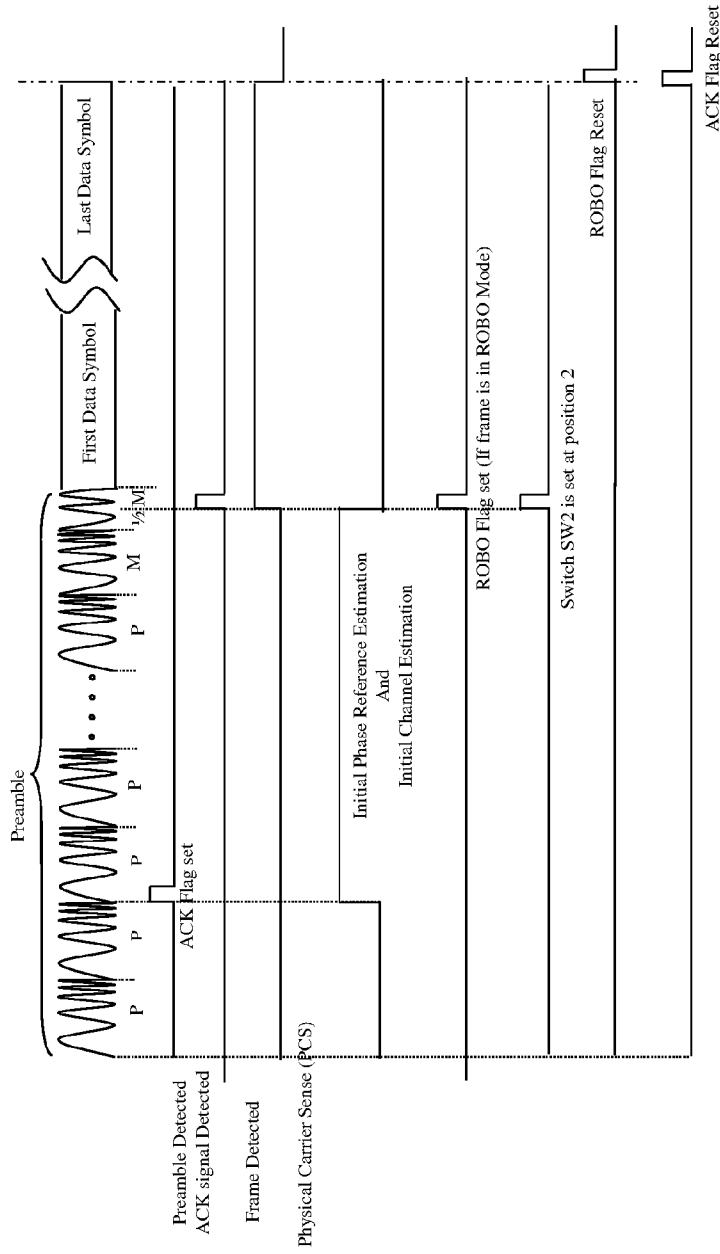


FIGURE 21

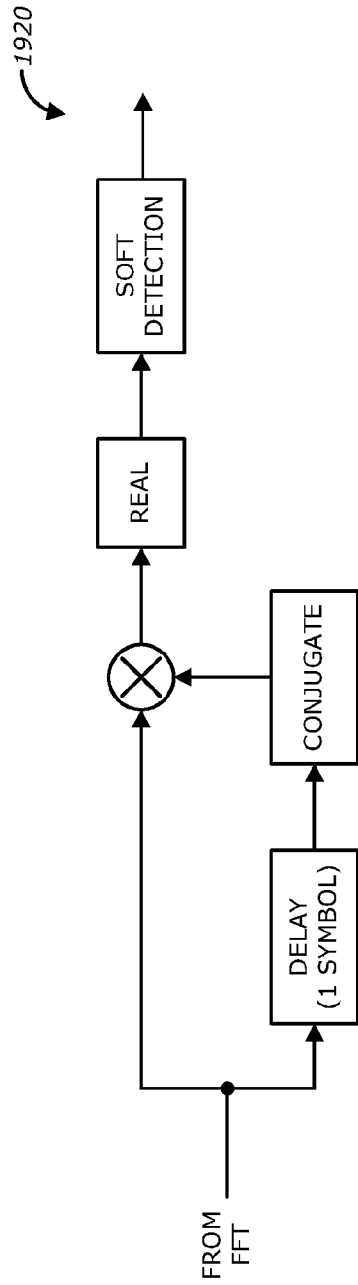


FIGURE 24

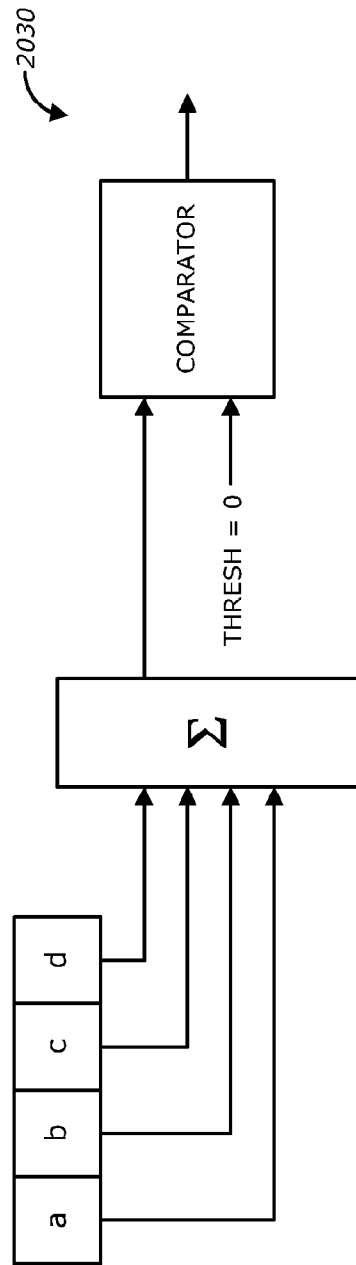


FIGURE 25

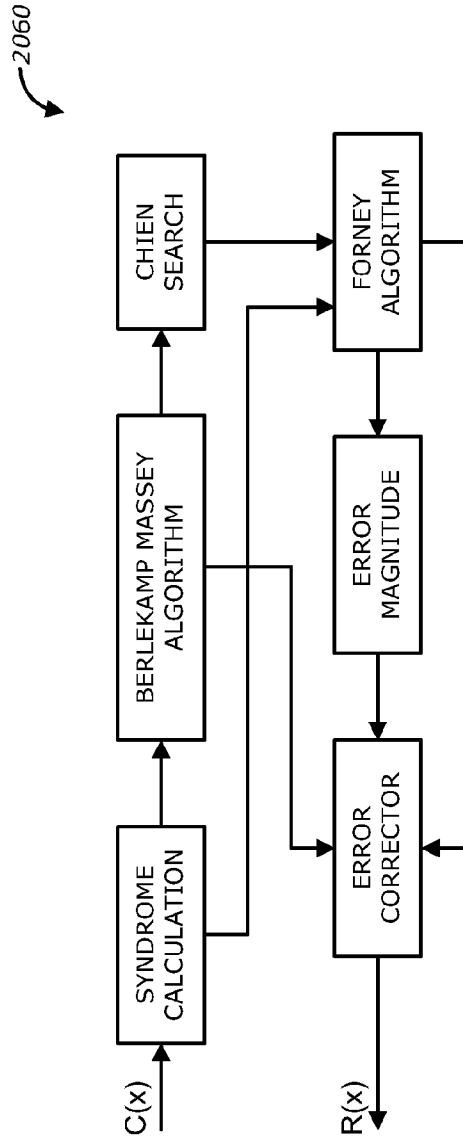


FIGURE 26

2700

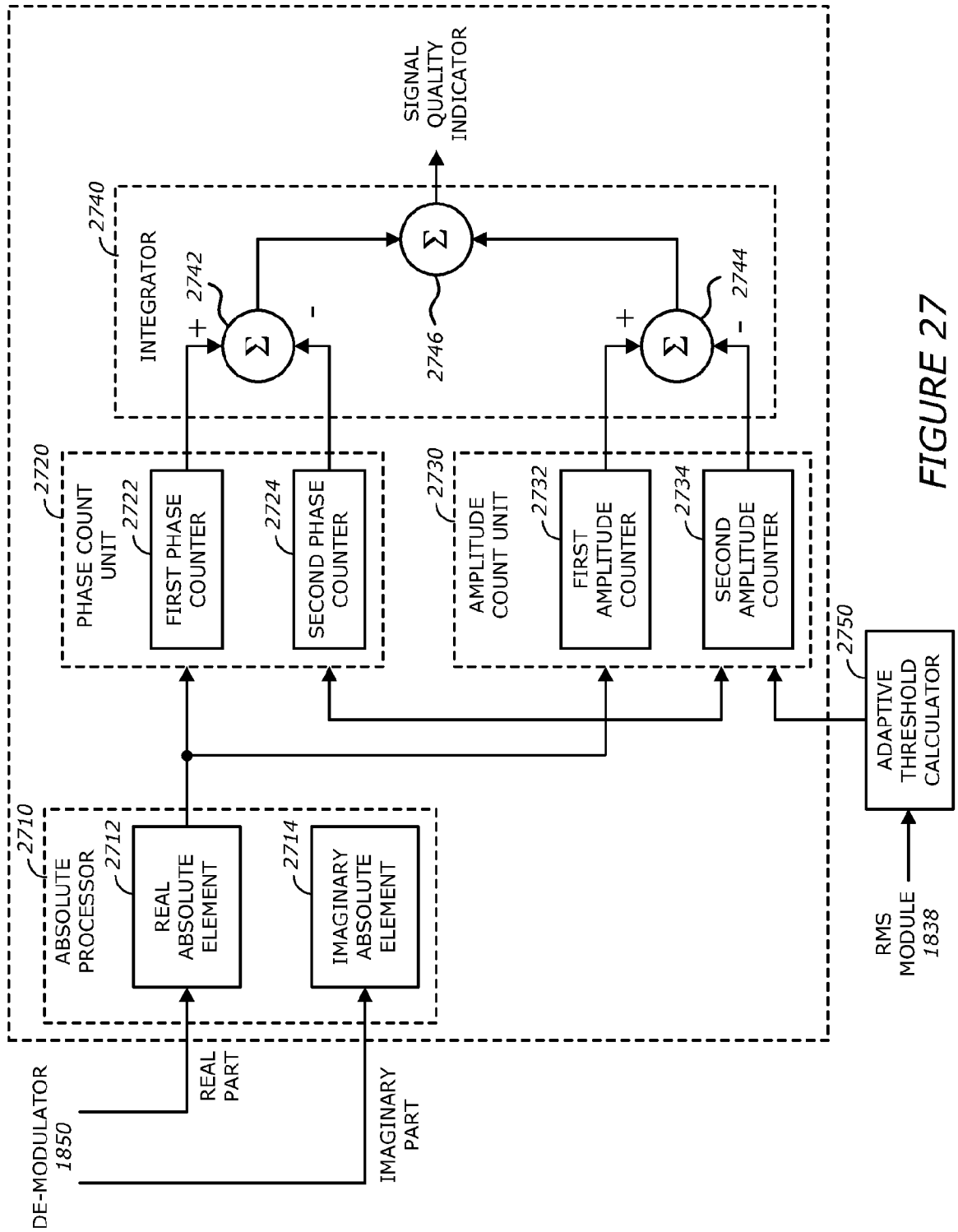


FIGURE 27

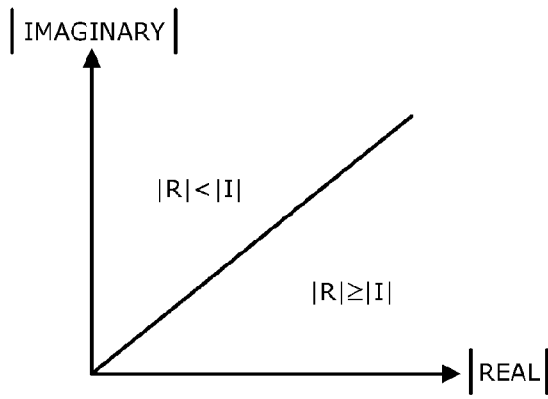


FIGURE 28A

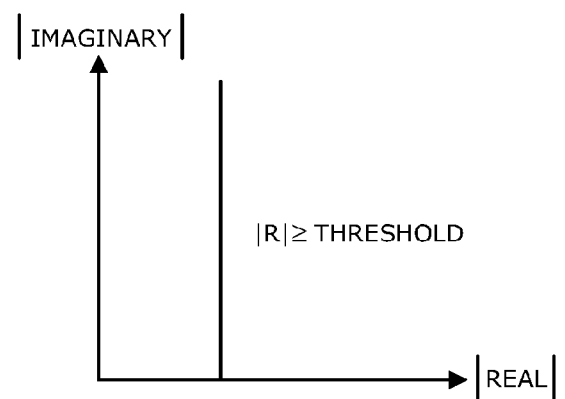


FIGURE 28B

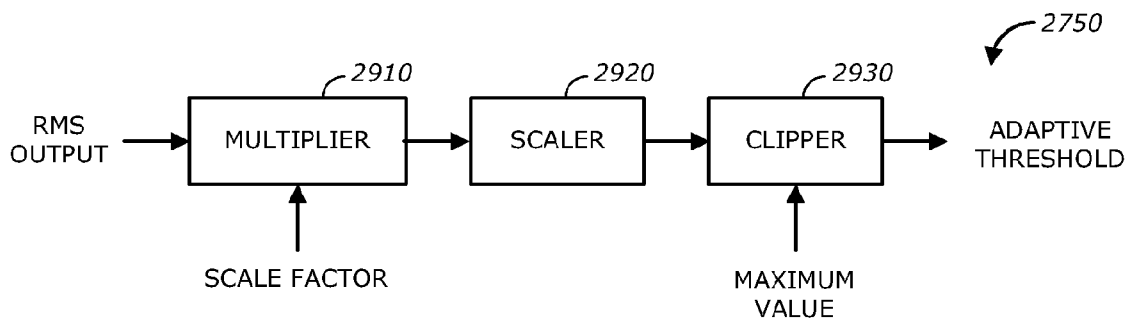
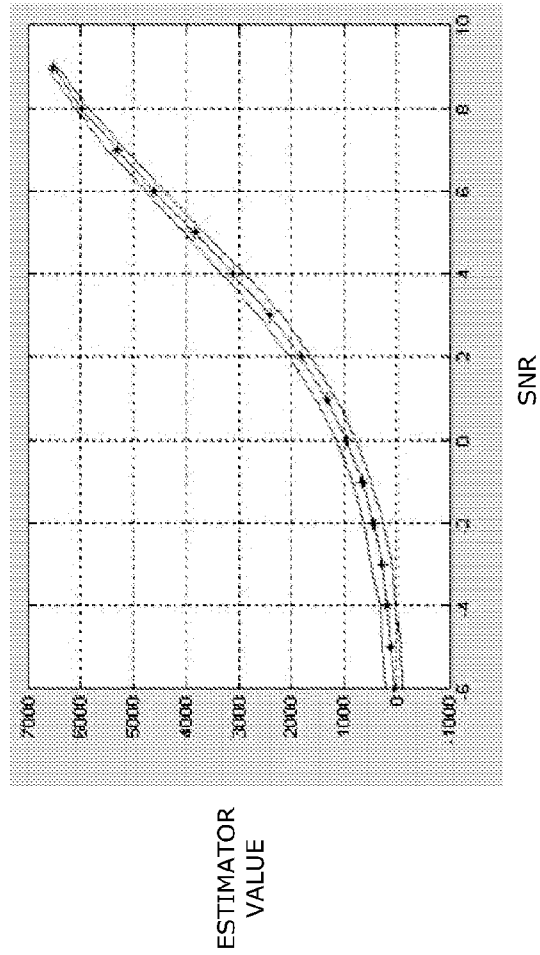
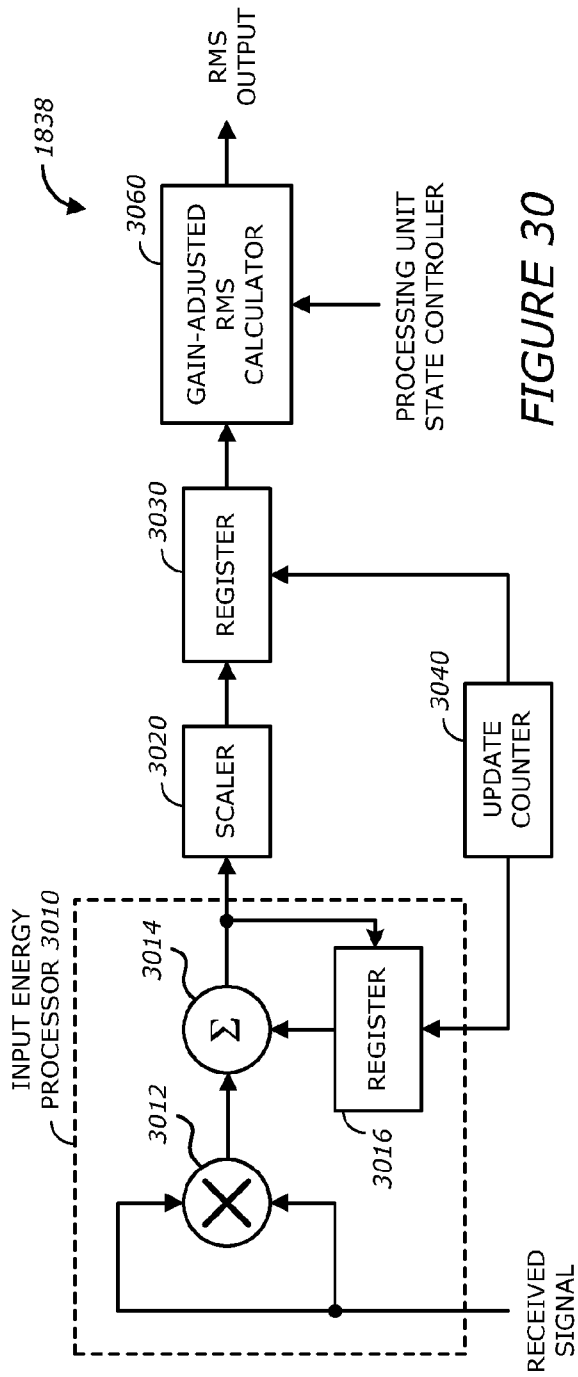


FIGURE 29



INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/046507

A. CLASSIFICATION OF SUBJECT MATTER INV. H04B3/54 H04L1/20 H04L27/26		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H04L H04B		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practical, search terms used) EPO-Internal, COMPENDEX, INSPEC		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 866 580 A (MATSUSHITA ELECTRIC IND CO LTD [JP]) 23 September 1998 (1998-09-23) page 6, line 21 - page 7, line 38 -----	1-22
A	WO 02/49263 A (VALENCE SEMICONDUCTOR INC [US]) 20 June 2002 (2002-06-20) paragraph [0036] - paragraph [0038]; figures 4,5 -----	1-22
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input checked="" type="checkbox"/> See patent family annex.		
* Special categories of cited documents :		
A document defining the general state of the art which is not considered to be of particular relevance *E* earlier document but published on or after the international filing date *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) *O* document referring to an oral disclosure, use, exhibition or other means *P* document published prior to the international filing date but later than the priority date claimed		*T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art. *&* document member of the same patent family
Date of the actual completion of the international search <p align="center">24 September 2009</p>		Date of mailing of the international search report <p align="center">01/10/2009</p>
Name and mailing address of the ISA/ European Patent Office, P.B. 5618 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016		Authorized officer <p align="center">Giglietto, Massimo</p>

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2009/046507

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
EP 0866580	A	23-09-1998	CN 1196621 A	21-10-1998
			DE 69836775 T2	31-10-2007
			JP 3568353 B2	22-09-2004
			JP 10262023 A	29-09-1998
			US 6111921 A	29-08-2000
WO 0249263	A	20-06-2002	US 2003007576 A1	09-01-2003