

Description

[0001] The present invention relates to an integrated current reference circuit using two interconnected current mirrors.

[0002] It is known to provide a constant current generating circuit using two interconnected current mirrors, of which one current mirror is of p FETs and the other is of n FETs. Such circuits have traditionally required one of the branches of the current generator to contain a resistor.

[0003] Use of resistors in integrated circuits is not desirable for a number of reasons, for instance because of the temperature dependence thereof, because of the area occupied by a resistor and the difficulty of manufacture.

[0004] The present invention therefore aims to at least partly mitigate the difficulties of the prior art.

[0005] According to the present invention there is provided an integrated current reference circuit comprising a first and a second current mirror, each current mirror having a respective diode connected transistor controlling a respective controlled transistor, the diode connected transistor of the first current mirror being connected to the controlled transistor of the second current mirror and the diode connected transistor of the second current mirror being connected to the controlled transistor of the first current mirror to form two branches connected between a positive and a negative supply rail, the two transistors of one of said current mirrors having mutually different threshold voltages.

[0006] Preferably one of said two transistors has a lower width to length ratio, and a lower threshold voltage than the other of said two transistors.

[0007] Alternatively the transistors of the other of said current mirrors are of mutually different current-carrying ability.

[0008] Preferably the two transistors of said one of said current mirrors are n FETs.

[0009] Advantageously the current reference circuit further comprises an output transistor controlled by the diode-connected transistor of the other of said current mirrors.

[0010] Preferably said output transistor is a p FET.

[0011] An embodiment of the present invention will be described, by way of example only, with reference to the accompanying drawings in which:-

Figure 1 shows a prior art constant current generating apparatus;

Figure 2 shows a current reference circuit in accordance with the present invention; and

Figure 3 shows a graph of current vs voltage for two transistors of Figure 2.

[0012] In the various figures like reference numer-

als refer to like parts.

[0013] Referring to Figure 1, a current reference circuit according to the prior art consists of a first current mirror comprising a first p FET 11 having a gate connected in common with its drain and a source connected to a positive supply terminal 1, and a second p FET 10 having a source connected to the positive supply terminal 1 and a gate connected to the commoned gate/drain electrodes of the first transistor 11.

[0014] The circuit further comprises a second current mirror which consists of a first n FET 12 having a gate electrode connected in common with its drain electrode, and a source electrode connected to a negative supply terminal 2. The second current mirror has a second n FET 13 whose gate is connected to the commoned gate and drain electrodes of the first n FET 12. The source of the second n FET 13 of the second current mirror is connected via a resistor 15 to the negative supply terminal 15.

[0015] The gate electrode of the second n FET 13 is also connected to the gate electrode of an output transistor 14, which has a source electrode connected to the negative supply terminal 2, the drain 15 of the output transistor 14 providing a circuit output.

[0016] The commoned gate and drain electrodes of the first transistor 11 of the first current mirror constitutes a controlling node of that current mirror and the drain of the second transistor 10 of the first current mirror constitutes a controlled node of that current mirror. As is known to those skilled in the art, as the parameters of the transistors 10 and 11 are matched by virtue of their being formed on an integrated circuit, application of a current to the controlling node causes a corresponding current at the controlled node, depending on the relative sizes of the transistors.

[0017] Similarly, the commoned gate and drain electrodes of the first transistor 12 of the second current mirror constitutes a controlling node of the second current mirror whereas the drain of the second transistor 13 of the second current mirror constitutes the controlled node of that transistor.

[0018] Further reference to Figure 1 shows that the controlled node of the first current mirror is connected to the controlling node of the second current mirror and the controlling node of the first current mirror is connected to the controlled node of the second current mirror.

[0019] In the arrangement described, the second transistor 13 of the second current mirror is "stronger" than the first transistor 12 of the second current mirror. It will be clear to those skilled in the art that the arrangement shown in Figure 1 has in fact two stable operating conditions, namely one in which no current flows through either current mirror and a second state in which a non-zero current is sunk by the output terminal 15.

[0020] Considering the second stable state, with second n FET 13 having a conductivity which is n times that of the first n FET 12. Naming the current through

the controlling transistor 11 of the first current mirror and the controlled transistor 13 of the second current mirror as I_2 , and the current through the controlled transistor 10 of the first current mirror and the controlling transistor 12 of the second current mirror as I_1 , the following arise:-

[0021] The first current mirror constrains the two currents such that

$$I_1 = I_2$$

[0022] The second current mirror constrains the two currents such that

$$I_2 = n \times I_1$$

[0023] Clearly these two constraints alone cannot be satisfied. However, the source potential of the transistor 13 is increased by the current flow through the resistor 15. This reduces the gate-source potential, and thus the ability of transistor 13 to conduct current under the bias conditions provided by the transistor 12.

[0024] The result is that the two currents I_1 and I_2 reach an equilibrium condition at which the two currents become equal and independent of the voltage applied to the circuit.

[0025] Referring now to Figure 2, the first current mirror comprising p FETs 10 and 11 also has an output p FET 24 having a gate terminal connected to the commoned gate terminals of transistors 10 and 11, and a source terminal connected to the positive supply 1.

[0026] The output transistor has an output 25 from its drain node.

[0027] The second current mirror comprises a first n FET 22 and a second n FET 23, of which the first n FET 22 has its gate connected to its drain to form the controlling node of the current mirror, this node being connected to the drain of the first transistor 10 of the first current mirror. The second n FET 23 is the controlled transistor and has its drain node connected to the controlling node of the first current mirror, at the commoned gate and drain nodes of the second p FET 11 of that current mirror. Both of the n FETs have source connections made to the second lower power supply line 2.

[0028] In this embodiment, the first n FET 22 has a higher width to length ratio than does the second n FET 23. Moreover, the first n FET 22 has a higher threshold voltage V_{THH} than the threshold voltage V_{THS} of the second n FET 23.

[0029] Again, in this embodiment the first p FET 10 and the second p FET 11 are identical so that the current I_1 is equal to the current I_{11} .

[0030] Referring now to Figure 3, which shows the variation of drain source current I_{ds} with gate source voltage V_{gs} for the transistors 22 and 23 it will be seen that the transistor 23 due to having a relatively lower threshold voltage, starts to conduct at a lower gate source voltage V_{THS} , but that the rate of increase of

current with increasing voltage is relatively low. By contrast, the first transistor 22 starts to conduct at a higher gate source voltage V_{THH} but its rate of change of current with applied voltage is substantially higher. Thus the two current characteristics for the transistors intersect at a unique current value I_{dsc} .

[0031] This unique value is independent of the supply voltage and determines the current output from the output node 25.

[0032] On a more quantitative basis, for a general transistor the drain source current I_{ds} is proportional to the product of the size of the transistor and the square of the difference between the applied gate source voltage and the threshold voltage.

[0033] Hence a transistor having larger size (width to length ratio) has a larger drain current per applied voltage. Moreover a transistor having a higher threshold voltage turns on at a higher voltage than a transistor having a lower threshold voltage.

[0034] The embodiment described with respect to Figures 2 and 3 combines differential size and differential threshold voltage in the n transistors. It will be understood by those skilled in the art that the two transistors 22 and 23 could be made identical in size, although having different threshold voltages with the current being determined instead by differential sizing of the p transistors 10 and 11. In such an arrangement, the low threshold voltage transistor (for example transistor 23) is supplied with a relatively low current from the corresponding transistor (here 11) of the other current mirror. By contrast, the high threshold voltage transistor (here 22) is supplied with a relatively high current from the corresponding transistor (here 10) of the other current mirror.

[0035] It will of course be understood that by suitably proportioning the transistor 24 with respect to the transistors 10 and 11 of the first current mirror, different values of output current can be achieved.

Claims

1. An integrated current reference circuit comprising a first and a second current mirror, each current mirror having a respective diode connected transistor controlling a respective controlled transistor, the diode connected transistor of the first current mirror being connected to the controlled transistor of the second current mirror and the diode connected transistor of the second current mirror being connected to the controlled transistor of the first current mirror to form two branches connected between a positive and a negative supply rail, the two transistors of one of said current mirrors having mutually different threshold voltages.
2. An integrated current reference circuit as claimed in claim 1 wherein one of said two transistors has a lower width to length ratio and a lower threshold

voltage than the other of said two transistors.

3. An integrated current reference circuit as claimed in claim 1 wherein the transistors of the other of said current mirrors are of mutually different current-carrying ability. 5
4. An integrated current reference circuit as claimed in any preceding claim wherein the two transistors of said one of said current mirrors are n FETs. 10
5. An integrated current reference circuit as claimed in any preceding claim further comprising an output transistor controlled by the diode-connected transistor of the other of said current mirrors. 15
6. An integrated current reference circuit as claimed in claim 5 wherein said output transistor is a p FET.

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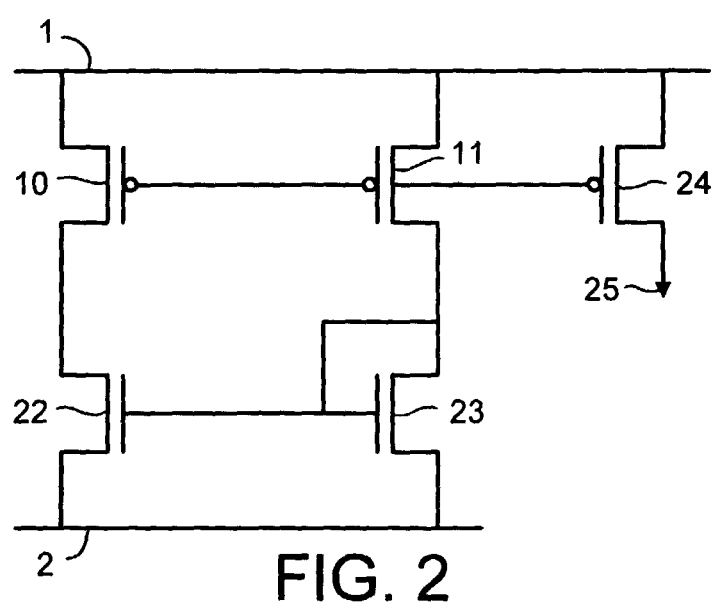
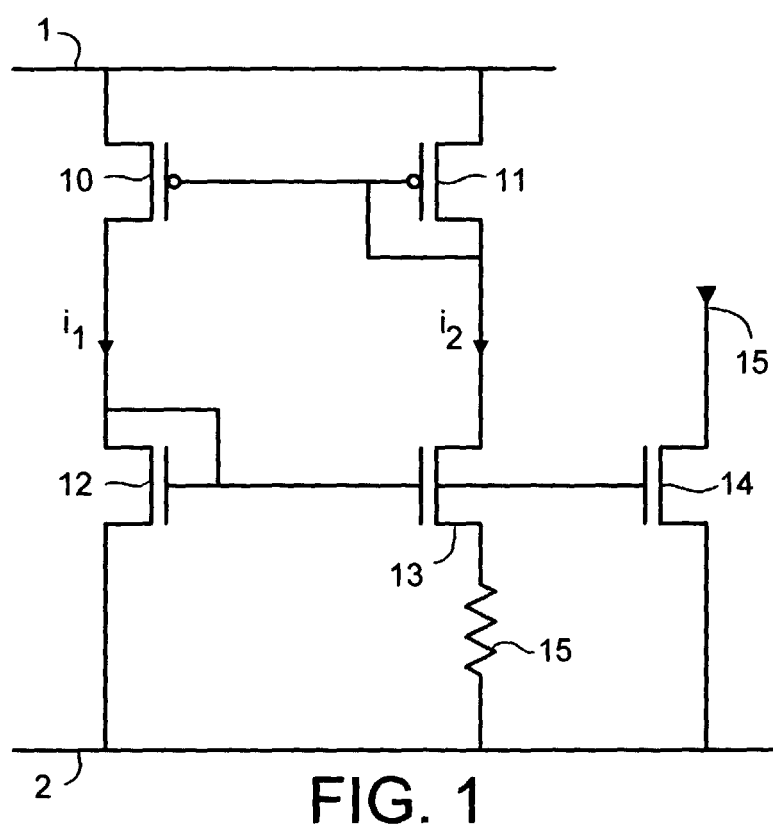
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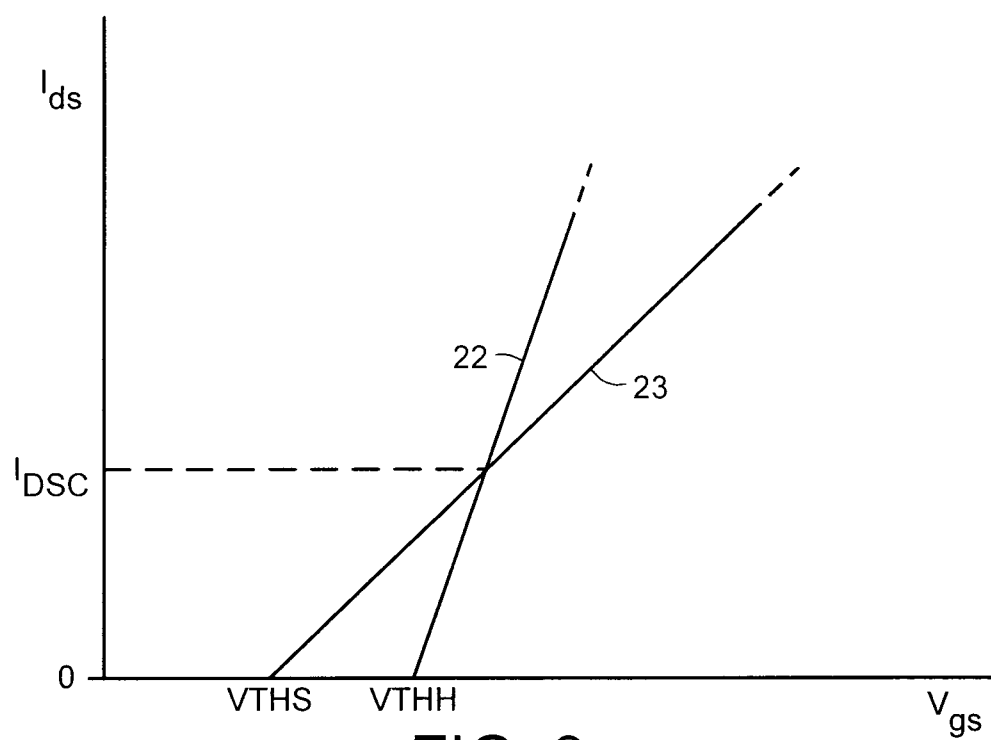


FIG. 3



European Patent
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EUROPEAN SEARCH REPORT

Application Number
EP 00 30 4668

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	GB 2 071 955 A (PHILIPS NV) 23 September 1981 (1981-09-23) * the whole document *	1-6	G05F3/26
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Place of search THE HAGUE		Date of completion of the search 6 October 2000	Examiner Schobert, D
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

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**ANNEX TO THE EUROPEAN SEARCH REPORT
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EP 00 30 4668

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06-10-2000

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