The present invention relates to a high voltage switch circuit, comprising an input port adapted to receive a pulse type input current and an output port, which can be used selectively to conduct an output current to a corresponding electrical load. The switch circuit comprises a buffer stage adapted to sense the input voltage at said input port and to provide a buffered voltage that follows said input voltage. The switch circuit comprises complementary switches electrically connected between said input port and said output port and a voltage level translator electrically connected with said switches, said buffer stage and a control terminal that provides a control signal. The voltage level translator provides suitable gate voltages at the gate terminals of said switches, so that the operation of these latter can be controlled by said control signal.
FIG. 4
FIG. 5
HIGH VOLTAGE CURRENT SWITCH CIRCUIT

[0001] The present invention relates to an electronic circuit of analog type, which can be of integrated type or realized with discrete components.

[0002] In particular, the present invention relates to a high voltage switch circuit for switching current signals, namely pulse type current signals, between an input port and a selectable output port.

[0003] In many applications, for example in the biomedical sector, multiplexers are used when it is necessary to supply a desired current signal to an output port, which can be activated selectively.

[0004] Italian patent application nr. MI2007A000595 describes a high voltage pulsed current generation circuit for a neuromuscular electrical stimulator. This document shows the use of a multiplexer having an input port adapted to receive a pulse type current signal, generated by a stimulation circuit, and a plurality of output ports, each of which can be selected to provide said current signal to a corresponding pair of stimulation electrodes.

[0005] Multiplexers, substantially of a type similar to the one described above, can also be used in biomedical applications of different type, such as in ultrasonic scanning apparatus.

[0006] Often, these devices do not have satisfactory galvanic isolation to ground of the output ports. In many devices, even if intended for use, for example, in biomedical applications, in which the presence of effective galvanic isolation is a very important design requirement, it is possible to encounter the presence of non-negligible leakage currents to ground. The intensity of said leakage currents increases, generally not linearly, with the voltage at the terminals of the input/output port.

[0007] Many prior art multiplexers have high power consumption, both in stand-by mode and during operation, which increases significantly if high voltages are present at the terminals of the input/output ports.

[0008] Another example of electronic stimulation device is disclosed in U.S. Pat. No. 5,052,391.

[0009] In this document, an electronic circuit to provide high voltage, high rise-time, and charge balanced current pulses is disclosed.

[0010] This electronic circuit does not actually have current multiplexing functionalities but it basically provides for the splitting of one output for a parallel connection with a plurality of output channels.

[0011] Moreover, such a circuit shows relevant drawbacks in terms of weight and size, since multiple transformers have to be used to transfer the energy of a stimulation pulse to the corresponding output channels. The overall bulkiness of such a system makes it difficult to use in portable stimulators.

[0012] Further, the output current supplied to each output port is often subject to relevant waveform distortions due to the current adsorbed by the adopted switching devices.

[0013] The main object of the present invention is to provide a switch circuit, which is capable of overcoming the drawbacks described above.

[0014] A further object of the present invention is to provide a switch circuit that can be controlled by logic type signals to switch an input current towards a selectable output port.

[0015] A further object of the present invention is to provide a switch circuit, in which input and output terminals have high impedance to ground for voltages within the specification ranges.

[0016] A further object of the present invention is to provide a switch circuit having low quiescent and active power consumption for voltages within the specification ranges.

[0017] A further object of the present invention is to provide a switch circuit that can be supplied by high voltage power supplies.

[0018] A further object of the present invention is to provide a switch circuit that is easy to produce at industrial level, as an integrated circuit or as a discrete component circuit, at competitive costs with respect to prior art devices.

[0019] These objects, together with other objects that will be more apparent from the subsequent description and from the accompanying drawings, are achieved, according to the invention, by a high voltage switch circuit according to claim 1, proposed hereafter, and the related dependent claims which refer to preferred embodiments of the present invention.

[0020] Further characteristics and advantages of the present invention will be more apparent with reference to the description given below and to the accompanying figures, provided purely for explanatory and non-limiting purposes, wherein:

[0021] FIG. 1A, 1B illustrate block diagrams showing the general operation and structure of the high voltage switch circuit, according to the present invention;

[0022] FIG. 2 illustrates a block diagram of a multiplexer comprising the high voltage switch circuit, according to the present invention;

[0023] FIG. 3 illustrates a block diagram of the output stage included in an embodiment the high voltage switch circuit, according to the invention;

[0024] FIG. 4 schematically illustrates the buffer stage included in the high voltage switch circuit, according to the invention;

[0025] FIG. 5-6 illustrate in more details the circuit structure of the output stage of the high voltage switch circuit, in the embodiment shown in FIG. 3.

[0026] With reference to the aforesaid figures, the present invention relates to a high voltage switch circuit 1.

[0027] The high voltage switch circuit 1 is particularly adapted for use in a muscular or neuromuscular electrical stimulator and it will now be described with reference to such an implementation for simplicity of exposition.

[0028] However, this is not intended to limit in any way the scope of the present invention.

[0029] In fact, the switch circuit 1 can be used in different biomedical applications, for example in an ultrasonic device, or in other types of devices in which it is necessary to selectively activate a plurality of current controlled ports, such as micro-electromechanical devices or systems (MEMS).

[0030] Referring to FIGS. 1A-1B, the switch circuit 1 comprises an input port IN adapted to receive an input current $I_{IN}$.

[0031] The input current $I_{IN}$ is predefined and is generated by a current generator circuit 500, electrically connected with a pair of terminals (positive and negative) $IN^+$ and $IN^-$ of the input port IN.

[0032] The input current $I_{IN}$ has a pulse type waveform, preferably of unipolar type.

[0033] The switch circuit 1 comprises an output port $O_1$ that can receive the input current $I_{IN}$ and conduct an output current $I_{O_1}$ to a corresponding electrical load $L$. 

[0034] The output circuit is the subject matter of the present invention.

[0035] The output circuit is described in detail in the following.

[0036] The output current $I_{O_1}$ is provided by the output port $O_1$ of the switch circuit 1.
The switch circuit 1 is capable of directing the input current $I_y$ to the output port $O_2$ when this latter is selected to conduct the output current $I_{y2}$ to the load $L_T$. An input voltage $V_{IN}$ is present between the terminals IN$^+$ and IN$^-$ of the input port IN, which is a function of the input current $I_y$ and of the downstream equivalent impedance seen from the terminals of the input port IN.

The input voltage $V_{IN}$ can assume high values, for example values of a few hundreds of volts in an electrical stimulator.

The switch circuit 1 comprises an electronic buffer stage BUF that is electrically connected to the input port IN. The buffer stage BUF is adapted to sense the input voltage $V_{IN}$ at the terminals IN$^+$, IN$^-$ of the input port IN, and to supply, at a buffer output BF, a buffered voltage $V_{BUF}$ which follows the sensed input voltage $V_{IN}$.

The switch circuit 1 comprises complementary switches $T_1$, $T_2$ that operate as current switches and are electrically connected between the input port IN and the output port $O_2$.

The switch circuit 1 comprises a first control terminal $K_1$ for providing a first control signal $C_1$ of logic type (for example at 0V and 3.3V).

Preferably, the switch circuit 1 is operates associated with an electronic control stage COM adapted to generate the control signal $C_1$ and to send it to the control terminal $K_1$ connected thereto.

In some embodiments of the present invention, the control stage COM may be physically included in the switch circuit 1.

Preferably, the control stage COM may comprise a digital processing device, for example a microprocessor, or a shift register or another circuit of similar type.

The switch circuit 1 comprises a first voltage level translator $A_1$ that is electrically connected with the buffer stage BUF, with the switches $T_1$, $T_2$ and with the control terminal $K_1$.

The voltage level translator $A_1$ is adapted to provide a first and second gate voltage $V_{G1}$, $V_{G2}$ respectively at a first and a second gate terminal $G_1$, $G_2$ of the first and second switch $T_1$, $T_2$ to control said switches through the control signal $C_1$.

Depending on the control signal $C_1$, the switches $T_1$, $T_2$ enable or disable the flow of the input current $I_{y2}$ from the input port IN to the output port $O_2$, thus providing or blocking a current path from the input port $I_{y}$ to the output port $O_2$ for the input current $I_{y2}$.

The connectivity between the input port IN and each output port $O_1$ is determined by the control signal $C_1$ that selects the output port $O_1$ to receive the input current $I_{y1}$.

The output current provided by the switches $T_1$, $T_2$ is thus equal to $(I_{y1} + C_1)$ where $C_1$ is a logic signal having logic values equal to 0 or 1.

The adoption of the voltage level translator $A_1$ for providing the gate voltages $V_{G1}$, $V_{G2}$ is quite advantageous since it allows to properly set the voltage across the gate-source junctions of the switches $T_1$, $T_2$ in order to make it possible to control (in particular to turn on) said switches through the control signal $C_1$. The switches $T_1$, $T_2$ are in fact transistors in which the voltage across the gate-source junction may vary, since they have the source terminals electrically connected with the terminals of the input port IN.

As shown in FIGS. 1B and 3, the switches $T_1$, $T_2$, the voltage level translator $A_1$ and the input terminal $K_1$ form an output circuit $NET_1$ that is comprised in an electronic output stage $M_1$ of the switch circuit 1.

The output stage $M_1$ is electrically connected to the input port IN, the buffer stage BUF, the output port $O_2$ and preferably to the control stage COM.

According to a preferred embodiment of the present invention (FIG. 4), the buffer stage BUF comprises a circuit structure divided into two sections, substantially symmetrical with respect to ground.

Each of the aforesaid sections comprises a sensing circuit $B_1$, $B_2$ arranged in such a manner as to sense the voltage of a corresponding terminal IN$^+$, IN$^-$ of the input port IN, and a voltage follower circuit $F_1$, $F_2$ arranged in such a manner that the voltage of the positive and negative terminals $BF^+$, $BF^-$ of the buffer output BF follow the sensed voltage.

This solution makes it possible to maintain a high impedance to ground for the input port IN and the buffer output BF, the voltages at the terminals of which are floating with respect to ground.

The buffer output BF provides, between the terminals BF$^+$, BF$^-$, the buffered voltage $V_{BUF}$ that follows the variations of the voltage $V_{IN}$ at the terminals IN$^+$, IN$^-$ of the input port IN.

This makes it possible to power the voltage level translator $A_1$ with high voltages ($V_{PP}$ and $V_{NN}$) that are different from $V_{IN}$ thereby without introducing significant distortions (for example due to unwanted current absorptions) in the input current $I_{y}$ when this latter flows toward the output port $O_2$.

In a first section, the buffer stage BUF preferably comprises a first sensing circuit $B_1$ and a first follower circuit $F_1$.

Preferably, the sensing circuit $B_1$ is electrically connected with the positive terminal IN$^+$ of the input port IN, with the sensing node $S_1$ and with a first power supply $V_{CC}$.

The sensing circuit $B_1$ senses the voltage of the positive terminal IN$^+$ of the input port IN and establishes an offset with respect to this voltage to compensate the threshold gate-source voltage of a transistor $T_1$ of the voltage follower circuit $F_1$ and prevent an unwanted conduction of the switch $T_1$.

Preferably, the sensing circuit $B_1$ comprises a Zener diode $D_{z1}$ and a capacitor $Z_{cap}$, connected in parallel between the positive terminal IN$^+$ and the sensing node $S_1$.

The diode $D_{z1}$ advantageously prevents from overvoltages at the sensing node $S_1$ while the capacitor $Z_{cap}$ maintains the voltage offset with respect to the voltage of the positive terminal IN$^+$.

Preferably, the sensing circuit $B_1$ comprises a resistor $R_{z1}$ and a diode $D_{z2}$ electrically connected in series between the power supply $V_{CC}$ and the sensing node $S_1$.

The voltage follower circuit $F_1$ is electrically connected with the sensing node $S_1$, with the positive terminal $BF^+$ of the buffer output BF and with a second power supply $V_{PP}$ which is a high voltage power supply.

In the voltage follower circuit $F_1$, the voltage of the positive terminal $BF^+$ substantially follows the voltage of the positive terminal IN$^+$.

Preferably, the voltage follower circuit $F_1$ comprises the transistor $T_2$, for example an n-type enhancement mode MOSFET, connected between the power supply $V_{PP}$ and grounded through the resistor $R_{z2}$.

The transistor $T_2$ has the gate terminal connected with the sensing node $S_1$, the drain terminal connected with
the power supply $V_{PS}$ and the source terminal connected with the terminal $BF^+$ and to a resistor $R_{250}$, in turn connected with ground.

[0067] Operation of the first section of the stage $BUF$ is now described in greater detail.

[0068] When there is no current flow toward the load $I_{L}$ (e.g. the input current $I_{IN}$ has no current pulses) the sensing node $S_{1}$ is at a voltage approximately equal to $V_{CC}$.

[0069] The voltage of the terminal $BF^-$ is therefore approximately equal to $V_{IN}$ minus the voltage drop on the network composed of the circuit elements $Z_2$, $Z_{21}$, $D_{24}$ and $R_2$, and the voltage $V_{GSOH}(19)$, i.e. the threshold gate-source voltage of the transistor $T_{10}$.

[0070] The voltage of the sensing node $S_{1}$ follows the voltage of the terminal $IN^+$, so that the voltage of the terminal $BF^-$ follows the voltage of the terminal $IN^+$ and the switch $T_{1}$ is in an OFF state.

[0071] If there is a current flowing toward the load $I_{L}$ (i.e. the switch $T_{1}$ is in an ON state), the voltage of the terminal $IN^+$ depends substantially on the voltage drop across said load. In this case, the voltage variations at the terminal $IN^+$ are sensed by the sensing circuit $B_{2}$ and followed by the voltage at the terminal $BF^-.

[0072] A second section of the buffer stage $BUF$ preferably has a circuit structure substantially symmetrical to that of the first section described above, which comprises a second sensing circuit $B_{2}$ and a second follower circuit $F_{2}$.

[0073] Preferably, the sensing circuit $B_{2}$ is electrically connected with the negative terminal $IN^-$ of the input port $IN$, with a second sensing node $S_{2}$ and with a third power supply $V_{PD}$.

[0074] The sensing circuit $B_{2}$ senses the voltage of the negative terminal $IN^-$ of the input port $IN$ and establishes a voltage offset with respect thereto to compensate the threshold gate-source voltage of a transistor $T_{10}$ of the follower circuit $F_{2}$ and prevent an undesired conduction of the switch $T_{2}$.

[0075] Preferably, the sensing circuit $B_{2}$ comprises a Zener diode $D_{22}$ and a capacitor $Z_{22}$ connected in parallel between the negative terminal $IN^-$ and the sensing node $S_{2}$.

[0076] The diode $D_{22}$ advantageously prevents from overvoltages at the sensing node $S_{2}$ while the capacitor $Z_{22}$ maintains the voltage offset with respect to the voltage of the negative terminal $IN^-.

[0077] Preferably, the sensing circuit $B_{2}$ comprises a resistor $R_{250}$ and a diode $D_{24}$ electrically connected in series between the power supply $V_{PD}$ and the sensing node $S_{2}$.

[0078] The follower circuit $F_{2}$ is electrically connected with the sensing node $S_{2}$ and with the negative terminal $BF^-$ of the buffer output $BF$.

[0079] In the follower circuit $F_{2}$, the voltage of the negative terminal $BF^-$ substantially follows the voltage of the negative terminal $IN^-.

[0080] Preferably, the follower circuit $F_{2}$ comprises the transistor $T_{10}$, for example a $p$-type enhancement mode MOSFET, connected between a fourth power supply $V_{NN}$ which is a high voltage power supply, and ground through the resistor $R_{250}$.

[0081] In the transistor $T_{10}$, the gate terminal is connected with the sensing node $S_{1}$, the drain terminal is connected with the power supply voltage $V_{NN}$ and the source terminal of the transistor $T_{10}$ is electrically connected with the terminal $BF^-$ and to a resistor $R_{250}$, in turn connected with ground.

[0082] Operation of the second section of the stage $BUF$ is substantially similar to that of the first section.

[0083] When there is no current flow toward the load $I_{L}$ (e.g. the input current $I_{IN}$ does not have current pulses), the sensing node $S_{2}$ is at a voltage approximately equal to $V_{PD}$.

[0084] The voltage of the terminal $BF^-$ is therefore approximately equal to $V_{IN}$ minus the voltage drop on the network composed of the circuit elements $D_{22}$, $Z_{22}$, $D_{24}$ and $R_2$, and the voltage $V_{GSOH}(19)$, i.e. the threshold gate-source voltage of the transistor $T_{10}$.

[0085] The voltage of the sensing node $S_{2}$ follows the voltage of the terminal $IN^-$, so that the voltage of the terminal $BF^-$ follows the voltage of the terminal $IN^-$ and the switch $T_{2}$ is in OFF state.

[0086] If there is current flow toward the load $I_{L}$ (i.e. the switch $T_{2}$ is in a ON state), the voltage of the terminal $IN^-$ depends substantially on the voltage drop across said load.

[0087] In this case, the voltage variations at the terminal $IN^-$ are sensed by the sensing circuit $B_{2}$ and followed by the voltage at the terminal $BF^-.

[0088] The buffer stage $BUF$ is thus capable of supplying a buffered voltage $V_{BUF}$ that follows the input voltage $V_{IN}$ with a small power consumption and negligible distortions of the input current $I_{IN}$.

[0089] The structure of the first output circuit $NET_1$, in a preferred embodiment of the switch circuit $I$ of the present invention (FIGS. 3 and 5), is now described in greater detail.

[0090] As mentioned above, the output circuit $NET_1$ comprises the switches $T_{1}$, $T_{2}$, the voltage level translator $A_{1}$ and the control terminal $K_1$.

[0091] Preferably, the output circuit $NET_1$ comprises a first output $Y_{1}$, electrically connected with the output port $O_{1}$.

[0092] The first output $Y_{1}$ comprises a pair of terminals (positive and negative) $Y_{1}^{+}$, $Y_{1}^{-}$ electrically connected with a pair of terminals (positive and negative) $O_{1}^{+}$, $O_{1}^{-}$ the output port $O_{1}$.

[0093] As shown in FIG. 3, the output $Y_{1}$ is electrically connected with the output port $O_{1}$ in such a manner that the output current $I_{NP}$ which is supplied by the output port $O_{1}$ to the corresponding electrical load $L_{1}$ has a waveform with the same polarity as the input current $I_{IN}$.

[0094] In this case, the terminals $Y_{1}^{+}$, $Y_{1}^{-}$ of the output $Y_{1}$ are electrically connected with the terminals $O_{1}^{+}$, $O_{1}^{-}$ the output port $O_{1}$ with direct polarity, i.e. with the positive terminal $Y_{1}^{+}$ electrically connected with the positive terminal $O_{1}^{+}$ and the negative terminal $Y_{1}^{-}$ electrically connected with the negative terminal $O_{1}^{-}$ the output port $O_{1}$.

[0095] Of course, the output $Y_{1}$ may be electrically connected with the output port $O_{1}$ in such a manner that the output current $I_{NP}$ has a waveform with reversed polarity with respect to the input current $I_{IN}$.

[0096] The switch $T_{1}$ is electrically connected between the positive terminal $IN^+$ of the input port $IN$ and the positive terminal $Y_{1}^{+}$ of the output $Y_{1}$ and the switch $T_{2}$ is electrically connected between the negative terminal $IN^-$ of the input port $IN$ and the negative terminal $Y_{1}^{-}$ of the output $Y_{1}$.

[0097] The switches $T_{1}$ and $T_{2}$ are complementary and are preferably field effect transistors (J-FETs or MOSFETs), respectively of $p$- and $n$-enhancement mode type.

[0098] Advantageously, the transistors $T_{1}$ and $T_{2}$ are arranged to have the drain terminals electrically connected with the terminals $Y_{1}^{+}$ and $Y_{1}^{-}$ and the source terminals electrically connected with the terminals $IN^+$ and $IN^-$, respectively.
In this way, when the transistors $T_1$ and $T_2$ are in conduction state (switches $T_1$ and $T_2$ in ON state), the input current $I_{IN}$ can flow from the terminals of the input port IN to the terminals of the output $Y_1$.

Instead, when the two transistors $T_1$ and $T_2$ are in cut-off state (switches $T_1$ and $T_2$ in OFF state), the passing of the input current $I_{IN}$ toward the output $Y_1$ is prevented.

As mentioned above, the voltage level translator $A_1$ is advantageously adapted to control the switches $T_1$ and $T_2$ through the control signal $C_1$.

The voltage level translator $A_1$ is electrically connected between the terminals (positive and negative) $BF^+$, $BF^-$ of the buffer output $BF$ and with the gate terminals $G_1$, $G_2$ of the switches $T_1$ and $T_2$.

The voltage level translator $A_1$ comprises a first polarization circuit including the circuit series of the resistor $R_1$, the third transistor $T_3$, the resistor $R_2$, the fourth transistor $T_4$ and the resistor $R_3$.

The transistors $T_1$, $T_2$ are preferably bipolar junction transistors (BJT), respectively of npn and pnp type, and are adapted to enable/prevent flow of a first polarization current $I_{PF}$, along said first polarization circuit.

The transistors $T_3$, $T_4$ are arranged in such a manner to be controlled by the terminal $K_1$, according to the state of the control signal $C_1$.

Preferably, the transistor $T_3$ has its collector terminal electrically connected with the resistor $R_3$, which is in turn connected in series with the positive terminal $BF^+$ of the buffer output $BF$, and is connected with the control terminal $K_1$, at the base terminal thereof.

Instead, the transistor $T_4$ has the base terminal connected to ground and the collector terminal electrically connected with the resistor $R_3$, which is in turn connected in series with the negative terminal $BF^-$ of the buffer output $BF$.

The transistors $T_3$ and $T_4$ have their emitter terminals connected with the terminals of the resistor $R_3$.

As an alternative, the transistors $T_3$, $T_4$ may have their base terminals connected to the ground and to the terminal $K_1$, respectively.

Preferably, the voltage level translator $A_1$ comprises a first circuit network to protect the switches $T_1$ and $T_2$ (in particular their gate terminals $G_1$, $G_2$) against over-voltages.

This protective network advantageously comprises first and second over-voltage protection elements $D_1$ and $D_2$ (preferably Zener diodes) that are respectively connected between the gate terminals $G_1$, $G_2$ of the transistors $T_1$ and $T_2$ and the terminals $IN^+$ and $IN^-$ of the input port IN.

Preferably, the voltage level translator $A_1$ also comprises some stabilizing circuit elements, such as the resistor $R_3$ and the capacitor $C_1$, connected in parallel with the resistor $R_3$, and the protection resistor $R_4$ and $R_5$, connected in series with the base terminals of the transistor $T_3$ and $T_4$, respectively.

Operation of the output circuit $NET_1$ is now described in greater detail.

Let us assume that the output circuit $NET_1$ is initially in a deactivated or stand-by state and the terminal $K_1$ receives a control signal $C_1$ at "low" logic level.

The transistors $T_1$ and $T_2$ are in the cut-off state and there is no flow of the polarization current $I_{PF}$.

If the input current $I_{IN}$ does not have any current pulses, the voltage at the terminal $BF^+$ is approximately $V_{GSS}(T_1)$ while the voltage at the terminal $BF^-$ is approximately $V_{DSS}(T_1)$, where $V_{GSS}(T_1)$ and $V_{DSS}(T_1)$ are the gate-source voltages of the transistors $T_1$ and $T_2$, respectively.

If the input current $I_{IN}$ has a current pulse, the voltage at the terminals $BF^+$ and $BF^-$ increases up to $V_{PF}$ and $V_{NN}$ respectively.

In both cases, as there is no flow of the polarization current $I_{PF}$, the voltage level translator $A_1$ provides gate voltages $V_{PF}$, $V_{NN}$ to the gate terminals $G_1$, $G_2$, such as to maintain the switches $T_1$ and $T_2$ in the cut-off state.

From the above, it is evident how, with a control signal $C_1$ at a "low" logic level, whatever the voltage $V_{IN}$ and the input current $I_{IN}$ (within the specification range of the circuit), the switches $T_1$ and $T_2$ remain in the OFF state and the input current $I_{IN}$ cannot flow toward the output $Y_1$.

The output circuit $NET_1$ is therefore maintained in deactivated or stand-by state.

When the terminal $K_1$ receives a control signal $C_1$ at "high" logic level, the transistors $T_1$ and $T_2$ are taken to conduction state and the polarization current $I_{PF}$ can flow.

In this situation, before the switching of the transistors $T_3$, $T_4$ is completed, the voltage at the terminals $BF^+$ and $BF^-$ initially tends to increase up to $V_{PF}$ and $V_{NN}$ respectively.

Due to the voltage drop across the resistors $R_1$ and $R_3$, which is determined by flow of the current $I_{PF}$, the voltage level transistor $A_1$ provides gate voltages $V_{PF}$, $V_{NN}$ to the gate terminals $G_1$, $G_2$, such as to take the switches $T_1$ and $T_2$ to the conduction state (ON state).

The switches $T_1$ and $T_2$ are taken to the ON state and the input current $I_{IN}$ is free to flow toward the output $Y_1$.

At this point, the voltage at the terminals $BF^+$ and $BF^-$ depends substantially on the voltage across the load $L_f$ but the voltage drop across the resistors $R_1$ and $R_3$, due to flow of the current $I_{PF}$, ensures that the gate terminals $G_1$, $G_2$ are always at voltages such as to maintain the switches $T_1$ and $T_2$ in conduction state.

Therefore, with a control signal $C_1$ at a high logic level, whatever the voltage $V_{IN}$ and the input current $I_{IN}$ (within the specification range of the circuit), the switches $T_1$ and $T_2$ are always in ON state and the input current $I_{IN}$ can flow toward the output $Y_1$.

From the above, it is apparent that the voltage level translator $A_1$ provides a voltage level shifting of the control signal $C_1$, to safely control the switches $T_1$, $T_2$, despite of the variations of the input voltage $V_{IN}$, since these latter are constantly followed by the buffered voltage $V_{BB}$.

Given that the terminals of the output $Y_1$ are preferably connected with direct polarity to the terminals of the output port $O_2$, the output current $I_{PF}$ supplied to the electrical load $L$, has a waveform with the same polarity as the input current $I_{IN}$.

In other words, the condition $II_f = I_{PF}$, is obtained.

In this way, when the output circuit $NET_1$ is enabled by the control signal $C_1$ to transmit an input current $I_{IN}$ of pulse type toward the output port $O_2$, the output current $I_{PF}$ has pulses with the same polarity and amplitude as the pulses of the input current $I_{IN}$.

When the terminal $K_1$ again receives a control signal $C_1$ at "low" logic level, the transistors $T_1$ and $T_2$ return to the cutoff state and ideally there should be no flow of the polarization current $I_{PF}$. 
[0132] In this situation, in fact, the voltage level translator $A_1$ supplies, respectively to the gate terminals $G_1$, $G_2$ voltages $V_{p1}$, $V_{p2}$ such as to take the transistors $T_1$, $T_2$ to cut-off state (OFF state).

[0133] Regardless of this, due to the presence of stray capacitances between the gate terminals $G_1$, $G_2$ and the terminal IN$^*$ of the input port IN, the transistors $T_1$, $T_2$ do not switch immediately but are taken to OFF state only when the input current $I_{IN}$ reaches zero, i.e. at the end of the input current pulse.

[0134] Based on the above, it can be observed that:

[0135] Activation of the output circuit NET$_1$ is determined simply by the transition of the control signal $C_3$ from a “low” logic level to a “high” logic level,

[0136] the deactivation of the output circuit NET$_1$ is instead determined by transition of the control signal $C_3$ to “low” logic level by the pass of the input current $I_{IN}$ through zero.

[0137] It is therefore evident how the output circuit NET$_1$ behaves, from a functional viewpoint, in a manner substantially similar to that of a DIAC electronic device.

[0138] In an embodiment of the present invention, particularly suitable for use in a muscular or neuromuscular electrical stimulator, the switch circuit 1 comprises the fifth and sixth complementary switches $T_{5}$, $T_{6}$ that operate as current switches and that are electrically connected between the input port IN and the output port $O_p$ in parallel with the switches $T_1$, $T_2$.

[0139] The switch circuit comprises a second control terminal $K_2$ for providing a second control signal $C_2$ of logic type.

[0140] Preferably, the second control signal $C_2$ is received from the control stage COM.

[0141] The switch circuit 1 comprises a second voltage level translator $A_2$ that is electrically connected with the buffer stage BUF with the switches $T_5$, $T_6$ and with the control terminal $K_2$.

[0142] The voltage level translator $A_2$ is adapted to provide a third and fourth gate voltage $V_{p3}$, $V_{p4}$ respectively at a third and fourth gate terminal $G_3$, $G_4$ of the switches $T_5$, $T_6$ in order to control these latter through the control signal $C_2$.

[0143] Depending on the control signal $C_2$, the switches $T_5$, $T_6$ can enable or disable the flow of the input current $I_{IN}$ from the input port IN to the output port $O_p$ thereby providing or blocking a current path from the input port IN towards the output port $O_p$ for the input current $I_{IN}$.

[0144] The connectivity between the input port IN and each output port $O_p$ is determined by the control signal $C_2$ and the output current provided by the switches $T_5$, $T_6$ is thus equal to ($I_{IN}$* $C_2$), where $C_2$ is a logic signal having logic values equal to 0 or 1.

[0145] The adoption of the voltage level translator $A_2$ for providing the gate voltages $V_{p3}$, $V_{p4}$ is quite advantageous since it allows to properly set the voltage across the gate-source junction of the switches $T_5$, $T_6$ in order to make it possible to control (in particular to turn on) them through the control signal $C_2$.

[0146] As shown in FIGS. 3 and 6, the switches $T_5$, $T_6$, the voltage level translator $A_2$ and the control terminal $K_2$ form an output circuit NET$_2$, which is comprised in an output stage $M_3$ of the switch circuit 1 and which is connected between the input port IN and the output port $O_p$ as the output circuit NET$_1$.

[0147] Referring to FIG. 6, the output circuit NET$_2$ has a circuit structure similar to that of the circuit NET$_1$, described above.

[0148] The output circuit NET$_2$ comprises a second output $Y_2$ electrically connected with the output port $O_p$.

[0149] The second output $Y_2$ comprises a pair of terminals (positive and negative) $Y_{2+}$, $Y_{2-}$ electrically connected with the terminals $O_{2+}$, $O_{2-}$ of the output port $O_p$.

[0150] Preferably, the output circuit NET$_2$ is electrically connected with the output port $O_p$ in such a manner that the output current $I_{2P}$, which is supplied by the output port $O_p$ to the corresponding electrical load $L_p$, has a waveform with reverse polarity with respect to that of the input current $I_{IN}$.

[0151] In this case, the terminals $Y_{2+}$, $Y_{2-}$ of the output $Y_2$ are electrically connected with the terminals $O_{2+}$, $O_{2-}$ of the output port $O_p$ with reverse polarity, i.e. with the positive terminal $Y_{2+}$ electrically connected with the negative terminal $O_{2-}$ and the negative terminal $Y_{2-}$ electrically connected with the positive terminal $O_{2+}$ of the output port $O_p$.

[0152] Of course, the output circuit NET$_2$ may be electrically connected with the output port $O_p$ in such a manner that the output current $I_{2P}$ has a waveform with direct polarity with respect to the input current $I_{IN}$.

[0153] The switch $T_5$ is electrically connected between the positive terminal $IN^*$ of the input port $IN$ and the positive terminal $Y_{2+}$ of the output $Y_2$ and the switch $T_6$ is electrically connected between the negative terminal $IN^*$ of the input port $IN$ and the negative terminal $Y_{2-}$ of the output $Y_2$.

[0154] The switches $T_5$ and $T_6$ are complementary and preferably effect field effect transistors (FET or MOSFET), respectively of p- and n-port enhancement mode type.

[0155] Advantageously, the switches $T_5$ and $T_6$ are arranged in such a manner as to have the drain terminals electrically connected with the terminals $Y_{2+}$ and $Y_{2-}$ and the source terminals electrically connected with the terminals $IN^*$ and IN*, respectively.

[0156] In this way, when the transistors $T_5$ and $T_6$ are in conduction state (switches $T_5$ and $T_6$ in ON state), the input current $I_{IN}$ can flow from the terminals of the input port IN to the terminals of the output $Y_2$.

[0157] Instead, when the transistors $T_5$ and $T_6$ are in the cut-off state (switches $T_5$ and $T_6$ in OFF state), the passage of the input current $I_{IN}$ toward the output $Y_2$ is prevented.

[0158] Preferably, the voltage level translator $A_2$, adapted to control the transistors $T_5$ and $T_6$, is electrically connected between the terminals (positive and negative) BF$^*$ and BF$^*$ of the buffer output BF and with the gate terminals $G_3$, $G_4$ of the switches $T_5$ and $T_6$.

[0159] The voltage level translator $A_2$, advantageously comprises a second polarization circuit formed by the circuit series consisting of the resistor $R_{11}$, the seventh transistor $T_7$, the resistor $R_{12}$, the eighth transistor $T_8$ and the resistor $R_{13}$.

[0160] The transistors $T_5$ and $T_6$ are preferably bipolar junction transistors (BJT), respectively of nnp and pnp type, and are adapted to enable/prevent flow of a second polarization current $I_{p2}$ along said second polarization circuit.

[0161] Preferably, the transistor $T_7$ has its collector terminal electrically connected with the resistor $R_{11}$, in turn connected in series with the positive terminal BF$^*$ of the buffer output BF, and is connected with the terminal $K_3$ at the base terminal thereof.

[0162] The transistor $T_8$ has the base terminal connected with ground and the collector terminal electrically connected...
with the resistor $R_{13}$, in turn connected in series with the negative terminal $BF^-$ of the buffer output $BF$.

[0163] The transistors $T_2$ and $T_8$ have their emitter terminals connected to the terminals of the resistor $R_{12}$.

[0164] As an alternative, the transistors $T_7$, $T_9$ may have their base terminals connected to the ground and to the terminal $K_2$, respectively.

[0165] Preferably, the voltage level translator $A_3$ comprises a second circuit network to protect the gate terminals of the transistors $T_7$ and $T_9$ against over-voltages.

[0166] This protective network advantageously comprises third and fourth over-voltage protection elements $D_{10}$ and $D_{11}$ (preferably Zener diodes) that are respectively connected between the gate terminals $G_3$, $G_4$ of the transistors $T_7$ and $T_9$ and the terminals $IN^+$ and $IN^-$ of the input port $I_{in}$.

[0167] Preferably, the voltage level translator $A_3$ also comprises some stabilizing circuit elements, such as the resistor $R_{14}$ and the capacitor $C_{10}$, connected in parallel with the resistor $R_{12}$, and the protection resistor $R_{10}$ and $R_{11}$ connected in series with the base terminals of the transistors $T_7$ and $T_9$, respectively.

[0168] Operation of the output circuit $NET_2$ is similar to that of the output circuit $NET_1$.

[0169] Let us assume that the output circuit $NET_2$ is initially in a deactivated state and the terminal $K_2$ receives a logic control signal $C_2$ at “low” level. The transistors $T_7$ and $T_9$ are in the cut-off state and there is no flow of the polarization current $I_{p2}$.

[0170] In this situation, the presence or absence of pulses of the input current $I_{p2}$, the gate terminals of the switches $T_7$ and $T_9$ are always at gate voltages $V_{p3}$, $V_{p4}$ such as to maintain them in a cut-off state.

[0171] Therefore, with a control signal $C_2$, at a low logic level, the switches $T_7$ and $T_9$ remain in the OFF state and the input current $I_{o2}$ cannot in any case flow toward the output $Y_2$.

[0172] The output circuit $NET_2$ is therefore maintained in a deactivated or stand-by state.

[0173] When the terminal $K_2$ receives a logic control signal $C_2$ at “high” level, the transistors $T_7$ and $T_9$ switch to conduction state and the polarization current $I_{p2}$ can flow.

[0174] In this situation, due to the voltage drop across the resistors $R_{11}$ and $R_{13}$, determined by the flow of the current $I_{p2}$, the gate terminals $G_3$, $G_4$ of the transistors $T_7$ and $T_9$ are polarized at gate voltages $V_{p3}$, $V_{p4}$ such as to take the transistors $T_7$ and $T_9$ to conduction state.

[0175] The switches $T_7$ and $T_9$ are then taken to the ON state and the input current $I_{o2}$ is free to flow toward the output $Y_2$.

[0176] At this point, the voltage at the terminals $BF^+$ and $BF^-$ depends substantially on the voltage across the load $I_{p2}$ but the voltage drop across the resistors $R_{11}$ and $R_{13}$, due to circulation of the current $I_{p2}$, ensures that the gate terminals $G_3$, $G_4$ are always at gate voltages $V_{p3}$, $V_{p4}$ such as to maintain the transistors $T_7$ and $T_9$ in conduction state.

[0177] Therefore, with a control signal $C_2$ at high logic level, whatever the voltage $V_{IN}$ and the input current $I_{IN}$ (within the specification range of the circuit), the switches $T_7$ and $T_9$ are always in the ON state and the input current $I_{o2}$ can in any case flow toward the output $Y_2$.

[0178] From the above, it is apparent that the voltage level translator $A_3$ provides a voltage level shifting of the control signal $C_2$ to safely control the switches $T_7$, $T_9$, despite of the variations of the input voltage $V_{IN}$, since these latter are constantly followed by the buffered voltage $V_{BUF}$.

[0179] Given that the terminals of the output $Y_2$ are preferably connected with reverse polarity to the terminals of the output port $O_2$, the output current $I_{o2}$ supplied to the electrical load $I_{p2}$ will have a waveform with reverse polarity with respect to the input current $I_{IN}$.

[0180] In other words, the condition $I_{o2} = -I_{IN}$ is obtained.

[0181] In this way, when the output circuit $NET_2$ is enabled by the control signal $C_2$, the output current $I_{o2}$ toward the output port $O_2$, the output current $I_{o2}$ has pulses with the same amplitude but with reverse polarity with respect to the pulses of the input current $I_{o2}$.

[0182] When the terminal $K_2$ once again receives a control signal $C_2$ at “low” logic level, the transistors $T_7$ and $T_9$ are again taken to the cut-off state and ideally there should be no flow of the polarization current $I_{p2}$.

[0183] In this situation, the voltage level translator $A_3$ supplies, respectively to the gate terminals of the transistors $T_7$ and $T_9$, gate voltages $V_{p3}$, $V_{p4}$ such as to take the same transistors $T_7$ and $T_9$ in the cut-off state.

[0184] Regardless of this, due to the presence of stray capacitances between the gate terminals of the transistors $T_7$, $T_9$ and the terminal $IN^-$ of the input port, the transistors $T_7$, $T_9$ do not switch immediately but are taken to the cut-off state only when the input current $I_{o2}$ reaches zero, i.e. at the end of the input current pulse.

[0185] On the basis of the above, it can be observed that: activity of the output circuit $NET_2$ is determined simply by transition of the control signal $C_2$ from a “low” logic level to a “high” logic level; desactivation of the output circuit $NET_2$ is determined by transition of the control signal $C_2$ at “low” logic level and by passage of the input current $I_{IN}$ through zero.

[0186] Therefore, also the output circuit $NET_2$ behaves, from a functional viewpoint, in a manner substantially similar to that of a DIAC electronic device.

[0187] Referring to FIG. 2, the high voltage switch circuit 1, which does not have multiplexing functionalities per se, is particularly suitable for implementation in a multiplexer 100.

[0190] The multiplexer 100 comprises a common input port $IN$ and a plurality of output ports $O_n$, each of which can be selected by logic control signals.

[0191] The multiplexer 100 receives an input current $I_{IN}$ at the input port $IN$ and it directs it towards the selected output ports $O_n$.

[0192] The multiplexer 100 thus implements a multiplexing function of the type $1 \rightarrow N$, with $N>1$, for the current signals received at the input port $IN$.

[0193] The adoption of the high voltage switch circuit 1 in a multiplexer 100 is particularly advantageous for use in an electrical stimulator.

[0194] In this case, each of the mentioned output ports can be electrically connected with a pair of stimulation electrodes and the output current, supplied by each output port, is the current effectively injected by the electrodes during stimulation, while the electrical load connected to each output port typically consists of the impedance offered by the stimulation electrodes and by the portion of the patient’s body affected by the stimulation current.

[0195] The multiplexer 100 comprises a common buffer stage BUF (as described above), which senses the voltage $V_{IN}$ between the terminals of the input port IN and provides, at the buffer output BUF, a buffered voltage $V_{BUF}$ that substantially follows the input voltage $V_{IN}$. 

[0196] Moreover, the multiplexer 100 is characterized by having an output current $I_{o2}$ substantially equal to the input current $I_{IN}$, so that the current $I_{o2}$ is not sensed by the buffer stage BUF and the voltage $V_{BUF}$ is substantially equal to the input voltage $V_{IN}$. 

[0197] In this way, the buffer stage BUF, which senses the input voltage $V_{IN}$ and operates according to the bipolar switching voltage $V_{BUF}$, is characterized by having a substantially equal input and output voltage, which substantially satisfies the condition $V_{IN} = V_{BUF}$.
The multiplexer 100 comprises a plurality of output stages \( M_i \), each of which is electrically connected with the input port IN, the common buffer stage BUF and a corresponding output port \( O_j \).

Each of the output stages \( M_i \) comprises the output circuit \( \text{NET}_1 \) and preferably also the output circuit \( \text{NET}_2 \), as described above.

Preferably, the control terminals \( K_1 \) (and possibly \( K_2 \)) of each output stage \( M_i \) are electrically connected with a common control stage \( \text{COM} \) that may be physically included in the multiplexer 1.

It is apparent that the common buffer stage BUF and each of the output stages \( M_i \) form a switch circuit 1, according to the invention, which is electrically connected between the input port IN and the corresponding output port \( O_j \) (FIG. 2).

The operation of the multiplexer 100 is now briefly described.

Normally, the output stages \( M_i \) are maintained in a deactivated state.

Therefore, the control signals sent by the control stage \( \text{COM} \) are normally maintained at a "low" logic level.

To direct the input current \( I_{IN} \) toward any desired output port \( O_j \), the control stage \( \text{COM} \) must activate the output circuit \( \text{NET}_1 \) (or optionally the output circuit \( \text{NET}_2 \)) of the output stage \( M_i \) which is operatively associated with the chosen output port \( O_j \).

The control signal \( C_1 \) (or possibly \( C_2 \)) sent to the output circuit \( \text{NET}_1 \) (or possibly \( \text{NET}_2 \)) of the output stage \( M_i \) is therefore taken to "high" logic level, enabling the input current \( I_{IN} \) to flow toward the output port \( O_j \).

If the output \( Y_1 \) (or possibly \( Y_2 \)) of the output circuit \( \text{NET}_1 \) (or \( \text{NET}_2 \)) is connected with direct polarity to the output port \( O_j \), the output current \( I_{O_j} \) has the same waveform as the input current \( I_{IN} \).

If the output \( Y_1 \) (or possibly \( Y_2 \)) of the output circuit \( \text{NET}_1 \) (or \( \text{NET}_2 \)) is connected with reverse polarity to the output port \( O_j \), the output current \( I_{O_j} \) has a waveform with pulses of opposite polarity with respect to the input current \( I_{IN} \).

It can be noted how by suitably managing the output circuit \( \text{NET}_1 \) (or \( \text{NET}_2 \)), one or more pulses of the input current \( I_{IN} \) can be "neutralized", simply by maintaining the control signals \( C_1 \) (or \( C_2 \)) in the "low" logic state. The pulses of the input current \( I_{IN} \) thus "neutralized", do not appear, with direct or reverse polarity, in the output current \( I_{O_j} \).

In this case, the output current \( I_{O_j} \) has a different time distribution of the pulses, with respect to the input current \( I_{IN} \).

Operation of the output stage \( M_j \) as adjusted by the control signals \( C_1, C_2 \), can be summarized in the following exemplificative table:

<table>
<thead>
<tr>
<th>( C_1 )</th>
<th>( C_2 )</th>
<th>( M_j )</th>
<th>( I_{O_j} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>OFF</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Circuit ( \text{NET}_1 ) ON (reversing)</td>
<td>( -I_{IN} )</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Circuit ( \text{NET}_1 ) ON (not reversing)</td>
<td>( I_{IN} )</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Short circuit</td>
<td>( 0 ) (( Y_{\text{NOC}} ))</td>
</tr>
</tbody>
</table>

From the table above it is evident how the output current from each output stage \( M_i \) is equal to \( (I_{IN} \cdot C_1) \) or \( (I_{IN} \cdot C_2) \), where \( C_1, C_2 \) are logic signals that assume the logic values 0 or 1.

The multiplexer 1 is therefore not only capable of reversing the polarity of the pulses of the input current \( I_{IN} \) (for example, by alternately activating the switching circuits \( \text{NET}_1 \) and \( \text{NET}_2 \) where both are present) but also of modifying the waveform of this latter.

The use of the switching circuits \( \text{NET}_1 \) and (optionally) \( \text{NET}_2 \) in each output stage \( M_i \), with the functionalities described above, is particularly useful in the case in which the multiplexer is used in a muscular or neuromuscular electrical stimulator.

For different biomedical applications or for other scopes of use of the multiplexer 1, the output stages \( M_i \) may however have different structure and functionality and comprise only the output circuit \( \text{NET}_1 \).

It has been seen in practice how the high voltage switch circuit 1, according to the present invention, allows the set objects to be achieved.

With respect to prior art devices, the switch circuit 1 has improved functionalities, in terms of reduction of dissipated power and high impedance of inputs/outputs.

The switch circuit 1 ensures effective high impedance of inputs and outputs. It is arranged in such a manner that the voltages present between the terminals of the input port IN, of any output port \( O_j \) and of the buffer output \( \text{BUF} \) are virtually floating with respect to ground.

An advantage of the switch circuit 1 is the absence of working point bias currents for the active elements (transistors). This substantially reduces the power consumption to what is caused by leakage currents in the transistors.

Additional power consumption in active state is caused by charging/discharging of the parasitic capacitances trough the polarization currents \( I_{P_1}, I_{P_2} \). This can be minimized through reducing the time periods during which the control signals \( C_1, C_2 \) are at a logic level commanding the ON state for the switches \( T_1, T_2, T_3, T_4 \). This is basically a design factor that depends on the parasitic capacitances, mainly in said switches.

The switch circuit 1 is particularly suitable for operating in the presence of high voltages to the terminals of the input port IN or of the output port.

For this purpose, it is sufficient to select in the most appropriate manner the type of transistor of each output stage.

The switch circuit 1 is characterized by considerable flexibility of use.

It is particularly suitable for use in biomedical applications, such as in a muscular or neuromuscular electrical stimulator.

In this application, the use of the output circuits \( \text{NET}_1 \) and \( \text{NET}_2 \) for the output stage \( M_i \), according to the description above, enables simple and effective adjustment of the polarity and time distribution of the output current \( I_{O_j} \) at each output port \( O_j \).

However, the switch circuit 1 can be easily integrated in other biomedical applications, for example in ultrasonic devices or micro-electromechanical devices or systems (MEMS).

The switch circuit 1 has a simple structure and is easy and inexpensive to produce at industrial level, with manufacturing techniques using discrete or integrated components.

A high voltage switch circuit (1) which comprises an input port (IN) and an output port (OUT), a buffer stage (BUF) that is electrically connected with said input port, a first switch (T1) and a second switch (T2) operating as current
switches, which are complementary and are electrically connected between said input port (IN) and said output port (OI), a first control terminal (K1) for providing a first control signal (C1), a first voltage level translator (A1) that is electrically connected with said buffer stage (BUF), with said first and second switch (T1, T2) and with said first control terminal (K1), said first voltage level translator providing a first and second gate voltage (VP1, VP2) at a first and second gate terminal (G1, G2) of said first and second switch (T1, T2) to control said first and second switch (T1, T2) through said first control signal (C1), said first and second switch, controlled by said first control signal (C1), enabling or disabling the flow of an input current (IN) from said input port to said output port.

2. The high voltage switch circuit, according to claim 1, wherein said first and second switch (T1, T2) are field effect transistors.

3. The high voltage switch circuit, according to claim 1, wherein said first voltage level translator (A1) is electrically connected between a pair of terminals (BF+, BF-) of a buffer output (BF) of said buffer stage (BUF), said voltage level translator comprising a third transistor (T3) and a fourth transistor (T4) to provide said first and second gate voltage (VP1, VP2), said third and fourth transistor (T3, T4) being electrically connected with said first control terminal (K1) and to ground, respectively, or vice versa.

4. The high voltage switch circuit, according to claim 1, wherein said first voltage level translator (A1) comprises a first over-voltage protection element (D1) that is electrically connected between the first gate terminal (G1) of said first switch (T1) and a positive terminal (IN+) of said input port (IN) and a second over-voltage protection element (D2) that is electrically connected between said second gate terminal (G2) of said second switch (T2) and a negative terminal (IN-) of said input port (IN).

5. The high voltage switch circuit, according to claim 1, wherein said buffer stage (BUF) comprises:
   a first sensing circuit (B1), electrically connected with a positive terminal (IN+) of said input port (IN), with a first sensing node (S1) and with a first power supply (VCC), said first sensing circuit sensing the voltage of the positive terminal (IN+) of said input port (IN) and establishing a voltage offset with respect thereto;
   a first voltage follower circuit (F1), electrically connected with said first sensing node (S1), with a positive terminal (BF+) of the buffer output (BF) of said buffer stage (BUF) and with a high voltage second power supply (VPV), said first voltage follower circuit providing a voltage at the positive terminal (BF+) of the buffer output (BF), which follows the voltage of the positive terminal (IN+) of said input port (IN);
   a second sensing circuit (B2), electrically connected with a negative terminal (IN-) of said input port (IN), with a second sensing node (S2) and with a third power supply (VDD), said second sensing circuit sensing the voltage of the negative terminal (IN-) of said input port (IN) and establishing a voltage offset with respect thereto;
   a second voltage follower circuit (F2), electrically connected with said second sensing node (S2), with a negative terminal (BF-) of said buffer output (BF) and with a high voltage fourth power supply (VNW), said second voltage follower providing a voltage at the negative terminal (BF-) of the buffer output (BF), which follows the voltage of the negative terminal (IN-) of said input port (IN).

6. The high voltage switch circuit, according to claim 1, wherein it is operatively associated with or it comprises a control stage (COM) that outputs said first control signal (C1).

7. The high voltage switch circuit, according to claim 1, which comprises a fifth switch (T5) and a sixth switch (T6) operating as current switches, which are complementary and are electrically connected between said input port (IN) and said output port (OI), in parallel with respect to said first and second switch (T1, T2), a second control terminal (K2) for providing a second control signal (C2), a second voltage level translator (A3) that is electrically connected with said buffer stage (BUF), with said fifth and sixth switch (T5, T6) and with said second control terminal (K2), said second voltage level translator providing a third and fourth gate voltage (VP3, VP4) at a third and fourth gate terminal (G3, G4) of said fifth and sixth switch (T5, T6) to control said fifth and sixth switch (T5, T6) through said second control signal (C2), said fifth and sixth switch, controlled by said second control signal (C2), enabling or disabling the flow of an input current (IN) from said input port to said output port.

8. The high voltage switch circuit, according to claim 7, wherein said fifth and sixth switch are field effect transistors.

9. The high voltage switch circuit, according to claim 7, which comprises a first output (Y1) that is electrically connected with said first and second switch (T1, T2) and a second output (Y2) that is electrically connected with said fifth and sixth switch (T5, T6), said first output (Y1) being electrically connected with said output port (OI) with a direct polarity and said second output (Y2) being electrically connected with said output port (OI) with an inverse polarity, or vice versa.

10. The high voltage switch circuit, according to claim 7, wherein said second voltage level translator (A2) is electrically connected between a pair of terminals (BF+, BF-) of a buffer output (BF) of said buffer stage (BUF), said voltage level translator comprising a seventh transistor (T7) and an eighth transistor (T8) to provide said third and fourth gate voltage (VP3, VP4), said seventh and eighth transistor (T7, T8) being electrically connected with said second control terminal (K2) and to ground, respectively, or vice versa.

11. The high voltage switch circuit, according to claim 7 wherein said second voltage level translator (A2) comprises a third over-voltage protection element (D10) that is electrically connected between the third gate terminal (G1) of said fifth switch (T5) and a positive terminal (IN+) of said input port (IN) and a fourth over-voltage protection element (D11) that is electrically connected between the fourth gate terminal (G4) of said sixth switch (T6) and a negative terminal (IN-) of said input port (IN).

12. A high voltage current multiplexer (100) which comprises a high voltage switch circuit (1), according to claim 1.

13. A muscular or neuromuscular electrical stimulator which comprises a high voltage switch circuit (1), according to claim 1.

14. An ultrasonic device which comprises a high voltage switch circuit (1), according to claim 1.

15. A micro-electromechanical device which comprises a high voltage switch circuit (1), according to claim 1.

16. The high voltage switch circuit, according to claim 7, wherein said first voltage level translator (A1) is electrically connected between a pair of terminals (BF+, BF-) of a buffer output (BF) of said buffer stage (BUF), said voltage level translator comprising a third transistor (T3) and a fourth transistor (T4) to provide said first and second gate voltage.
(VP1, VP2), said third and fourth transistor (T3, T4) being electrically connected with said first control terminal (K1) and to ground, respectively, or vice versa.

17. The high voltage switch circuit, according to claim 2, wherein said first voltage level translator (A1) comprises a first over-voltage protection element (D1) that is electrically connected between the first gate terminal (G1) of said first switch (T1) and a positive terminal (IN+) of said input port (IN) and a second over-voltage protection element (D2) that is electrically connected between the second gate terminal (G2) of said second switch (T2) and a negative terminal (IN−) of said input port (IN).

18. The high voltage switch circuit, according to claim 3, wherein said first voltage level translator (A1) comprises a first over-voltage protection element (D1) that is electrically connected between the first gate terminal (G1) of said first switch (T1) and a positive terminal (IN+) of said input port (IN) and a second over-voltage protection element (D2) that is electrically connected between the second gate terminal (G2) of said second switch (T2) and a negative terminal (IN−) of said input port (IN).

19. The high voltage switch circuit, according to claim 2, wherein said buffer stage (BUF) comprises:
   - a first sensing circuit (B1), electrically connected with a positive terminal (IN+) of said input port (IN), with a first sensing node (S1) and with a first power supply (VCC), said first sensing circuit sensing the voltage at the positive terminal (IN+) of said input port (IN) and establishing a voltage offset with respect thereto;
   - a first voltage follower circuit (F1), electrically connected with said first sensing node (S1), with a positive terminal (BF+) of the buffer output (BF) of said buffer stage (BUF) and with a high voltage second power supply (VPV), said first voltage follower circuit providing a voltage at the positive terminal (BF+) of the buffer output (BF), which follows the voltage of the positive terminal (IN+) of said input port (IN);
   - a second sensing circuit (B2), electrically connected with a negative terminal (IN−) of said input port (IN), with a second sensing node (S2) and with a third power supply (VDD), said second sensing circuit sensing the voltage of the negative terminal (IN−) of said input port (IN) and establishing a voltage offset with respect thereto;
   - a second voltage follower circuit (F2), electrically connected with said second sensing node (S2), with a negative terminal (BF−) of said buffer output (BF) and with a high voltage fourth power supply (VNN), said second voltage follower providing a voltage at the negative terminal (BF−) of the buffer output (BF), which follows the voltage of the negative terminal (IN−) of said input port (IN).

20. The high voltage switch circuit, according to claim 3, wherein said buffer stage (BUF) comprises:
   - a first sensing circuit (B1), electrically connected with a positive terminal (IN+) of said input port (IN), with a first sensing node (S1) and with a first power supply (VCC), said first sensing circuit sensing the voltage at the positive terminal (IN+) of said input port (IN) and establishing a voltage offset with respect thereto;
   - a first voltage follower circuit (F1), electrically connected with said first sensing node (S1), with a positive terminal (BF+) of the buffer output (BF) of said buffer stage (BUF) and with a high voltage second power supply (VPV), said first voltage follower circuit providing a voltage at the positive terminal (BF+) of the buffer output (BF), which follows the voltage of the positive terminal (IN+) of said input port (IN);
   - a second sensing circuit (B2), electrically connected with a negative terminal (IN−) of said input port (IN), with a second sensing node (S2) and with a third power supply (VDD), said second sensing circuit sensing the voltage of the negative terminal (IN−) of said input port (IN) and establishing a voltage offset with respect thereto;
   - a second voltage follower circuit (F2), electrically connected with said second sensing node (S2), with a negative terminal (BF−) of said buffer output (BF) and with a high voltage fourth power supply (VNN), said second voltage follower providing a voltage at the negative terminal (BF−) of the buffer output (BF), which follows the voltage of the negative terminal (IN−) of said input port (IN).