



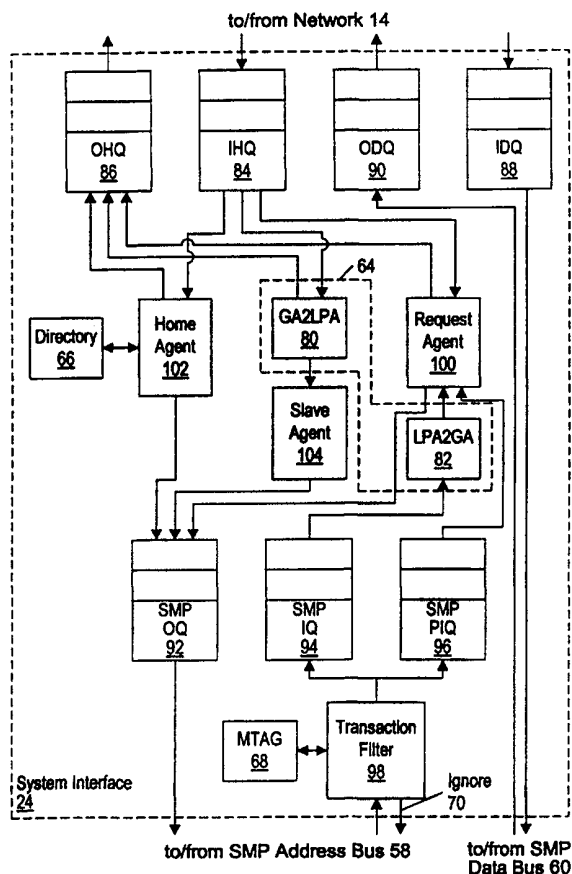
INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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(21) International Application Number: PCT/US98/18469 (22) International Filing Date: 4 September 1998 (04.09.98) (30) Priority Data: 08/924,385 5 September 1997 (05.09.97) US (71) Applicant: SUN MICROSYSTEMS, INC. [US/US]; 901 San Antonio Road, Palo Alto, CA 94303 (US). (72) Inventors: HAGERSTEN, Erik, E.; 3451 Cork Oak Way, Palo Alto, CA 94303 (US). HILL, Mark; 272 Covington Road, Los Altos, CA 94024 (US). (74) Agent: KIVLIN, B., Nöel; Conley, Rose & Tayon, P.C., P.O. Box 398, Austin, TX 78767-0398 (US).		(81) Designated States: JP, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published <i>With international search report.</i> <i>Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i> (88) Date of publication of the international search report: 3 June 1999 (03.06.99)	

(54) Title: SCALABLE SHARED MEMORY MULTIPROCESSOR SYSTEM

(57) Abstract

A portion of the global memory of a multiprocessing computer system is allocated to each node, called local memory space. Data from a remote node may be copied to local memory space of a node such that accesses to the data may be performed locally rather than globally. The copied data is referred to as a shadow page. The global address of the data is translated to a local physical address for the node to which the data is copied. To reduce the size of the translation tables for converting between global addresses and local physical addresses, the page to which shadow copies may be stored and which global addresses may be converted to local physical addresses may be restricted. Multiple page of local memory space may be allocated to one entry of a local physical address to global address (LPA2GA) table. When a page is allocated to store shadow pages, an entry in the LPA2GA table associated with that page is marked as unavailable. In a similar manner, multiple pages of the global address space are mapped to an entry in a global address to local physical address (GA2LPA) translation table. To decrease the probability that an entry is not available for a page, the GA2LPA table may be implemented as a set associative table. To further increase the availability of entries in the GA2LPA table, a skewed-associative cache that implements an insertion algorithm that realigns the translations in the table to maximize the utilization of the available entries is implemented. A coherent memory replication (CMR) address space stores shadow pages of data from remote nodes and a local address space stores local data. A bit within a local physical address identifies whether data is a shadow page, which is stored in CMR space, or local data, which is stored in local address space.



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INTERNATIONAL SEARCH REPORT

national Application No

PCT/US 98/18469

A. CLASSIFICATION OF SUBJECT MATTER

IPC 6 G06F12/10 G06F12/08

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
3 A	EP 0 780 769 A (SUN MICROSYSTEMS INC) 25 June 1997 see the whole document ---	1-21
11 A	AGARWAL A ET AL: "COLUMN-ASSOCIATIVE CACHES: A TECHNIQUE FOR REDUCING THE MISS RATE OF DIRECT-MAPPED CACHES" PROCEEDINGS OF THE ANNUAL INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE, SAN DIEGO, MAY 16 - 19, 1993, no. SYMP. 20, 16 May 1993, pages 179-190, XP000398997 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS see page 181, right-hand column, paragraph 3.1 --- -/--	1-5, 11-21

☒ Further documents are listed in the continuation of box C.☒ Patent family members are listed in annex.

° Special categories of cited documents :

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search

8 January 1999

Date of mailing of the international search report

13. 04. 1999

Name and mailing address of the ISA

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INTERNATIONAL SEARCH REPORT

national Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

11

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	SEZNEC A: "ABOUT SET AND SKEWED ASSOCIATIVITY ON SECOND-LEVEL CACHES" PROCEEDINGS OF THE INTERNATIONAL CONFERENCE ON COMPUTER DESIGN: VLSI IN COMPUTERS AND PROCESSORS, CAMBRIDGE, MA., OCT. 3 - 6, 1993, 3 October 1993, pages 40-43, XP000463373 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS see page 41, paragraph 2; figure 3 -----	1-5, 11-21

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 98/18469

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-21

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest.
- ☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

1. Claims: 1-21

A look-up table accessed using a first and a second index function and having means for moving a datum stored therein when an indexed entry is not available for a new datum to be stored and method.

2. Claims: 22-38

Multiprocessing system having multiple processing nodes in which a first node is inhibited from storing a copy of data local to a second node if a translation for the data cannot be stored in a translation table and method.

3. Claims: 39-58

Multiprocessing system having two local address spaces in each node for local data and replicated remote data respectively and selectively performing local to global address translations for global bus requests.

INTERNATIONAL SEARCH REPORT

Information on patent family members

national Application No

PCT/US 98/18469

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0780769 A	25-06-1997	US 5710907 A	20-01-1998
		JP 9185549 A	15-07-1997
