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(54) **Title**: METHOD FOR MANUFACTURING DUAL-GATE OXIDE SEMICONDUCTOR DEVICES

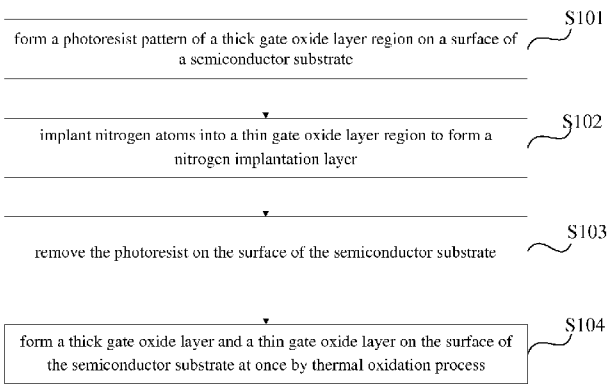

Fig. 1

(57) **Abstract**: A method is provided for manufacturing a dual-gate oxide semiconductor device. The method includes providing a substrate including a first gate oxide layer region and a second gate oxide layer region, and forming a photoresist pattern of the second gate oxide layer region on a surface of the substrate (S101). The method also includes implanting nitrogen atoms into the first gate oxide layer region by an ion implantation process using the photoresist pattern of the second gate oxide layer region as a mask to form a nitrogen implantation layer (S102). Further, the method includes removing the photoresist pattern on the surface of the substrate to expose the second gate oxide layer region (S103), and forming a first gate oxide layer and a second gate oxide layer on the surface of the substrate at the same time by a single thermal oxidation process (S104). Furthermore, the first gate oxide layer has a first thickness and the second gate oxide layer has a second thickness, which is different from the first thickness.

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Description

Title of Invention: METHOD FOR MANUFACTURING DUAL-GATE OXIDE SEMICONDUCTOR DEVICES

[1] FIELD OF THE INVENTION

[2] The present invention generally relates to the field of semiconductor manufacturing and, more particularly, to the methods and processes for manufacturing dual-gate oxide semiconductor devices .

[3] BACKGROUND

[4] A dual-gate oxide semiconductor device generally includes a source, a drain and two gates, and the two gates are mutually independent. Gate oxide layers respectively under the two gates are of different thickness, so as to meet the need of different applications. For example, a thicker gate oxide layer is used in a high voltage device for input or output; while a thinner gate oxide layer is used in a low voltage device for digital logic operation. These characteristics make it possible to use the dual-gate oxide semiconductor device as a high-frequency amplifier, a mixer, a demodulator, a gain control amplifier and so on. Therefore, dual-gate oxide semiconductor devices are widely used in large scale integrated circuits.

[5] An existing process for manufacturing dual-gate oxide semiconductor devices usually includes: forming a thick gate oxide layer on a surface of a semiconductor substrate by a thermal oxidation process; forming a photoresist pattern of a thick gate oxide layer region on the surface of the thick gate oxide layer region by performing steps of applying photoresist, exposure, developing and so on sequentially; removing the thick gate oxide layer in a thin gate oxide layer region through an etching process using the photoresist pattern of the thick gate oxide layer region as a mask; and forming, by another thermal oxidation process, a thin gate oxide layer in the region where the thick gate oxide layer is removed.

[6] However, there are certain disadvantages in the existing process for manufacturing the dual-gate oxide semiconductor device. To form the thick gate oxide layer and the thin gate oxide layer, respectively, the thermal oxidation process has to be performed twice. Therefore, the process flow is complicated, leading to higher production cost and lower production efficiency when manufacturing dual-gate oxide semiconductor devices.

[7] The disclosed methods and systems are directed to solve one or more problems set forth above and other problems.

[8] BRIEF SUMMARY OF THE DISCLOSURE

[9] One aspect of the present disclosure includes a method for manufacturing a dual-gate

oxide semiconductor device. The method includes providing a substrate including a first gate oxide layer region and a second gate oxide layer region, and forming a photoresist pattern of the second gate oxide layer region on a surface of the substrate. The method also includes implanting nitrogen atoms into the first gate oxide layer region by an ion implantation process using the photoresist pattern of the second gate oxide layer region as a mask to form a nitrogen implantation layer. Further, the method includes removing the photoresist pattern on the surface of the substrate to expose the second gate oxide layer region, and forming a first gate oxide layer and a second gate oxide layer on the surface of the substrate at same time by a single thermal oxidation process. Furthermore, the first gate oxide layer has a first thickness and the second gate oxide layer has a second thickness, which is different from the first thickness.

[10] Other aspects of the present disclosure can be understood by those skilled in the art in light of the description, the claims, and the drawings of the present disclosure.

[11] BRIEF DESCRIPTION OF THE DRAWINGS

[12] Figure 1 illustrates an exemplary flow diagram of a method of manufacturing a dual-gate oxide semiconductor device consistent with the disclosed embodiments;

[13] Figure 2 illustrates a dual-gate oxide semiconductor device after forming a photoresist pattern of a thick gate oxide layer;

[14] Figure 3 illustrates a dual-gate oxide semiconductor device after forming a nitrogen implantation layer;

[15] Figure 4 illustrates a dual-gate oxide semiconductor device after removing photoresist on a surface of a semiconductor substrate;

[16] Figure 5 illustrates a dual-gate oxide semiconductor device after forming a gate oxide layer;

[17] Figure 6 illustrates a semiconductor device after forming a silicon oxide layer on the surface consistent with the disclosed embodiments;

[18] Figure 7 illustrates a dual-gate oxide semiconductor device including a silicon oxide layer during forming a nitrogen implantation layer;

[19] Figure 8 illustrates a dual-gate oxide semiconductor device after forming a well region;

[20] Figure 9 illustrates a dual-gate oxide semiconductor device after forming a silicon nitride layer consistent with the disclosed embodiments ;

[21] Figure 10 illustrates a dual-gate oxide semiconductor device after forming a pattern of a local field oxidation isolation region;

[22] Figure 11 illustrates a dual-gate oxide semiconductor device after forming a local field oxidation isolation region; and

[23] Figure 12 illustrates a dual-gate oxide semiconductor device consistent with the disclosed embodiments.

[24] DETAILED DESCRIPTION

[25] Reference will now be made in detail to exemplary embodiments of the invention, which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[26] Figure 1 illustrates an exemplary flow diagram of a method of manufacturing a dual-gate oxide semiconductor device consistent with the disclosed embodiments . Figure 2 illustrates a corresponding dual-gate oxide semiconductor device 200.

[27] As shown in Figure 2, device 200 may include a substrate 201, a predetermined thin gate oxide layer region 204 (i.e., a first gate oxide layer region), a predetermined thick gate oxide layer region 205 (i.e., a second gate oxide layer region), and an isolation region 202 between the thin gate oxide layer region 204 and the thick gate oxide layer region 205.

[28] Substrate 201 may be provided first as the base for the dual-gate oxide semiconductor device 200 . The substrate 201 may include any appropriate material for making double-gate structures. For example, the substrate 201 may include a semiconductor structure, e.g., silicon, silicon germanium (SiGe) with a monocrystalline, polycrystalline, or amorphous structure. The substrate 201 may also include a hybrid semiconductor structure, e.g., carborundum, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide or gallium antimonide, alloy semiconductor, or a combination thereof. Further, the substrate 201 may include a silicon-on-insulator (SOI) structure. In addition, the substrate 201 may also include other materials, such as a multi-layered structure of epitaxial layer or buried layer. Other materials may also be used.

[29] Further, the thin gate oxide layer region 204 may be used to form a first gate oxide layer with a first thickness (i.e., a thin gate oxide layer); and the thick gate oxide layer region 205 may be used to form a second gate oxide layer with a second thickness (i.e., a thick gate oxide layer). The first thickness is different from the second thickness and, more specifically, the first thickness may be less than the second thickness. However, the degree of difference may be depending on particular dual-gate oxide semiconductor device, and the thin gate oxide layer and the thick gate oxide layer may be formed at the same time as a single gate oxide layer with corresponding different thicknesses.

[30] As shown in Figure 1, after the substrate 201 is provided, a photoresist pattern of the thick gate oxide layer region may be formed on a surface of the semiconductor substrate 201 (S101). The photoresist pattern may be formed by performing steps such as applying photoresist, exposure and developing sequentially.

[31] Figure 2 shows the photoresist pattern 203 of the thick gate oxide layer region 205.

After a photoresist layer is developed, the surface of the thin gate oxide layer region 204 is not covered with any photoresist and the surface of the thick gate oxide layer region 205 is covered with photoresist pattern 203. The thick gate oxide layer region and the thin gate oxide layer region are regions before a gate oxide layer is formed.

[32] Returning to Figure 1, after forming the photoresist pattern 203 (S101), nitrogen atoms are implanted into the thin gate oxide layer region 204 to form a nitrogen implantation layer (S102). The nitrogen atoms may be implanted through an ion implantation process using the photoresist pattern 203 of the thick gate oxide layer region 205 as a mask. Figure 3 shows the corresponding dual-gate oxide semiconductor device 200 after forming the nitrogen implantation layer.

[33] As shown in Figure 3, a nitrogen implantation layer 206 is formed in the thin gate oxide layer region 204. The shape (not shown) of the nitrogen implantation layer 206 may also coincide with the shape of the thin gate oxide layer region 204. Any appropriate shape or any appropriate number of regions may be used. Further, parameters of the ion implantation, such as the concentration of ion (e.g., nitrogen atoms), may be predetermined based on desired thickness of the thin gate oxide layer and/or the thick gate oxide layer, as further described in the disclosed embodiments. Thus, the ion implantation can be controlled according to the predetermined ion implantation parameters during the manufacturing process.

[34] Returning to Figure 1, after forming the nitrogen implantation layer 206, the photoresist on the surface of the semiconductor substrate 201 is removed (S103). That is, the photoresist pattern located on the surface of the semiconductor substrate 201 and corresponding to the thick gate oxide layer region 205 is removed.

[35] Figure 4 shows the corresponding dual-gate oxide semiconductor device 200 after removing photoresist on the surface of the semiconductor substrate 201. As shown in Figure 4, both the thin gate oxide layer region 204 and the thick gate oxide layer region 205 are exposed, with the nitrogen implantation layer 206 in the thin gate oxide layer region 204.

[36] Returning to Figure 1, after removing the photoresist on the surface of the semiconductor substrate 201 (S103), a thick gate oxide layer and a thin gate oxide layer are formed on the surface of the semiconductor substrate 201 at same time by a thermal oxidation process (S104). Other processes may also be used.

[37] That is, during the process of forming the gate oxide layer (i.e., the thick gate oxide layer and the thin gate oxide layer) on the surface of the semiconductor substrate 201 by a single thermal oxidation process, the nitrogen implantation layer 206 may reduce the oxidation speed of the surface of the semiconductor substrate. On the other hand, the oxidation speed of the surface of the semiconductor substrate without the nitrogen implantation layer 206 is normal. Thus, only one single thermal oxidation process can

be used to form the thin gate oxide layer on the surface of the semiconductor substrate in the thin gate oxide layer region with the nitrogen implantation layer 206, and to form the thick gate oxide layer on the surface of the semiconductor substrate in the thick gate oxide layer region without the nitrogen implantation layer 206.

[38] More specifically, the nitrogen implantation layer 206 in the thin gate oxide layer region 204 may reduce the oxidation speed of the surface of the semiconductor substrate 201, while the oxidation speed is normal at the surface of the semiconductor substrate corresponding to the thick gate oxide layer region 205 without a nitrogen implantation layer. Further, the oxidation speed at the surface of the semiconductor substrate corresponding to the nitrogen implantation layer 206 can be controlled by controlling the nitrogen atom concentration and thickness of the nitrogen implantation layer 206. Thus, the thickness of the thin gate oxide layer formed by thermal oxidation process can be controlled with desired precision to produce substantial thin gate oxide layers.

[39] Figure 5 shows the corresponding dual-gate oxide semiconductor device 200 after forming a gate oxide layer. As shown in Figure 5, a thin gate oxide layer 207 is formed in the thin gate oxide layer region 204, and a thick gate oxide layer 208 is formed in the thick gate oxide layer region 205.

[40] Additionally or optionally, other processes may also be performed together with the above processes for manufacturing the dual-gate oxide semiconductor device 200. For example, before forming the photoresist pattern of the thick gate oxide layer region 205 (e.g., before applying photoresist), a silicon oxide layer may be formed on the surface of the semiconductor substrate.

[41] As shown in Figure 6, a silicon oxide layer 209 is formed on the surface of the device 200. That is, the silicon oxide layer 209 is formed on substrate 201. The silicon oxide layer 209 may be formed by, for example, a deposition process. In subsequent processes, such as forming a well region or a nitrogen implantation layer, the silicon oxide layer 209 may be used as a blocking and protective layer to control depth and concentration of the ion or atom implantation and to prevent the semiconductor substrate from being excessively damaged during the implantation process. Further, the thickness of the silicon oxide layer 209 may be in a range of approximately 150-300 Å.

[42] Figure 7 shows the dual-gate oxide semiconductor device 200 including a silicon oxide layer 209 after forming a nitrogen implantation layer. As shown in Figure 7, similar to Figure 3, a nitrogen implantation layer 206 may be formed in the thin gate oxide layer region 204 on the surface of the substrate 201, covered by the silicon oxide layer 209 so as to protect and/or control the formation of the nitrogen implantation layer 206. Moreover, the silicon oxide layer 209 may be removed after the nitrogen implantation layer 206 is formed.

[43] Additionally or optionally, a well region may also be formed on the surface of substrate 201 after forming the silicon oxide layer 209. Figure 8 shows the dual-gate oxide semiconductor device 200 after forming a well region.

[44] As shown in Figure 8, a well region 210 is formed on the surface of substrate 201 and covered by the silicon oxide layer 209. The well region 210 may be an n-well or a p-well according to the conduction type of device 200. Further, the well region 210 may be formed by an ion implantation process. More specifically, the process of forming the well region 210 may include forming a photoresist pattern of a well region by applying photoresist, exposure and developing sequentially on the surface of the silicon oxide layer 209; and performing ion implantation using the photoresist pattern of the well region as a mask. During the formation of the well region 210, the silicon oxide layer 209 may be used as a blocking and protective layer to control depth and concentration of the ion implantation.

[45] Further, processes may be performed to form an isolation region between a thin gate oxide layer and a thick gate oxide layer of the dual-gate oxide semiconductor device 200. The isolation region may be a local field oxidation isolation or a shallow trench isolation. Other type of isolation region may also be used.

[46] More particularly, after forming the silicon oxide layer 209 and/or well region 210, but before applying photoresist for forming thick gate oxide region pattern, a silicon nitride layer is deposited on the surface of the silicon oxide layer 209.

[47] Figure 9 shows the dual-gate oxide semiconductor device 200 after forming the silicon nitride layer. As shown in Figure 9, a silicon nitride layer 211 is formed on the silicon oxide layer 209. The silicon nitride layer 211 may be a layer of firm mask material which may protect an active region of the semiconductor substrate 201 during the formation of the local field oxidation isolation and may be used as blocking material during polishing process.

[48] Further, a pattern of a local field oxidation isolation region is formed in the silicon nitride layer 211. Figure 10 shows the dual-gate oxide semiconductor device 200 after forming the pattern of the local field oxidation isolation region. As shown in Figure 10, a pattern of the local field oxidation isolation region 212 is formed in the silicon nitride layer 211.

[49] After forming the pattern of the local field oxidation isolation region 212, a local field oxidation isolation is formed between the thin gate oxide layer region and the thick gate oxide layer region. Figure 11 shows the dual-gate oxide semiconductor device 200 after forming the local field oxidation isolation.

[50] As shown in Figure 11, local field oxidation isolation 202 is formed between the thin gate oxide layer region 204 and the thick gate oxide layer region 205. The local field oxidation isolation 202 may be formed through an oxidation process using the silicon

nitride layer 211 as a mask, so as to separate the thin gate oxide layer region 204 and the thick gate oxide layer region 205.

[51] That is, local field oxidation isolation 202 is formed in a local field oxidation isolation region. The thick gate oxide layer region may be provided at one side of the local field oxidation isolation 202, and a thin gate oxide layer region may be provided at the other side of the local field oxidation isolation 202. Since there is insulating silicon oxide in the local field oxidation isolation region, the isolation between the thin gate oxide layer region 204 and the thick gate oxide layer region 205 can be realized.

[52] Further, the silicon nitride layer 211 is removed and other steps for forming the gate oxide layer may also be applied. Figure 12 shows the dual-gate oxide semiconductor device 200 after removing the silicon nitride layer 211 and other steps. As shown in Figure 12, similar to Figure 5, thin gate oxide layer 207 is formed in the thin gate oxide layer region 204, and thick gate oxide layer 208 is formed in the thick gate oxide layer region 205. The thin gate oxide layer 207 and the thick gate oxide layer 208 are separated by local field oxidation isolation 202.

[53] Additionally or alternatively, a shallow trench isolation may be formed instead of the local field oxidation isolation 202. Because the shallow trench isolation forming process is similar to the process of forming the local field oxidation isolation 202, only brief description is provided for the illustrative purposes.

[54] After forming the silicon oxide layer 209 and before applying the photoresist for forming thick gate oxide region pattern, a silicon nitride layer 211 is deposited on the surface of the silicon oxide layer 209. A pattern of a shallow trench isolation region may then be formed in the silicon nitride layer 211.

[55] Further, a shallow trench isolation is formed through an etching process using the silicon nitride layer 211 as a mask, so as to separate the thick gate oxide layer region 205 and the thin gate oxide layer region 204. The shallow trench isolation may then be filled with an insulating material, and the silicon nitride layer 211 is removed afterwards.

[56] Compared to the local field oxidation isolation region, the shallow trench isolation region may occupy smaller area and may have a better isolation effect than the local field oxidation isolation region. Thus, the shallow trench isolation region may be suitable for small-sized dual-gate oxide semiconductor devices.

[57] By using the disclosed methods and processes, the gate oxide layer of the dual-gate oxide semiconductor device can be formed on the surface of the semiconductor substrate by a single thermal oxidation process, which simplifies the process flow, reduces the production cost, and improves the production efficiency of the manufacturing of the dual-gate oxide semiconductor device.

[58] It is understood that the disclosed embodiments may be applied to any dual-gate

semiconductor devices, and can also be extended to the manufacturing of multi-gate and other types of semiconductor devices. Various alternations, modifications, or equivalents to the technical solutions of the disclosed embodiments can be obvious to those skilled in the art.

Claims

[Claim 1] A method for manufacturing a dual-gate oxide semiconductor device , comprising:
providing a substrate including a first gate oxide layer region and a second gate oxide layer region ;
forming a photoresist pattern of the second gate oxide layer region on a surface of the substrate ;
implanting nitrogen atoms into the first gate oxide layer region by an ion implantation process using the photoresist pattern of the second gate oxide layer region as a mask to form a nitrogen implantation layer;
removing the photoresist pattern on the surface of the substrate to expose the second gate oxide layer region ; and
forming a first gate oxide layer and a second gate oxide layer on the surface of the substrate at same time by a single thermal oxidation process,
wherein the first gate oxide layer has a first thickness and the second gate oxide layer has a second thickness, different from the first thickness.

[Claim 2] The method according to claim 1, wherein:
the first thickness is less than the second thickness;
the first gate oxide layer is a thin gate oxide layer; and
the second gate oxide layer is a thick gate oxide layer.

[Claim 3] The method according to claim 1, wherein:
the nitrogen implantation layer is configured to control the different thicknesses of the first gate oxide layer and the second gate oxide layer during the single thermal oxidation process.

[Claim 4] The method according to claim 1, wherein:
the implantation parameters are determined based on a thickness difference between the first gate oxide layer and the second gate oxide layer.

[Claim 5] The method according to claim 1, wherein forming the photoresist pattern includes :
performing steps of applying photoresist, exposure, and developing sequentially on the surface of the substrate.

[Claim 6] The method according to claim 5, further including:
before applying the photoresist, forming a silicon oxide layer on the surface of the substrate; and

before forming the first gate oxide layer and the second and gate oxide layer, removing the silicon oxide layer.

[Claim 7] The method according to claim 6, wherein
the silicon oxide layer is formed by a deposition process.

[Claim 8] The method according to claim 6, wherein
the thickness of the silicon oxide layer is in a range of approximately 150-300 Å.

[Claim 9] The method according to claim 6, wherein:
after forming the silicon oxide layer and before applying the photoresist, forming a well region in the substrate by an ion implantation process.

[Claim 10] The method according to claim 6, wherein
the first gate oxide layer and the second gate oxide layer are separated by a local field oxidation isolation.

[Claim 11] The method according to claim 10, wherein the local field oxidation isolation is formed by :
after forming the silicon oxide layer and before applying the photoresist, depositing a silicon nitride layer on the surface of the silicon oxide layer;
forming a pattern of a local field oxidation isolation region in the silicon nitride layer;
forming a local field oxidation isolation through an oxidization process using the silicon nitride layer as a mask; and
removing the silicon nitride layer.

[Claim 12] The method according to claim 6, wherein
the first gate oxide layer and the second gate oxide layer are separated by a shallow trench isolation.

[Claim 13] The method according to claim 12, wherein the shallow trench isolation is formed by :
after forming the silicon oxide layer and before applying the photoresist, depositing a silicon nitride layer on the surface of the silicon oxide layer;
forming a pattern of a shallow trench isolation region in the silicon nitride layer;
forming the shallow trench isolation through an etching process using the silicon nitride layer as a mask;
filling the shallow trench isolation with an insulating material; and
removing the silicon nitride layer.

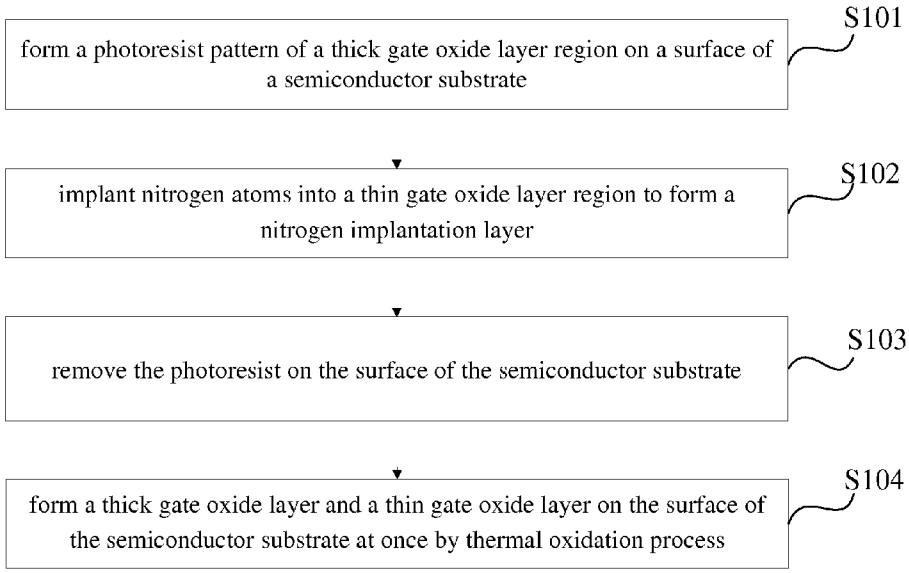
form a photoresist pattern of a thick gate oxide layer region on a surface of a semiconductor substrate
S101
implant nitrogen atoms into a thin gate oxide layer region to form a nitrogen implantation layer
S102
remove the photoresist on the surface of the semiconductor substrate
S103
form a thick gate oxide layer and a thin gate oxide layer on the surface of the semiconductor substrate at once by thermal oxidation process
S104

Fig. 1

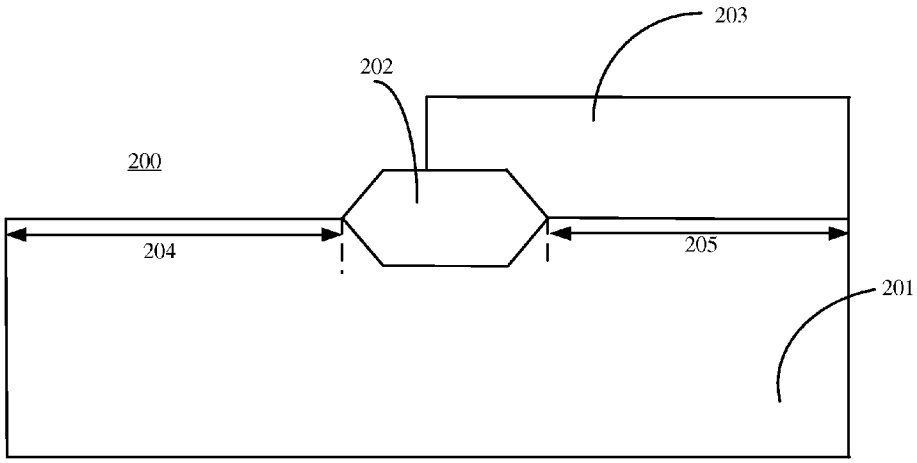
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Fig. 2

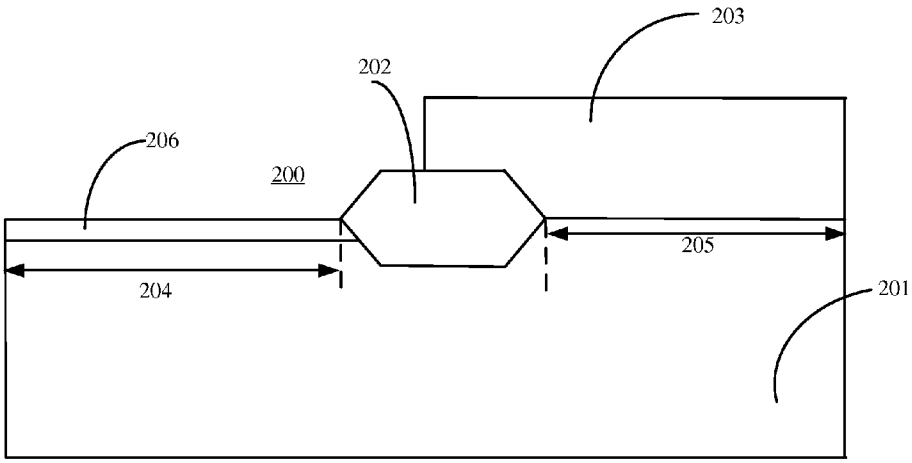

Fig. 3

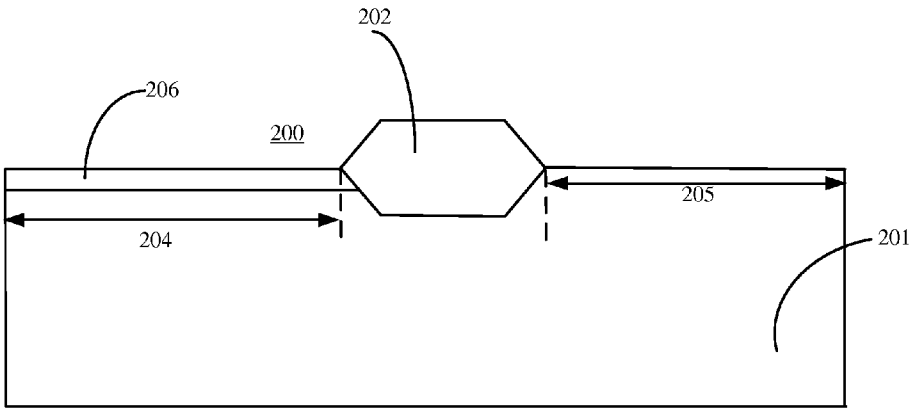

Fig. 4

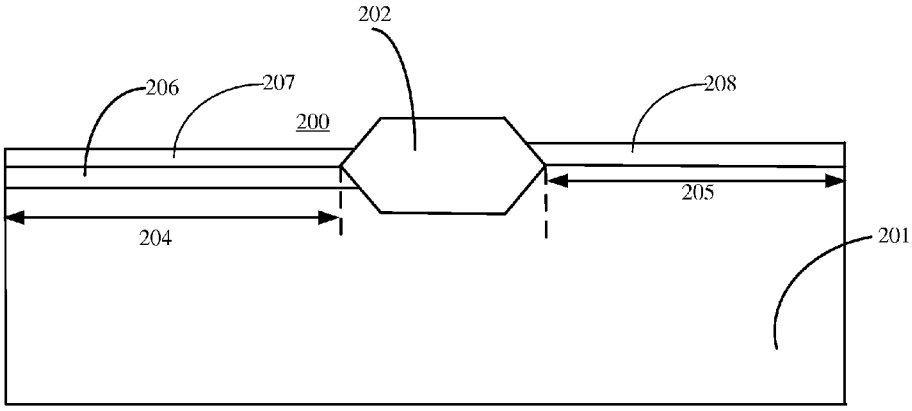

Fig. 5

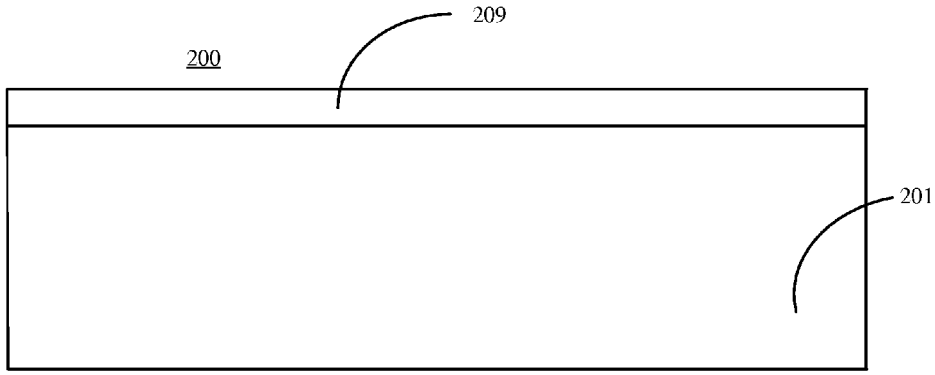

Fig. 6

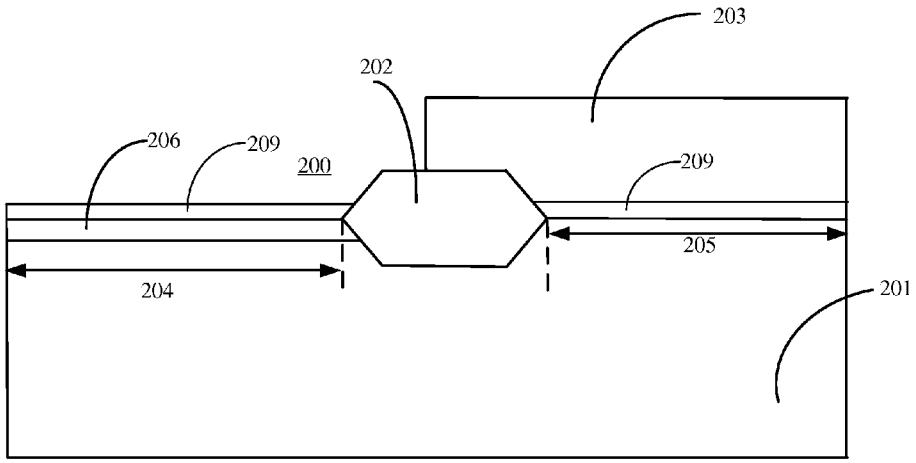

Fig. 7

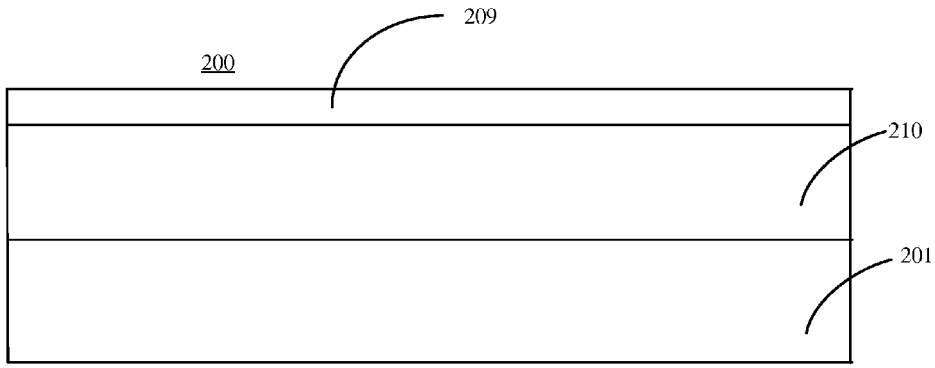

Fig. 8

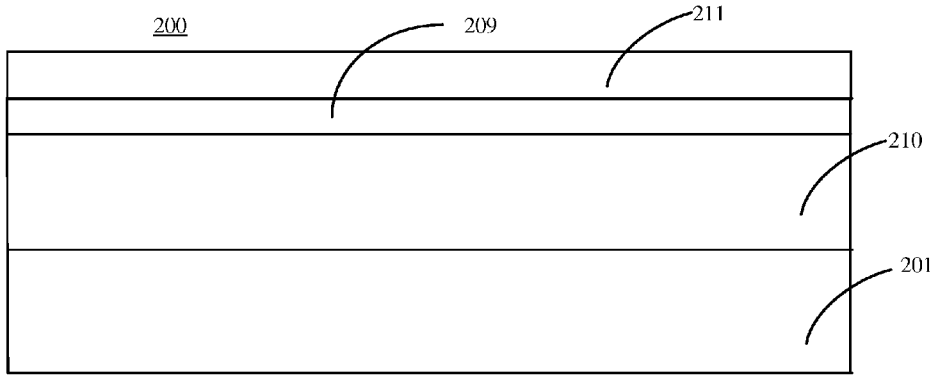

Fig. 9

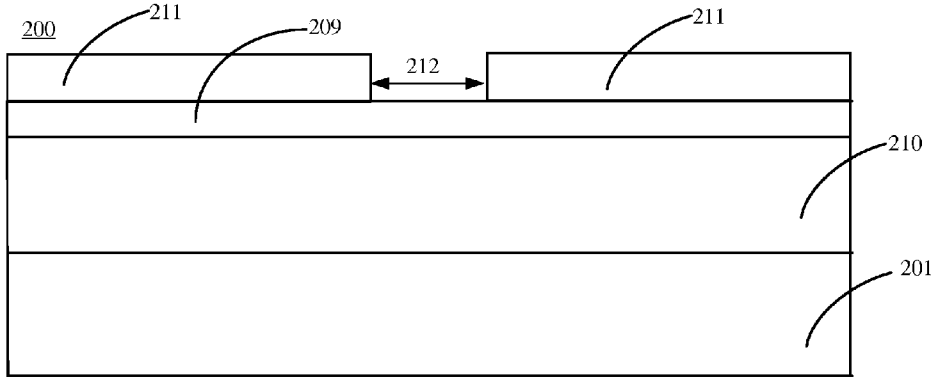

Fig. 10

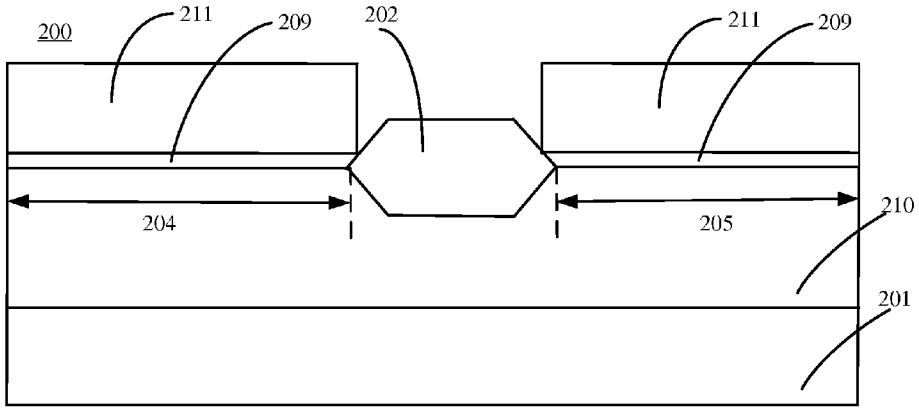
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Fig. 11

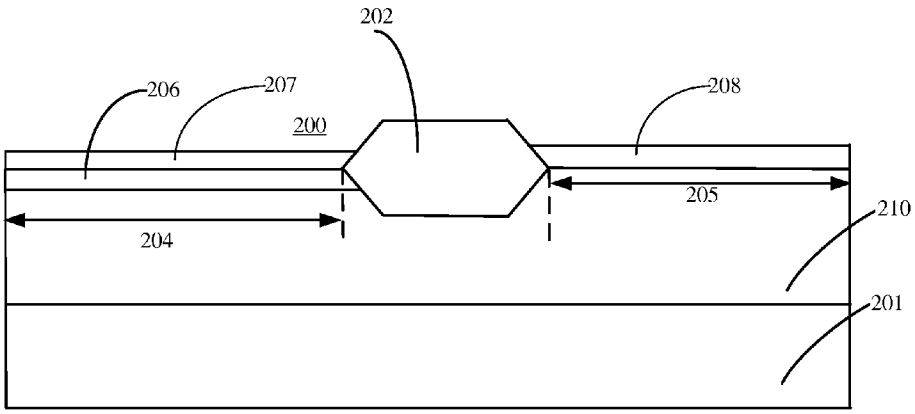
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Fig. 12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2011/082395

A. CLASSIFICATION OF SUBJECT MATTER

See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H01L 21/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI, EPODOC, CNPAT, CNKI: thickness, nitrogen

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US5576226 A (HWANG) 19 November 1996 (19.11.1996) column 3 line 30- column 4 line 44; figures 3a-3f	1-5
Y		6-13
Y	US5672521 A (BARSAN ET AL.) 30 September 1997 (30.09.1997) column 3 lines 33- 39, column 5 lines 20-57; figures 1a-1d, 6a-6d	6-13

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
09 Feb. 2012 (09.02.2012)	**01 Mar. 2012 (01.03.2012)**
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer WANG,Xin Telephone No. (86-10)62411567

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2011/082395

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
US5576226 A	19.11.1996	JP7297298 A	10.11.1995
		KR0136935B1	24.04.1998
		JP2663107B2	15.10.1997
US5672521 A	30.09.1997	none	

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2011/082395

Continuation of: A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/8234 (2006.01) i

H01L 21/31 (2006.01) i

H01L 21/266 (2006.01) i

H01L 29/78 (2006.01) i