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(54) Title: SYSTEM FOR OPTIMIZING THE PERFORMANCE AND RELIABILITY OF A STORAGE CONTROLLER CACHE OFFLOAD CIRCUIT

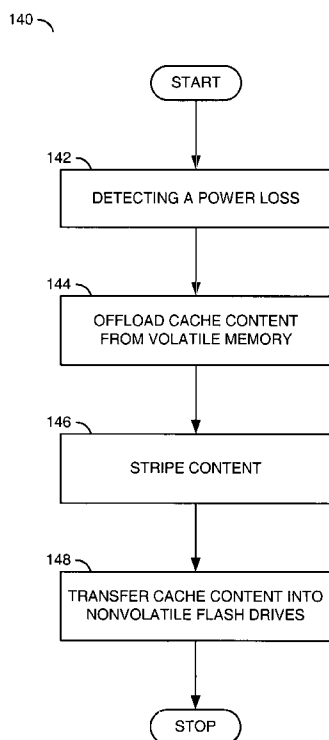


FIG. 3

(57) Abstract: A method for offloading a cache memory is disclosed (140). The method generally includes the steps of (A) reading all of a plurality of cache lines from the cache memory in response to an assertion of a signal to offload of the cache memor (144), (B) generating a plurality of blocks by dividing the cache lines in accordance with a RAID configuration (146) and (C) writing the blocks among a plurality of nonvolatile memories in the RAID configuration, wherein each of the nonvolatile memories has a write bandwidth less than a read bandwidth of the cache memory (148).



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European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI,
FR, GB, GR, HU, IE, **IS**, **IT**, LT, LU, LV, MC, MT, NL, PL,
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A. CLASSIFICATION OF SUBJECT MATTER

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USPC: 711/ 14;713/300,340

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 711/1 14; 713/300, 340

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|------------|---|-----------------------|
| X | US 2006/0107005 A1 (Philippe Andre et al) 18 May 2006 , Figures 1 and 3, Paragraphs [0023], [0049], [0056], [0059]-[0060], [0070J-007I], [0087]-[0088] | 1-15, 17-20 |
| Y | US 2006/0265624 A1 (Moshayed et al.) 23 November 2006, Figure 2 Claim 7 | 16 |



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