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(54) Title: METHODS OR STRUCTURES FOR RECONSTRUCTION OF SUBSTANTIALLY UNIFORM SAMPLES FROM SUBSTANTIALLY NONUNIFORM SAMPLES

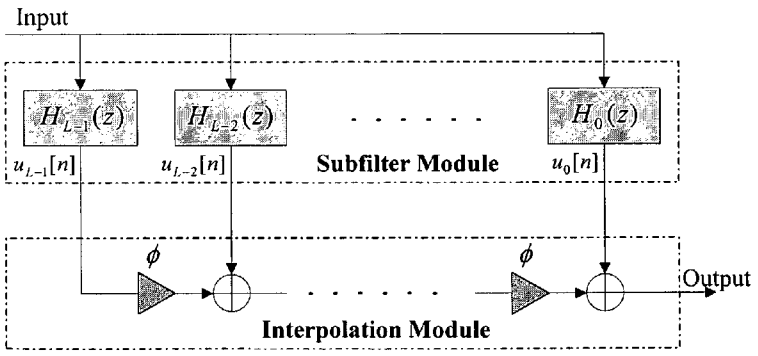


FIG. 2

(57) Abstract: Briefly, embodiments of methods or structures for reconstruction of uniform digital signal sample values from nonuniform digital signal sample values are disclosed.

Methods or Structures for Reconstruction of Substantially Uniform Samples from Substantially Nonuniform Samples

Field:

This disclosure relates generally to resampling in the field of digital signal processing.

Background:

Sampling of digital signal values occurs in many applications, such as signal, speech and video processing, high-speed data converters, power spectral estimation, etc. Many signal processing processes or display systems work with substantially uniformly spaced samples; however, at times, substantially nonuniform digital signal samples are available, rather than substantially uniform signal samples.

For nonuniform sampling, if a signal to be sampled is assumed to be sampled nonuniformly and periodically, conventional reconstruction methods may involve use of a filter bank structure. One application addresses timing mismatch in time-interleaved (TI) analog-to-digital converters (ADCs).

Assuming, for example, that timing mismatches in TI ADCs are known and fixed, a synthesis filter bank may potentially be realized using time varying finite impulse response (FIR) filters. See, for example, Eldar Y. C. and Oppenheim A. V., "Filterbank reconstruction of bandlimited signals from nonuniform and generalized samples," *IEEE Trans. Signal Process.*, vol. 48, no. 10, pp. 2864-2875, Oct. 2000; H. Johansson and P. Löwenborg, "Reconstruction of nonuniformly sampled bandlimited signals by means of digital fractional delay filters," *IEEE Trans. Signal Process.*, vol. 50, no. 11, pp. 2757–2767, Nov. 2002; and S. Prendergast, B. C. Levy, and P. J. Hurst, "Reconstruction of bandlimited periodic nonuniformly sampled signals through multirate filter banks," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 51, no. 8, pp. 1612–1622, Aug. 2004. However, issues may arise if time-skew errors change during operation. This may occur for a variety of reasons, such as component aging, temperature variation, or other reasons, for example. A synthesis filter bank may be redesigned to deal with timing mismatch. However, this may involve the use of general-

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purpose multipliers, which may tend to increase implementation costs, power consumption at high data rates, or have other disadvantages.

Recently, use of more sophisticated digital filters, such as multivariate polynomial impulse response time varying FIR filters, has been proposed to realize a tunable synthesis filter bank See, for example, H. Johansson, P. Löwenborg, and K. Vengattaramane, "Reconstruction of M-periodic nonuniformly sampled signals using multivariate polynomial impulse response time-varying FIR filters," in *Proc. XII Eur. Signal Process. Conf.*, Florence, Italy, Sep. 4–8, 2006; and S. Huang and B. C. Levy, "Blind calibration of timing offset for four-channel time-interleaved ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 4, pp. 863–876, April 2006. Time-skew errors for different channels may be included in a synthesis filter bank so that a filter response may be adjusted by several tuning variables. From an implementation point of view, a synthesis filter bank may be implemented without multipliers, except for a limited number of tuning variables, which may be advantageous. While relatively successful with a small number of channels or small range of time-skew errors, otherwise issues may exist. For instance, an M-channel TI ADC generally has at least $(M - 1)$ synthesis filters which are functions of M variables. Consequently, a design may become challengingly difficult, as M increases. Moreover, high implementation complexity may be another drawback.

Alternate reconstruction methods that do not use a filter bank structure exist for various classes of nonuniformly sampled signals. For example, iterative methods, such as described in F. Marvasti, M. Analoui, and M. Gamshadzahi, "Recovery of signals from nonuniform samples using iterative methods," *IEEE Trans. Signal Process.*, vol. 39, pp. 872-877, April 1991, and E. I. Plotkin, M. N. S. Swamy and Y. Yoganandam, "A novel iterative method for the reconstruction of signals from nonuniformly spaced samples," *Signal Process.*, vol. 37, pp. 203-213, 1994, were commonly used for recovery of nonperiodically sampled signals. However, implementation complexities of these approaches may at times be higher than those of filter banks, making them less attractive in real-time applications, such as TI ADCs. Another disadvantage is a possibility of an ill-behaved system matrix formed by a truncated sinc series, which may result in a relatively low convergence rate or may potentially raise implementation cost.

Another class of parallel ADC arrays called hybrid filter bank (HFB) ADC makes use of analog analysis bank and may be capable of attenuating timing mismatch. See, for example, S. R Velazquez, T. Q. Nguyen and S. R. Broadstone, "Hybrid filter bank analog/digital converter," United States Patent 5568142, Oct. 1996. Although performance of HFB ADCs may typically be less sensitive to mismatch than conventional TI ADCs, design of accurate frequency-selective analog analysis filters and sophisticated digital synthesis filters may make implementation more complicated.

Brief Description of the Invention:

The invention provides an integrated circuit comprising: a digital filter, said digital filter having an input port and an output port; said input port of said digital filter to receive substantially non-uniform digital signal samples; said output port of said digital filter to provide substantially uniform digital signal samples; said digital filter to further process said non-uniform digital signal sample values using a variable delay digital filter to iteratively recover said uniform digital signal sample values.

The invention provides a method comprising: digital filtering substantially non-uniform digital signal sample values using a variable delay digital filter implemented as an iterative process; and outputting substantially uniform digital signal sample values.

The invention provides a system comprising: a digital filter to receive substantially non-uniform digital signal samples and to provide substantially uniform digital signal samples; said digital filter to further process said non-uniform digital signal sample values using a variable delay digital filter to iteratively recover said substantilally uniform digital signal sample values; wherein said digital filter is structured to apply iterative processes that comprise one or more variable digital filters, at least one of said variable digital filters comprising L subfilters and a tuning parameter implemented using a Farrow structure.

The invention provides a signal converter system, comprising: an M-channel time-interleaved analog-to-digital converter, wherein M analog-to-digital subconverters with approximately similar speed are operated in parallel such that an output sampling rate is M times faster than that of one of said subconverters; and an iterative timing mismatch adjuster used to reduce

timing mismatch of the output sequence from said M-channel time-interleaved analog-to-digital converter.

Brief Description of the Figures:

Non-limiting and non-exhaustive embodiments will be described with reference to the following figures, wherein like reference numerals refer to like parts throughout various figures unless otherwise specified.

FIGs. 1(a), 1(b), and 1(c), respectively, are two signal plots illustrating uniform sampling and nonuniform sampling of a continuous-time signal, and a block diagram illustrating an embodiment producing signal sample values.

FIG. 2 is a block diagram illustrating an embodiment of a Farrow structure for an example implementation of a variable digital filter.

FIG. 3(a), 3(b) and 3(c) are block diagrams illustrating embodiments of variable digital filter structures for example implementations of Richardson, Jacobi and Gauss-Seidel iterations.

FIG. 4 is a signal plot illustrating reconstruction accuracies of Richardson, Jacobi and Gauss-Seidel iterations with an increasing number of iterations, for randomly distributed time-skew in interval (-0.1,0.1).

FIG. 5 is a block diagram illustrating an embodiment of an example implementation of an *M*-channel time-interleaved analog-to-digital converter.

FIG. 6 is a block diagram illustrating an embodiment of a modified Farrow structure for an example implementation of a variable digital filter for periodic nonuniform sampling.

FIGs. 7(a) and 7(b) are signal plots to illustrate respectively a spectrum of a multi-sinusoidal signal before and after techniques are applied to address timing mismatch.

FIG. 8 is a block diagram illustrating an embodiment of an example implementation that includes a linear analog system.

Detailed Description:

In the following description of embodiments, reference is made to accompanying drawings which form a part hereof, and in which it is shown by way of illustration specific embodiments of claimed subject matter. It is to be understood that other embodiments may be used; for example, changes or alterations, such as structural changes, may be made. Embodiments, changes or alterations, such as structural changes, are not intended to be departures from scope with respect to claimed subject matter.

FIG. 1(a) is a signal plot illustrating an example of uniform sampling of a continuous-time (CT) signal $x_c(t)$, where a discrete-time (DT) sequence $x[n]$ is obtained by sampling a signal at regular intervals using an ADC. Sequence $x[n]$ comprises a series of digital signal sample values. FIG. 1(b) is a signal plot illustrating an example of nonuniform sampling of $x_c(t)$, where a DT sequence $y[n]$ is defined as $y[n] = x_c(nT - \phi_n T)$; T comprises a sampling interval and $|\phi_n| \le 0.5$. FIG. 1(c) shows a block diagram of one embodiment to generate $y[n]$ from $x_c(t)$ via a nonuniform sampler. Again, sequence $y[n]$ comprises a series of digital signal sample values. In some situations, it may be desirable to have the ability to determine $x[n]$ from $y[n]$. On the other hand, a reverse problem (e.g., to compute a set of nonuniform samples from a uniformly sampled sequence of digital signal sample values) may also be encountered in sampling rate conversion. In what follows, we shall first introduce the reverse problem and provide an example implementation of an embodiment for addressing. Likewise, from this particular embodiment, we shall also demonstrate an example implementation for addressing the forward problem. Of course, claimed subject matter is not intended to be limited to these example embodiments or implementations. These are provided for illustration purposes. Therefore, it is intended that subject matter of the present application encompass much more than these illustrative examples.

Assuming that $x_c(t)$ has a frequency limit $f_{\max}$ and a sampling rate $f_s = 1/T$ applied to $x_c(t)$ is greater than the Nyquist rate $2f_{\max}$, according to sampling theorem, a substantially nonuniformly sampled sequence $y[n]$ may be expressed in terms of a substantially uniformly sampled sequence $x[n]$ as

$$y[n] = x_c(nT - \phi_n T) = \sum_{k=-\infty}^{\infty} x[k] \cdot \mathrm{sinc}(n - \phi_n - k), \ \forall n . \qquad (1)$$

For purposes of this patent application, the term "substantially" is in general understood to be included through out the specification, even in situations where the term is not expressly employed. As simply one example, uniformly sampled sequences are understood to include substantially uniformly sampled sequences. If ϕ_n is given, $y[n]$ may comprise a delayed version of a uniform sampled sequence $x[n]$. From (1), a DT impulse response of a fractional delay operation may be expressed as

$$h_{ideal}[n_0,\phi] = \text{sinc}(n_0 - \phi),\ n_0 = ...,-1,0,1,..., \tag{2}$$

and a discrete-time Fourier transform (DTFT) of $h_{ideal}[n,\phi]$ may comprise:

$$H_{ideal}(e^{j\omega},\phi) = e^{-j\omega\phi},\ \omega \in [-\pi,\pi]. \tag{3}$$

As seen in (2), an ideal delay operation may be represented since it has impulse response with infinite length. Appropriate approximation to $h_{ideal}[n_0,\phi]$ is considered below.

In conventional iterative methods, an infinite sinc series may be truncated to approximate an ideal fractional delay operation, such as in (2). However, due at least in part to slow decay of the sinc function, truncation error for an approximation may at times be substantial. As a common practice, it may be assumed that a continuous-time signal $x_c(t)$ is slightly oversampled, and hence a DTFT of $x[n]$ is zero for $\alpha\pi \le |\omega| \le \pi$, $0 < \alpha < 1$. This assumption permits one to relax specification of $H_{ideal}(e^{j\omega},\phi)$ as follows:

$$H_{ideal}(e^{j\omega},\phi) = e^{-j\omega\phi},\ \omega \in [-\alpha\pi,\alpha\pi]. \tag{4}$$

Let $h[n_0,\phi]$ be a corresponding approximation of an ideal impulse response $h_{ideal}[n_0,\phi]$. Assume that a frequency response of $h[n_0,\phi]$ is designed to approximate $H_{ideal}(e^{j\omega},\phi)$ in a frequency band of interest, Eqn. (1) may be rewritten as

$$y[n] \approx \sum_{k=n-N_{h2}}^{n+N_{h1}} x[k]\cdot h[n-k,\phi_n],\ \forall n. \tag{5}$$

where, N_{h1} and N_{h2} are positive integers. Let us now consider two possible cases.

Case 1: N_{h1} and N_{h2} are finite; $h[n_0,\phi]$ may be realized as a FIR filter parameterized by fractional delay ϕ_n.

Case 2: N_{h1} is finite and N_{h2} are infinite; $h[n_0,\phi]$ may be realized as an IIR filter parameterized by fractional delay ϕ_n. Now let us consider a matrix form of (5):

$$\boldsymbol{y} = \boldsymbol{A}\boldsymbol{x}, \tag{6}$$

where $y=[y[-\infty],\cdots,y[\infty]]^T$, $x=[x[-\infty],\cdots,x[\infty]]^T$ and $[A]_{n,k}=a_{n,k}=h[n-k,\phi_n]$, for $n,k=\cdots,-1,0,1,\cdots$.

One challenge may be to recover a uniform sequence x, given its nonuniform counterpart y. For example, it may be desired to process a system of linear equations in (7), provided below. For sake of presentation, $\{y[n]\}$ and $\{x[n]\}$ are assumed to be DT signals with a finite but sufficiently large number of digital signal samples values. Thus, y and x may be described in this particular embodiment as $(N\times 1)$ vectors and A comprises $(N\times N)$ matrix. Also, $h[n_0,\phi_n]$ is assumed to be noncausal, although, of course, claimed subject matter is not limited in scope in this respect. Furthermore, for implementation purposes, introducing appropriate delays may be provided.

Matrix A may have characteristics, such as: (i) Assuming that $\phi_n\in(-0.5,0.5)$, A is nonsingular. (ii) A effectively comprises a banded matrix because $h[n_0,\phi_n]$ is zero for $n_0<-N_{h1}$ and $n_0>N_{h2}$. (iii) Since $h[n_0,\phi_n]$ tends to zero as $|n_0|$ increases, absolute values of diagonal elements of A are greater than those of other off-diagonal elements. For small ϕ_n, A comprises a diagonally dominant matrix (e.g., $|a_{n,n}|>\sum_{n\neq k}|a_{n,k}|$, for all n).

For high-speed applications, directly inverting A to find x may be undesirable at least partially due to computational complexity. However, it is noted that A exhibits a relatively sparse structure. Therefore, one may have the ability to determine x using iterative methods. Various iterative methods have been studied; see, for example, Y. Saad, "Iterative methods for sparse linear systems," *Boston, Mass.: PWS Publ., Company*, 1996. For implementation, methods which may be realized in a sample-by-sample manner, for example, may provide a desirable approach. Many may take a form

$$x^{(m+1)}=Gx^{(m)}+f, \tag{7}$$

where G and f are derived from A and y, and $x^{(m)}$ denotes a solution in an m-th iteration.

We next consider partitioning A to form G. For example, let's define a decomposition: $A=D-L-U$, where D , $-L$ and $-U$ are respectively diagonal negative strictly lower triangular and diagonal negative strictly upper triangular parts of matrix A. Iterative methods may include, without limitation, for example:

(i) Richardson Iteration (RI):

With $\boldsymbol{G} = \boldsymbol{I} - \mu\boldsymbol{A}$ and $\boldsymbol{f} = \mu\boldsymbol{y}$ for some μ, component-wise form may be given by:

$$x^{(m+1)}[n] = x^{(m)}[n] + \mu\left(y[n] - \sum_{k=n-N_{h2}}^{n+N_{h1}} x^{(m)}[k] \cdot h[n-k,\phi_n] \right),\ n = 0,\cdots,N-1.$$

(ii) Jacobi iteration (JI):

With $\boldsymbol{G} = \boldsymbol{D}^{-1}(\boldsymbol{L} + \boldsymbol{U})$ and $\boldsymbol{f} = \boldsymbol{D}^{-1}\boldsymbol{y}$, component-wise form may be given by:

$$x^{(m+1)}[n] = h[0,\phi_n]^{-1}\left(y[n] - \sum_{k=n-N_{h2}}^{n-1} x^{(m)}[k] \cdot h[n-k,\phi_n] - \sum_{k=n+1}^{n+N_{h1}} x^{(m)}[k] \cdot h[n-k,\phi_n] \right),\ n = 0,\cdots,N-1.$$

(iii) Gauss-Seidel iteration (GSI):

With $\boldsymbol{G} = (\boldsymbol{D} - \boldsymbol{L})^{-1}\boldsymbol{U}$ and $\boldsymbol{f} = (\boldsymbol{D} - \boldsymbol{L})^{-1}\boldsymbol{y}$, component-wise form may be given by:

$$x^{(m+1)}[n] = h[0,\phi_n]^{-1}\left(y[n] - \sum_{k=n-N_{h2}}^{n-1} x^{(m+1)}[k] \cdot h[n-k,\phi_n] - \sum_{k=n+1}^{n+N_{h1}} x^{(m)}[k] \cdot h[n-k,\phi_n] \right),\ n = 0,\cdots,N-1.$$

Alternatively, other similar iterative methods may be used as well. As just one additional example, successive over relaxation may be applied. Therefore, claimed subject matter is not limited in scope to application of any particular method of iterating or iterative partitioning or decomposition.

It should be noted that iterative methods such as described in F. Marvasti, M. Analoui, and M. Gamshadzahi, "Recovery of signals from nonuniform samples using iterative methods," *IEEE Trans. Signal Process.*, vol. 39, pp. 872-877, April 1991; E. I. Plotkin, M. N. S. Swamy and Y. Yoganandam, "A novel iterative method for the reconstruction of signals from nonuniformly spaced samples," *Signal Process.*, vol. 37, pp. 203-213, 1994; and F. Marvasti, *Nonuniform Sampling, Theory and Practice*. Norwell, MA: Kluwer, 2001 are similar to RI. However, in a particular embodiment, a system matrix may be formed by truncating a sinc series. A matrix entry may be nonzero for $\phi_n \neq 0$. However, matrix multiplications with a large batch of digital signal sample values may be involved to recover one uniform sample, making them less attractive in real-time applications, such as TI ADCs. Another disadvantage may be an ill-behaved system matrix formed by a truncated sinc series, which may result in a lower convergence rate or potentially raise implementation cost.

Two embodiments to approximate an ideal fractional delay operation are provided, although claimed subject matter is not limited in scope to these two approaches alone. One simple approach may include approximating a fractional delay operation as in (5) by a digital FIR filter with fixed coefficients. A possible or potential drawback may be determining $h[n_0,\phi_n]$ for various values of ϕ_n, which may make real-time applications more challenging to implement.

Another alternative, however, may include employing so-called variable digital filters (VDFs) or, more appropriately, variable fractional delay digital filters (VFDDFs). In a VFDDF, digital signal sample values at fractional sampling intervals may be computed by tuning a parameter, known as a tuning or spectral parameter. An ideal zero-phase response may be substantially identical to (4), where, in contrast to fixed filter coefficients, tuning parameter ϕ may be assumed to vary in a finite interval, such as $(-0.5,0.5)$, for example. Therefore, the amount of delay of a desired VFDDF output may be continually adjusted by changing ϕ. In one example embodiment, an impulse response of a VFDDF may comprise polynomial in ϕ, although claimed subject matter is not limited in scope to employing only a polynomial approach. For one particular embodiment or sample implementation:

$$h[n_0,\phi]=\sum_{l=0}^{L-1}h_l[n_0]\cdot\phi^l,\ n_0=-N_{h1},\cdots,0,\cdots,N_{h2}. \tag{8}$$

in which L comprises the number of sub-filters and $h_l[n_0]$ comprises an impulse response of an l-th sub filter.

If $N_{h1}=N_{h2}=N_h$ for some finite positive integer N_h and $h[0,\phi]$ is chosen as the center of symmetry of the impulse response if $\phi=0$, $h[n_0,\phi]$ may exhibit coefficient symmetry, such as: $h[n_0,\phi]=h[-n_0,-\phi]$, $n_0=-N_h,\cdots,0,\cdots,N_h$. Subfilter coefficients $h_l[n_0]$ may also satisfy $h_l[n_0]=(-1)^l h_l[-n_0]$, $n_0=-N_h,\cdots,0,\cdots,N_h$, $l=0,\cdots,L-1$. Complexity of a design or implementation of an VFDDF, for such an embodiment, for example, may be reduced approximately by a factor of two. VFDDF may be referred to as a linear-phase FIR VFDDF, for example.

One potential or possible disadvantage of an embodiment or approach employing VDFs or VFDDFs may be that coefficients of $h[n_0,\phi_n]$ may change with time instant n. Therefore, multipliers may be included in an implementation. High implementation complexity or

power consumption which at times may be associated with general-purpose multipliers, however, may be typically undesirable for high-speed real-time applications. Nonetheless, in one embodiment, as explained in more detail below, an iterative method may be implemented where the number of general purpose multipliers is limited, providing more desirable results. Although claimed subject matter is not limited in scope to a particular embodiment, a Farrow structure may be utilized in at least one embodiment, as described in more detail below.

For example, it may be possible to write RI as:

$$x^{(m+1)}[n] = x^{(m)}[n] + \mu e^{(m)}[n], \quad n = 0, \cdots, N-1, \tag{9}$$

where $e^{(m)}[n] = y[n] - y^{(m)}[n]$ and $y^{(m)}[n] = \sum_{k=n-N_{h2}}^{n+N_{h1}} x^{(m)}[k] h[n-k, \phi_n]$. RI may, therefore be implemented by digital filtering to obtain $y^{(m)}[n]$. We begin with a derivation of an transfer operation between input signal sample values and output signal sample values for $x^{(m)}[n]$ and $y^{(m)}[n]$. According to (8) and (9), we have

$$H_{RI}(z,\phi) = H(z,\phi) = \sum_{l=0}^{L-1} H_l(z)\phi^l = \sum_{l=0}^{L-1}\left[\sum_{n_0=-N_{h1}}^{N_{h2}} h_l[n_0] z^{-n}\right]\phi^l, \tag{10}$$

where $H_l(z)$ comprises a z-transform of l-th subfilters. Note for Case 1 wherein N_{h2} is finite, $H_{RI}(z,\phi)$ comprises an FIR VDF. On the other hand, for Case 2 where N_{h2} is infinite, $H_{RI}(z,\phi)$ comprises an IIR VDF. Of course, again, these are examples and claimed subject matter is not limited in scope in these respects necessarily.

FIG. 2 is a block diagram of an example implementation of an embodiment of a Farrow structure used to implement a VDF. For example, referring to (10), an implementation may employ L subfilters $H_l(z)$ and a tuning parameter ϕ. In a subfilter module, subfilter output sequences of digital signal sample values $u_l[n]$ may be obtained by filtering a DT input sequence of digital signal sample values using subfilters $H_l(z)$, $l = 0, \cdots, L-1$, respectively. In an interpolation module, an output sequence of digital signal sample values may be given by the value of a polynomial of degree $L-1$ evaluated at a given ϕ, where coefficients in ascending powers of a polynomial are given by subfilter output sequences of digital signal sample values $u_l[n]$. Again, claimed subject matter is, of course, not limited in scope to a particular embodiment. Nonetheless, as one example, a subfilter module of a Farrow structure may include digital filters with fixed coefficients. It may, therefore, in at least one embodiment, be implemented using sum-of-power-of-two (SOPOT) coefficients or canonical

signed digits to replace general-purpose multipliers. See, for example, Y. C. Lim and S. R. Parker, "FIR filter design over a discrete power-of-two coefficient space," *IEEE Trans. ASSP-31*, pp. 583-591, April 1983. In addition, if subfilters are implemented in transposed form, redundancy in realizing multiplications of SOPOT coefficients may also be reduced by a multiplier-block technique, which may give rise to an implementation that reduces the number of adders employed. See, for example, A. G. Dempster and M. D. MacLeod, "Use of minimum-adder multiplier blocks in FIR digital filters," *IEEE Trans. Circuits Syst. II*, pp. 569-577, Sept. 1995. A structure may be implemented, such as on an integrated circuit, as one example with a limited number of general purpose multipliers.

Nonetheless, in other or additional embodiments, additional improvements may additionally be possible, although claimed subject matter is not limited in scope to employing the additional improvements provided below. By substituting an impulse response of a VDF $H_{RI}(z,\phi)$ into (9), $y^{(m)}[n]$ may be provided as a sequence of digital signal sample values of a VDF with appropriate values of ϕ_n:

$$y^{(m)}[n] = \sum_{l=0}^{L-1} (x^{(m)} * h_l)[n] \cdot \phi_n^l , \tag{11}$$

where $*$ denotes a discrete-time convolution operation. FIG. 3(a) illustrates one example structure implemention of a VDF of the form of an m-th RI. From a digital signal processing point of view, RI delays a uniform sequence $x^{(m)}[n]$ by ϕ_n samples using a VDF to approximate $y^{(m)}[n]$, calculates error digital signal sample values, and updates $x^{(m)}[n]$ to get $x^{(m+1)}[n]$ until error is sufficiently small or a limit on number of iterations is reached.

In an m-th iteration, a particular implementation of RI may comprise:

- calculating a sequence $y^{(m)}[n]$ of digital signal sample values by filtering a sequence $x^{(m)}[n]$ of digital signal sample values with L subfilters of a variable digital filter $H_{RI}(z,\phi) = \sum_{l=0}^{L-1} \left[\sum_{n_0=-N_{h1}}^{N_{h2}} h_l[n_0] z^{-n} \right] \phi^l$, and combining L sequences of digital signal sample values using a Farrow structure with $\phi = \phi_n$ at time instant n,
- calculating a sequence $e^{(m)}[n]$ of digital signal sample values by subtracting filtered sequence $y^{(m)}[n]$ of digital signal sample values from a nonuniformly sampled sequence $y[n]$ of digital signal sample values,

- multiplying a sequence $e^{(m)}[n]$ of digital signal sample values with a scalar constant μ,
- calculating another uniform sequence $x^{(m+1)}[n]$ of digital signal sample values by adding a scaled sequence of digital signal sample values to $x^{(m)}[n]$, and
- repeating until an error sequence of digital signal sample values is sufficiently small or a number of iterations is reached.

Similarly, FIGs. 3b and 3c illustrate example implementations of structures of VDF-based approaches in the form of an m-th JI and GSI, respectively.

In an m-th iteration, JI comprises:

- calculating a sequence $p_1[n]$ of digital signal sample values by filtering a sequence $x^{(m)}[n]$ of digital signal sample values with L subfilters of a variable digital filter $H_{JI}(z,\phi)=\sum_{l=0}^{L-1}\left[\sum_{n_0=-N_{h1},n_0\neq 0}^{N_{h2}} h_l[n_0]z^{-n}\right]\phi^l$, and combining L sequences of digital signal sample values using a Farrow structure with $\phi=\phi_n$ at time instant n,
- calculating a sequence $p_2[n]$ of digital signal sample values by subtracting a filtered sequence of digital signal sample values from a nonuniformly sampled sequence $y[n]$ of digital signal sample values,
- calculating a sequence $x^{(m+1)}[n]$ of digital signal sample values by multiplying a subtracted sequence $p_2[n]$ of digital signal sample values with a time-varying constant $h[0,\phi_n]^{-1}$,
- repeating until an error sequence of digital signal sample values is sufficiently small or a number of iterations is reached.

Note for Case 1 wherein N_{h2} is finite, $H_{JI}(z,\phi)$ comprises an FIR VDF. On the other hand, for Case 2 wherein N_{h2} is infinite, $H_{JI}(z,\phi)$ comprises an IIR VDF.

In an m-th iteration, GSI comprises:

- calculating a sequence $s_1[n]$ of digital signal sample values by filtering a sequence $x^{(m)}[n]$ of digital signal sample values with L subfilters of a variable digital filter

$H_{GSI,1}(z,\phi)=\sum_{l=0}^{L-1}\left[\sum_{n_0=-N_{h1}}^{-1}h_l[n_0]z^{-n}\right]\phi^l$, and combining L sequences of digital signal sample values using a Farrow structure with $\phi=\phi_n$ at time instant n,

- calculating a sequence $s_2[n]$ of digital signal sample values by filtering a sequence $x^{(m+1)}[n]$ of digital signal sample values with L subfilters of a variable digital filter $H_{GSI,2}(z,\phi)=\sum_{l=0}^{L-1}\left[\sum_{n_0=1}^{N_{h2}}h_l[n_0]z^{-n}\right]\phi^l$, and combining L sequences of digital signal sample values using Farrow structure with $\phi=\phi_n$ at time instant n,
- calculating a sequence $s_3[n]$ of digital signal sample values by subtracting two filtered sequences $s_1[n]$ and $s_2[n]$ of digital signal sample values from a nonuniformly sampled sequence $y[n]$ of digital signal sample values,
- calculating a sequence $x^{(m+1)}[n]$ of digital signal sample values by multiplying a subtracted sequence $s_3[n]$ of digital signal sample values with a time-varying constant $h[0,\phi_n]^{-1}$,
- repeating until an error sequence of digital signal sample values is sufficiently small or a number of iterations is reached.

Note for Case 1 wherein N_{h2} is finite, $H_{GSI,2}(z,\phi)$ comprises an FIR VDF. On the other hand, for Case 2 wherein N_{h2} is infinite, $H_{GSI,2}(z,\phi)$ comprises an IIR VDF. In both cases, $H_{GSI,1}(z,\phi)$ may therefore be implemented as a FIR VDF, if desired.

One aspect of iterative methods relates to conditions for convergence. It is known that an iteration in (8) converges for any $\boldsymbol{f}$ and $\boldsymbol{x}^{(0)}$ if and only if (iff) a spectral radius of $\boldsymbol{G}$, $\rho(\boldsymbol{G})$, is less than one. However, due at least in part to large N and time-varying parameter ϕ_n (and hence $\boldsymbol{A}$) in general, it may at times be difficult to derive a necessary and sufficient condition based even at least in part on the spectral radius of $\boldsymbol{G}$.

For RI, for example, using $\rho(\boldsymbol{G})\le\|G\|$ for a matrix norm, RI converges for $\boldsymbol{f}$ and $\boldsymbol{x}^{(0)}$ iff $\|\boldsymbol{G}\|<1$ [11]. We shall consider:

$$\|\boldsymbol{G}_\mu\|_\infty=\|\boldsymbol{I}-\mu\boldsymbol{A}\|_\infty=\max_{0\le n\le N-1}\left\{\sum_{k=0}^{N-1}\left|\delta_{n,k}-\mu\cdot a_{n,k}\right|\right\}=\max_{0\le n\le N-1}\left\{\sum_{n_0=-N_{h1}}^{N_{h2}}\left|g_\mu[n_0,\phi_n]\right|\right\},$$

where $g_\mu[0,\phi_n]=1-\mu h[0,\phi_n]$ and $g_\mu[n_0,\phi_n]=-\mu h[n_0,\phi_n]$ for $n_0\neq 0$. Here, we define a cost function or operation:

$$C_1(\mu,\phi_{\max})=\max_{|\phi|\leq\phi_{\max}}\left\{\sum_{n_0=-N_{h1}}^{N_{h2}}\left|g_\mu[n_0,\phi]\right|\right\}.$$

where $\phi_{\max}$ denotes a limit on absolute time-skew error given by $\max\{|\min\{\phi_n\}|,|\max\{\phi_n\}|\}$. For a relatively fast convergence, it would be desirable to find μ for a given $\phi_{\max}$ such that $C_1(\mu,\phi_{\max})$ comprises a limited value. Here, conditions for convergence may be handled numerically by considering values of μ and $\phi_{\max}$ that achieve a limited value for $C_1(\mu,\phi_{\max})$.

In contrast, for JI and GSI, JI and GSI converge for f and $x^{(0)}$ iff A comprises a diagonally dominant matrix. See, for example, Y. Saad, "Iterative methods for sparse linear systems," *Boston, Mass.: PWS Publ., Company*, 1996. That is $|a_{n,n}|>\sum_{n\neq k}|a_{n,k}|$, for all n, which is equivalent to

$$|h[0,\phi_n]|>\sum_{n_0\neq 0}|h[n_0,\phi_n]|, \text{ for all } \phi_n.$$

We define a cost function:

$$C_2(\phi_{\max})=\max_{|\phi|\leq\phi_{\max}}\left\{|h[0,\phi]|-\sum_{n_0\neq 0}|h[n_0,\phi]|\right\},$$

to check whether A comprises a diagonally dominant matrix for a given $\phi_{\max}$.

Experiments have been conducted on several VFDDFs with different conditions being specified. A useful condition for three iteration processes discussed comprises $\phi_{\max}$ being at least 0.15. This range of support may be satisfactory for many applications. For example, $\phi_{\max}$ is around a few percent of a sampling period in the case of TI ADCs.

In a possible iterative embodiment, reconstruction performance may be assessed using a signal to noise and distortion ratio (SNDR):

$$SNDR=\frac{\sum_n(x[n])^2}{\sum_n(x[n]-x^{(m)}[n])^2}.$$

For example, although claimed subject matter is not limited in scope in this respect, a VFDDF may be designed, for example, using convex programming, see, for example, K. M.

Tsui, S. C. Chan and K. W. Tse, "Design of complex-valued variable digital filters and its application to the realization of arbitrary sampling rate conversions for complex signals," *IEEE Trans. Circuits Syst. II*, vol. 52, issue 7, pp. 424-428, July, 2005, with the following specifications: $N_{h1} = N_{h2} = N_h = 35$, number of subfilters $L = 4$, $\omega \in [-0.9\pi, 0.9\pi]$, and $\phi \in [-0.1, 0.1]$. A sequence of input digital signal sample values may be given by $\sum_{k=1}^{10} \cos[nk(0.09\pi)]$ for evaluation. Timing mismatch error ϕ_n may be randomly chosen in an interval $(-\phi_{\max}, \phi_{\max})$. FIG. 4 is a signal plot illustrating performances if $\phi_{\max} = 0.1$, respectively, for various iteration approaches. While GSI offers the fastest convergence rate among the three, RI and JI exhibit similar performances. Generally, SNDR should improve with (i) increased filter order (ii) increased number of subfilters, (iii) reduced passband width, or (iv) reduced tuning range of the VFDDF.

FIG. 5 is a block diagram of an example implementation of an embodiment of a *M*-channel time-interleaved analog-to-digital converter with iterative timing mismatch being addressed at least in part. In an *M*-channel TI ADC, *M* ADCs may be operated in parallel, but sampling instants between two adjacent ADCs may differ by their clock period. Ideally, if *M* ADCs are nearly identical functionally and channel output signal sample values are combined appropriately, an equivalent high-speed ADC should provide at least similar or approximately the same precision as channel ADCs, but offering a speed *M* times faster. However, small mismatches between *M* ADCs may lead to degraded performance. TI ADCs may provide time-skew between different subconverters. If time-skew for channel ADCs remains relatively stable over a period, however, this may be satisfactorily employed in connection with periodic nonuniform sampling as follows:

$$\phi_n = \phi_{n+M} \text{ , for all } n,$$

which belongs to a subclass of nonuniform sampling as shown in FIG. 1(b). Implementations or example embodiments of iterative methods or structures may therefore be applied to at least in part address timing mismatch in TI ADCs.

Making use of periodicity of a nonuniform sampling pattern, for example, FIG. 6 is a block diagram of an embodiment for an example implementation. Although claimed subject matter is not limited in scope in this respect, an implementation may include a modified Farrow structure. For example, an implementation may include

- A subfilter module arranged to calculate subfilter output sequences $u_l[n]$ of digital signal sample values by filtering an input sequence of digital signal sample values using subfilters $H_l(z)$, $l = 0,\cdots,L-1$, respectively.
- L demultiplexers arranged to divide respective subfilter output sequences $u_l[n]$ of digital signal sample values to form M subsequences $v_{l,m}[n]$, $m = 0,\cdots,M-1$, of digital signal sample values in a cyclic manner so that data rate is lowered by a factor of M.
- M interpolation modules arranged to calculate respective interpolated subsequences $w_m[n]$ of digital signal sample values by calculating a signal sample value of a respective polynomial of degree $L-1$ evaluated at ϕ_m, where coefficients in ascending powers of the polynomial are given by demultiplexed subsequences $v_{l,m}[n]$ of digital signal sample values where $l = 0,\cdots,L-1$.
- A multiplexer arranged to combine M interpolated subsequences $w_m[n]$ of digital signal sample values to form a desired output sequence of digital signal sample values.

In an interpolation module, an embodiment, for example, multiplication with respective tuning parameter ϕ_m per unit time may be reduced by a factor of M. For example, a power-consuming module may be operated at a subconverter data rate.

In yet another embodiment, to speed-up the iterative process, iterative timing mismatch may be addressed as shown in FIG. 5 through a pipelined implementation such that a pipeline stage may comprise one iteration, as shown in FIG 3, for example.

As still another example implementation, in an eight-channel TI ADC, using input digital signal sample values and a VFDDF, without limitation, FIG. 7(a) shows an uncorrected signal spectrum with timing offsets given by $\phi_0 = 0$, $\phi_1 = 0.05$, $\phi_2 = 0.1$, $\phi_3 = -0.04$, $\phi_4 = -0.08$, $\phi_5 = 0.07$, $\phi_6 = 0.02$ and $\phi_7 = -0.06$. The plot shows that the largest aliasing component is about -19.6 dB. FIG. 7(b) shows the spectrum of a reconstructed signal which is obtained by passing an uncorrected signal through a VFDDF-based implementation in the form of RI four times. The largest aliasing component is reduced to about -95 dB as a result. Similar results are possible for embodiments of JI and GSI as previously described.

In yet another embodiment, a linear time varying analog filter may be employed before a nonuniform sampler, such as the embodiment shown in FIG. 1(c). FIG. 8 comprise a block

diagram illustrating an embodiment that includes a linear time varying analog filter implementation, although claimed subject matter is not limited in scope to this particular example implementation. One advantage of this particular example implementation includes that the relationship in (6) may made more general:

$$y = \boldsymbol{ABx},$$

where $\boldsymbol{B}$ comprises DT description or representation of a linear time varying analog filter system. Thus, for example, assuming $\boldsymbol{AB}$ satisfies conditions mentioned earlier, iterative methods may be employed to determine $\boldsymbol{x}$ from $\boldsymbol{y}$, similar to approaches previously discussed. A variety of processes may take this particular form; although, again, this is merely one example of an illustrative embodiment and claimed subject matter is not intended to be limited in scope to this example.

It is further noted that while the previous discussion has focused on embodiments involving signals employing one spatial domain, claimed subject matter is not so limited. Therefore, embodiments may include signals in two or three spatial domains, if desired. Furthermore, other multi-dimensional approaches may be employed beyond three dimensions, although additional dimensions typically will not comprise spatial dimensions.

In summary, implementations for digital filtering have been described with a nonuniformly sampled sequence $y[n]$ of digital signal sample values, which may be obtained by sampling a bandlimited continuous-time signal $x_c(t)$ at irregular time instants substantially according to $y[n] = x_c(nT - \phi_n T)$, where T comprises a sampling period and $|\phi_n| \le 0.5$. An embodiment is provided in which reconstruction of uniform samples from nonuniform samples may be constructed and an embodiment is provided where, likewise, a similar approach may be applied to address timing mismatch in M-channel time-interleaved (TI) analog-to-digital converters (ADCs). In one particular embodiment, a system of linear equations may be constructed to represent the relation of $x[n]$ and $y[n]$ using an approximation of the sinc function in a frequency range of interest, e.g., the signal bandwidth. For example, a CT signal $x_c(t)$ may be slightly oversampled. This approximation therefore leads to a variety of practical implementations of the system. Approximated sinc series may be represented, for example, by coefficients of fractional delay digital filters. A system of linear equations may also be processed using iterative approaches.

Some embodiments may be implemented efficiently by variable digital filters based at least in part on a Farrow structure implementation, such as described, for example, in C. W. Farrow, "A Continuously Variable Digital Delay Element," in *Proc. IEEE ISCAS*, vol. 3, pp. 2641-2645, 1988. One advantage of a Farrow structure is that its coefficients may be varied in real-time to cope with possibly changing timing mismatch. Furthermore, it may be implemented relatively efficiently in hardware without multiplications, apart from a limited number of general purpose multipliers to implement tuning variables in a Farrow structure implementation. For application to timing mismatch in TI ADC, in one particular embodiment, a modified Farrow structure may be employed to accomplish multiplication with a tuning parameter at a subconverter data rate.

Although embodiments have been fully described with reference to accompanying drawings, it is to be noted that various changes or modifications, for example extension to two-spatial dimension signal reconstruction or three-spatial dimension signal reconstruction, for example, may be accomplished. Changes or modifications, whether apparent to one of ordinary skill in the art or not, are to be understood as being included within the scope of claimed subject matter.

Claims:

1. An integrated circuit comprising:

a digital filter, said digital filter having an input port and an output port;

said input port of said digital filter to receive substantially non-uniform digital signal samples;

said output port of said digital filter to provide substantially uniform digital signal samples;

said digital filter to further process said non-uniform digital signal sample values using a variable delay digital filter to iteratively recover said uniform digital signal sample values.

2. The integrated circuit of claim 1, wherein said digital filter is part of an analog-to-digital converter.

3. The integrated circuit of claim 2, wherein said digital filter is applied to address timing mismatch for time-interleaved analog-to-digital conversion.

4. The integrated circuit of claim 1, wherein at least one of the following is integrated within said integrated circuit (IC) so as to be performed during IC operation: a Richardson iteration; a Jacobi iteration; a Gauss-Seidel iteration; or any combination thereof.

5. The integrated circuit of claim 1, wherein said digital filter is implemented without employing multiplication other than a limited number of general purpose multipliers.

6. A method comprising:

digital filtering substantially non-uniform digital signal sample values using a variable delay digital filter implemented as an iterative process; and

outputting substantially uniform digital signal sample values.

7. The method of claim 6, and further comprising;

prior to said digital filtering, receiving said substantially non-uniform digital signal sample values.

8. The method of claim 6, wherein said substantially non-uniform digital signal sample values are obtained by sampling an analog signal.

9. The method of claim 8, wherein said analog signal is pre-filtered by a linear time varying analog filter.

10. The method of 6, and further comprising:

applying an iterative process to a system of relationships to characterize the relation between said substantially uniform digital signal sample values and said substantially nonuniform digital signal sample values so as to determine a sequence to approximate said substantially uniform digital signal sample values.

11. The method of claim 10, wherein said system of relationships employs coefficients of a fractional delay digital filter to approximate an ideal frequency response.

12. The method of claim 11, wherein said fractional delay digital filter is realized as a finite duration impulse response (FIR) or an infinite duration impulse response (IIR) digital filter with fixed or variable coefficients.

13. The method of claim 10, wherein said iterative process operates in a sample-by-sample manner.

14. The method of claim 13, wherein said iterative process comprises at least one of the following: a Richardson iteration process; a Jacobi iteration process; a Gauss-Seidel iteration process; or any combination thereof.

15. The method of claim 6, wherein said digital filtering comprises: parallel digital sampling of M channels wherein sampling instants between two consecutive digital signal sample values are shifted by a fraction 1/M of the clock period.

16. A method comprising: the sampling method of claim 14, wherein accuracy or computational speed is increased by a factor of the sampling period.

17. The method of claim 15, wherein at least some of said channels include a sub-converter; and further comprising: processing said non-uniform system sample values to reduce time-skew between different subconverters.

18. A method comprising: a useful application of said integrated circuit of claim 1, wherein said uniform digital signal sample values are utilized for ADC processing.

19. A system comprising:

a digital filter to receive substantially non-uniform digital signal samples and to provide substantially uniform digital signal samples;

said digital filter to further process said non-uniform digital signal sample values using a variable delay digital filter to iteratively recover said substantilally uniform digital signal sample values;

wherein said digital filter is structured to apply iterative processes that comprise one or more variable digital filters, at least one of said variable digital filters comprising L subfilters and a tuning parameter implemented using a Farrow structure.

20. The system of claim 19, wherein said Farrow structure comprises: a subfilter arranged to calculate subfilter output sequences $u_l[n]$ of digital signal sample values by filtering an input sequence of digital signal sample values with subfilters $H_l(z)$, $l = 0, \cdots, L-1$, respectively; and

an interpolation filter arranged to calculate an output sequence of digital signal sample values by calculating a signal sample value of an expression evaluated at a given ϕ, wherein coefficients in ascending powers of said expression are given by said sequences $u_l[n]$ of digital signal sample values.

21. The system of claim 20, wherein said interpolation filter is arranged to calculate an output sequence of digital signal sample values by calculating an signal sample value of a polynomial of degree $L-1$ evaluated at a given ϕ, wherein coefficients in ascending powers of said polynomial are given by said sequences $u_l[n]$ of digital signal sample values.

22. The system of claim 21, wherein filtering operations in said subfilter module are implemented via adders and shift registers.

23. The system of claim 21, wherein said addition or shift operations are implemented via a sum-of-power-of-two coefficient representation and multiplier-block realization.

24. A signal converter system, comprising:

an M-channel time-interleaved analog-to-digital converter, wherein M analog-to-digital subconverters with approximately similar speed are operated in parallel such that an output sampling rate is M times faster than that of one of said subconverters; and

an iterative timing mismatch adjuster used to reduce timing mismatch of the output sequence from said M-channel time-interleaved analog-to-digital converter.

25. The system of claim 24, wherein said iterative timing mismatch adjuster is based at least in part on an iterative process including at least one of the following: a Richardson iteration process; a Jacobi iteration process; a Gauss-Seidel iteration process; or any combination thereof.

26. The system of claim 25, wherein said iterative timing mismatch adjuster comprises one or more variable digital filters, a variable filter comprising L subfilters and a tuning parameter ϕ, and is implemented via a modified Farrow structure.

27. The system of claim 26, wherein said modified Farrow structure comprises:

a subfilter arranged to calculate subfilter output sequences $u_l[n]$ by filtering an input sequence of digital signal sample values with subfilters $H_l(z)$, $l = 0, \cdots, L-1$, respectively;

L demultiplexers, at least one of said demultiplexers arranged to divide respective subfilter output sequences $u_i[n]$ of digital signal sample values to form M subsequences $v_{i,m}[n]$, $m = 0, \cdots, M-1$, of digital signal sample values in a cyclic manner such that data rate is lowered by a factor of approximately M;

M interpolation filters, at least one of said interpolation filters arranged to calculate respective interpolated subsequences $w_m[n]$ of digital signal sample values by calculating respective signal sample values of a polynomial of degree $L-1$ evaluated at ϕ_m, wherein coefficients in ascending powers of said polynomial are given by demultiplexed subsequences $v_{i,m}[n]$, $i = 0, \cdots, L-1$ of digital signal sample values; and

a multiplexer arranged to combine M interpolated subsequences $w_m[n]$ of digital signal sample values to form a desired output sequence of digital signal sample values.

28. The system of claim 27, wherein said iterative timing mismatch adjuster is pipelined such that at least one pipeline stage is constructed to implement at least one iteration.

29. The method of claim 1, wherein said digital signal samples comprise digital signal samples of a two-spatial dimension or of a three-spatial dimension continuous time signal.

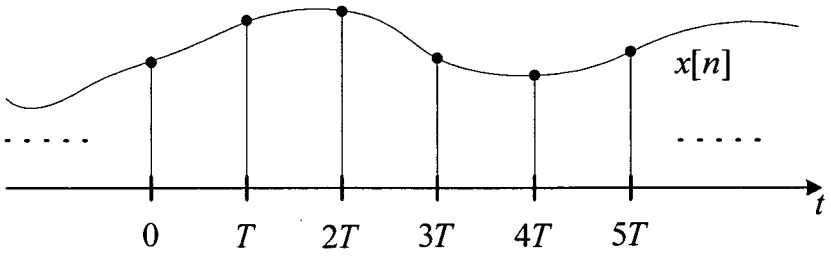


FIG. 1(a)

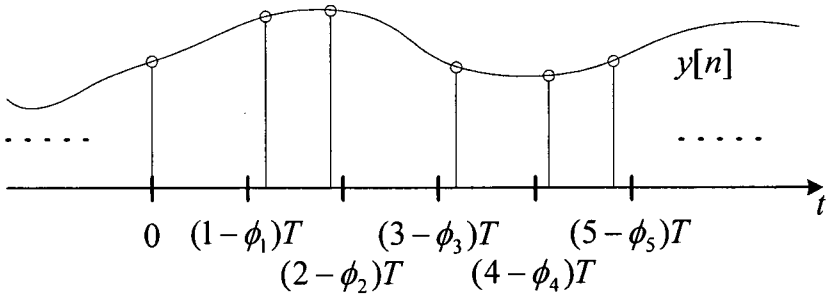


FIG. 1(b)

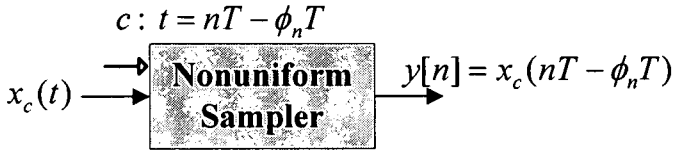


FIG. 1(c)

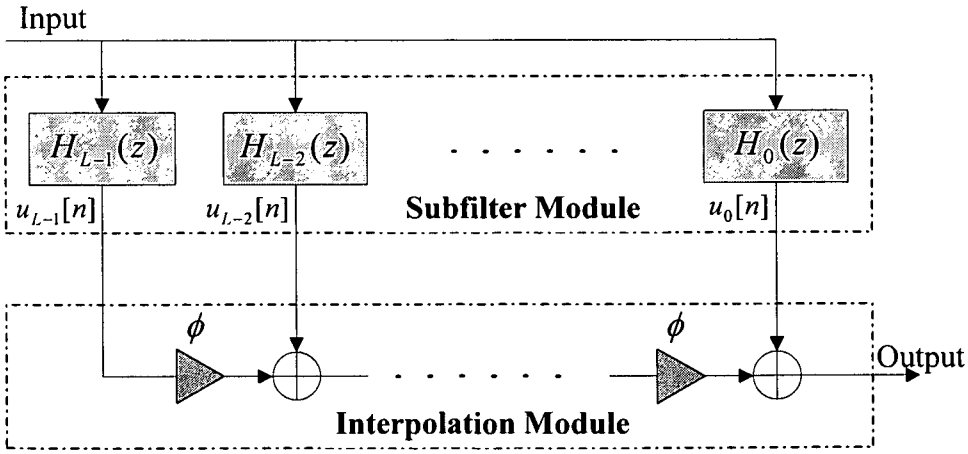


FIG. 2

$$H_{RI}(z,\phi) = H(z,\phi) = \sum_{l=0}^{L-1}\left[\sum_{n_0=-N_{h1}}^{N_{h2}} h_l[n_0]z^{-n}\right]\phi^l$$

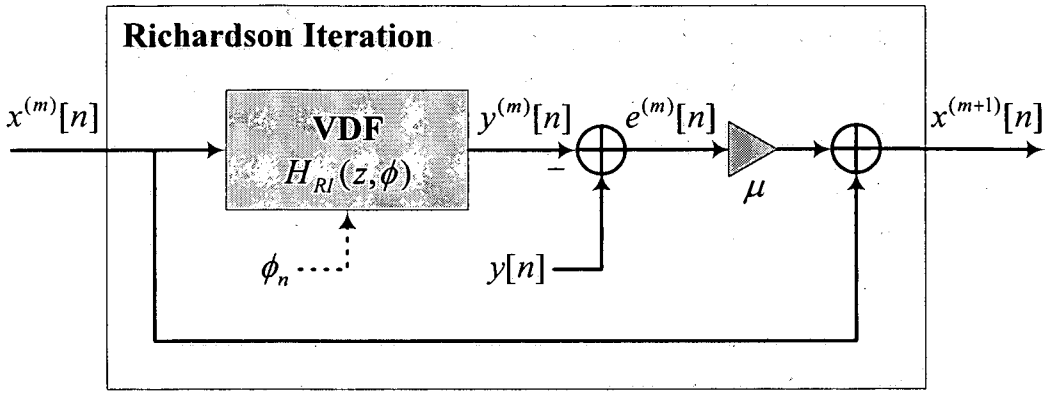


FIG. 3(a)

$$H_{JI}(z,\phi) = \sum_{l=0}^{L-1}\left[\sum_{n_0=-N_{h1},n_0\neq 0}^{N_{h2}} h_l[n_0]z^{-n}\right]\phi^l$$

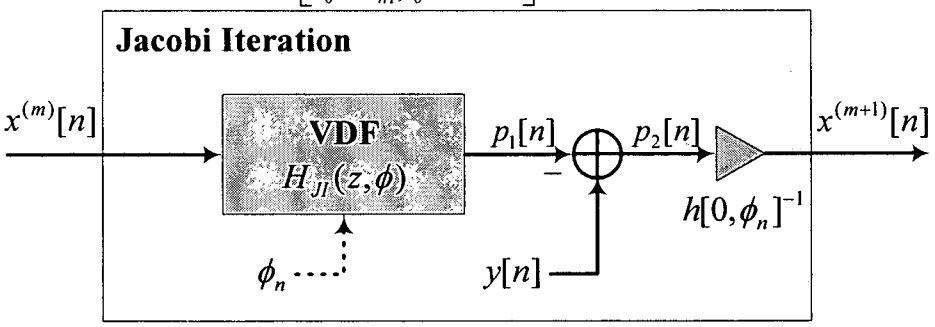


FIG. 3(b)

$$H_{GSI,1}(z,\phi) = \sum_{l=0}^{L-1}\left[\sum_{n_0=-N_{h1}}^{-1} h_l[n_0]z^{-n}\right]\phi^l,\ H_{GSI,2}(z,\phi) = \sum_{l=0}^{L-1}\left[\sum_{n_0=1}^{N_{h2}} h_l[n_0]z^{-n}\right]\phi^l$$

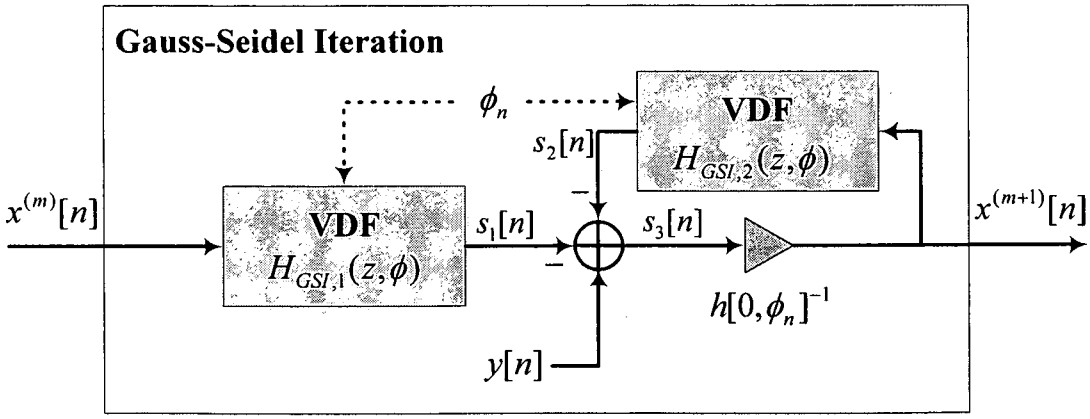


FIG. 3(c)

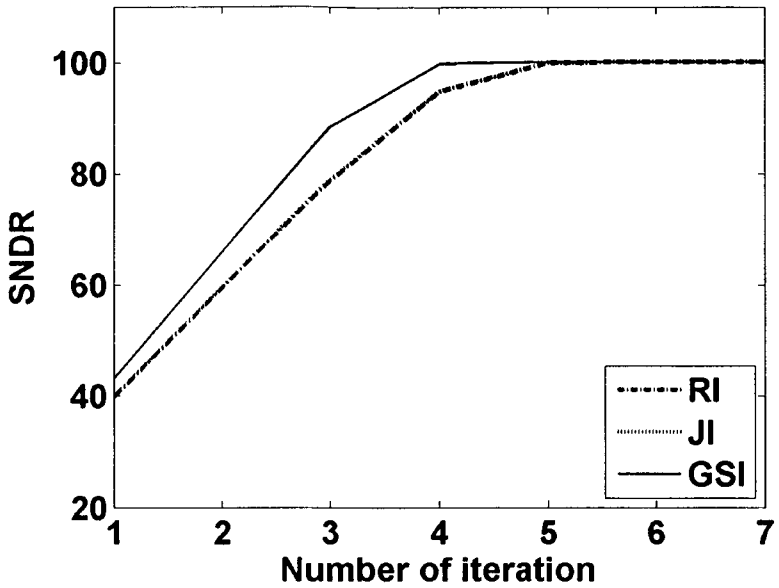

SNDR
100
80
60
40
20
1
2
3
4
5
6
7
Number of iteration
RI
JI
GSI

FIG. 4

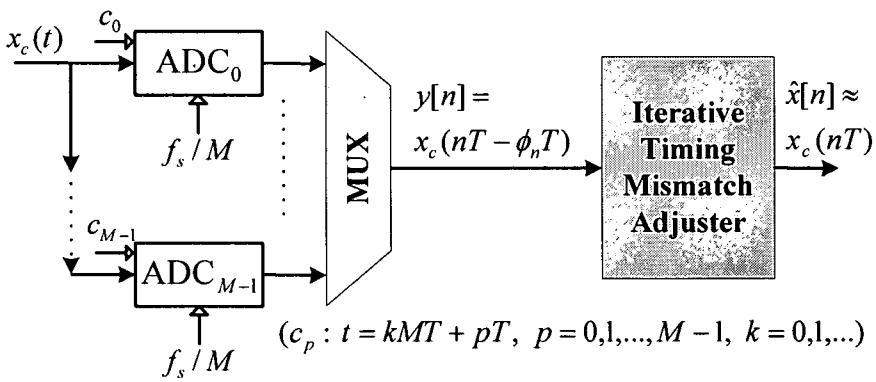

$x_c(t)$
c_0
ADC_0
f_s / M
c_{M-1}
ADC_{M-1}
f_s / M
MUX
$y[n] = x_c(nT - \phi_n T)$
Iterative Timing Mismatch Adjuster
$\hat{x}[n] \approx x_c(nT)$
$(c_p : t = kMT + pT,\ p = 0,1,...,M-1,\ k = 0,1,...)$

FIG. 5

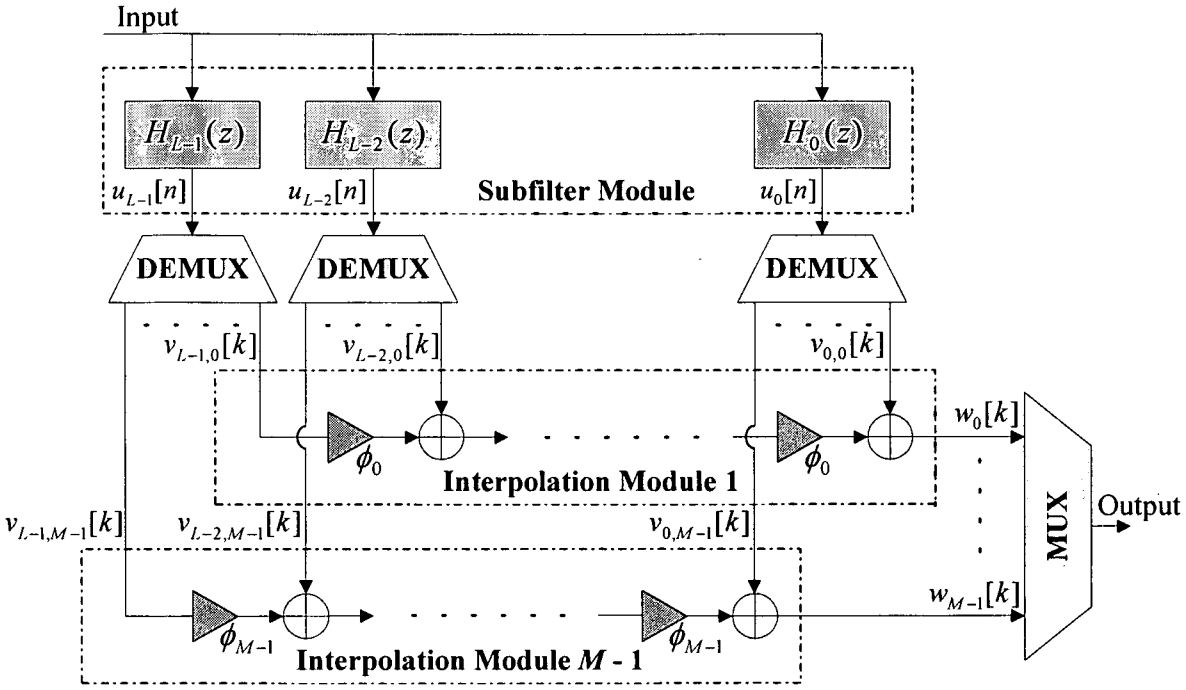

Input
$H_{L-1}(z)$
$H_{L-2}(z)$
$H_0(z)$
$u_{L-1}[n]$
$u_{L-2}[n]$
Subfilter Module
$u_0[n]$
DEMUX
DEMUX
DEMUX
$v_{L-1,0}[k]$
$v_{L-2,0}[k]$
$v_{0,0}[k]$
ϕ_0
ϕ_0
Interpolation Module 1
$w_0[k]$
$v_{L-1,M-1}[k]$
$v_{L-2,M-1}[k]$
$v_{0,M-1}[k]$
MUX
Output
$w_{M-1}[k]$
ϕ_{M-1}
ϕ_{M-1}
Interpolation Module M - 1

FIG. 6

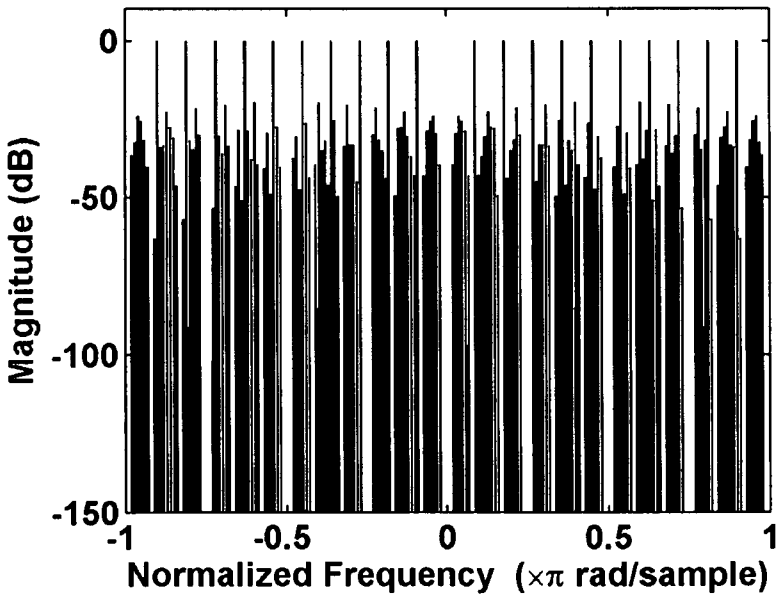

0
-50
-100
-150
Magnitude (dB)
-1
-0.5
0
0.5
1
Normalized Frequency (×π rad/sample)

FIG. 7(a)

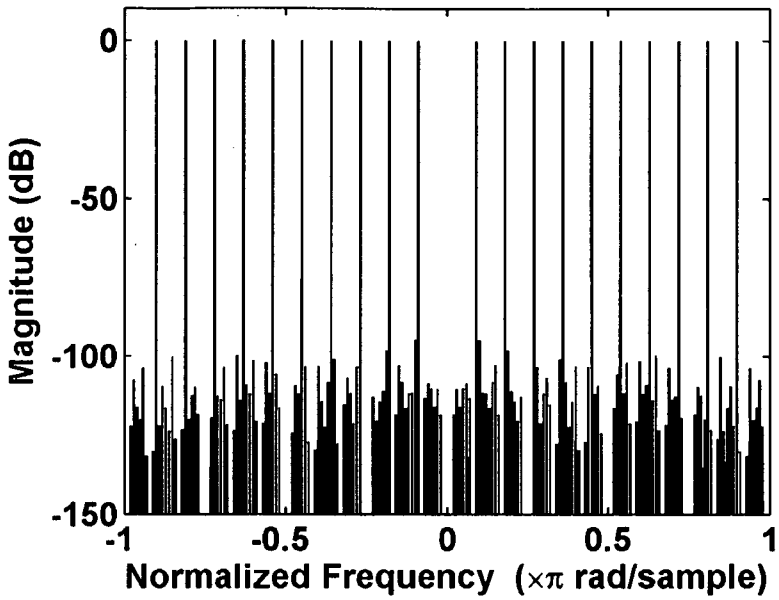

0
-50
-100
-150
Magnitude (dB)
-1
-0.5
0
0.5
1
Normalized Frequency (×π rad/sample)

FIG. 7(b)

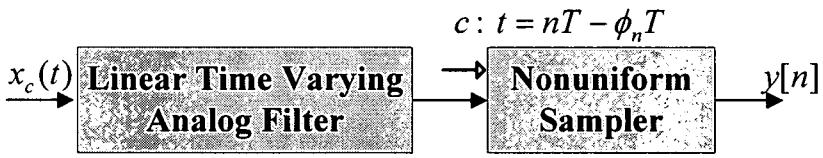

$c: t = nT - \phi_n T$
$x_c(t)$
Linear Time Varying Analog Filter
Nonuniform Sampler
$y[n]$

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2010/000549

A. CLASSIFICATION OF SUBJECT MATTER

H03M 1/12 (2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H03M1/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI,EPODOC,CNPAT: delay, filter, uniform, ADC, iterative

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	CN1468433A (INFINEON TECHNOLOGIES AG) 14 Jan. 2004 (14.01.2004) description page 1, 5-6 & Fig. 1b, 4	1,2,6,7,8,18
A		3-5, 9-17,19-29
Y	CN1358352A (INFINEON TECHNOLOGIES AG) 10 July 2002 (10.07.2002) description page 3-6 & Fig. 4	1,2,6,7,8,18
A		3-5, 9-17,19-29

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
05.July 2010 (05.07.2010)	**22 Jul. 2010 (22.07.2010)**
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer MA, Chi Telephone No. (86-10)62411641

Form PCT/ISA /210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2010/000549

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Claims 1,6,16,18,19 and 29 relate to a digital filter or a digital filtering step which uses a variable delay digital filter to iterative recover the uniform signal sample values.

Claim 24 does not relate to above features.

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☒ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2010/000549

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
CN1468433A	14.01.2004	WO0229806A1	11.04.2002
		SE0003549A	03.04.2002
		US2002075177A1	20.06.2002
		AU9048301A	15.04.2002
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		EP1330824A1	30.07.2003
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		CN100379154C	02.04.2008
		DE60132797T2	12.02.2009
CN1358352A	10.07.2002	WO0079684A1	28.12.2000
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		AU6035500A	09.01.2001
		SE516156C2	26.11.2001
		EP1205030A1	15.05.2002
		US6392575B1	21.05.2002
		KR20020013934A	21.02.2002
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		TW498621A	11.08.2002
		EP1205030B1	31.08.2005
		DE60022361E	06.10.2005
		CN1145263C	07.04.2004
		DE60022361T2	18.05.2006