

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
12 March 2009 (12.03.2009)

(10) International Publication Number
WO 2009/031076 A3

- (51) **International Patent Classification:**
H01L 21/266 (2006.01) *H01L 21/265* (2006.01)
H01L 21/336 (2006.01) *H01L 29/08* (2006.01)
- (21) **International Application Number:**
PCT/IB2008/053448
- (22) **International Filing Date:** 27 August 2008 (27.08.2008)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
07115716.8 5 September 2007 (05.09.2007) EP
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- (81) **Designated States (unless otherwise indicated, for every kind of national protection available):** AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) **Designated States (unless otherwise indicated, for every kind of regional protection available):** ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:

— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

Published:

— with international search report
— before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

(88) **Date of publication of the international search report:**
28 May 2009

(54) **Title:** A TRANSISTOR AND A METHOD OF MANUFACTURING THE SAME

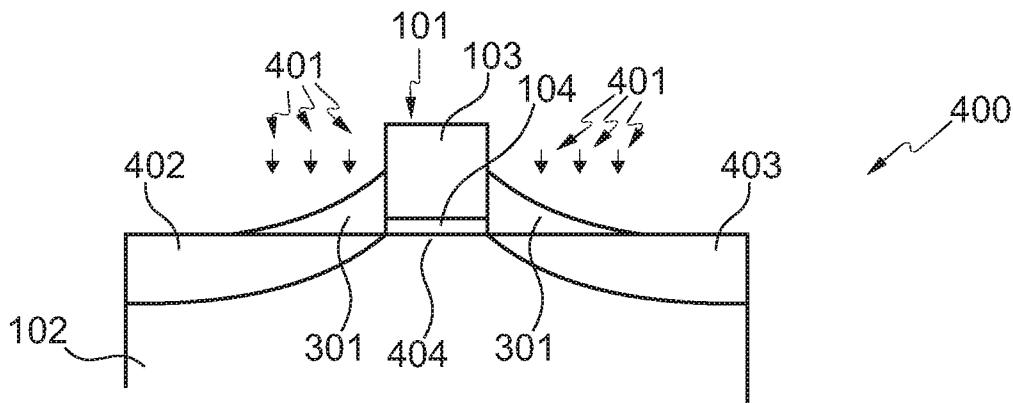


Fig. 4

(57) **Abstract:** A method of manufacturing a transistor (400), the method comprising forming a gate (101) on a substrate (102), forming a spacer (201) on lateral side walls of the gate (101) and on an adjacent portion (202) of the substrate (102), rearranging material of the spacer (201) so that the rearranged spacer (301) covers only a lower portion (303) of the lateral side walls of the gate (101) and an increased portion (302) of the substrate (102), and providing source/drain regions (402, 403) in a portion of the substrate (102) below the rearranged spacer (301).

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INTERNATIONAL SEARCH REPORT

International application No PCT/IB2008/053448

A. CLASSIFICATION OF SUBJECT MATTER
 INV. H01L21/266 H01L21/336 H01L21/265 H01L29/08

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

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X	US 2006/194398 A1 (OISHI AMANE [JP] ET AL) 31 August 2006 (2006-08-31) paragraphs [0058], [0060], [0061]; figures 7b-7e -----	8-10
X	US 5 811 342 A (WU SHYE-LIN [TW]) 22 September 1998 (1998-09-22) column 2, line 23 - line 53; figures 1-4 -----	8-10
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Further documents are listed in the continuation of Box C.

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Date of the actual completion of the international search

7 April 2009

Date of mailing of the international search report

16/04/2009

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INTERNATIONAL SEARCH REPORT

International application No

PCT/IB2008/053448

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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