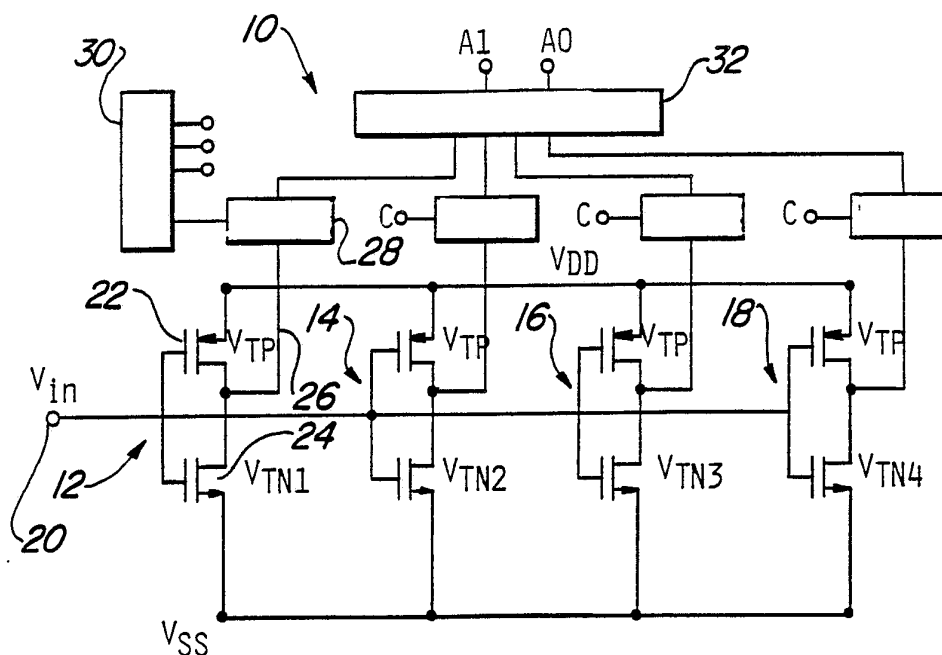


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(54) Title: ANALOG-TO-DIGITAL CONVERTER MADE WITH FOCUSED ION BEAM TECHNOLOGY



(57) Abstract

An analog-to-digital converter (10) employs a series of comparators (12, 14, 16 and 18). Each comparator includes at least one inverter consisting of a CMOS transistor pair including a P-channel transistor (22) and N-channel transistor (24). The threshold levels of the transistors (22, 24) are modified using focused ion beam implantation techniques to provide the comparators with monotonically increasing transition levels.

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ANALOG TO DIGITAL CONVERTER MADE
WITH FOCUSED ION BEAM TECHNOLOGY

BACKGROUND OF THE INVENTION

1. Technical Field

This invention relates to analog-to-digital converters and, more particularly, to techniques for making such converters using focused ion beam implantation techniques.

2. Discussion

Analog-to-digital (A/D) converters are widely used to convert an analog signal into a binary or digital signal. Many A/D converters are employed to interface high speed analog signals with ultra-fast digital signal processors. As the speed and level of integration of digital circuits increases, it becomes important to fabricate A/D converters and digital processing circuitry on the same semiconductor substrate. GaAs FET or silicon complementary metal oxide semiconductor (CMOS) technology is especially attractive for this approach because of its suitability for both analog and digital applications. However, in order to be able to accomplish this, it is necessary to implement the A/D converter in such a way that it requires little area on the substrate and minimizes power dissipation, yet performs the conversion process at high speed.

1 High speed A/D converters are often realized using
so-called "flash" type circuitry. As an example, a
two-bit flash A/D converter of the prior art is shown
in FIG. 1. This converter generally includes a
5 resistor string (R1-R4), four comparators and latches,
and a decoder. In operation, the analog input voltage
(V_{in}) is applied simultaneously to all comparators and
compared to corresponding fractions of the reference
voltage (V_{ref}). If the analog input voltage is greater
10 than the fractional portion of the reference voltage at
its input, the comparator output will be high;
otherwise it will be low. The latches are typically
implemented by flip flops, which amplify and store the
output states of the comparators. The latched
15 comparator output signals are then decoded to produce
the digital outputs A1 and A0 which may be processed
into binary coded decimal (BCD) format.

A CMOS comparator circuit, which can be used in
the FIG. 1 embodiment, is shown in FIG. 2. During the
20 half clock cycle when the clock voltage (ϕ) is high,
the fractional share of the reference voltage (V_i) is
applied to the capacitor C and, at the same time, the
inverter is auto zeroed, which eliminates its offset
voltage. During the second half of the clock cycle,
25 when ϕ is low, the analog input voltage (V_{in}) is
applied to capacitor C and the resulting difference
($V_i - V_{in}$) is amplified by the inverter and provided to
the input of the latch. The minimum clock period is
largely determined by the length of time required for
30 the comparator to achieve a change of state, or by the
time required by auto zeroing. This period determines
the maximum sampling rate of the converter.

Some of the disadvantages of the A/D converter
shown in FIGS. 1 and 2 are that the circuit speed is
35 significantly degraded by the necessity for auto
zeroing the comparator once per clock period. In

1 addition, the parasitic capacitance of capacitor C
further degrades the achievable speed. Also, the
resistor ladder requires excessive area and power
dissipation.

5 Another example of a CMOS A/D converter is
disclosed in the paper by Silburt et al., "A Novel
Multiple Threshold MOSFET Structure for A/D and D/A
Conversion", IEEE Journal of Solid State Circuits, Vol.
SC-19, No. 5, October 1984. In the disclosed
10 implementation a string of inverters is used to perform
the A/D conversion. Each inverter has a unique
threshold voltage. However, the threshold voltage is
adjusted by varying the bias voltage of each
transistors' substrate. This is a somewhat cumbersome
15 technique to implement and has other disadvantages.
For example, the optimum substrate bias voltage is
temperature dependent, and each transistor requires its
own temperature compensated bias supply. The technique
is not applicable to CMOS/SOS or GaAs technologies,
20 which are inherently faster than typical CMOS
processes.

SUMMARY OF THE INVENTION

Pursuant to the present invention, an
25 analog-to-digital converter is implemented through the
use of a plurality of comparators each with different
transition levels defined by FET transistors with
different threshold levels. The threshold levels are
set by using focused ion beam (FIB) implantation
30 techniques to implant impurities in the channel regions
of the field effect transistors used in the
comparators. By appropriately changing the
concentration of the impurity levels in the transistor
channel regions, each comparator will switch state at
35 different amplitudes of the applied analog input
signal.

1 Among the advantages of the present invention is
that the A/D converter can be implemented on a small
portion of the same semiconductor substrate as other
digital circuits without sacrificing speed.

5

BRIEF DESCRIPTION OF THE DRAWINGS

The various advantages of the present invention
will become apparent to those skilled in the art upon
reading the following specification and by reference to
10 the drawings in which:

FIG. 1 is a block diagram of a prior art A/D
converter;

FIG. 2 is a circuit diagram of a comparator
circuit which can be used in the prior art converter of
15 FIG. 1;

FIG. 3 is a schematic diagram of a CMOS A/D
converter made in accordance with the teachings of one
embodiment of the present invention;

FIG. 4 is a graph showing DC transfer curves that
20 may be obtained for the inverters of FIG. 3;

FIG. 5 is a graph illustrating output responses of
the inverters of FIG. 3 that may be obtainable under
certain conditions;

FIG. 6 is a schematic diagram of a second
25 embodiment of an A/D converter made in accordance with
the teachings of this invention; and

FIG. 7(A-M1) comprise simplified cross sectional
and/or top plan views of sequential processing steps
according to one embodiment of this invention for
30 making an integrated circuit including both a CMOS
analog device for an A/D converter and a CMOS digital
device on the same substrate.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

35 FIG. 3 illustrates a two-bit A/D converter 10 made
in accordance with one embodiment of this invention. A

1 comparison of FIG. 3 with the designs shown in FIGS. 1 and 2
illustrates that the inventive implementation eliminates the
need for the resistor string and switches or pass gates TG1
and TG2. The autozero switch TG3 of the other implementation
5 has also been eliminated. According to the present invention
the converter 10 includes a plurality of different
comparators 12, 14, 16 and 18. Each comparator is coupled to
receive the analog input voltage to be converted (V_{in}) on
line 20. Each comparator is designed so that it will switch
10 states when the amplitude of the analog input signal on line
20 exceeds its transition level. Monotonically increasing
transition levels are provided for each comparator of
converter 10 by appropriately modifying the threshold level
of the gate regions of at least one of the field effect
15 transistors (FET) in each comparator. The threshold levels
are set by using ion beam implantation techniques to implant
different impurity concentrations into the FET transistor
gate regions.

In the embodiment of FIG. 3, each comparator utilizes
20 at least one complimentary metal oxide semiconductor (CMOS)
inverter employing two transistors 22 and 24. As is known in
the art, each transistor includes its own drain, source, and
gate regions. The gate region overlies a channel in the
underlying semiconductor substrate. Transistor 22 is of a P-
25 channel construction whereas transistor 24 is of an N-channel
construction. As is known in the art, the threshold level of
a CMOS inverter is essentially defined by the threshold
levels of the P-channel and N-channel transistors, as well as
the dimensions of the channels themselves. Thus, each
30 transistor 22 of the comparators 12, 14, 16 and 18 can be of
identical design while only modifying the threshold levels of
transistors 24 in each of the

1 comparators. However, as will be discussed in more
detail later herein, the threshold levels for both
transistors are preferably modified using focused ion
beam implantation technology so that each of the
5 comparators 12, 14, 16 and 18 have monotonically
increasingly different threshold levels with relatively
small increments in order to provide for high A/D
resolution. For purposes of this invention, the term
"threshold level" means the voltage level that must be
10 applied between the gate and source terminals of an FET
transistor to allow current to flow between the source
and drain. Likewise, for purposes of this invention,
the term "transition voltage" means the input voltage
required by the comparator to switch from one stable
15 output state to another.

In the embodiment of FIG. 3, the analog input
voltage is simultaneously applied to the gates of the
CMOS pair of each comparator 12, 14, 16 and 18. If the
threshold level of the particular inverter is exceeded
20 by the analog input voltage, the N-channel transistor
24 will conduct thereby bringing the output line 26 to
 V_{SS} . This state will be amplified and stored in the
latch 28 associated with each comparator. The contents
of the latches 28 are then appropriately clocked via
25 clock generator 30 into a suitable decoder 32. Decoder
32 serves to decode the number of latches which have
been set into a binary output on lines A1, A0. It
should be understood that while FIG. 3 is shown in
connection with a two-bit A/D converter that the
30 present invention has much broader applicability, and
the resolution can be increased by including additional
comparator and latch circuits in parallel.

As shown in FIG. 4, it is expected that good DC
transfer characteristics can be obtained from this
35 construction, but that the response time can be limited
in some circumstances where the analog input voltage is

1 close to the comparator's transition level as
illustrated for stage 2 in FIG. 5.

FIG. 6 illustrates an alternative comparator
circuit that can accept a differential input signal.
5 This configuration employs a CMOS differential
amplifier. The two input devices 34 and 35 each have a
unique threshold voltage, and the difference between
the two determines the comparator transition point.
This differential configuration should minimize noise
10 problems and is especially advantageous for high speed
applications.

As is known in the art, it is desirable to have
all of the digital devices on an integrated circuit
chip to have the same threshold voltage. On the other
15 hand, the inverters in the A/D converter of the present
invention will have different threshold voltages. This
can be accomplished by the method which will now be
described.

FIG. 7 illustrates one possible sequence of
20 processing steps for making a CMOS integrated circuit
device 58 containing one analog CMOS device 60 for use
in the comparator and one digital CMOS device 62 on the
same semiconductor substrate. There are many other
ways of accomplishing this. The analog device 60 may
25 represent the transistors 22 and 24 of the CMOS
inverters referred to above. The digital device 62 can
be any of a wide variety of devices. For example, it
can be part of one of the latches 28.

In FIG. 7(A), mesas 64 and 66 are formed in a
30 silicon epitaxial layer or substrate that has
previously been formed on a sapphire base 68. The
processing of the P-channel transistors for the analog
60 and digital device 62 begins with simultaneously
implanting suitable impurities to form N-type islands
35 70 and 72 in the mesas 64 and 68, respectively, as
illustrated in FIG. 7(B). In this particular

1 embodiment, phosphorous ions are implanted at 60 kev at
a dose of 2×10^{12} , arsenic ions are implanted at 340 kev
at a dose of 3.3×10^{12} and arsenic ions are also
5 implanted in a third implant at 550 kev at a dose of
 7×10^{12} .

As shown in FIG. 7(C) N-channel device processing
similarly utilizes a deep channel implant of suitable
impurities to form P-type islands 74 and 76. To
accomplish this, boron ions at 70 kev at a dose of
10 7×10^{12} are utilized.

Turning to FIGS. 7(D) and 7(E), conventional
implantation techniques are utilized to set the
threshold level of both transistors in the digital
device 62. This implant step is applied at the same
15 time to all the digital devices on the integrated
circuit substrate. In this embodiment, the P-channel
device is implanted with a shallow implant of boron
ions at 20 kev at a dose of 5.2×10^{12} . The threshold
for the N-channel device is set by implanting boron
20 ions at 20 kev at a dose of 1.8×10^{12} . Once again, all
digital devices are implanted equally.

FIGS. 7(F) and 7(G) illustrate the formation of
focused ion beam alignment targets 80, 82 in a
deposited aluminum layer 78. These are used to
25 individually implant the comparator devices. In FIG.
7(G), two such alignment targets 80, 82 are shown on
either side of analog mesa 64. In practice, targets
80, 82 are generally cross shaped and there are
typically more than two alignment targets employed.
30 The targets should be made of conductive material and
be located close to the target. This is because the
focused ion beam apparatus requires the alignment
targets to be relatively close to the areas to be
implanted. Conventional photolithographic techniques
35 are employed typically to etch the aluminum layer 78 to
form the targets 80, 82.

1 The next steps as illustrated in FIG. 7(H) is to
 employ a series of focused ion beam implantations in
 the P-channel 70 and N-channel portion 74 of the
 comparator device mesa 64. These implants uniquely
 5 define the P- and N-channel threshold, and hence the
 comparator transition voltage. As will appear, the
 P-channel transistor 70 is of the buried channel type.
 In the preferred embodiment, both of the N-channel and
 P-channel implants utilize boron ions at 20 kev using
 10 the focused ion beam. The follow Table I sets forth
 the dosage for the PMOS and NMOS transistor for 16
 different comparators making up a four-bit A/D
 converter. The resultant threshold levels (Vt) are
 also listed in Table I.

15

TABLE I

Comparator	NMOS Vt	PMOS Vt	NMOS Dose	PMOS Dose

20 1	1.84	0.56	1.21E13	6.15E12
2	1.75	0.65	1.08E13	5.89E12
3	1.66	0.74	9.56E12	5.62E12
4	1.57	0.83	8.41E12	5.34E12
5	1.48	0.92	7.33E12	5.04E12
6	1.39	1.01	6.33E12	4.72E12
25 7	1.30	1.10	5.40E12	4.38E12
8	1.21	1.19	4.55E12	4.02E12
9	1.12	1.28	3.77E12	3.63E12
10	1.03	1.37	3.06E12	3.23E12
11	0.94	1.46	2.42E12	2.80E12
12	0.85	1.55	1.86E12	2.34E12
13	0.76	1.64	1.38E12	1.86E12
14	0.67	1.73	9.62E11	1.34E12
30 15	0.58	1.82	6.22E11	8.04E11
16	0.49	1.91	3.56E11	2.32E11

Briefly, the focused ion beam apparatus focuses a
 high energy beam of ionized impurity atoms onto a
 precise spot, with a precise diameter, on the
 35 integrated circuit substrate. By controlling the

1 location, energy, and duration of the beam, the ionized
impurity atoms can be arbitrarily added to the
integrated circuit. More information on focused ion
beam technology, and its application to integrate
5 circuits, can be obtained by reading Lee et al.,
"Threshold Adjustments for Complementary
Metal-Oxide-Semiconductor Optimization Using B and As
focused Ion Beams", Applied Physics Lett. 48(10), 10
March 1986, and Melngailis, J., "Focused Ion Beam
10 Technology and Applications", J. Vac. Technol. B5, p.
469-495, Mar/Apr 1987, which are both hereby
incorporated by reference.

Turning now to FIGS. 7(I) and 7(J), the aluminum
layer 78 is stripped and the wafer is annealed. Then,
15 the gate oxidation layer 84 is deposited. Thereafter,
polysilicon gates 86, 88, 90 and 92 are formed over the
transistors in the analog and digital devices.

The next general step is to form the source and
drain regions in the P-channel transistors 70, 72 for
20 the analog 60 and digital 62 devices, respectively.
This process is illustrated in FIG. 7(K1) and 7(K2).
FIG. 7(K2) is a top view of FIG. 7(K1) which has been
rotated 180 degrees in a counterclockwise direction.
Of particular note is the notch 96 formed in the source
25 98 of the P-channel transistor 70 in the analog device
60. Boron atoms are implanted through the masks shown
in FIG. 7(K2) at 15 kev at a dose of 2×10^{15} . The notch
96 in mask 100 prevents the underlying region from
being converted to P-type semiconductor material.

30 A similar source/drain implant for the N-channel
transistors are illustrated in FIGS. 7(L1) and 7(L2).
In this specific example, two arsenic ion implants of
150 kev with a dose of 2.5×10^{15} , and a second implant
at 80 kev at a dose of 2.5×10^{15} are utilized to define
35 the source and drain regions in N-channel analog
transistor 74 and source 111/drain 113 in N-channel

1 digital transistor 76. As illustrated in FIG. 7(L2) a
similar notch 106 is provided in the analog N-channel
transistor mask 108. This provision similarly provides
the advantages discussed above in connection with the
5 P-channel transistor.

As illustrated in FIGS. 7(M1) and 7(M2)
metalization is provided over an oxide layer 110 to
form contacts for the various regions on the
transistors. This can be accomplished using
10 conventional processing techniques. As illustrated in
FIG. 7(M2) the metalizing contact 110 for the source
region of analog P-channel transistor 70 bridges the
two P-type regions isolated by the N-type island 112
created by the mask notch 96. Similarly, metalization
15 114 for the N-channel transistor 74 bridges the similar
island formed therein. Rounding out FIG. 7(M2) contact
116 is provided on top of the gates for both
transistors to thereby short the gates together.
Contacts 118 and 120 are provided for the drain regions
20 of the two transistors. The remainder of the wafer can
be processed using conventional techniques.

In summary, the present invention provides a
number of advantages over conventional A/D converters.
Extremely high speed and small size can be obtained
25 while using technology that enables the devices to be
operated at very low power and implemented on the same
semiconductor substrate as other digital circuits. For
example, sample rates exceeding one gigahertz at a
power dissipation of 80 milliwatts can be expected.
30 The use of focused ion beam technology facilitates the
extremely small size of the transistors which can be in
the sub-half micrometer range. In addition, the
inventive design simplifies the A/D circuitry by
eliminating the need for conventional resistor ladders
35 and the like. Various other advantages will become
apparent to those skilled in the art upon a study of

- 1 the specification, drawings and following claims. For
example, this A/D converter can be implemented in GaAs
FET technology where a localized FIB implant uniquely
sets the threshold voltage of the FETs, and hence the
5 transition voltage of the inverters. In addition, the
present invention enables the manufacturer to use many
conventional processing steps while providing an
improved device.

CLAIMS

What is Claimed is:

- 1 1. An analog-to-digital (A/D) converter
comprising:
 a plurality of comparators having
monotonically increasing transition levels, each
5 comparator including at least one field effect
transistor having drain, source and gate regions; the
gate region overlying a channel in a semiconductor
substrate;
 input means for providing an analog input
10 signal simultaneously to each comparator;
 the transistors in each comparator each
having a different threshold level due to different
concentrations of impurities implanted in the channel
regions thereof by focused ion beam implantation
15 techniques thereby defining said transition levels for
each of the comparators; and
 decoder means coupled to outputs of each of
the comparators for generating a digital output signal
as a function of the comparator outputs.
- 1 2. The converter of Claim 1 wherein each
comparator includes at least one complementary metal
oxide (CMOS) inverter employing an N-channel and
P-channel transistor.
- 1 3. The converter of Claim 2 wherein the
threshold levels of the P-channel and N-channel
transistor in each inverter are different.

1 4. The converter of Claim 3 which further
 comprises:

 latch means coupled between an output of each
comparator and an input to the decoder means; and

5 clock generator means coupled to each of the
 latches.

1 5. The converter of Claim 2 wherein each
 comparator comprises:

 a pair of cross coupled inverters adapted to
receive differential analog input signals.

1 6. The converter of Claim 5 wherein outputs of
each inverter are coupled directly to said decoder
means.

- 1 7. An integrated circuit device comprising:
- a digital device having at least one
- transistor with a given threshold level;
- a plurality of analog device comparators
- 5 having monotonically increasing transition levels, each
- comparator including at least one field effect
- transistor having drain, source and gate regions; the
- gate regions overlying a channel in said semiconductor
- substrate;
- 10 said channels in each transistor having
- different concentrations of impurities therein
- implanted by focused ion beam implantation techniques
- thereby defining monotonically different transition
- levels for the comparators;
- 15 said digital and analog devices being formed
- on the same semiconductor substrate.

- 1 8. The device of Claim 7 which includes metallic
- alignment targets adjacent the transistors.

- 1 9. The device of Claim 7 wherein each comparator
- includes at least one inverter having a CMOS transistor
- pair having a P-channel and N-channel transistor, the
- impurity concentration in the gate regions of the
- 5 N-channel and P-channel transistors being different
- thereby providing each comparator with a different
- transition level.

1 10. The device of Claim 9 wherein said digital
device includes at least one CMOS transistor pair
having an N-channel and P-channel transistor, with the
impurity concentration in the channel regions of the
5 N-channel transistors of the digital device being
different than the N-channel transistors in the analog
device, and wherein the channel regions in the
P-channel transistors of the digital device have
different impurity concentration levels than the
10 P-channel transistors of the analog device.

1 11. The device of Claim 10 wherein said analog
and digital devices are formed in silicon mesas
supported by a sapphire base.

1 12. The device of Claim 11 wherein the source
region of at least one transistor in the analog device
has two regions of one type impurity separated by an
island of another type impurity which is connected to
5 and is of the same type as the gate region.

1 13. A method of making an analog-to-digital converter comprising:

 forming a plurality of analog comparators on a semiconductor substrate, each comparator having at
5 least one field effect transistor with drain, source and gate regions; the gate region overlying a channel in a semiconductor substrate;

 forming alignment targets on the substrate adjacent each of the transistors;

10 using the alignment targets to focus an ion beam onto the gate regions of each of the transistors and implanting different impurity concentration levels therein to thereby provide each transistor with a different threshold level; and

15 whereby the threshold levels of the transistors define monotonically increasing transition levels for each of the comparators.

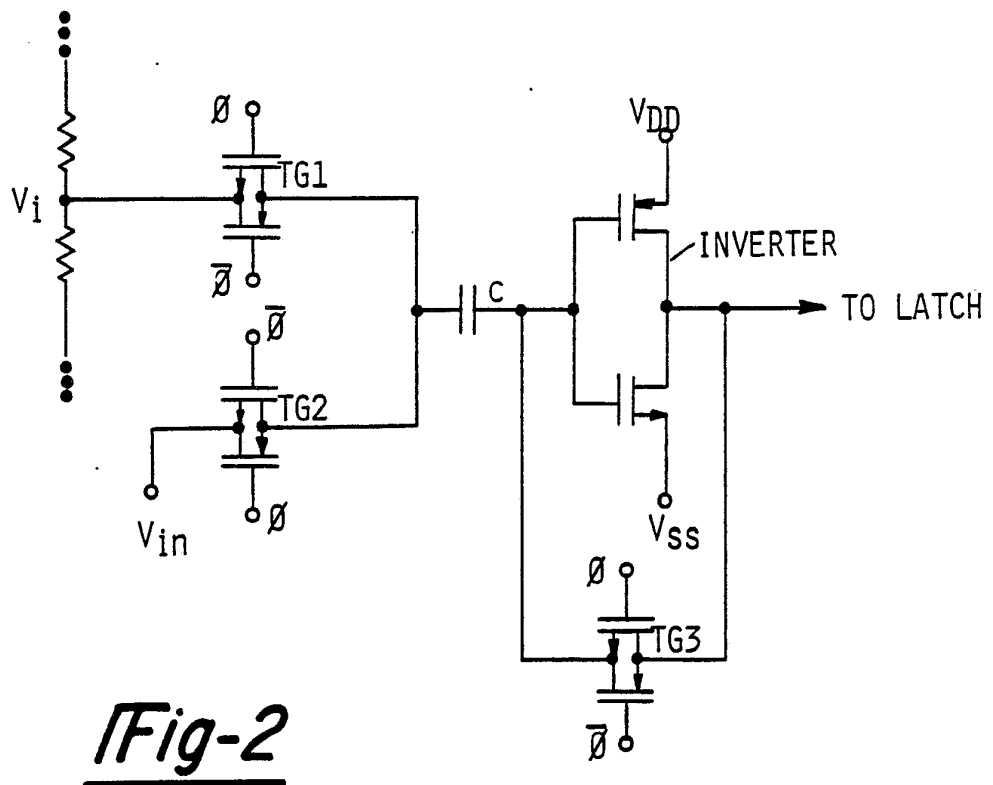
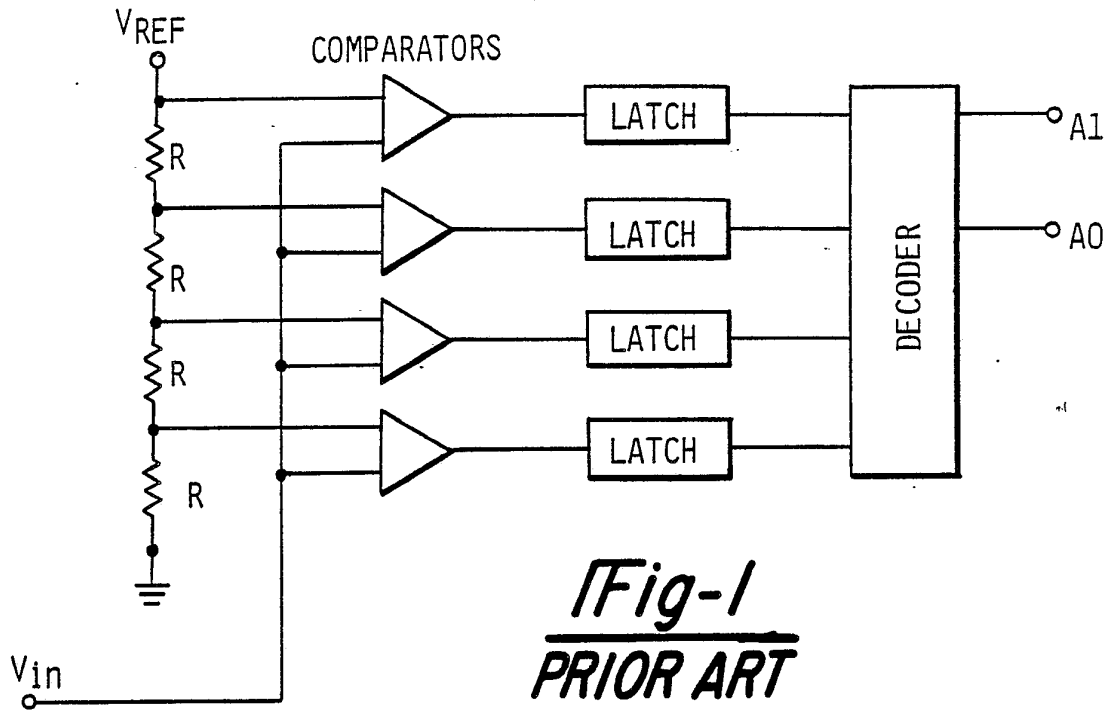
1 14. The method of Claim 13 wherein each comparator includes a complimentary metal oxide semiconductor transistor pair having an N-channel and P-channel transistor, and wherein the method further
5 comprises:

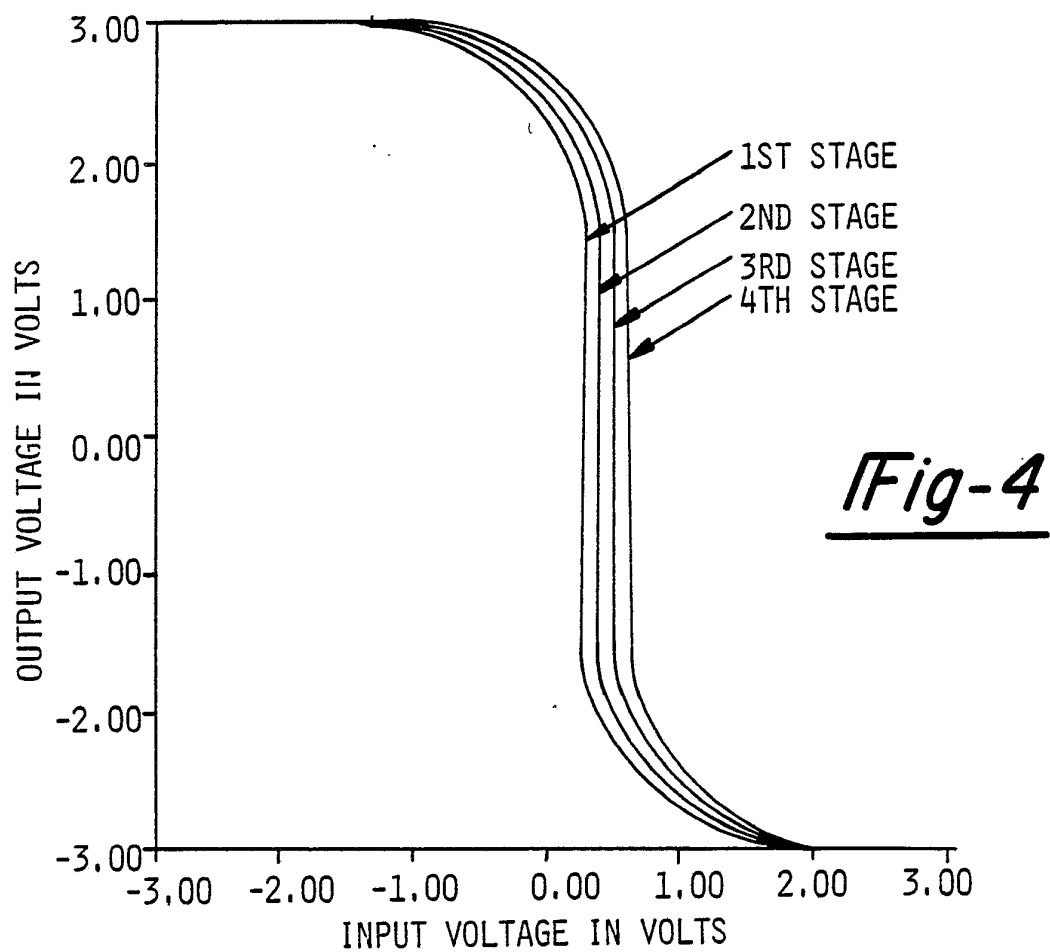
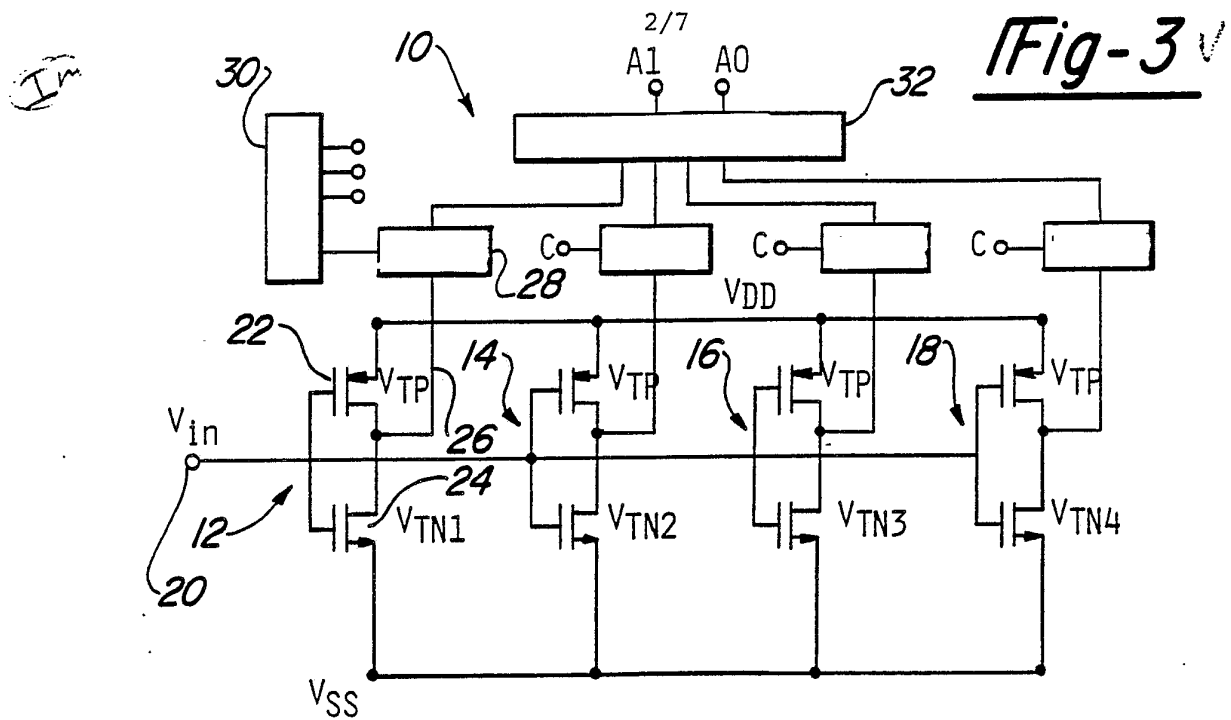
 using the focused ion beam to implant different impurity concentration levels in the channel regions of the P-channel and N-channel transistors of each pair.

1 15. The method of Claim 14 wherein the N-channel
transistor of each pair is provided with a decreasing
dose of impurities while the P-channel transistor of
each pair is provided with an increasing dose of
5 impurities such that the N-channel transistor in a
first comparator has the highest threshold level and
the P-channel transistor in the first converter has the
lowest threshold level, with the last comparator in the
converter including an N-channel transistor with the
10 lowest threshold level and a P-channel transistor with
the highest threshold level.

1 16. The method of Claim 15 wherein the P-channel
transistor of each pair is of the buried channel type,
and wherein both the P-channel and N-channel
transistors are implanted with the same impurity.

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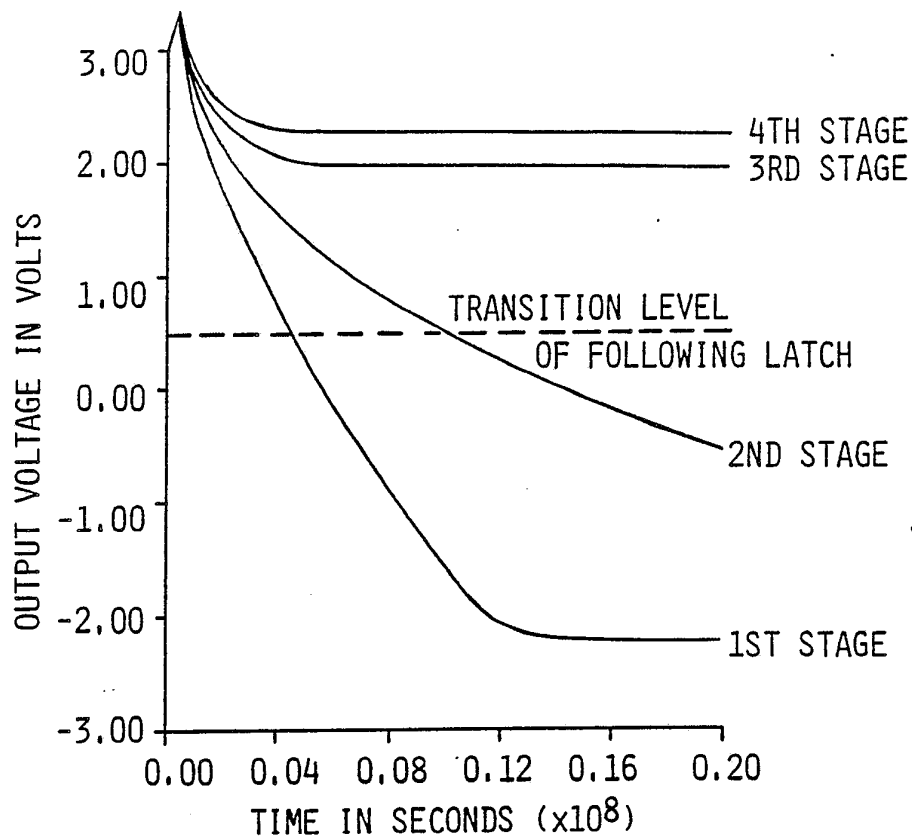


Fig-5

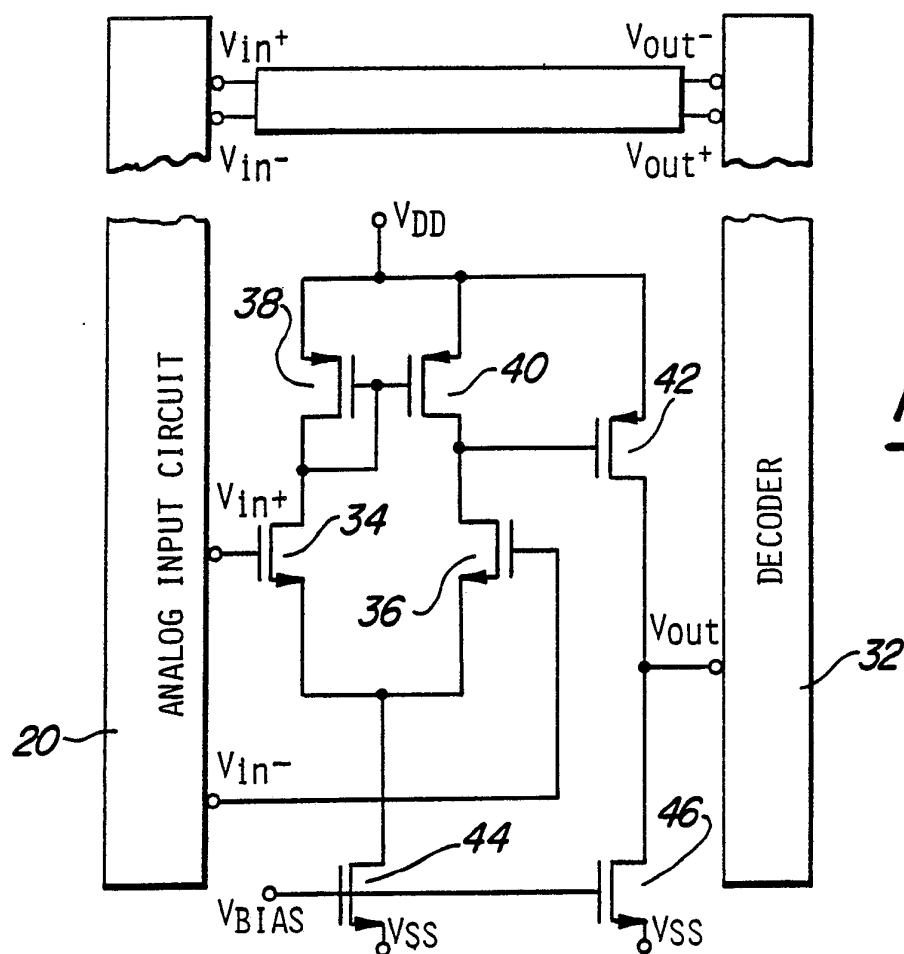


Fig-6

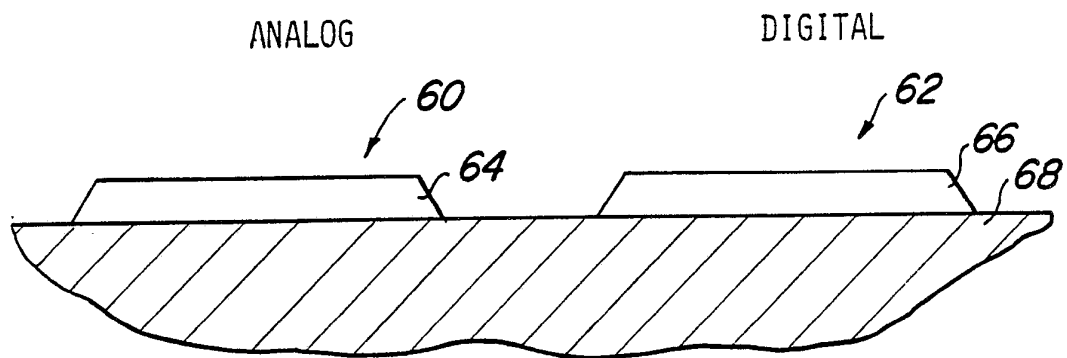


Fig-7A

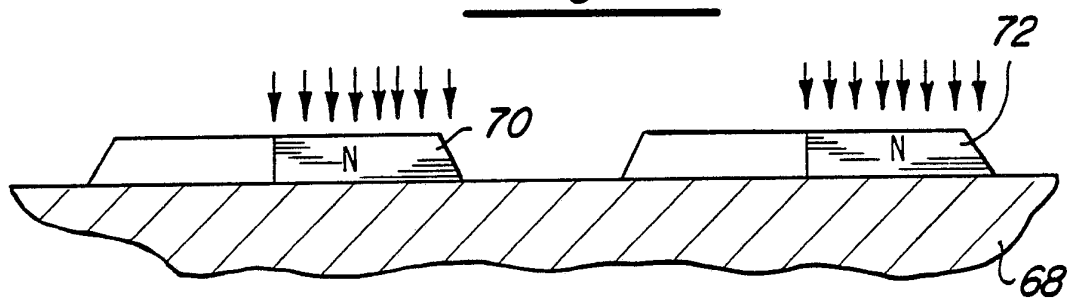


Fig-7B

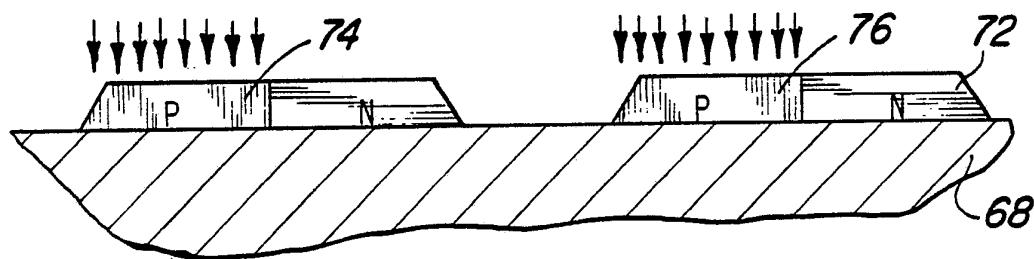


Fig-7C

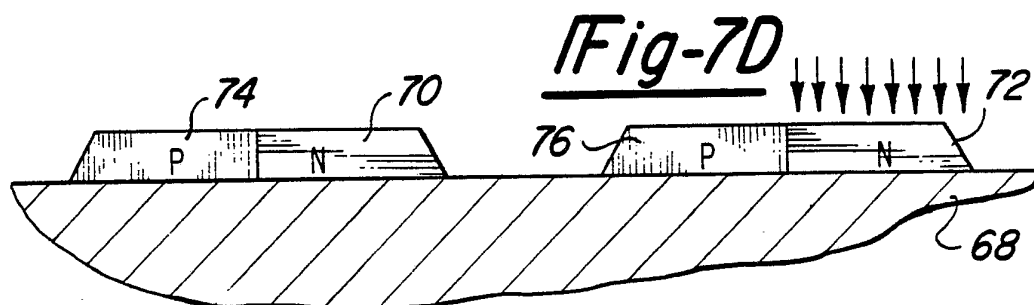


Fig-7D

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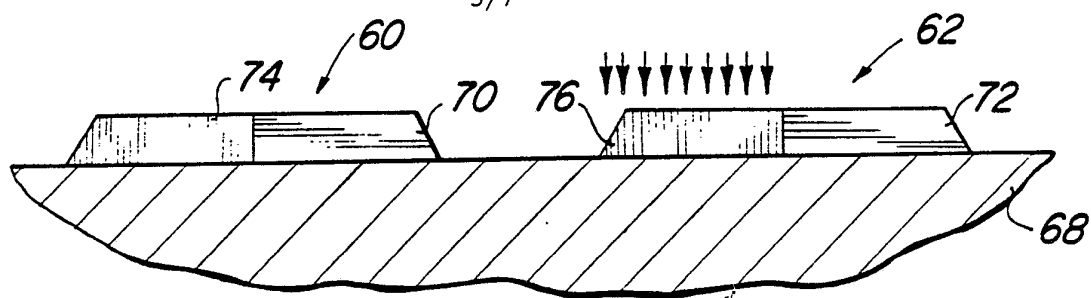


Fig-7E

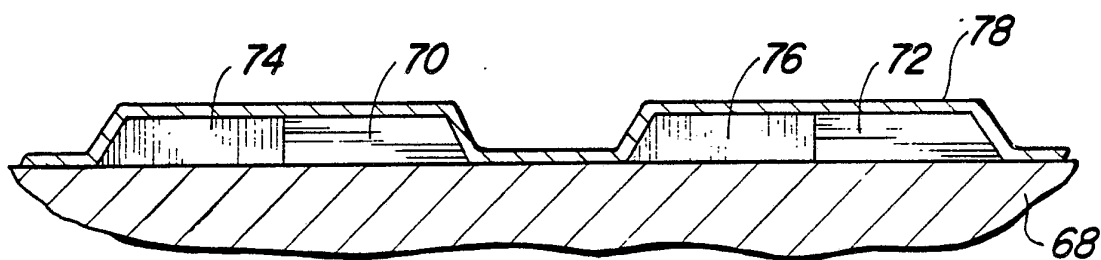


Fig-7F

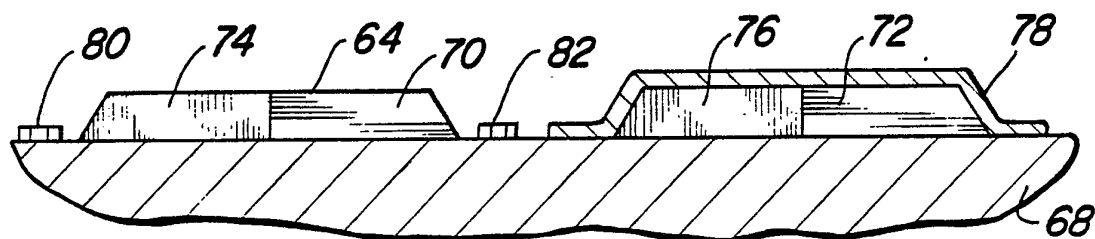


Fig-7G

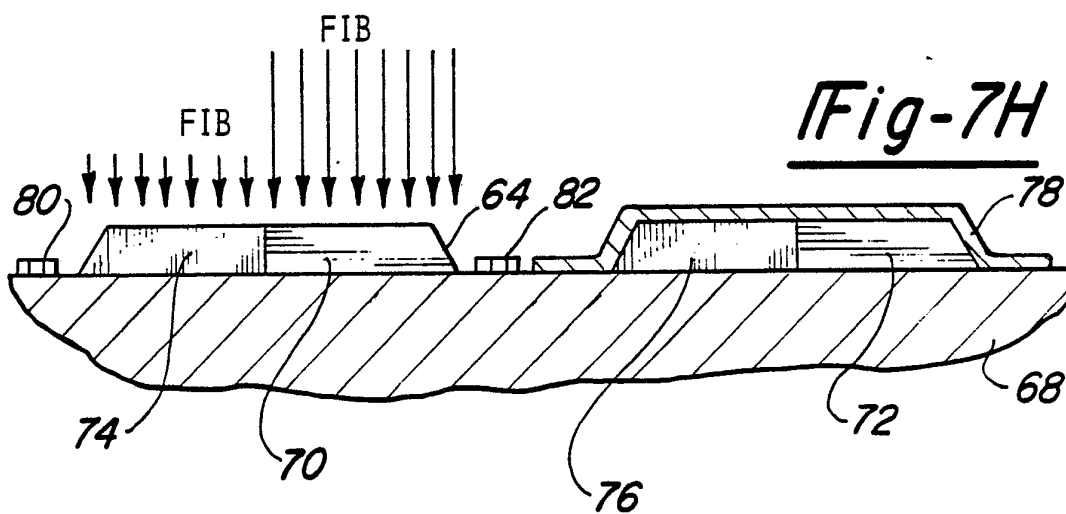


Fig-7H

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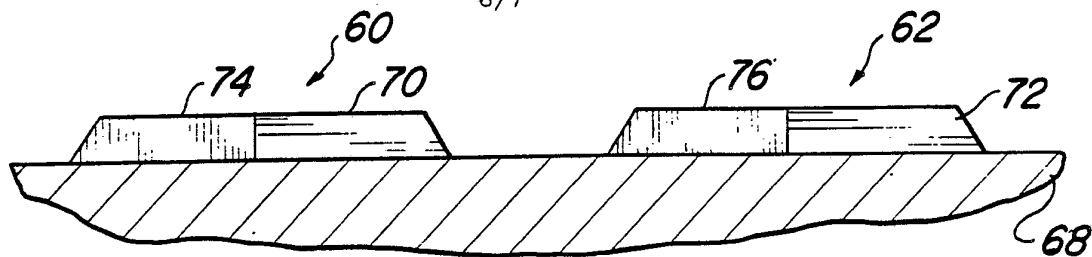


Fig-7I

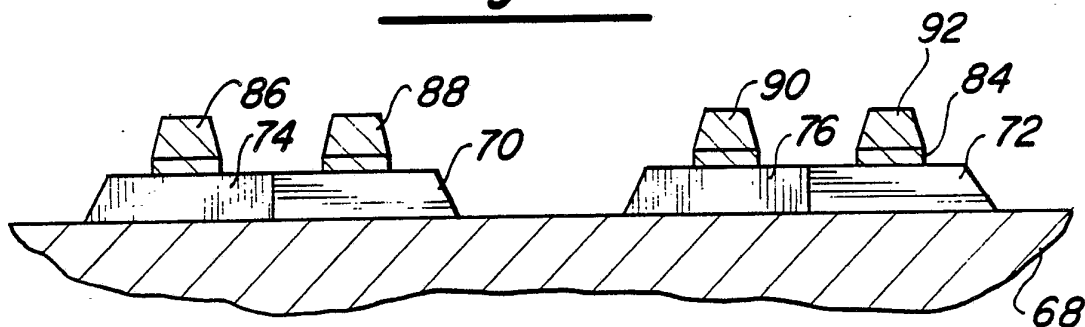


Fig-7J

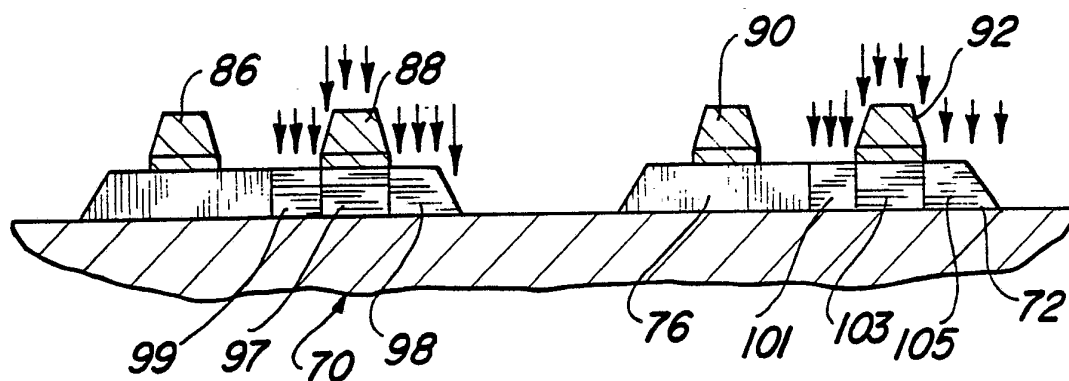


Fig-7K1

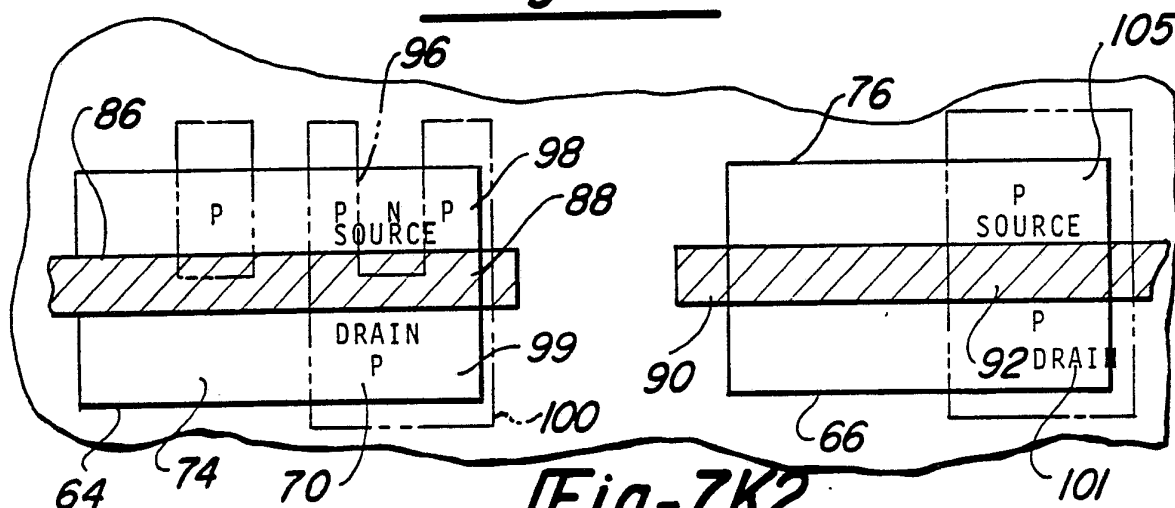


Fig-7K2

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Fig-7L1

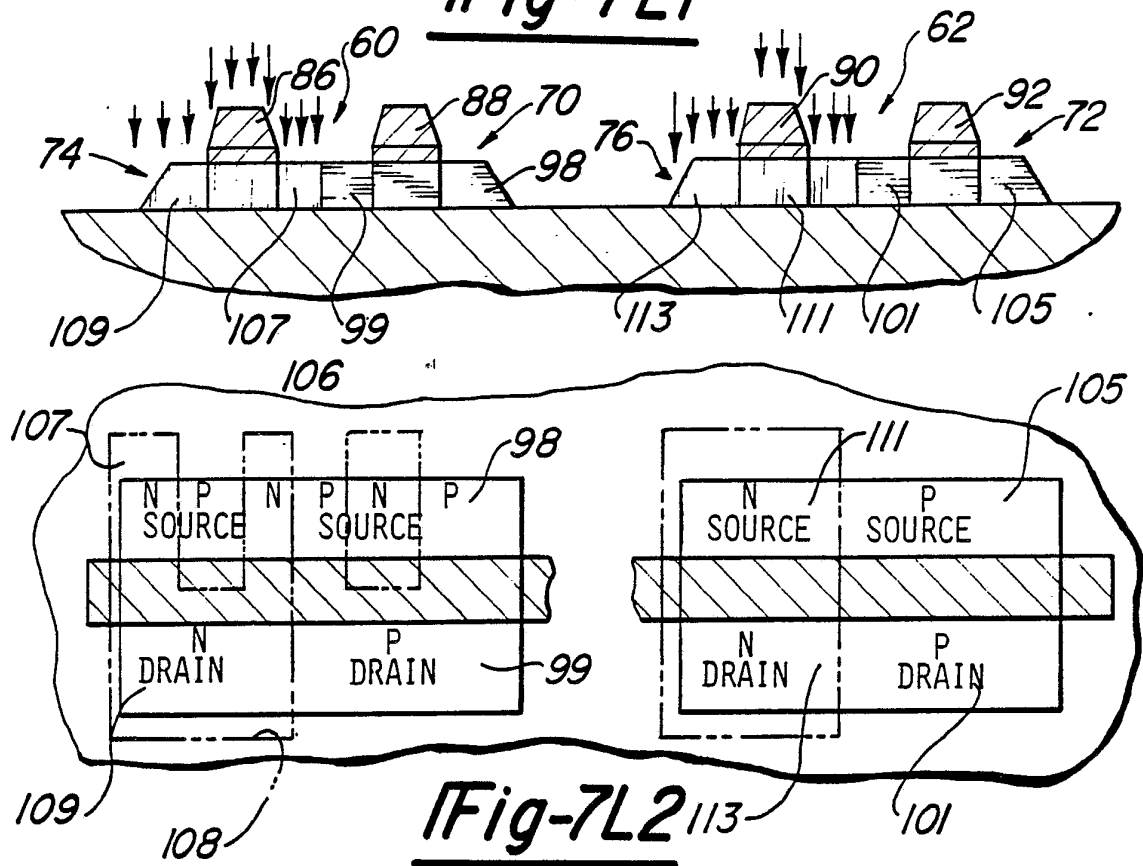


Fig-7L2

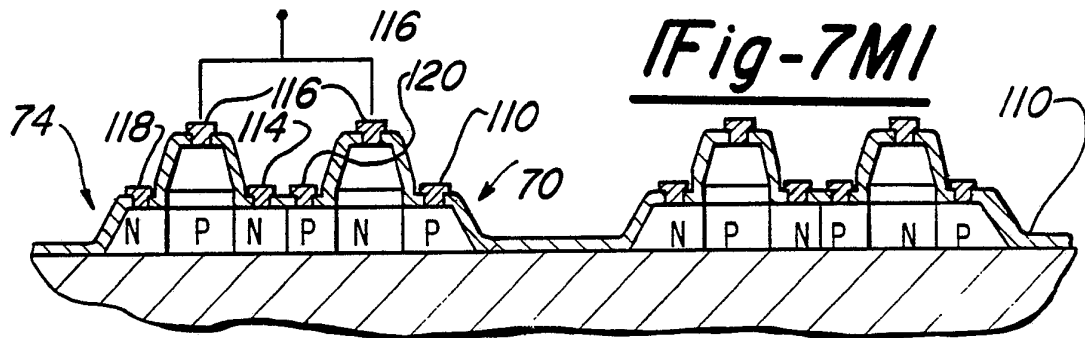


Fig-7M1

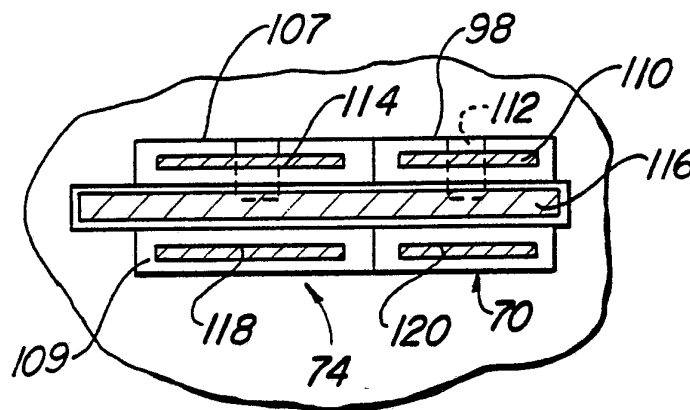


Fig-7M2