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Hook

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(54) **VIDEO LOAD BALANCING AND ERROR DETECTION BASED ON MEASURED CHANNEL BANDWIDTH**

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H04N 17/00	(2006.01)
G06F 13/40	(2006.01)
H04L 1/00	(2006.01)

(52) **U.S. Cl.**
CPC ***H04N 17/002*** (2013.01); ***G06F 13/4027*** (2013.01); ***H04J 3/16*** (2013.01); ***H04L 1/0061*** (2013.01)

(58) **Field of Classification Search**
CPC . H04J 3/16; H04J 1/02; H04N 17/002; H04N 19/23; H04N 19/46; H04N 19/149; H04N 19/103; G06F 13/4027; H04L 1/0061
USPC 370/437, 442, 493; 348/192, 723, 725
See application file for complete search history.

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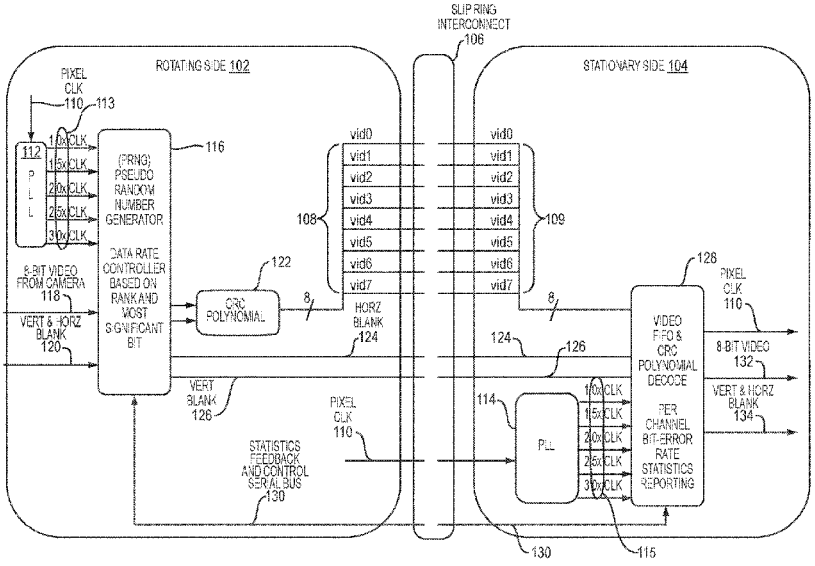
(57) **ABSTRACT**

An interconnect apparatus performs real time scoring and data throughput measurement of parallel data channels. The scoring and measurement information is communicated as feedback across the interconnect. Processing circuitry in the interconnect apparatus routes data to channels that have the best performance and reduces the data rate on channels that have lower performance based on the feedback information. This provides a method of dynamic load balancing to achieve optimal video data rates in a dynamic impedance environment. The interconnect apparatus also adjusts phase and data sampling times for improved fidelity of data transported across the interface.

13 Claims, 7 Drawing Sheets



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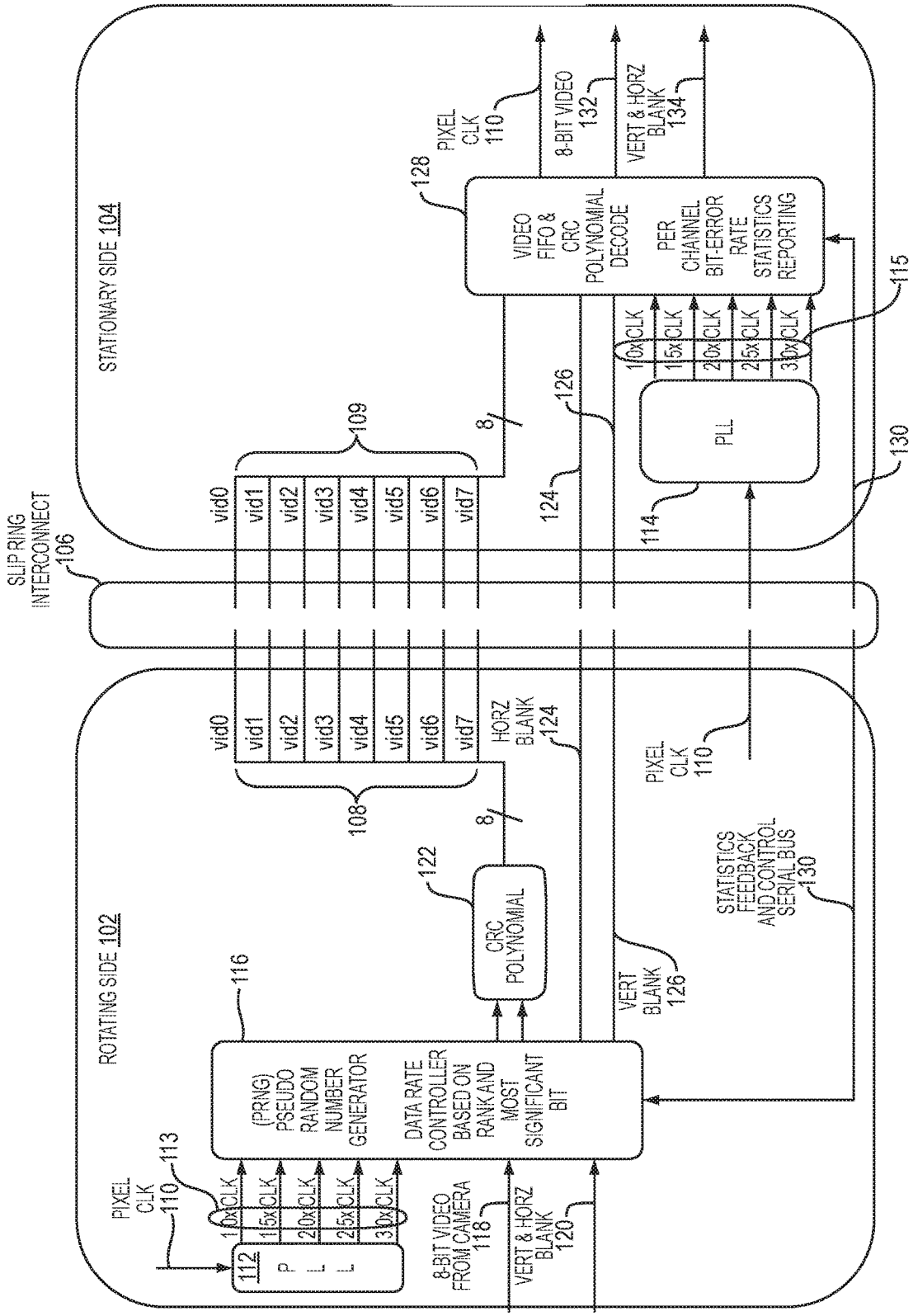
SLIP RING INTERCONNECT 106
STATIONARY SIDE 104
ROTATING SIDE 102
PIXEL CLK 110
113
112
PLL
10xCLK
15xCLK
20xCLK
25xCLK
30xCLK
(PRNG) PSEUDO RANDOM NUMBER GENERATOR
116
DATA RATE CONTROLLER BASED ON RANK AND MOST SIGNIFICANT BIT
8-BIT VIDEO FROM CAMERA 118
VERT & HORZ BLANK 120
CRC POLYNOMIAL
122
8
108
vid0
vid1
vid2
vid3
vid4
vid5
vid6
vid7
HORZ BLANK 124
VERT BLANK 126
PIXEL CLK 110
STATISTICS FEEDBACK AND CONTROL SERIAL BUS 130
109
VIDEO FIFO & CRC POLYNOMIAL DECODE
128
PER CHANNEL BIT-ERROR RATE STATISTICS REPORTING
PIXEL CLK 110
8-BIT VIDEO 132
VERT & HORZ BLANK 134
PLL
114
115

FIG. 1

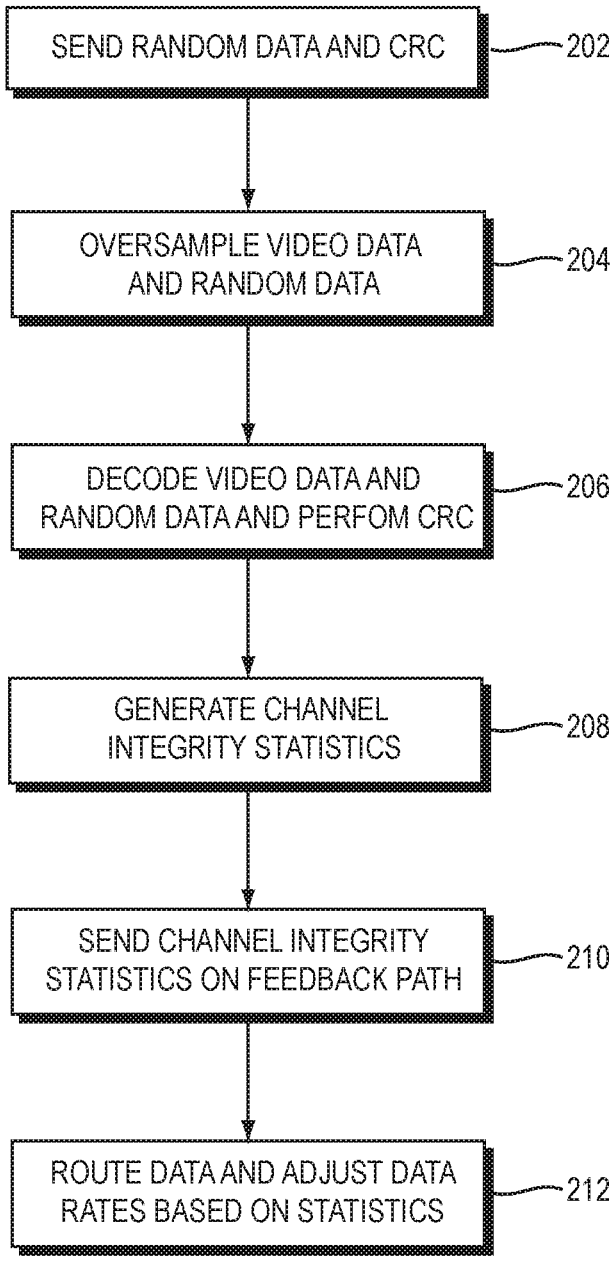
SEND RANDOM DATA AND CRC
202
OVERSAMPLE VIDEO DATA AND RANDOM DATA
204
DECODE VIDEO DATA AND RANDOM DATA AND PERFOM CRC
206
GENERATE CHANNEL INTEGRITY STATISTICS
208
SEND CHANNEL INTEGRITY STATISTICS ON FEEDBACK PATH
210
ROUTE DATA AND ADJUST DATA RATES BASED ON STATISTICS
212

FIG. 2

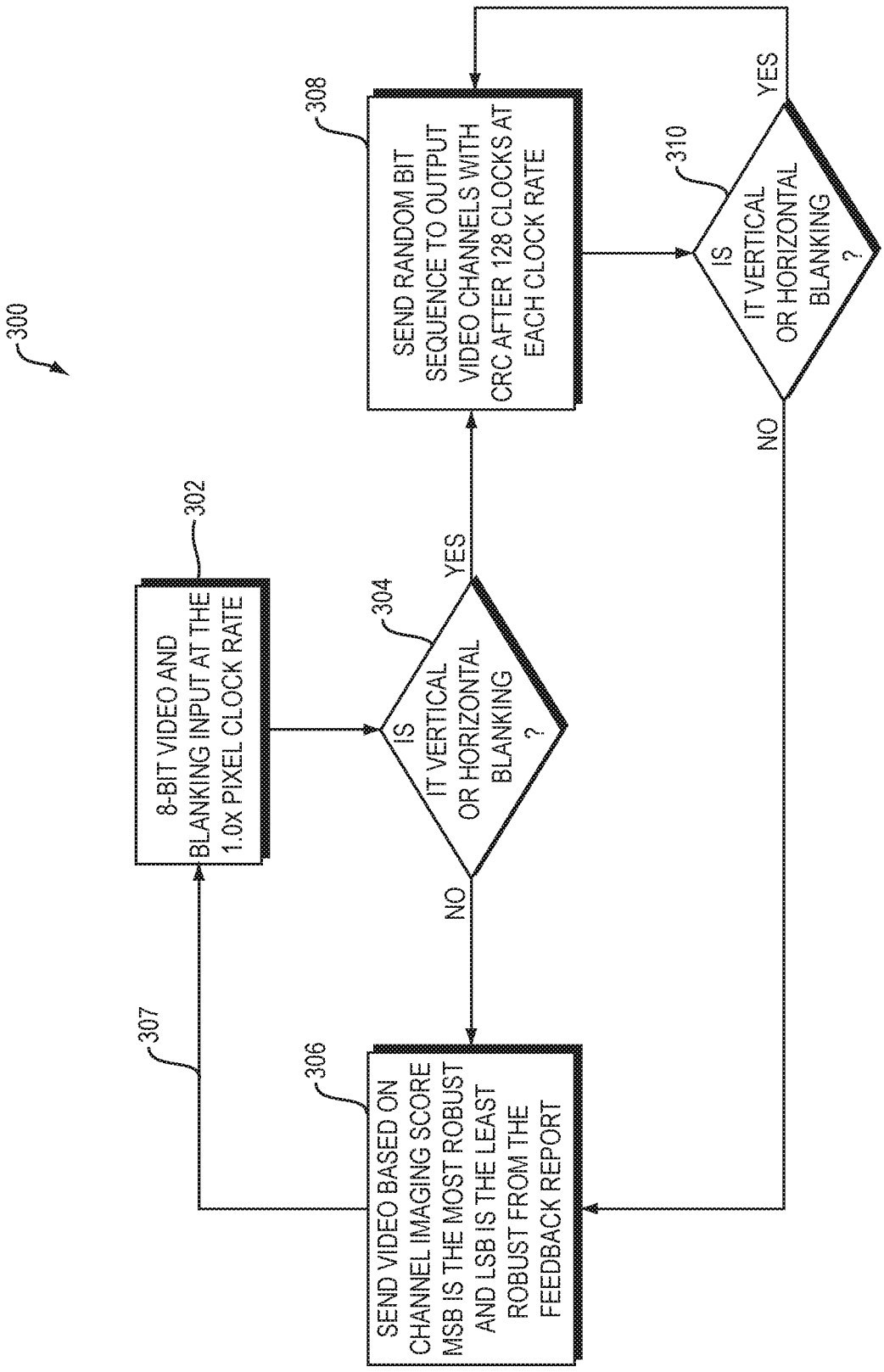
300
8-BIT VIDEO AND BLANKING INPUT AT THE 1.0x PIXEL CLOCK RATE
302
IS IT VERTICAL OR HORIZONTAL BLANKING ?
304
YES
NO
SEND RANDOM BIT SEQUENCE TO OUTPUT VIDEO CHANNELS WITH CRC AFTER 128 CLOCKS AT EACH CLOCK RATE
308
IS IT VERTICAL OR HORIZONTAL BLANKING ?
310
YES
NO
SEND VIDEO BASED ON CHANNEL IMAGING SCORE MSB IS THE MOST ROBUST AND LSB IS THE LEAST ROBUST FROM THE FEEDBACK REPORT
306
307

FIG. 3

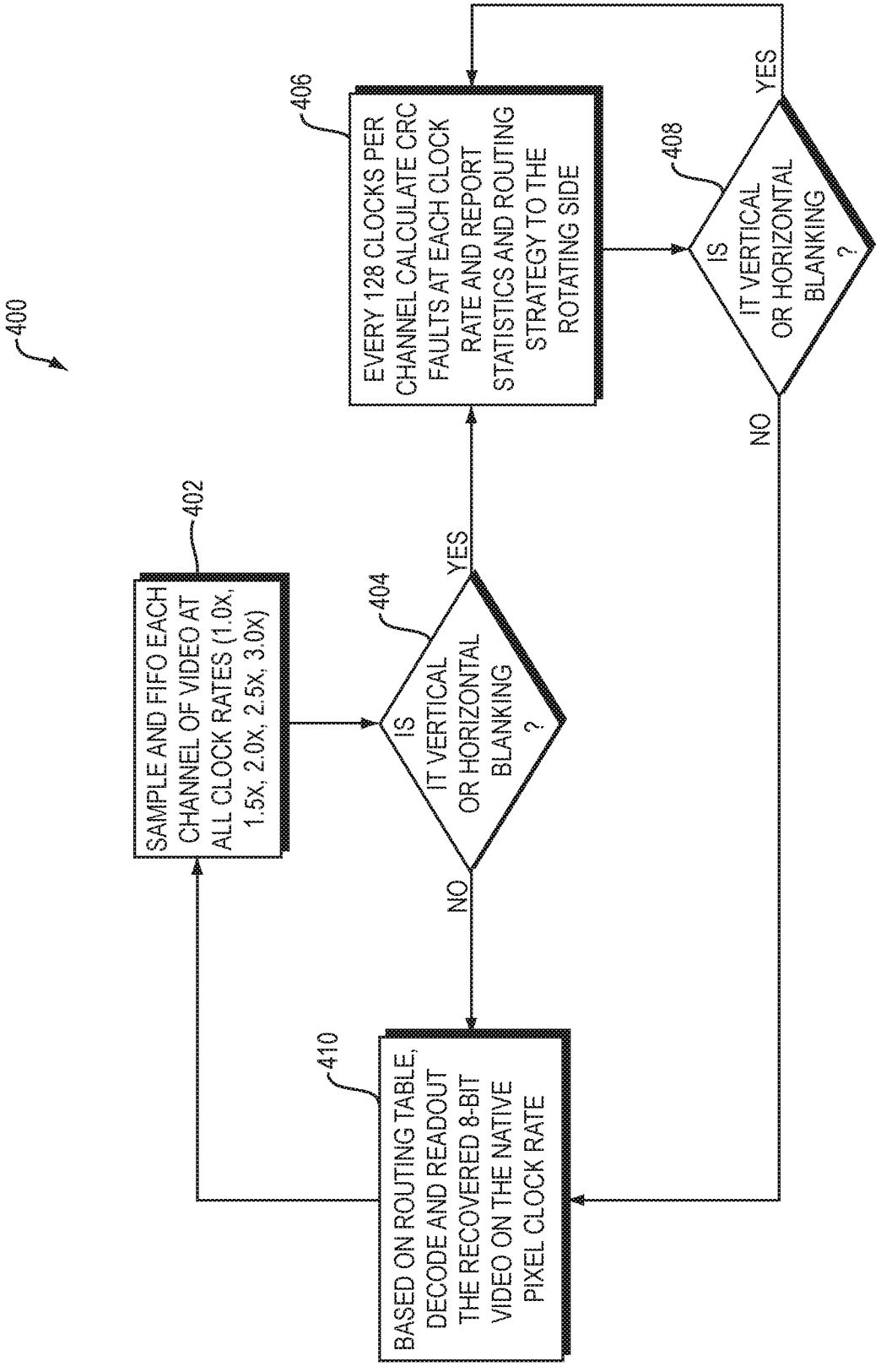
400
402
SAMPLE AND FIFO EACH CHANNEL OF VIDEO AT ALL CLOCK RATES (1.0x, 1.5x, 2.0x, 2.5x, 3.0x)
404
IS IT VERTICAL OR HORIZONTAL BLANKING ?
YES
NO
406
EVERY 128 CLOCKS PER CHANNEL CALCULATE CRC FAULTS AT EACH CLOCK RATE AND REPORT STATISTICS AND ROUTING STRATEGY TO THE ROTATING SIDE
408
IS IT VERTICAL OR HORIZONTAL BLANKING ?
YES
NO
410
BASED ON ROUTING TABLE, DECODE AND READOUT THE RECOVERED 8-BIT VIDEO ON THE NATIVE PIXEL CLOCK RATE

FIG. 4

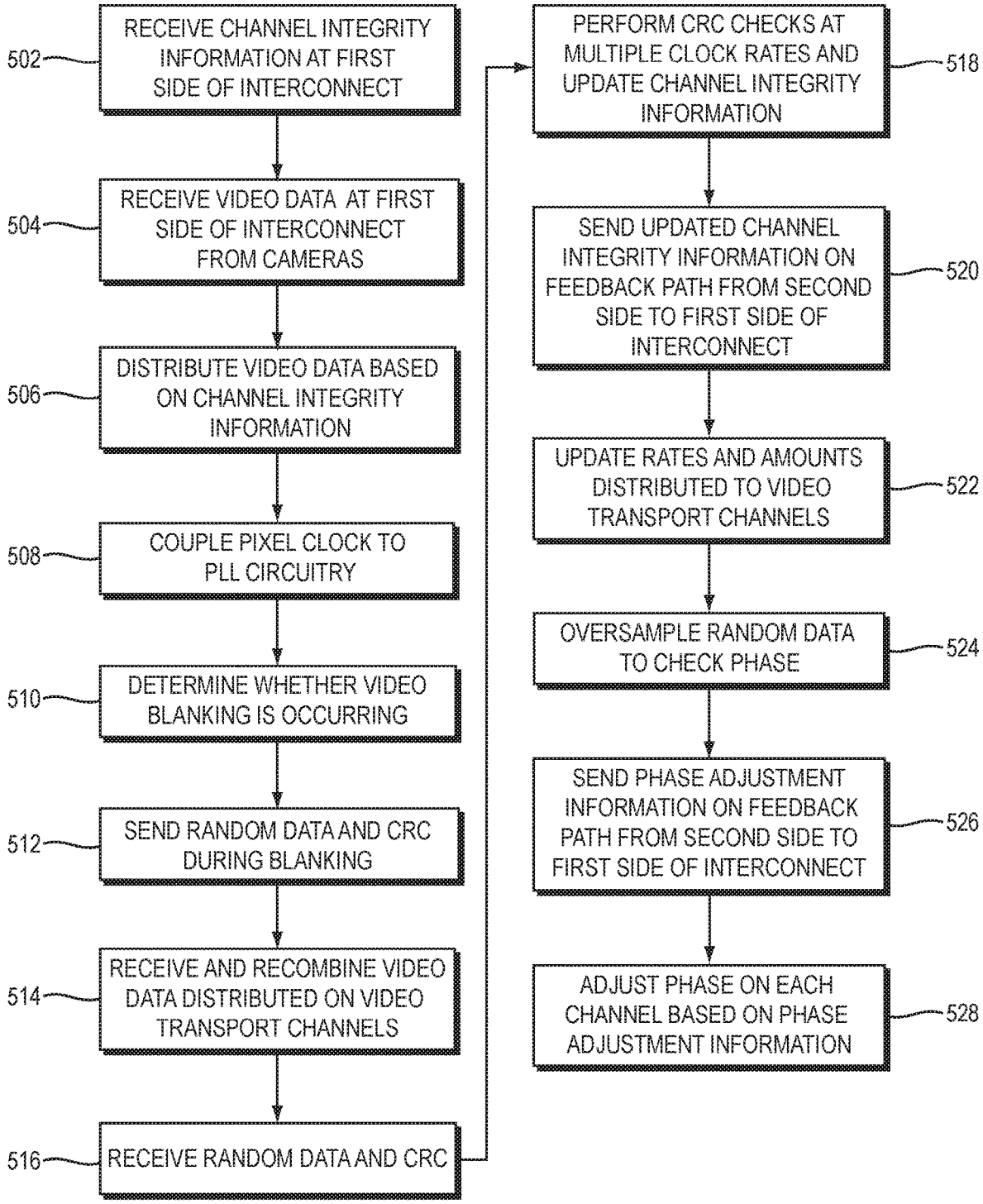
502
RECEIVE CHANNEL INTEGRITY INFORMATION AT FIRST SIDE OF INTERCONNECT
504
RECEIVE VIDEO DATA AT FIRST SIDE OF INTERCONNECT FROM CAMERAS
506
DISTRIBUTE VIDEO DATA BASED ON CHANNEL INTEGRITY INFORMATION
508
COUPLE PIXEL CLOCK TO PLL CIRCUITRY
510
DETERMINE WHETHER VIDEO BLANKING IS OCCURRING
512
SEND RANDOM DATA AND CRC DURING BLANKING
514
RECEIVE AND RECOMBINE VIDEO DATA DISTRIBUTED ON VIDEO TRANSPORT CHANNELS
516
RECEIVE RANDOM DATA AND CRC
518
PERFORM CRC CHECKS AT MULTIPLE CLOCK RATES AND UPDATE CHANNEL INTEGRITY INFORMATION
520
SEND UPDATED CHANNEL INTEGRITY INFORMATION ON FEEDBACK PATH FROM SECOND SIDE TO FIRST SIDE OF INTERCONNECT
522
UPDATE RATES AND AMOUNTS DISTRIBUTED TO VIDEO TRANSPORT CHANNELS
524
OVERSAMPLE RANDOM DATA TO CHECK PHASE
526
SEND PHASE ADJUSTMENT INFORMATION ON FEEDBACK PATH FROM SECOND SIDE TO FIRST SIDE OF INTERCONNECT
528
ADJUST PHASE ON EACH CHANNEL BASED ON PHASE ADJUSTMENT INFORMATION

FIG. 5

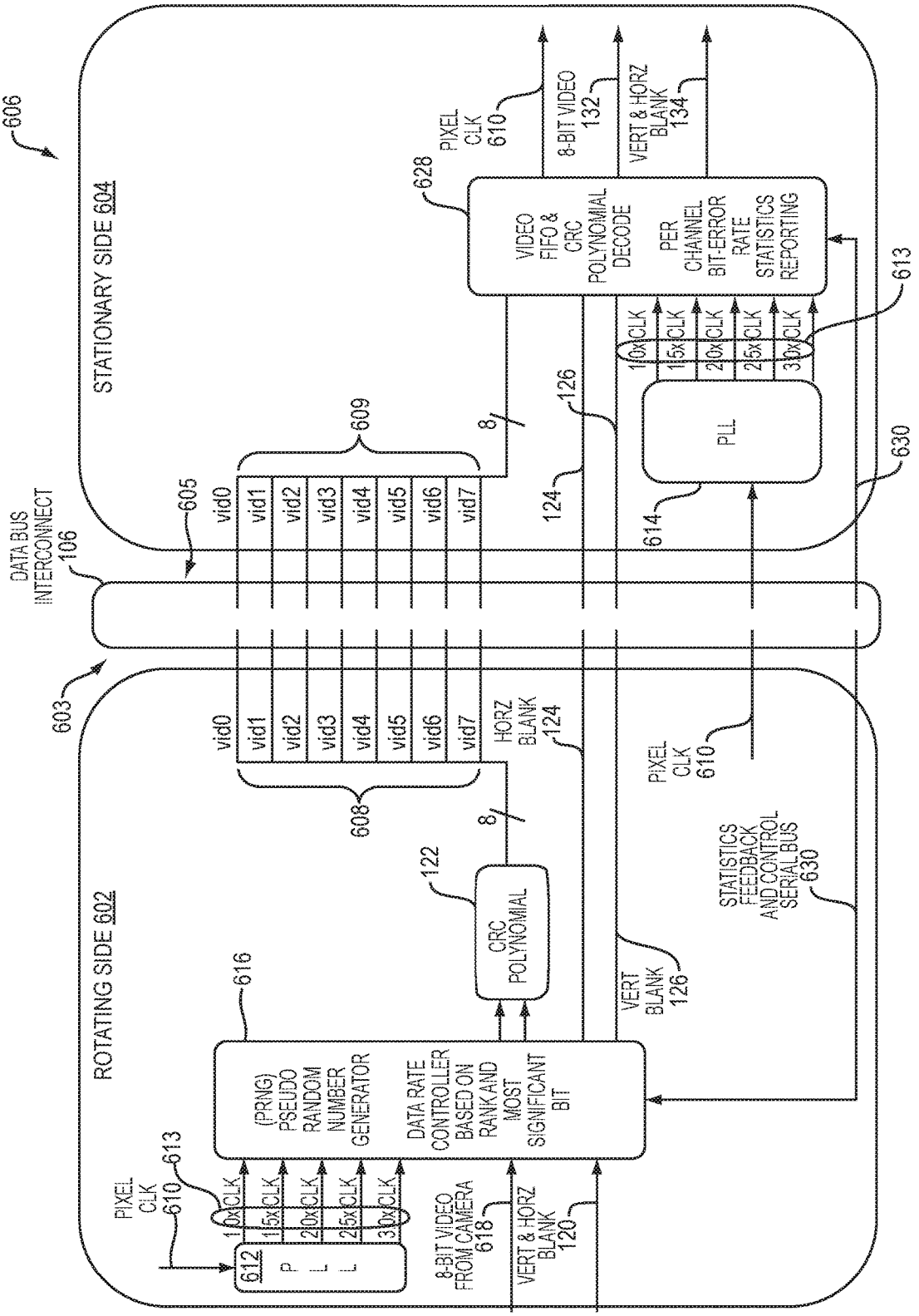
606
STATIONARY SIDE 604
ROTATING SIDE 602
603
605
DATA BUS INTERCONNECT 106
PIXEL CLK 610
8-BIT VIDEO 132
VERT & HORZ BLANK 134
628
VIDEO FIFO & CRC POLYNOMIAL DECODE
PER CHANNEL BIT-ERROR RATE STATISTICS REPORTING
613
10x CLK
15x CLK
20x CLK
25x CLK
30x CLK
PLL
614
630
126
124
8
609
vid0
vid1
vid2
vid3
vid4
vid5
vid6
vid7
608
HORZ BLANK 124
PIXEL CLK 610
STATISTICS FEEDBACK AND CONTROL SERIAL BUS 630
VERT BLANK 126
122
CRC POLYNOMIAL
616
(PRNG) PSEUDO RANDOM NUMBER GENERATOR
DATA RATE CONTROLLER BASED ON RANK AND MOST SIGNIFICANT BIT
PIXEL CLK 610
613
612
PLL
8-BIT VIDEO FROM CAMERA 618
VERT & HORZ BLANK 120

FIG. 6

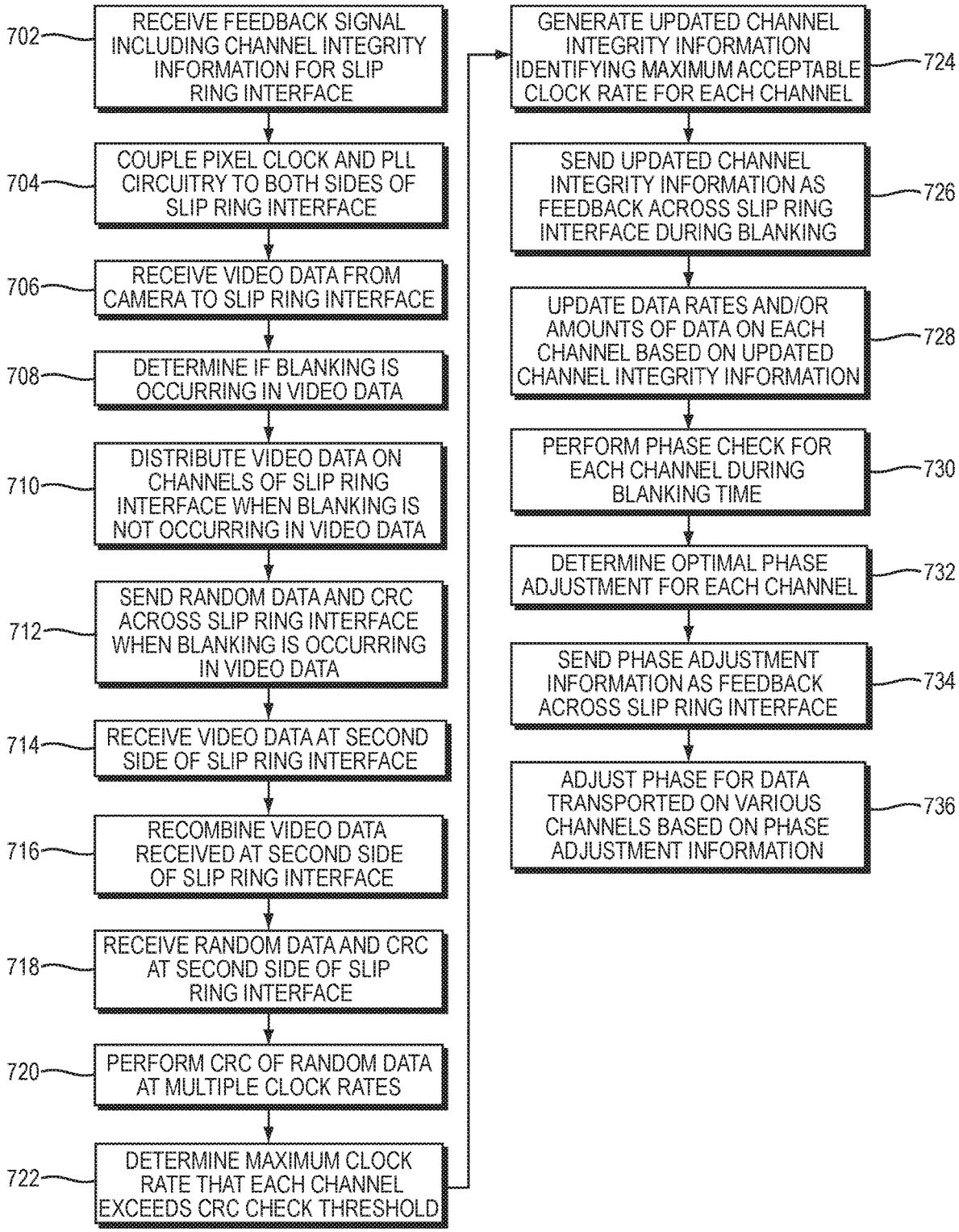
702
RECEIVE FEEDBACK SIGNAL INCLUDING CHANNEL INTEGRITY INFORMATION FOR SLIP RING INTERFACE
704
COUPLE PIXEL CLOCK AND PLL CIRCUITRY TO BOTH SIDES OF SLIP RING INTERFACE
706
RECEIVE VIDEO DATA FROM CAMERA TO SLIP RING INTERFACE
708
DETERMINE IF BLANKING IS OCCURRING IN VIDEO DATA
710
DISTRIBUTE VIDEO DATA ON CHANNELS OF SLIP RING INTERFACE WHEN BLANKING IS NOT OCCURRING IN VIDEO DATA
712
SEND RANDOM DATA AND CRC ACROSS SLIP RING INTERFACE WHEN BLANKING IS OCCURRING IN VIDEO DATA
714
RECEIVE VIDEO DATA AT SECOND SIDE OF SLIP RING INTERFACE
716
RECOMBINE VIDEO DATA RECEIVED AT SECOND SIDE OF SLIP RING INTERFACE
718
RECEIVE RANDOM DATA AND CRC AT SECOND SIDE OF SLIP RING INTERFACE
720
PERFORM CRC OF RANDOM DATA AT MULTIPLE CLOCK RATES
722
DETERMINE MAXIMUM CLOCK RATE THAT EACH CHANNEL EXCEEDS CRC CHECK THRESHOLD
724
GENERATE UPDATED CHANNEL INTEGRITY INFORMATION IDENTIFYING MAXIMUM ACCEPTABLE CLOCK RATE FOR EACH CHANNEL
726
SEND UPDATED CHANNEL INTEGRITY INFORMATION AS FEEDBACK ACROSS SLIP RING INTERFACE DURING BLANKING
728
UPDATE DATA RATES AND/OR AMOUNTS OF DATA ON EACH CHANNEL BASED ON UPDATED CHANNEL INTEGRITY INFORMATION
730
PERFORM PHASE CHECK FOR EACH CHANNEL DURING BLANKING TIME
732
DETERMINE OPTIMAL PHASE ADJUSTMENT FOR EACH CHANNEL
734
SEND PHASE ADJUSTMENT INFORMATION AS FEEDBACK ACROSS SLIP RING INTERFACE
736
ADJUST PHASE FOR DATA TRANSPORTED ON VARIOUS CHANNELS BASED ON PHASE ADJUSTMENT INFORMATION

FIG. 7

VIDEO LOAD BALANCING AND ERROR DETECTION BASED ON MEASURED CHANNEL BANDWIDTH

FIELD OF TECHNOLOGY

The present disclosure is in the field of digital image processing and more particularly in the field of improving channel integrity for transporting high definition and ultra-high definition imagery.

BACKGROUND

Digital imaging systems that include mechanically oriented cameras and sensors commonly include signal paths that extend along rotatable mechanical booms or mounting structures. Signal paths that extend across rotatable structures typically include a slip ring interface which include a rotating side and a stationary side. For each channel in a slip ring interface, a contact on the stationary side wipes on a conductive track on the rotating side or vice versa to provide electrical contact there between.

It is often desirable to replace older cameras and/or sensors of a digital imaging system with newer generations of cameras and sensors without replacing the mounting and orienting hardware of the system. The newer cameras and sensors generally provide more advanced features and higher resolution imagery and output much more data at much higher data rates than older cameras and sensors.

Mechanical contacts such as those used in a slip ring interface can degrade and become unreliable due to wear, mechanical interference, vibration, or thermal effects that can vary channel impedances across the slip ring interface. Some degradation and the resulting variations in channel impedance may be tolerable in older video systems where a relatively small amount of data is transported across a channel. However, in more modern high definition and ultra-high definition imaging systems, the much larger amount of data being transported across a slip ring interface may be corrupted by high or varying channel impedances.

High impedance spots on a channel of a slip ring interconnect can result in a dropped line of video or even a whole dropped frame, for example. Image noise such as dropped lines or frames may cause errors or inaccuracies in many downstream processes such as tracking algorithms which are configured to process continuous imagery.

Prior attempt to improve data integrity across slip interconnects have included performing cyclic redundancy checks (CRC) at the conclusion of each video line to determine if the video line includes bit errors. When bit errors are detected the previous video line is substituted in place of the line of video with the errors. Such passive techniques are generally inadequate to provide data integrity of high speed video data transported across a slip ring interconnect. The previously known passive techniques for improving data integrity across slip ring interconnects do not adequately support transporting high speed video data over degraded slip rings, slip rings that are bandwidth limited from data line to data line, or slip ring interconnects that are temporally changing while under extreme rotations or temperatures, for example.

Other attempts to mitigate data integrity problems at a slip ring interface include replacing the slip ring with another type of interconnect, such as a cable wrap. However, the other type of interconnects generally do not have the dynamic functionality of a true slip ring. For example, a cable wrap interconnect can only be rotated through some limited angular range, whereas a slip ring interconnect can be rotated through an unlimited angular range.

Another technique for transporting high speed video data over a degraded interconnect is to compress the video data so that it can be transported over fewer channels and/or at a lower data rate. However, it is often desirable to transport uncompressed video data because compressed data generally includes undesirable artifacts and many tracker algorithms are optimized to operate with uncompressed data. Moreover, when a frame of compressed video data is corrupted, more data is lost than would be if the frame had included uncompressed video data.

SUMMARY

The disclosed method and apparatus monitors the integrity of data received at a downstream side of a video data interconnect from an upstream side of the video data interconnect for each channel of the video data interconnect.

Statistical information characterizing channel integrity for each channel of the video data interconnect is accumulated by processing circuitry on the downstream side of the video data interconnect and fed back across the video data interconnect to processing circuitry on the upstream side of the video data interconnect.

According to an aspect of the present disclosure, the video data to be transported across the interconnect is distributed over the plurality of channels by the processing circuitry on the upstream side of the video data interconnect. According to another aspect of the present disclosure the data rate on each channel is adjusted by the processing circuitry on the upstream side of the video data interconnect based on the statistical information.

During horizontal blanking (time between consecutive lines of video) and vertical blanking (time between consecutive frames of video), data on each of the channels is tested by sending pseudo-random data across the interconnect at a plurality of data rates and determining bit error rates for each channel at each of the data rates.

According to an aspect of the present disclosure, near real-time video transport health scoring and max data throughput measurements are performed on each of the multiple parallel video channels in the video data interconnect. The channel scoring is used to perform automatic dynamic load balancing across multiple video transport streams to achieve optimal video data rates across a video data interconnect in a dynamic impedance environment. Data is automatically routed to the channels that have the best metrics while slowing down and reducing the load on channels that are poorer performers to avoid poor performing channels and take advantage of higher performing channels without performing compression of the video data.

Aspects of the present disclosure also allow for a dynamic clock to facilitate data centering/alignment so as to extract the optimal performance by this unique interconnect type. In addition the data phase is adjusted relative to the shared pixel clock. Digital pulses of the video data can be oversampled at a high clock rate of the dynamic clock to determine which pulse of the sampling clock is best aligned with a center of the data pulse. In other words, the sampling time can be adjusted to be centered in an eye diagram of the data signal pulses. Alternatively, or in addition, the video data can be delayed before it is sampled so that the sampling time is centered in the eye diagram of the data signal pulses.

BRIEF DESCRIPTION OF THE DRAWINGS

Various aspects of at least one embodiment are discussed below with reference to the accompanying figures, which are

not intended to be drawn to scale. The figures are included to provide illustration and a further understanding of the various aspects and embodiments, and are incorporated in and constitute a part of this specification, but are not intended as a definition of the limits of the invention. Where technical features in the figures, detailed description or any claim are followed by reference signs, the reference signs have been included for the sole purpose of increasing the intelligibility of the figures and description. In the figures, each identical or nearly identical component that is illustrated in various figures is represented by a like numeral. For purposes of clarity, not every component may be labeled in every figure. In the figures.

FIG. **1** is a schematic block diagram illustrating a system for video load balancing and error detection based on measured channel bandwidth according to an aspect of the present disclosure.

FIG. **2** is a process flow diagram showing a method of using blanking time to assess channel health during video blanking times according to an aspect of the present disclosure.

FIG. **3** is a diagram illustrating process flow in an upstream state machine that may be implemented to facilitate measuring channel integrity according to an aspect of the present disclosure.

FIG. **4** is a diagram illustrating process flow in a downstream state machine that can be implemented to perform the channel integrity measurements according to an aspect of the present disclosure.

FIG. **5** is a process flow diagram illustrating a method for interconnecting video signal pathways according to an illustrative embodiment of the present disclosure.

FIG. **6** is a schematic block diagram illustrating an apparatus for video load balancing according to an aspect of the present disclosure.

FIG. **7** is a process flow diagram illustrating a method of dynamic load balancing on data bus interconnect in a dynamic impedance environment according to an aspect of the present disclosure.

DETAILED DESCRIPTION

The disclosed system and method performs status checks on parallel channels of data bus interface such as a video data interface and optimizes throughput across the data bus interface based on the status checks. Throughput is optimized by routing data to different channels, changing the data rates of selected channels, and/or changing the frequency at which data is transmitted across each individual channel in the parallel channel environment, for example.

The disclosed system and method determines the maximum data rate at which each channel can reliably transport data. More data is routed to channels that can support higher data rates and less data is routed to channels that may incur errors at the higher data rates, for example. Channel integrity is continuously or periodically monitored because it generally changes over time in a dynamic interface. A rotating slip ring interface may have varying channel impedances and dead spots at various angels of rotation, for example.

In most video systems, image data for each image is transported as a sequence of frames in which each frame is made up of a sequence of lines. Traditionally, an image data signal transporting image data includes some small blanking time between each line and between each video frames. The blanking time in an image data signal does not include the image data representing pixels of a line or frame, but may include some encoded information about the image data and/or about the image data signal, for example.

The disclosed system and method performs the channel status checks and controls data routing and data rate management of channels during the blanking times to take advantage of bandwidth during the blanking times, which is otherwise underutilized.

Blanking time has historically been used to allow the electron beam to raster its way to the beginning of the next line/row on a cathode ray tube (CRT) display. In general, blanking times are determined by the camera/sensor, and in some cases the camera or system may encode metadata, or ancillary data in this dead space/blanking time. For instance, digital audio data, timestamps, etc. is sometimes transported in this dead time between lines of video. According to aspects of the present disclosure this dead time is used to transmit a priori test patterns at multiple clock rates to determine the quality of the link across a slip-ring or dynamic interconnect before sending the next line/frame of video. Thus, maximizing the possibility that the image data will be correctly transported without/minimal errors.

FIG. **1** illustrates a system for video load balancing and error detection based on measured channel bandwidth. The system includes a data bus interconnect **106** that couples a plurality of signal lines between an upstream processing module **102** and a downstream processing module **104**. In an illustrative embodiment, the data bus interconnect **106** may be a slip ring interface, for example. The data bus interconnect **106** couples the signal lines, which include a plurality of video output paths **108** of the upstream processing module **102** coupled to a plurality of video input paths **109** of the downstream processing module **104**. In the illustrative embodiment, the upstream processing circuitry **102** is coupled to a rotating side of a slip ring interconnect, and the downstream processing module **104** is coupled to a stationary side of the slip ring interconnect.

A pixel clock signal **110** in the upstream processing module **102** is input to phase locked loop circuitry **112** in the upstream processing module **102**. The pixel clock signal **110** is also transported across the data bus interface **106** and coupled to phase locked loop circuitry **114** in the downstream processing module **104**. The phase locked loop circuitry **112**, **114** in both the upstream processing module **102** and the downstream processing module **104** outputs a plurality of clock signals **113**, **115** having clock rates that are multiples of the rate of the pixel clock signal **110**. In an illustrative embodiment, the plurality of phase locked loop circuitry clock signals **113**, **115** have clock rates of 1.0×, 1.5×, 2.0×, 2.5× and 3.0× multiples of the rate of the pixel clock signal **110**. The phased lock loop circuitry **112**, **114** ensures that plurality of clock signals **113** in the upstream processing module **102** are synchronized with the corresponding clock signals **115** in the downstream processing module **104**.

The upstream processing module **102** includes upstream processing circuitry **116** coupled to the upstream module's phase locked loop circuitry **112**. The upstream processing circuitry **116** receives the plurality of output clock signals **113** from the upstream module's phase locked loop circuitry **112**. The upstream processing circuitry **116** receives video data signals on an upstream video input path **118** from a camera or sensor and also receives a vertical and horizontal blanking signal from the camera or sensor on an upstream blanking signal path **120**.

The upstream processing circuitry **116** includes a pseudo random number generator for generating a test signal to test a plurality of video channels on the video output paths **108**.

The upstream processing module **102** also includes cyclical redundancy check circuitry **122** coupled between the upstream processing circuitry **116** and the plurality of video output paths **108**. The plurality of video output paths **108** transport a plurality of channels of video data from the cyclical redundancy check circuitry **122** across the data bus interconnect **106** to the plurality of downstream video input paths **109** of the downstream processing module **104**.

A horizontal blanking signal path **124** and a vertical blanking signal path **126** transport a horizontal blanking signal and a vertical blanking signal across the data bus interconnect **106** to downstream processing circuitry **128** in the downstream processing module **104**.

According to an aspect of the present disclosure, the upstream processing circuitry **116** includes video encoding circuitry and data rate control circuitry for each of the video output paths **108**. The downstream processing circuitry **128** is coupled to the phase locked loop circuitry **114** in the downstream module **104**. The downstream processing circuitry **128** receives the plurality of output clock signals **115** from the phase locked loop circuitry **114**. The downstream processing circuitry **128** receives video data from the plurality of downstream video input paths **109**.

The downstream processing circuitry **128** includes video decoding circuitry and channel integrity monitoring circuitry. The channel integrity monitoring circuitry is coupled across the video channel interconnect via a statistics feedback and control path **130** to data rate control circuitry in the upstream processing circuitry **116**. In an illustrative embodiment, the statistics feedback and control path **130** is implemented as a bi-directional serial bus which transports data across the data bus interconnect **106** at a relatively slow rate compared to the rate that video data is transported across the data bus interconnect **106**.

According to an aspect of the present disclosure, for every frame of video data that is transported across the data bus interconnect **106**, the channel integrity monitoring circuitry in the downstream processing circuitry **128** monitors the integrity of each of the video channels received on the video input paths **109** and compiles statistics that characterize the channel integrity of each of the video channels. The statistics are fed back to the data rate control circuitry over the statistics feedback and control path **130**. The statistics are compiled much faster than they can be transported to the data rate control circuitry, which performs adjustments based on those statistics. In an illustrative embodiment, the data rate on statistics feedback and control path **130** is on the order of about 30 Hz to 120 Hz, for example.

In an illustrative embodiment in which the statistics feedback and control path **130** operates at 60 Hz, the data rate provides a time period of 16 milliseconds in which the channel integrity monitoring circuitry can send the channel integrity statistics to the data rate control circuitry. Due to its low data rate, the statistics feedback and control path **130** is not significantly affected by the signal integrity issues that can detrimentally affect video data being transported across the data bus interconnect **106**.

In general, data integrity across the data bus interconnect **106** can vary significantly from time to time due to variable contact impedances on various channels of a mechanical connection, for example. High or varying impedance resulting in poor data integrity on a channel may be caused by worn portion of a data bus interconnect **106**, such as a slip ring interconnect or by environmental conditions such as icing, and/or thermal expansion and contraction of the data bus interconnect **106**. Because channel integrity can vary from time to time, the disclosed channel integrity monitoring circuitry constantly updates the channel integrity statistics and provide feedback information including the updated statistics to the data rate control circuitry.

The channel integrity statics are used by the data rate control circuitry to distribute video data across the video output paths **108** and to control data rates on each of the video output paths **108**. The controlled distribution of the video data and controlled data rates on the video out paths **108** based on the channel integrity statics significantly mitigates signal integrity issues on the data bus interconnect **106**.

In an illustrative embodiment, a portion of the video data input signal is distributed to each video transport channel at a data rate that is appropriate for the channel. The amount of video data in the portion and the data rate of the portion is based on the channel integrity information associated with the corresponding video data transport channel. The portions of the video data input signal are received at the downstream processing module of the interconnect apparatus, on the corresponding video transport channels. According to an aspect of the present disclosure, the portions of the video data input signal received on the plurality of video transport channels are recombined, according to how they had been distributed based on the channel integrity information associated with each channel to reproduce the video data input signal.

In one example, it is desirable to transport eight bits of data across a slip ring interface at a rate of 100 MB per second. This corresponds to transporting eight bits of data every 10 ns, where the pixel clock runs at 100 MHz. If it is determined based on feedback statistics from the last frame that six out of eight video transport channels could reliably send data every 4 ns (250 MHz) or more, and two of the video transport channels were unable to reliably send any data, then the video data is redistributed according to aspects of the present disclosure. In this example, the downstream processing module would instruct the upstream processing module to route the eight bits of data down the six high bandwidth channels. More specifically, a routing table generated by the downstream processing module would instruct the upstream processing module to send two bits of data on the six high bandwidth video transport channels at a clock rate of 200 MHz or period of 5 ns. This provides two bits of data on each channel every 10 ns, which effectively doubles the transport rate of the six good video transport channels.

The downstream processing circuitry **128** generates an uncompressed reproduction of the video data signals that were received on the upstream video input paths **109**. The reproduction of the video data signals are output from the downstream processing circuitry **128** on a downstream video output path **132** along with a reproduction of the vertical and horizontal blanking signal, which is provided on a downstream blanking signal path **134**. The downstream processing circuitry **128** also outputs the pixel clock signal **110**.

According to an aspect of the present disclosure, the downstream processing module **104** is also configured to measure and correct the phase of video data received on the video input paths **109** relative to the time that the video data is sampled. The downstream processing circuitry **128** can perform out of phase sampling of video data on some video output paths **108** and video input paths **109** if some of the video output paths **108** or video input paths **109** are physically longer than other video input paths **108** or video output paths **109**, for example. If uncorrected, this can cause the sampling time of video data to be too close to the time of one to zero transitions in the video data on some channels, which

prevents accurate reproduction of the video data by the downstream processing module **104**.

The phase the video data on a video output paths **108** can be adjusted in the upstream processing module **102** by selectively delaying the video data by some amount in response to phase measurement information received from the downstream processing module **104**. In an illustrative embodiment the video data signal on a selected video transport channel is delayed by increasing increments to determine the phase where the downstream processing module **104** begins to detect an increase in errors.

Alternatively, the sampling time may be incrementally changed relative to the data signal by the downstream processing module **104** to determine the phase where the downstream processing module **104** begins to detect errors. Either of these techniques can be used to adjust the phase of the video data signal relative to the sampling time so that a sampling time is optimally synchronized with the video data signal for each channel.

The ability to adjust the data's phase with respect to the pixel clock signal **110** is commonly built in on to many types of FPGAs, typically called an JO delay block for alignment of data to a clock signal. The JO delay block typically delays when a data signal is sampled.

During a video blanking time for each channel, the disclosed apparatus adjusts the sampling times relative to the video data on each video input path **109** by altering sampling times or delaying video data being written to the video output paths **108**.

In an illustrative embodiment, the downstream processing module **104** uses the pixel clock frequency multiplied by 3× to oversample the video data and determine where the optimal sampling time for sampling inside the eye diagram for each channel. The optimal sampling timing is reported as feedback to the upstream processing module **104** vie the statistics feedback and control path **130**. This information can be used to optimize the sampling time on each channel and/or to delay the video data such that the sampling occurs at an optimal time.

In an illustrative embodiment, the statistics feedback and control path **130** is implemented as a bi-directional serial bus which transports data across the data bus interconnect **106** at a relatively slow rate compared to the rate that video data is transported across the video channel interconnect. In an illustrative embodiment, the data rate on the serial bus is on the order of about 30 Hz to 120 Hz and the video data rate, for example.

A method of using blanking time to assess channel health during video blanking times according to an aspect of the present disclosure is described with reference to FIG. **2**.

At block **202** a random data test signal and cyclical redundancy checks are sent for every line at various clock rates during the blanking times. In an illustrative embodiment, the random data and cyclical redundancy checks are sent at the various clock rates every 128 clock cycles. The random data and cyclical redundancy checks are sent from the upstream processing circuitry **116** and the cyclical redundancy check circuitry **122**, respectively, to the downstream processing circuitry **128** via the video output paths **108** and video input paths **109**.

At block **204**, the video data and random data received by the downstream processing circuitry **128** are continuously oversampled at the various clock rates.

At block **206**, the video data and random data are decoded by the downstream processing circuitry **128** and a cyclical redundancy check is performed on the random data by the downstream processing circuitry **128**.

At block **208**, the downstream processing circuitry **128** generates channel integrity statistics during the blanking times for each channel based on the cyclical redundancy checks of the random data.

At block **210**, the channel integrity statistics are sent by the downstream processing circuitry **128** once per frame via the statistics feedback and control path **130** to the upstream processing circuitry **116**.

At block **212**, the upstream processing circuitry **116** routes the video data to selected video data output paths **108** and adjusts the data rates of each of the video data output paths **108** based on the channel integrity statistics received from the downstream processing circuitry **128**.

Although illustrative embodiments of the disclosed system and method are described herein as implementing cyclical redundancy checks to assess data integrity, it should be understood that various alternative techniques of data integrity checking are well known and may be used instead of or in addition to cyclical redundancy check within the scope of the present disclosure.

An example of an upstream state machine **300** that may be implemented in a field programmable gate array (FPGA) in the upstream processing module **102** once per frame to facilitate measuring channel integrity according to an aspect of the present disclosure is described with reference to FIG. **3**.

At block **302** an 8-bit video signal and blanking signal is received at the 1.0× clock rate. The 8-bit video signal is received by the upstream processing module **102** from an external camera or sensor via the upstream video input path **118**. The blanking signal is received by the upstream processing module **102** from the camera or sensor via the upstream blanking signal path **120**.

At block **304**, the upstream state machine **300** determines from the blanking signal whether a vertical or horizontal blanking period is occurring. Blanking times can be determined by a high or low signal level coming from a sensor or camera to indicate valid pixel data and indicate where each pixel is located. Generally the most important information in a blanking signal identifies the first pixel of each frame, the last pixel in a frame, and the first and last pixels for each row or line of video. In one example, a "high" level on both horizontal and vertical blank indicates a valid image pixel (i.e. not blanking). For a 30 Hz frame rate imaging system, the vertical blanking signal will transition "high" at the first valid pixel in the frame and stay "high" until the last pixel in the frame, or toggle at a 30 Hz rate. The horizontal blank signal will transition "high" at the first pixel in a line/row, and stay "high" until the last valid pixel in that line/row. So for each line/row of video there is some amount of blanking.

At block **306**, when a vertical or horizontal blanking period is not occurring, video is sent based on channel integrity information. For example, the upstream processing circuitry **116** routes the video data to selected video data output paths **108** and adjusts the data rates of each of the video data output paths **108** based on the channel integrity statistics received from the downstream processing circuitry **128**, as described above with regards to FIG. **2**. At step **307**, the upstream state machine **300** jumps back to block **302**.

At block **308**, when a vertical or horizontal blanking period is occurring, a random bit sequence is sent by the upstream processing circuitry **116** to the video data output paths **108** with CRC data. In an illustrative embodiment, the random bit sequence and CRC data are sent after a predetermined number of cycles and at a number of different clock rates that are multiples of the pixel clock **110**. The predetermined number of cycles gives both sides of the video

processing system some small amount of time to reset any counters and/or state machines, as well as send any meta data or ancillary data before the disclosed calibration routine is implemented. In an illustrative embodiment, each horizontal blanking may include 1024 clock cycles and 128 clock cycles may be used to transport metadata, for example. The 128 clock cycles are sufficient to provide 128 bytes of data on an 8-bit, video channel in which to send timestamps and some position/pointing data. This leaves 896 clock cycles to perform the disclosed calibration routine.

At block **310**, the upstream state machine **300** again determines whether vertical or horizontal blanking period is occurring in the same manner as in block **304**, for example. When a vertical or horizontal blanking period is occurring, the upstream state machine **300** jumps to block **308**. When a vertical or horizontal blanking period is not occurring, the upstream state machine **300** jumps to block **306**.

An example of a downstream state machine **400** that can be implemented an FPGA in the downstream processing module **104** to perform the channel integrity measurements according to an aspect of the present disclosure is described with reference to FIG. **4**.

At block **402**, each channel of video is sampled and buffered. According to an aspect of the present disclosure, the sampling is performed by the downstream processing circuitry **128** at a number of different clock rates that are multiples of the pixel clock **110** rate. For example, in an illustrative embodiment, the sampling is performed at 1.0×, 1.5×, 2.0×, 2.5×, 3.0× the clock rate of the pixel clock **110**. Sampling at the plurality of clock rates generates a plurality of data streams that can be compared with each other to determine a highest sampling clock rate that can be used without an unacceptable error rate on each channel. The channel integrity statistics generated at block **208** (FIG. **2**) may include the highest sampling clock rate on each channel, for example.

At block **404**, the downstream state machine **400** determines whether a vertical or horizontal blanking period is occurring.

At block **406**, when vertical or horizontal blanking is occurring, CRC faults are calculated at every 128 clock cycles per channel at each of the different clock rates and statistics and routing strategy are reported to the upstream processing module **102**. The decoding of video data and random data and performing CRC at block **206** (FIG. **2**) may include the sampling performed at block **402** and the calculating CRC faults at block **406** of the downstream state machine **400**, for example. The sampling and performing CRC are performed in the downstream processing circuitry **128** (FIG. **1**).

Although various aspects and embodiments of the present disclosure are described as implementing cyclic redundancy checks (CRCs) to evaluate errors on the video output paths **108** and video input paths **109**, it should be understood that various alternative error checking techniques such as parity checks, checksums and the like may be used instead or in addition to CRCs within the scope of the present disclosure.

At block **408**, the downstream state machine **400** determines whether a vertical or horizontal blanking period is occurring. When a vertical or horizontal blanking period is occurring, the downstream state machine **400** jumps back to block **406**. When a vertical or horizontal blanking period is not occurring, the downstream upstream state machine **400** jumps to block **410**.

At block **410**, when a vertical or horizontal blanking period is not occurring, whether checked as part of block **404** or block **408**, the recovered 8-bit video is decoded based on a routing table and output at the pixel clock rate.

A method for interconnecting video signal pathways according to an illustrative embodiment of the present disclosure is described with reference to FIG. **5**. An apparatus for performing the disclosed method is described below with reference to FIG. **6**. At block **502**, the method includes receiving at an upstream processing module of an interconnect apparatus a feedback signal from a downstream processing module of the interconnect apparatus via a feedback path between the upstream processing module of the interconnect apparatus and the downstream processing module of the interconnect apparatus. In an illustrative embodiment, the feedback path may be the statistics feedback and control path **130** described herein with reference to FIG. **1**. The feedback signal includes channel integrity information for each of a plurality of video transport channels extending from the upstream processing module of the interconnect apparatus to the downstream processing module of the interconnect apparatus, for example.

At block **504**, the method includes receiving at the upstream processing module of the interconnect apparatus a video data signal from one or more cameras coupled to the upstream processing module of the interconnect apparatus. In an illustrative embodiment, the video data input is received by the upstream processing circuitry **116** described herein with reference to FIG. **1**.

At block **506**, the method includes distributing a portion of the video data input signal to the video transport channel for each of the video transport channels. The amount of video data in the portion and the data rate of the portion is based on the channel integrity information associated with the channel.

At block **508**, the method includes coupling a pixel clock to phased locked loop circuitry on the upstream processing module of the interconnect apparatus and to phased locked loop circuitry on the downstream processing module of the apparatus. The phased locked loop circuitry on the upstream processing module of the interconnect apparatus and the phased locked loop circuitry on the downstream processing module of the apparatus generate a plurality of phase locked clock signals having predetermined multiples of the pixel clock rate

At block **510**, the method includes determining whether the video data input signal represents a video blanking period. The blanking signals and clock are separate from the video data lines. The blanking signals are aligned temporally with the pixel data so that when both the horizontal and vertical blanking signals transition "high" this indicates the first pixel in a frame, and when they both go "low" this indicates the last pixel in the frame. If vertical blank in "high" and horizontal blank transitions "low" this indicates the last pixel in a line/row. The blanking signals identify when blanking is occurring and toggle at low rates, typically in the Hz to KHz ranges, which is slow when compared to the pixel and data rates.

At block **512**, the method include sending a random or pseudorandom signal during the video blanking period along with cyclical redundancy check information corresponding to the random or pseudorandom signal on the channel from the upstream processing module of the interconnect apparatus to the downstream processing module of the interconnect apparatus for each of the video transport channels. In an illustrative embodiment, the method includes sending the random or pseudorandom signals along with the cyclical redundancy check information at each of the predetermined multiples of the pixel clock rate.

At block **514**, the method includes receiving at the downstream processing module of the interconnect apparatus, on each of the video transport channels the portion of the video data input signal distributed to the corresponding video transport channel, and recombining the portions of the video data input signal received on the plurality of video transport channels based on the channel integrity information associated with each channel.

At block **516**, the method includes receiving at the downstream processing module of the interconnect apparatus on each of the video transport channels the random or pseudorandom signals and the cyclical redundancy check information associated with the corresponding video transport channels at each of the predetermined multiples of the pixel clock rate.

At block **518**, the method includes performing a channel integrity check for each of the video transport channels based on the random or pseudorandom signals and the cyclical redundancy check information at each of the predetermined multiples of the pixel clock rate and determining an updated channel integrity information for each of the video transport channels based on channel integrity check.

At block **520**, the method includes communicating the updated channel integrity information for each of the plurality transport channels from the downstream processing module of the interconnect apparatus to the upstream processing module of the interconnect apparatus.

In an illustrative embodiment performing the channel integrity check involves performing a cyclical redundancy check for each of the predetermined multiples of the pixel clock rate, determining a maximum one of the predetermined multiples of the pixel clock rate clock rates at which the cyclical redundancy check determines a bit error rate below a predetermined threshold of data integrity, and including the maximum data rate of the channel in the updated channel integrity information.

In the illustrative embodiment, the updated channel integrity information identifies for each of the video transport channels a maximum data rate of the channel as the maximum one of the predetermined multiples of the pixel clock rate at which the cyclical redundancy check determines the bit error rate below the predetermined threshold of data integrity.

At block **522**, the method includes for each of the video transport channels, updating the data rate of the channel to the maximum data rate of the channel identified in the updated channel integrity information associated with the channel and/or updating the amount of video data in the portion based on the updated channel integrity information associated with the channel.

According to an aspect of the present disclosure, communicating the updated channel integrity information to the upstream processing module of the interconnect apparatus is performed only during the video blanking period.

At block **524**, the method includes performing a phase check during the blanking time for each of the video transport channels at a predetermined multiple of the pixel clock rate that oversamples the random or pseudorandom signals and the cyclical redundancy check information, and determining a phase adjustment for each of the video transport channels based on the corresponding phase check. As described above with respect to FIG. **1**, the phase the video data on a video output paths **108** can be adjusted in the upstream processing module **102** by selectively delaying the video data by some amount in response to phase measurement information received from the downstream processing module **104**. In an illustrative embodiment the video data signal on a selected video transport channel is delayed by increasing increments to determine the phase where the downstream processing module **104** begins to detect an increase in errors.

At block **526**, the method includes communicating the phase adjustment in the feedback signal from the downstream processing module of the interconnect apparatus to first downstream processing module of the interconnect apparatus.

At block **528**, the method includes adjusting the phase for data transported on each of the video transport channels based on the phase adjustment received from the downstream processing module of the interconnect apparatus to first downstream processing module of the interconnect apparatus.

An example of an apparatus for video load balancing is configured to perform the method described in FIG. **5**. Referring to FIG. **6**, the apparatus includes a data bus interconnect **606** including a plurality of video transport channels **608**, **609** and a pixel clock channel **610** extending between an upstream processing module **603** of the data bus interconnect **606** and a downstream processing module **605** of the data bus interconnect **606**. An upstream processing module **602** is coupled between a video camera and the upstream processing module **603** of the data bus interconnect **606**. A downstream processing module **604** is coupled to the downstream processing module **606** of the data bus interconnect.

The upstream module **602** may be configured to receive a video data input signal from one or more cameras. According to an aspect of the present disclosure, the upstream processing module **602** is configured to receive a feedback signal from downstream processing module **604**. The feedback signal includes channel integrity information for each of the plurality of the video transport channels. For each of the video transport channels the upstream processing module is configured to distribute a portion of the video data input signal to the respective video transport channel. According to an aspect of the present disclosure, the amount of video data in the portion and the data rate of the portion is based on the channel integrity information associated with the channel.

According to an aspect of the present disclosure, the downstream processing module **604** is configured to perform a channel integrity check for each of the video transport channels **608**, **609** and determine an updated channel integrity information for each of the video transport channels **608**, **609** based on channel integrity check.

During a video blanking period, the downstream processing module **604** is configured to communicate the updated channel integrity information for each of the video transport channels **608**, **609** from the downstream processing module of the data bus interconnect to the upstream processing module of the data bus interconnect.

In an illustrative embodiment the upstream processing module **602** is also configured to determine whether the video data input signal represents a video blanking period. The upstream processing module **602** sends a random or pseudorandom signal to of the video transport channels **608**, **609** during the video blanking period along with cyclical redundancy check information corresponding to the random or pseudorandom signal on the respective channel from the upstream processing module **602** to the downstream processing module **604**. According to an aspect of the present disclosure, the random or pseudorandom signal and cyclical redundancy check information are sent at a plurality of predetermined multiples of the pixel clock rate.

In the illustrative embodiment, the downstream processing module **604** is configured to perform a cyclical redundancy check for each of the video transport channels **608**, **609** based on the random or pseudorandom signals and the cyclical redundancy check information at each of the predetermined multiples of the pixel clock rate. The downstream processing module **604** is configured to determine a maximum one of the predetermined multiples of the pixel clock rate clock rates at which the cyclical redundancy check determines a bit error rate below a predetermined threshold of data integrity and to include the maximum data rate of the channel in the updated channel integrity information.

According to an aspect of the present disclosure, for each of the video transport channels **608**, **609** the upstream processing module is further configured to update the data rate of the respective channel to the maximum data rate of the channel identified in the updated channel integrity information associated with the channel, and/or update the amount of video data in the portion based on the updated channel integrity information associated with the channel.

A method of dynamic load balancing on a data bus interconnect in a dynamic impedance environment according to an aspect of the present disclosure is descried with reference to FIGS. **6** and **7**.

At block **702**, the method includes receiving at an upstream processing module **602** of a data bus interconnect **606** a feedback signal from a downstream processing module **602** of the data bus interconnect **606** via a feedback path **630**. In an illustrative embodiment, the data bus interconnect **606** may comprise a slip ring interconnect **603**, for example. The feedback signal includes channel integrity information for each of a plurality of video transport channels **608**, **609** extending from the upstream processing module **602** to the downstream processing module **604**.

At block **704**, the method includes coupling a pixel clock **610** to phased locked loop circuitry **612** on the upstream processing module **602** and to phased locked loop circuitry **614** on the downstream processing module **604** of the data bus interconnect **606**. The phased locked loop circuitry **612** on the upstream processing module **602** and the phased locked loop circuitry **614** on the downstream processing module **604** generate a plurality of phase locked clock signals **613** having predetermined multiples of the pixel clock rate. At block **706**, the method includes receiving at the upstream processing module **602** a video data input signal from one or more cameras coupled to a video data input path **618** of the upstream processing module **602** of the data bus interconnect. At block **708**, the method includes determining whether the video data input signal represents a video blanking period.

At block **710**, the method includes distributing, by upstream processing circuitry **616**, a portion of the video data input signal to a video transport channel for each of the video transport channels when the video data input signal does not represent a video blanking period. The amount of video data in the portion and the data rate of the portion is based on the channel integrity information associated with the channel.

At block **712**, when the video data input signal represents a video blanking period the method includes, for each of the video transport channels, the upstream processing circuitry **616** sends a random or pseudorandom signal along with cyclical redundancy check information corresponding to the random or pseudorandom signal on the channel **608**, **609** from the upstream processing module **602** to the downstream processing module **604** at each of the predetermined multiples of the pixel clock rate.

At block **714**, the method includes receiving at the downstream processing module **604** on each of the video transport channels **609** the portion of the video data input signal distributed to the corresponding video transport channel **608**. At block **716**, the downstream processing circuitry **628** includes recombines the portions of the video data input signal received on the plurality of video transport channels **609** based on the channel integrity information associated with each channel **609**.

At block **718**, the method includes receiving at the downstream processing module **604** on each of the video transport channels **609**, the random or pseudorandom signals and the cyclical redundancy check information associated with the corresponding video transport channels **609** at each of the predetermined multiples of the pixel clock rate. At block **720**, the downstream processing circuitry **628** performs a cyclical redundancy check of the random or pseudorandom signals on each of the video transport channels **609** for each of the predetermined multiples of the pixel clock rate.

At block **722**, the method includes, the downstream processing circuitry **628** determines a maximum one of the predetermined multiples of the pixel clock rate clock rates at which the cyclical redundancy check determines a bit error rate below a predetermined threshold of data integrity for each of the video transport channels.

At block **724**, the downstream processing circuitry **628** generating updated channel integrity information for each of the video transport channels **609** based on the corresponding cyclical redundancy checks. The updated channel integrity information identifies a maximum data rate of the channel as the maximum one of the predetermined multiples of the pixel clock rate clock rates at which the cyclical redundancy check determines the bit error rate below the predetermined threshold of data integrity.

At block **726**, the method includes communicating the updated channel integrity information for each of the plurality transport channels **608**, **609** from the downstream processing module **604** of the data bus interconnect **606** to the upstream processing module **602** of the data bus interconnect **606** during a video blanking period.

At block **728**, the upstream processing module **606** updates the data rate for each of the video transport channels **608**, **609** to the maximum data rate of the respective channel identified in the updated channel integrity information associated with the channel, and/or updates the amount of video data in the portion based on the updated channel integrity information associated with each channel.

At block **730**, the downstream processing circuitry **628** performs a phase check during the blanking time for each of the video transport channels **608**, **609** at a predetermined multiple of the pixel clock rate that oversamples the random or pseudorandom signals and the cyclical redundancy check information.

At bock **732**, the downstream processing circuitry **628** determines a phase adjustment for each of the video transport channels based on the corresponding phase check.

At block **734**, the downstream processing circuitry **628** communicates the phase adjustment in the feedback signal from the downstream processing module **604** to upstream processing **606** module of the data bus interconnect **606**.

At block **736**, the upstream processing circuitry **616** adjusts the phase for data transported on each of the video transport channels based on the phase adjustment received from the downstream processing module **604** of the data bus interconnect apparatus.

The disclosed system and method provides near real-time dynamic load balancing based on frame by frame feedback of signal integrity statistics to achieve optimal video data rates across inherently unstable contact style data bus interconnection even when the data bus interconnection is under rotation. The disclosed system and method mitigates the inherent changing of signal integrity due to variable contact resistance, impedance, and capacitance across a mechanical data bus interface to improve data integrity across the data bus interconnect and accommodate transport ultra-high definition video data.

As widely deployed video systems get older, the disclosed system and method allows the continued use of their battle proven mechanical interfaces such as slip rings that may be partially defective. In addition to their utility in video data interconnects, the disclosed system and method may be implemented in various other dynamically changing interconnects having parallel data channels, such as interconnects in oil and gas drilling sensors at drill heads, for example.

The invention claimed is:

1. A method for interconnecting video signal pathways, the method comprising:

receiving at an upstream processing module of an interconnect apparatus a feedback signal from a downstream processing module of the interconnect apparatus via a feedback and control path between the upstream processing module of the interconnect apparatus and the downstream processing module of the interconnect apparatus, the feedback signal including channel integrity information for each of a plurality of video transport channels extending from the upstream processing module of the interconnect apparatus to the downstream processing module of the interconnect apparatus;

receiving at the upstream processing module of the interconnect apparatus a video data input signal from one or more cameras coupled to the upstream processing module of the interconnect apparatus; and

for each of the plurality of video transport channels, distributing a portion of the video data input signal to the video transport channel, wherein the amount of video data in the portion and the data rate of the portion is based on the channel integrity information associated with the channel;

for each of the plurality of video transport channels, sending a random or pseudorandom signal along with cyclical redundancy check information corresponding to the random or pseudorandom signal on the channel from the upstream processing module of the interconnect apparatus to the downstream processing module of the interconnect apparatus;

detecting a video blanking period at the upstream processing module;

sending the random or pseudorandom signal along with the cyclical redundancy check information only during the video blanking period;

coupling a pixel clock to phased locked loop circuitry on the upstream processing module of the interconnect apparatus and to phased locked loop circuitry on the downstream processing module of the apparatus, wherein the phased locked loop circuitry on the upstream processing module of the interconnect apparatus and the phased locked loop circuitry on the downstream processing module of the apparatus generate a plurality of phase locked clock signals having predetermined multiples of the pixel clock rate; and

sending the random or pseudorandom signals along with the cyclical redundancy check information at each of the predetermined multiples of the pixel clock rate.

2. The method of claim **1**, further comprising:

receiving at the downstream processing module of the interconnect apparatus, on each of the plurality of video transport channels the portion of the video data input signal distributed to the corresponding video transport channel; and

recombining the portions of the video data input signal received on the plurality of video transport channels based on the channel integrity information associated with each channel.

3. The method of claim **2**, further comprising:

receiving at the downstream processing module of the interconnect apparatus on each of the plurality of video transport channels, the random or pseudorandom signals and the cyclical redundancy check information associated with the corresponding video transport channels at each of the predetermined multiples of the pixel clock rate;

performing a channel integrity check for each of the plurality of video transport channels based on the random or pseudorandom signals and the cyclical redundancy check information at each of the predetermined multiples of the pixel clock rate;

determining an updated channel integrity information for each of the plurality of video transport channels based on channel integrity check; and

communicating the updated channel integrity information for each of the plurality transport channels from the downstream processing module of the interconnect apparatus to the upstream processing module of the interconnect apparatus.

4. The method of claim **3**, wherein performing the channel integrity check comprises:

performing a cyclical redundancy check for each of the predetermined multiples of the pixel clock rate;

determining a maximum one of the predetermined multiples of the pixel clock rate clock rates at which the cyclical redundancy check determines a bit error rate below a predetermined threshold of data integrity; and

including the maximum data rate of the channel in the updated channel integrity information.

5. The method of claim **4**, wherein for each of the plurality of video transport channels the updated channel integrity information identifies a maximum data rate of the channel as the maximum one of the predetermined multiples of the pixel clock rate clock rates at which the cyclical redundancy check determines the bit error rate below the predetermined threshold of data integrity.

6. The method of claim **5**, further comprising:

for each of the plurality of video transport channels, updating the data rate of the channel to the maximum data rate of the channel identified in the updated channel integrity information associated with the channel.

7. The method of claim **4**, comprising:

for each of the plurality of video transport channels, updating the amount of video data in the portion based on the updated channel integrity information associated with the channel.

8. The method of claim **3**, wherein communicating the updated channel integrity information to the upstream processing module of the interconnect apparatus is performed only during the video blanking period.

9. The method of claim 3, further comprising comprises:

during the blanking time, performing a phase check for each of the plurality of video transport channels at a predetermined multiple of the pixel clock rate that oversamples the random or pseudorandom signals and the cyclical redundancy check information; and

determining a phase adjustment for each of the plurality of video transport channels based on the corresponding phase check; and

communicating the phase adjustment in the feedback signal from the downstream processing module of the interconnect apparatus to first downstream processing module of the interconnect apparatus.

10. The method of claim 9, comprising:

adjusting the phase for data transported on each of the plurality of video transport channels based on the phase adjustment received from the downstream processing module of the interconnect apparatus to first downstream processing module of the interconnect apparatus.

11. An apparatus for video load balancing, comprising:

a data bus interconnect including a plurality of video transport channels extending between an upstream processing module of the data bus interconnect and a downstream processing module of the data bus interconnect and a pixel clock channel extending between the upstream processing module of the data bus interconnect and the downstream processing module of the data bus interconnect;

an upstream processing module coupled between a video camera and the upstream processing module of the data bus interconnect; and

a downstream processing module coupled to the downstream processing module of the data bus interconnect;

wherein the upstream processing module is configured to:

receive a feedback signal from downstream processing module, the feedback signal including channel integrity information for each of a plurality of the video transport channels;

receive a video data input signal from one or more cameras coupled to the upstream processing module of the data bus interconnect; and

for each of the plurality of video transport channels, distribute a portion of the video data input signal to the video transport channel, wherein the amount of video data in the portion and the data rate of the portion is based on the channel integrity information associated with the channel;

wherein the downstream processing module is configured to:

perform a channel integrity check for each of the plurality of video transport channels;

determine an updated channel integrity information for each of the plurality of video transport channels based on channel integrity check;

during a video blanking period, communicate the updated channel integrity information for each of the plurality transport channels from the downstream processing module of the data bus interconnect to the upstream processing module of the data bus interconnect;

wherein the upstream processing module is further configured to:

detect a video blanking period; and

for each of the plurality of video transport channels, send a random or pseudorandom signal during the video blanking period along with cyclical redundancy check information corresponding to the random or pseudorandom signal on the channel from the upstream processing module of the data bus interconnect to the downstream processing module of the data bus interconnect at a plurality of predetermined multiples of the pixel clock rate.

12. The apparatus of claim 11, wherein the downstream processing module is further configured to:

for each of the plurality of video channels, perform a cyclical redundancy check based on the random or pseudorandom signals and the cyclical redundancy check information at each of the predetermined multiples of the pixel clock rate; and

determine a maximum one of the predetermined multiples of the pixel clock rate clock rates at which the cyclical redundancy check determines a bit error rate below a predetermined threshold of data integrity;

include the maximum data rate of the channel in the updated channel integrity information.

13. The apparatus of claim 12, wherein the upstream processing is further configured to:

for each of the plurality of video transport channels, update the data rate of the channel to the maximum data rate of the channel identified in the updated channel integrity information associated with the channel, and update the amount of video data in the portion based on the updated channel integrity information associated with the channel.

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