(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
14 January 2016 (14.01.2016)

WIPO | PCT

(10) International Publication Number
WO 2016/007184 A1

(51) International Patent Classification:
G01R 19/00 (2006.01)

(21) International Application Number:
PCT/US2014/058197

(22) International Filing Date:
30 September 2014 (30.09.2014)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
14/327,331 9 July 2014 (09.07.2014) US

(63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:
US 14/327,331 (CON)
Filed on 9 July 2014 (09.07.2014)

(71) Applicant: **TEXAS INSTRUMENTS INCORPORATED** [US/US]; P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(71) Applicant *(for JP only)*: **TEXAS INSTRUMENTS JAPAN LIMITED** [JP/JP]; 24-1, Nishi-shinjuku 6-chome, Shinjuku-ku, Tokyo, 160-8366 (JP).

(72) Inventor: **SEEMAN, Michael, D.**; 1314 Fremont Street, San Jose, CA 95126 (US).

(74) Agents: **DAVIS, Michael A., Jr.** et al.; TEXAS INSTRUMENTS INCORPORATED, International Patent Manager, P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

(54) Title: SENSING CURRENT FLOWING THROUGH A CAPACITOR

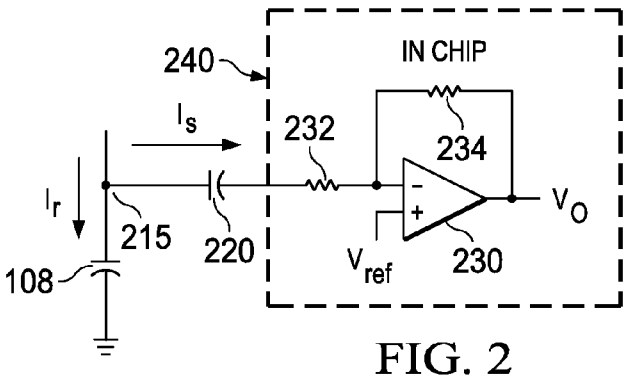

FIG. 2

(57) Abstract: In described examples of a method and circuit for sensing current, a first current (I_r) flows through a first capacitor (108). A second capacitor (220) is coupled to the first capacitor (108) to form a current divider. A second current (I_s) flows through the second capacitor (220) and is proportional to the first current (I_r). A transimpedance amplifier (240) is coupled to an output of the second capacitor (220) and has a voltage output (V_O) that is proportional to the second current (I_s).

WO 2016/007184 A1

SENSING CURRENT FLOWING THROUGH A CAPACITOR

[0001] This disclosure relates in general to electronic circuits, and in particular to sensing current flowing through a capacitor.

BACKGROUND

[0002] A DC-DC converter is an electronic circuit that converts a source of direct current from one voltage level to another. DC-DC converters are widely used in portable electronic devices to provide power from a battery or from an AC-DC converter, and are used generally in electronic circuits to regulate an output voltage. For example, a DC-DC converter may compensate for varying load current and/or variations in the input voltage.

[0003] Measuring current in a DC-DC converter is useful for a wide variety of control and safety purposes, with minimal power loss and inexpensively. However, such measurements can be difficult or require additional components, especially in switched power converters.

[0004] For example, an isolated switched converter, such as an LLC series-resonant converter, has an input powered from a high-voltage DC source. The circuit includes a half-bridge power stage, which is connected to the series elements of an LLC resonant circuit. The LLC resonant circuit is formed by a series combination of a magnetizing inductance and a transformer, and a combined capacitance on the output side of the bridge.

[0005] One solution for sensing the current adds a DC resistor in the primary circuit and senses the voltage drop over the resistor. While this solution is inexpensive, it also creates additional loss and reduces the overall efficiency of the power converter. Another solution incorporates a Hall Effect sensor, which is a transducer that senses the magnetic field generated by a current-carrying conductor and generates an output signal (voltage or current) in response to the magnetic field. However, this solution is expensive and complex. Yet another solution uses a capacitor connected to a capacitive node, but provides limited bandwidth and accuracy.

SUMMARY

[0006] In described examples of a method and circuit for sensing current, a first current flows through a first capacitor. A second capacitor is coupled to the first capacitor to form a current divider. A second current flows through the second capacitor and is proportional to the first

current. A transimpedance amplifier is coupled to an output of the second capacitor and has a voltage output that is proportional to the second current.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIG. 1 is a circuit schematic of a primary side circuit for a half-bridge-based LLC resonant isolated power converter.

[0008] FIG. 2 is a circuit schematic of a transimpedance amplifier for sensing current in the circuit of FIG. 1.

[0009] FIG. 3 is a schematic block diagram of a current feedback amplifier for the circuit of FIG. 2.

[0010] FIG. 4 is a circuit schematic of an integrated circuit that incorporates the transimpedance amplifier of FIG. 2.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0011] This disclosure describes a circuit for sensing current in a capacitive network. For example, a series-resonant DC-DC converter includes a resonant capacitor coupled (such as connected) between a first node and ground. The resonant capacitor carries the primary current to be measured. A sense capacitor is coupled to the resonant capacitor to form a current divider. A sense current flows through the sense capacitor that is proportional to the primary current through the resonant capacitor. A transimpedance amplifier is coupled to the sense capacitor and generates a voltage output that is proportional to the sense current flowing through the sense capacitor. In an embodiment, the transimpedance amplifier is implemented using a current feedback amplifier.

[0012] FIG. 1 is a simplified circuit schematic of a primary side circuit for an isolated power converter illustrating a conventional DC-DC converter 100. A PWM signal generating stage 101 generates logic voltage level PWM signals referenced to ground. A gate driver stage 102 is coupled to the signal generating stage 101 and provides: a PWM signal to the gate of a high-side power transistor 103; and an inverted, non-overlapping PWM signal to the gate of a low-side power transistor 104. The signal generating stage 101 and the gate driver stage 102 can be separate modules or fully integrated in a single control, logic and driver integrated circuit.

[0013] The drain of the high-side power transistor 103 is coupled to a voltage supply terminal, to which the voltage V_{in} is applied. The source of the high-side power transistor 103 is coupled to the drain of the low-side power transistor 104 at a switching node 105. The source of the

low-side power transistor 104 is coupled to a second voltage supply terminal, which is coupled to ground. An inductor 106 has one end coupled to the switching node 105 and the other end coupled to a primary winding of transformer 107. A capacitor 108 is coupled between the other end of the primary winding of transformer 107 and ground and carries the primary current I_r to be sensed. In some embodiments, multiple capacitors may be coupled between the primary winding of transformer 107 and ground, and the current I_r is then the sum of currents through the multiple capacitors. The secondary winding(s) of transformer 107 are connected to a rectifier circuit (not shown) to generate an isolated DC voltage output from the current developed across the inductor 106.

[0014] FIG. 2 is a circuit schematic of a transimpedance amplifier 240 for sensing current in the circuit of FIG. 1, and shows the resonant capacitor 108 of circuit 100 coupled to a common reference, such as ground, or a power rail with a DC offset from ground, or a voltage reference or other voltage with a DC offset (and low impedance) from ground. A smaller sense capacitor 220 is coupled in parallel with the resonant capacitor at node 215 to form a current divider. The sense capacitor 220 is an external component in many converter implementations, but it could instead be integrated on chip. The sense capacitor 220 is not connected directly to a ground, but instead is connected to a virtual ground or common reference in the form of a sense network. In an embodiment, the sensing network is the transimpedance amplifier 240. The sense current I_s from the sense capacitor 220 is fed into an amplifier module 240 having a transimpedance configuration, where the output voltage V_o of the amplifier module is proportional to the sense current I_s input to the amplifier module. Preferably, the transimpedance amplifier configuration is fully implemented "on-chip" as part of an integrated circuit for the power converter and/or other relevant applications.

[0015] In an embodiment, the transimpedance amplifier 240 has a voltage feedback configuration that includes an operational amplifier 230 having a series resistor 232 coupled in series between the sense capacitor 220 and the inverting input of the op amp, a feedback resistor 234 coupled between the output and the inverting input of the op amp, and a voltage reference V_{ref} coupled to the non-inverting input of the op amp. In this configuration, the output voltage $V_o(s)$ is directly proportional to the resonant current I_r, according to the following transfer function:

$$V_o(s) = \frac{1}{(R_s C_s j\omega + 1)} \times \frac{R_f C_s}{(C_s + C_r)} \times I_r$$

where R_s is the value of the series resistor 232; C_s is the value of the sense capacitor 220; C_r is the value of the resonant capacitor 108; R_f is the value of the feedback resistor 234; and ω is the frequency in radians per second.

[0016] Voltage-feedback ("VFB") operational amplifiers may suffer from bandwidth and stability limits in this application. For example, VFB amplifiers are known to have a single dominant pole above the crossover frequency (GWBP) that provides unity-gain stability, but also numerous poles after the crossover frequency. The added zero in the feedback path reduces the phase margin by 90 degrees and causes instability, unless R_s is large enough to create a cancelling pole at a low enough frequency. Further, a substantial R_s reduces the current sense bandwidth by several orders of magnitude below the amplifier GWBP.

[0017] FIG. 3 is a schematic block diagram of a current feedback amplifier ("CFB") 330 for replacing the VFB amplifier 230 of the transimpedance amplifier 240 (FIG. 2). The non-inverting input of the CFB 330 is coupled to the input of buffer 301 inside the op amp 330. The inverting input of the CFB is coupled to the output of buffer 301 inside the op amp 330. The buffer 301 has an impedance Z_B represented by resistance 302, and a gain G_B. A current I is developed through the impedance Z_B and is known as an error current. The current feedback amplifier 330 includes a voltage source 303 that develops voltage Z(I), a function of the current I through buffer 301, which is buffered through output buffer 304 to generate an output voltage V_{OUT}. The output buffer 304 has an impedance Z_{OUT} represented by resistance 305.

[0018] The substitution of a CFB amplifier 330 for the VFB amplifier 230 allows the transimpedance network of FIG. 2 to include the same components, but the bandwidth and stability of the network is dramatically improved by using the CFB amplifier. Further, the series resistor 232 is not needed for stability when a CFB amplifier is used and is therefore optional in this embodiment. However, the presence of the series resistor 232 allows the bandwidth of the network to be reduced to control noise at very high frequencies. The feedback resistor 234 controls the DC gain of the transimpedance amplifier circuit.

[0019] FIG. 4 is a circuit schematic of an application specific integrated circuit 400 implementing the transimpedance amplifier of FIG. 2. The application circuit 400 for a DC-DC converter includes an integrated circuit chip 401 that provides pulse width modulation controller

functions for the application circuit. For example, the integrated circuit ("IC") chip 401 generates a first pulse width modulated signal DPWM0A output at pin 402 and a second pulse width modulated signal DPWM0B output at pin 403. These pulse width modulated signals are coupled to an external converter circuit, such as circuit 100. The first signal DPWM0A is coupled to an isolation stage 411. The output of the isolation stage 411 is coupled to a gate driver integrated circuit 413. The output of the gate drive circuit 413 is coupled to the gate of the high-side transistor 103. The second signal DPWM0B is coupled to a gate driver IC 415, and the output of the gate driver IC 415 is coupled to the gate of the low-side transistor 104.

[0020] In an embodiment, the sense capacitor 220 is coupled to node 215. The output of the sense capacitor 220 is coupled as input to the controller 401 via pin 404, which is coupled to a transimpedance amplifier that is formed on-chip as part of the controller 401. Resistor 320 is used with a voltage amplifier to form a transimpedance amplifier. However, if a trans-impedance amplifier is provided internally to the controller IC 401, then resistor 320 is optional, as described above.

[0021] The transimpedance amplifier can also be implemented using a common-gate amplifier stage or common-base amplifier stage as a first stage or input stage to a multi-stage transistor amplifier. This method will reduce complexity of the amplifier and reduce power consumption for a given bandwidth, but will reduce accuracy somewhat if feedback around the amplifier is not used. The lack of accuracy can be acceptable if the current measurement is only used for cycle-by-cycle current control, as well as fault and short-circuit protection.

[0022] Capacitive current sensing using a transimpedance configuration may be extended to other forms of switching power converters. For example, the circuit can be useful for sensing current in a voltage-doubler output stage in LLC and other isolated transformer topologies. Capacitive current sensing may also be useful for detecting current reversal in an output stage to turn on and off transistors for synchronous rectification purposes.

[0023] For accurately sensing current, this solution is relatively inexpensive, does not result in significant power loss, and has a low component count. Using a current feedback amplifier as the transimpedance amplifier significantly improves bandwidth and stability.

[0024] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A circuit for sensing current flowing through a capacitor, the circuit comprising:

a sense capacitor coupled to a first capacitor, the sense capacitor having a sense current flowing through it that is proportional to a first current flowing through the first capacitor, the first capacitor being coupled to a common reference; and

a transimpedance amplifier coupled to the sense capacitor, wherein a voltage output of the transimpedance amplifier is proportional to the sense current flowing through the sense capacitor.

2. The circuit of claim 1, wherein the transimpedance amplifier uses a common-gate amplifier or a common-source amplifier as an input stage.

3. The circuit of claim 1, wherein the transimpedance amplifier is a current feedback amplifier.

4. The circuit of claim 3, wherein the current feedback amplifier is an operational amplifier having an inverting input, a non-inverting input, and an output, the sense capacitor is coupled to the inverting input of the operational amplifier, a feedback resistor is coupled between the output and the inverting input of the operational amplifier, and the non-inverting input of the operational amplifier is coupled to the common reference.

5. The circuit of claim 4, wherein the non-inverting input of the operational amplifier is coupled to a voltage reference.

6. The circuit of claim 5, further comprising: a series resistor coupled between the sense capacitor and the inverting input of the operational amplifier.

7. The circuit of claim 1, further comprising a plurality of first capacitors coupled to a common reference, wherein the first current equals a sum of currents through each of the first capacitors.

8. The circuit of claim 1, wherein the transimpedance amplifier is formed as part of an integrated circuit, and the sense capacitor is external to the integrated circuit.

9. A circuit for sensing current in a series-resonant DC-DC converter, the circuit comprising:

at least one power capacitor of the converter, the power capacitor for carrying a primary current and being coupled between a first node and a common reference;

a sense capacitor having a first terminal and a second terminal, wherein the first terminal is coupled to the first node, the sense capacitor having a sense current flowing through it that is proportional to the primary current flowing through the power capacitor; and

a transimpedance amplifier having an input coupled to the second terminal of the sense capacitor, wherein a voltage output of the transimpedance amplifier is proportional to a current flowing through the sense capacitor.

10. The circuit of claim 9, wherein the operational amplifier is implemented using one of a common-gate amplifier and a common-source amplifier as an input stage.

11. The circuit of claim 9, wherein the operational amplifier is implemented as a current feedback amplifier.

12. The circuit of claim 11, wherein the current feedback amplifier is an operational amplifier having an inverting input, a non-inverting input, and an output, the second terminal of the sense capacitor is coupled to the inverting input of the operational amplifier, a feedback resistor is coupled between the output and the inverting input of the operational amplifier, and the non-inverting input of the operational amplifier is coupled to the common reference.

13. The circuit of claim 12, wherein the non-inverting input of the operational amplifier is coupled to a voltage reference.

14. The circuit of claim 13, further comprising: a series resistor coupled between the second terminal of the sense capacitor and the inverting input of the operational amplifier.

15. The circuit of claim 9, further comprising a plurality of power capacitors coupled in parallel between the first node and the common reference, wherein the primary current equals the sum of currents through all the power capacitors

16. A method for sensing current flowing through a capacitor, the method comprising:

providing a first capacitor having a first current flowing through the first capacitor and coupled to a common reference;

coupling a second capacitor to the first capacitor to form a current divider, wherein a second current flowing through the second capacitor is proportional to the first current; and

coupling a transimpedance amplifier to an output of the second capacitor, wherein a voltage output of the transimpedance amplifier is proportional to the second current flowing through the second capacitor.

17. The method of claim 16, wherein the transimpedance amplifier uses a common-gate

amplifier or a common-source amplifier as an input stage.

18. The method of claim 16, wherein the transimpedance amplifier is a current feedback amplifier.

19. The method of claim 18, wherein the current feedback amplifier is an operational amplifier having an inverting input, a non-inverting input, and an output, the second capacitor is coupled to the inverting input of the operational amplifier, a feedback resistor is coupled between the output and the inverting input of the operational amplifier, and the non-inverting input of the operational amplifier is coupled to the common reference.

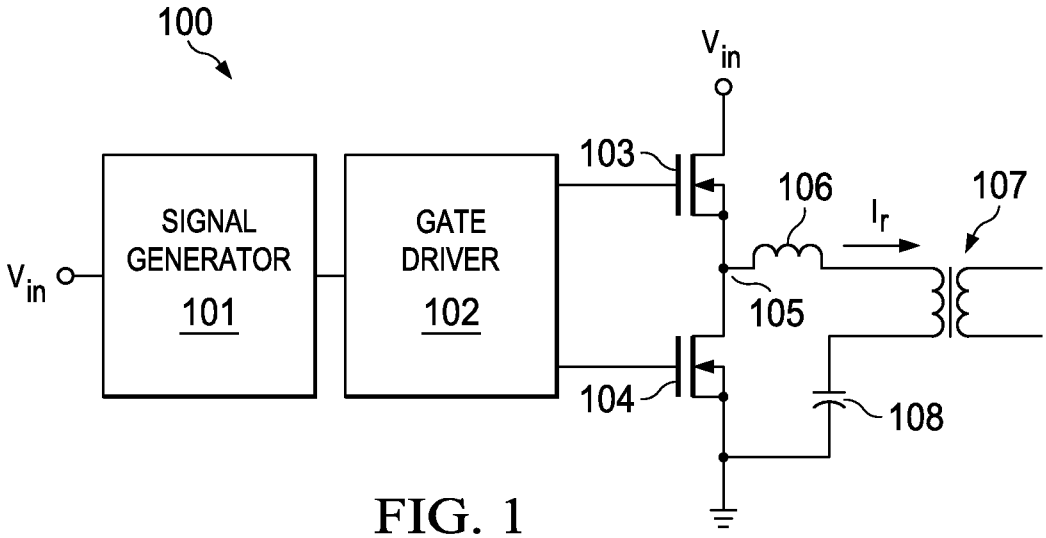

FIG. 1

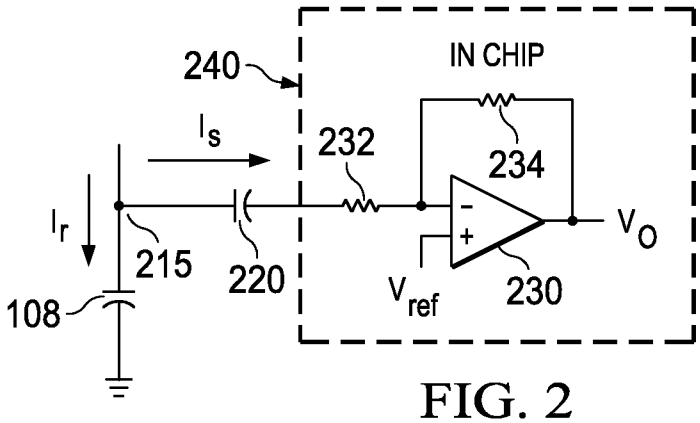

FIG. 2

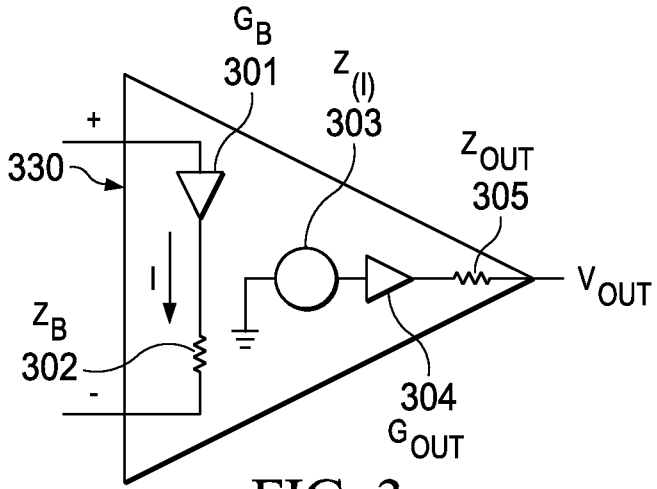

FIG. 3

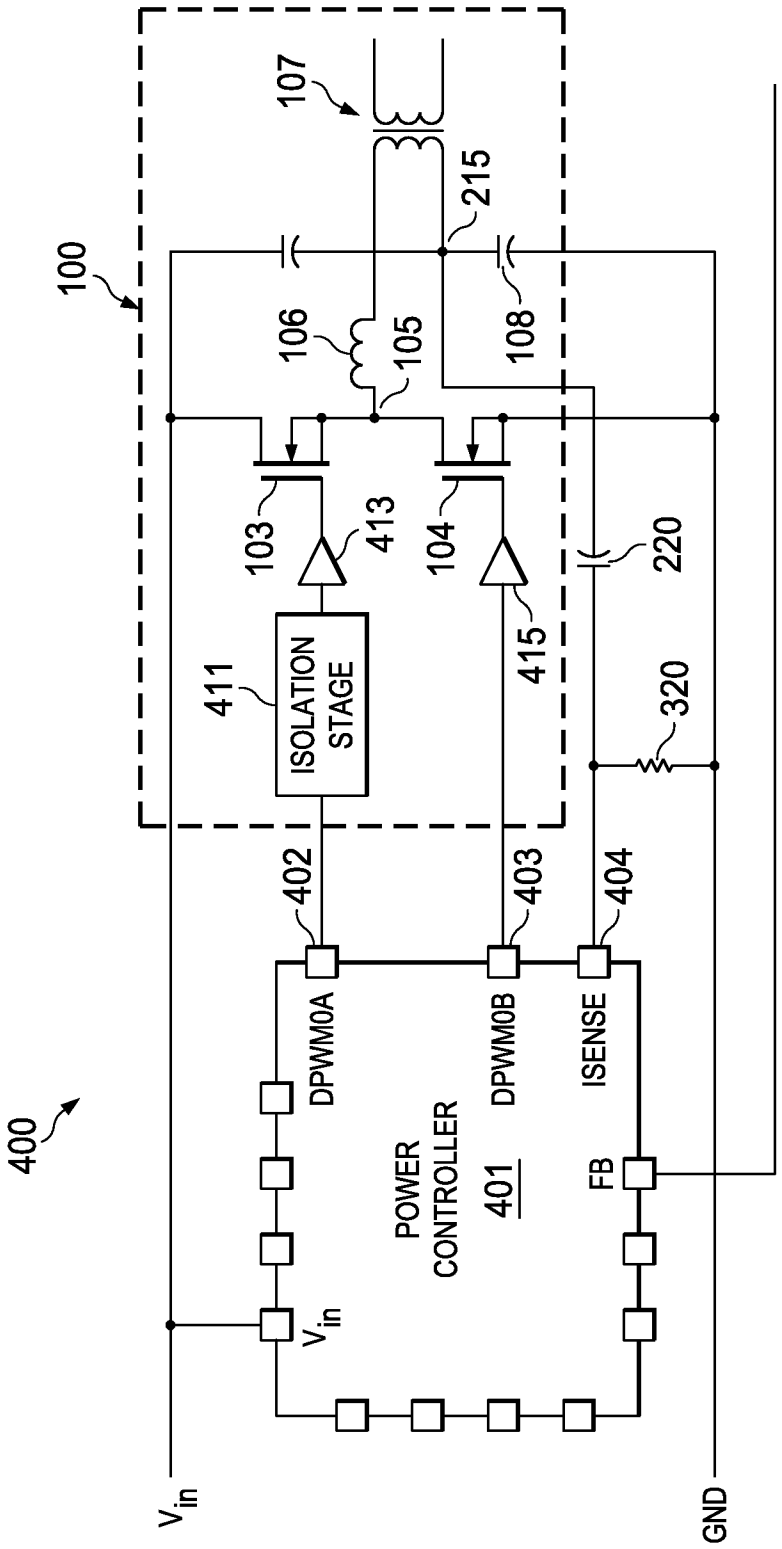
400
100
107
215
106
105
108
103
413
104
415
220
411
ISOLATION STAGE
320
402
403
404
DPWM0A
DPWM0B
ISENSE
POWER CONTROLLER
401
FB
V_{in}
V_{in}
GND

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2014/058197

A. CLASSIFICATION OF SUBJECT MATTER

G01R 19/00 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G01R 19/00, 19/02, 19/03, 19/04, 19/06, 19/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011/0227547 A1 (NATIONAL SEMICONDUCTOR CORPORATION) 22.09.2011, abstract, fig. 1, 2, par. [0026]-[0027], [0031]	1
Y		2-3, 8-11, 16-18
A		4-7, 12-15, 19
Y	EP 0516902 A1 (KABUSHIKI KAISHA TOSHIBA) 09.12.1992, fig. 5, claim 1	16-18
Y	US 2012/0069606 A1 (ONCHIP POWER) 22.03.2012, par. [0074]-[0079], [0181]-[0183], [0187], [0192], fig 2	9-11
Y	US 6218905 B1 (VITESSE SEMICONDUCTOR) 17.04.2001, abstract, fig.1	2-3, 10-11, 17-18

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 March 2015 (24.03.2015)	09 April 2015 (09.04.2015)
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	Authorized officer M. Markov Telephone No. 499-240-25-91

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2014/058197

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 6731121 B1 (MICROSENSORS CORP.) 04.05.2004, abstract, claim 1, fig. 1	8
A	RU 2452075 C1 (OTKRYTOE AKTSIONERNOE OBSCHESTVO "FEDERALNAYA SETEVAYA KOMPANIYA EDINOI ENERGETICHESKOI SISTEMY" (OAO "FSK EES") et al.) 27.05.2012	1-19