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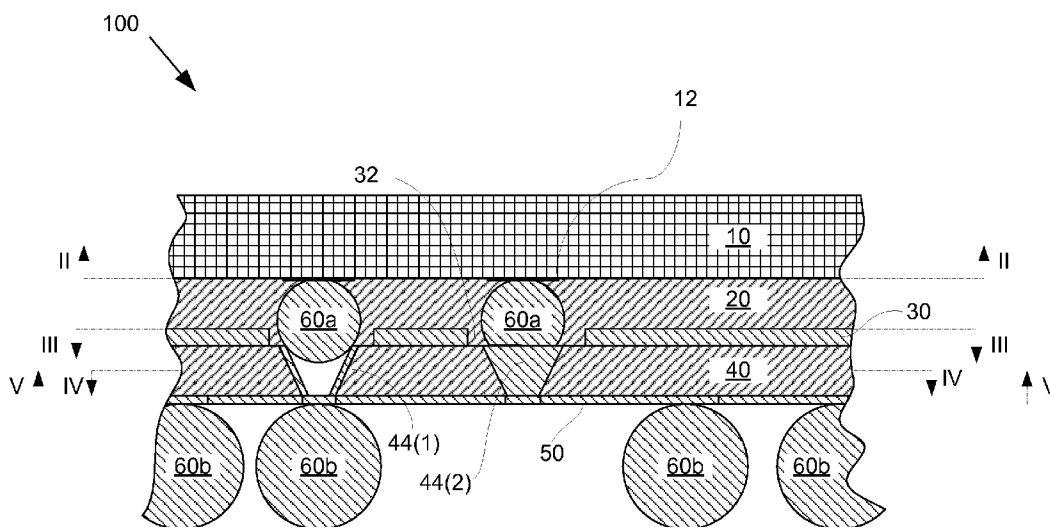
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(57) Abstract: The semiconductor package includes a dielectric layer, a trace layer, a conductive layer, a die and an underfill layer. The dielectric layer has first side and an opposing dielectric layer second side. Multiple vias extend through the dielectric layer from the dielectric layer first side to the dielectric layer second side. Multiple solder balls are disposed at the dielectric layer second side. Each of the solder balls is electrically coupled to a different one of the vias. The die is electrically coupled to the solder balls. The conductive layer is disposed between the dielectric layer second side and the die. The conductive layer defines a window there through for allowing the solder balls to electrically couple to the vias without contacting the conductive layer, i.e., no physical or electrical contact. The underfill layer is formed between the die and the conductive layer, while the trace layer is formed at the dielectric layer first side. Traces of the trace layer electrically couple the vias to other solder balls.

HIGH-SPEED MEMORY PACKAGE

BACKGROUND

[0001] The disclosure herein relates to a multi-layered semiconductor package, and more particularly to a memory package that includes a conductive layer defining a window there through.

[0002] Semiconductor packages are enclosures that house one or more semiconductor die. A semiconductor die is typically a single square or rectangular piece of semiconductor material in which various microelectronic circuits have been formed. A memory package serves to both protect the die contained therein from physical and environmental damage and to physically and electrically connect the die to a printed circuit board (PCB).

[0003] Recently, the demand for higher-speed signals within memory packages has created a need for a ground plane within the package to shield the circuitry. However, the longer the interconnections between the die and the PCB, the higher the impedance, which can lead to signal integrity problems, particularly for high-speed signals.

[0004] Flip-chip packages have been developed to provide short electrical interconnection lengths, but traditional flip-chip packages utilize expensive, thick build-up substrate layers to provide mechanical stability and high density signal routing. These packages are complex to design and manufacture.

[0005] It is therefore desirable to provide a grounded, electromagnetically shielded package that is thin and has short electrical interconnection lengths without compromising the mechanical strength of the package.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] For a better understanding of the nature and objects of the invention, reference should be made to the following detailed description taken in conjunction with the accompanying drawings, in which:

[0007] Figure 1 is a cross-sectional view of a semiconductor package according to an exemplary embodiment;

[0008] Figure 2 is a view taken along line II-II of Figure 1;

[0009] Figure 3 is a view taken along line III-III of Figure 1;

[0010] Figure 4 is a view taken along line IV-IV of Figure 1;

[0011] Figure 5 is a view taken along line V-V of Figure 1; and

[0012] Figure 6 is an exploded perspective view of a semiconductor package according to an exemplary embodiment.

[0013] Like reference numerals refer to the same or similar components throughout the several views of the drawings.

DETAILED DESCRIPTION

[0014] The exemplary embodiments described below address the problems of the prior art by providing a multi-layered semiconductor package having a die, a dielectric layer, an electrical path, and a conductive layer. The die includes an electrical connector. The dielectric layer includes a dielectric layer first side and an opposing dielectric layer second side. The electrical path extends through the dielectric layer from the dielectric layer first side to the dielectric layer second side. The conductive layer is disposed between the die and the dielectric layer first side. The conductive layer defines a window there through for allowing the electrical connector to electrically couple to the electrical path without contacting the conductive layer. In some embodiments, the conductive layer is electrically and/or thermally conductive, acts as a mechanical stiffener, a ground plane, a power plane, or electromagnetic shield.

[0015] FIG 1 shows an exemplary embodiment of a semiconductor package 100. In some embodiments, the semiconductor package 100 includes a dielectric layer 40, an optional trace layer 50, a conductive layer 30, a die 10, and an optional underfill layer 20. The package 100 may also include more or less layers. The dielectric layer 40 has opposing first and second sides. The dielectric layer 40 may be made of any suitable material, such as, without limitation, polyimide, liquid crystal polymer (LCP), or a resin epoxy-based composite, such as Flame Resistant 4 (FR-4) or BT.

[0016] Multiple electrical paths 44, such as vias, extend through the dielectric layer from the dielectric layer first side to the dielectric layer second side. Multiple electrical connectors 60a, such as solder bumps or balls, are disposed near the dielectric layer second side. In general, each of the electrical connectors 60a is electrically coupled to a different one of the electrical paths 44. The die 10 is electrically coupled to the electrical connectors 60a. The conductive layer 30 is disposed between the dielectric layer 40 and the die 10, and in some embodiments, is formed on the dielectric layer second side. The conductive layer 30

defines one or more windows 32 there through for allowing the electrical connectors 60a to electrically couple to the electrical paths 44 without contacting the conductive layer 30, *i.e.*, no physical or electrical contact with the conductive layer 30. The electrical connectors 60a are typically applied to the memory die 10 before the package is assembled. For example, when solder balls or bumps are used, the process is referred to as a bumping process.

[0017] The optional underfill layer 20 is formed between the die 10 and the conductive layer 30. The underfill layer 20 is made from a dielectric material, such as epoxy or the like.

[0018] The optional trace layer 50 is formed at the dielectric layer first side. Traces 56 (Figure 5) of the trace layer 50 electrically couple the electrical paths 44 to other electrical connectors 60a. In some embodiments, the dielectric layer 40 and trace layer 50 together make up a flex tape, such as, without limitation, a copper/polyimide tape. The flex tape may have one or two metal layers and a solder mask on the metal layer.

[0019] In some embodiments, the package 100 is configured to electrically connect to a printed circuit board (PCB) (not shown) through one or more second electrical connectors 60b, such as solder balls/bumps. The second electrical connectors 60b are typically applied to the trace layer 50 at the end of the package assembly process, and may form a ball grid array (BGA) or the like.

[0020] In some embodiments, the semiconductor die 10 is a memory die, such as a random access memory (RAM) die. In these embodiments, the RAM die may be, without limitation, dynamic random access memory (DRAM), double data rate RAM (DDR), DDR2, DDRn, Rambus XDR DRAM, or graphics memory, such as, without limitation, graphics DDR (GDDR), GDDR2, GDDRn, or any other high speed DRAM that uses a multi-layer substrate.

[0021] Figure 2 shows the bottom of the semiconductor die 10, as viewed from line II-II of Figure 1. Inputs into the die and outputs out from the die may be electrically coupled to electrical contacts, such as solder pads 12. These electrical contacts are configured to electrically couple to the electrical connectors 60a. In some embodiments, the electrical contacts are arranged in a row as shown in Figure 2.

[0022] Figure 3 shows the top of the conductive layer 30, as viewed from line III-III of Figure 1. The conductive layer 30 defines one or more windows 32 that extend entirely through the conductive layer, *i.e.*, from one substantially planar side of the conductive layer

to the other. It should be appreciated that the present invention is not limited to any specific number of windows 32. Indeed, Figure 6, discussed below, shows an embodiment having three windows 32. Each window 32 is configured and dimensioned to allow an electrical path to be formed between the die 10 and the electrical paths 44 without the electrical connectors 60a (or the electrical paths 44) making physical contact with the conductive layer 30. In other words, each window 32 is configured such that electrical paths from the electrical contacts 60b to the die 10 are electrically isolated from the conductive layer 30. For example, in some embodiments, as shown in the Figures, the electrical connectors 60a are disposed in at least one row along the length of the window. The electrical connectors 60a are narrower than each window 32 so as to be physically and electrically isolated from the edge of the window 32, and thus from the conductive layer 30. Therefore, the electrical connectors 60a never touch the sides of the windows 32. In some embodiments, each window 32 is substantially rectangular, and has a length of between about 5mm and 15mm, and a width between about 0.10mm and 3.0mm.

[0023] Also in some embodiments, solder pads 12 on the die 10 and the electrical paths 44 through the dielectric layer 40 are disposed in one or more rows along the length of the windows 32. This ensures that the solder pads 12 and electrical paths 44 are also physically and electrically isolated from the conductive layer 30.

[0024] In some embodiments, the conductive layer 30 is a metal foil, such as a FeNi36 (Invar), Cu and/or Cu-Invar-Cu, or alloy 42 material. In some embodiments, the thickness of the conductive layer 30 is between about 5 microns and 150 microns. Also in some embodiments, the conductive layer 30 is formed on the dielectric layer 30 using any suitable technique.

[0025] Figure 4 shows a cross-sectional view through the dielectric layer 40, as viewed from the line IV-IV of Figure 1. As described above, the electrical paths 44 may be electrically conductive vias that electrically and mechanically connect to the electrical contacts 60b and the trace layer 50 (Figure 1). In some embodiments, each via forms an electrically conductive path through the dielectric layer 40. In some embodiments, the vias have diameters of approximately 25-250 μm . In some embodiments, as shown, the vias are substantially frusto-conical, *i.e.*, tapered with the diameter nearer the die 10 being larger than the diameter near the trace layer 50. Alternatively, the vias may be cylindrical or the like.

[0026] Each via may include a central, or “drill” portion formed using a number of techniques. For example, and without limitation, the via holes may be formed using various mechanical drilling, laser drilling, or photolithographic techniques. After the via holes have been formed in the various layers, one or more electrically conductive materials, such as copper or the like, are deposited into the via holes. The electrically conductive material may fill the via holes completely, as shown by reference numeral 44(2), or the electrically conductive material may only plate the walls of the via holes, leaving a hollow space in the electrically conductive material, as shown by reference numeral 44(1). In the case where the electrically conductive material only plates the via holes, the hollow space within the vias may be filled with various dielectric materials, or left hollow. The electrically conductive material may be applied or deposited in the via holes using a number of different techniques, including plating or paste filling. In some embodiments, the vias may be solid, formed, for example, using lithographic techniques.

[0027] Figure 5 shows a view through the trace layer 50, as viewed from the line V-V of Figure 1. In some embodiments, the trace layer 50 includes electrically conductive traces 56 electrically connected to first solder pads 54(1) that are aligned with and coupled to the electrical paths 44. The conductive traces 56 are also electrically connected to second solder pads 54(2) that are configured and dimensioned to mechanically and electrically connected to the electrical connectors 60b (Figure 1). The traces 56 may be formed using photolithography, laser etching, or any other suitable method, and may be composed of various electrically conductive materials, such as copper or the like.

[0028] In some embodiments, in which the conductive layer 30 is used as a ground plane or a power plane, as will be described below, the conductive layer 30 may be electrically connected to the PCB (not shown) through electrical paths 44 through the dielectric layer, the trace layer, and the electrical connectors 60b. These electrical connections between the conductive layer 30 and the PCB (not shown) can include any appropriate electrically conductive elements, such as, without limitation, a combination of vias, traces, and solder balls/bumps similar to those described above. Regardless of their composition, these electrical interconnection paths are physically and electrically isolated from the electrical interconnection paths connecting the die 10 to the PCB (not shown).

[0029] Figure 6 is an exploded perspective view of a semiconductor package according to another exemplary embodiment. The semiconductor package includes many of

the same structures described above, including a semiconductor die 110, a conductive layer 130, a dielectric layer 140, and a trace layer 150. In this embodiment, however, the conductive layer includes three windows 132 configured and dimensioned for receiving at least four rows of solder balls or bumps 160a there through.

5 **[0030]** During manufacture of the die 110, solder balls or bumps 160a may be mechanically and electrically coupled to contact pads 112 on the underside of the die 110. For example, where the semiconductor package is a flip-chip, or Controlled Collapse Chip Connection (C4) memory package, that may or may not include any wire bonds, solder bumps are deposited on the chip pads 112 during the final wafer processing step.

10 **[0031]** During assembly of the package, the trace layer 150 and the conductive layer 130 may be formed on opposing sides of the dielectric layer 140. Solder balls or bumps 160b may then be formed on the trace layer 150. It should be noted that while a two-metal layer assembly is described for simplicity, in some embodiments, any number of metal layers can be used. For example, the dielectric layer 140 may be substituted with multiple alternating
15 dielectric and conductive layers.

[0032] The die 110 is then aligned over the remainder of the package so that the solder balls or bumps 160a pass through the windows 132 of the conductive layer 130 without touching the conductive layer 130. The solder balls or bumps 160a are then mechanically and electrically coupled to the vias 144, such as through a solder reflow process
20 or the like. In other embodiments, the solder balls or bumps 160a penetrate into and are directly electrically and mechanically connected to the vias 144, such as to the tapered side walls described above.

[0033] An underfill layer (similar to layer 20 in Figure 1) may then be formed between the conductive layer 30 and the die 10, which will cover the sides of the die, similar
25 to an encapsulation process.

[0034] The conductive layer 130 can be designed to have any desired characteristics. For example, the material and thickness of the conductive layer 30, as well as the size, shape, and placement of the windows 132 can be selected when designing the package. The conductive layer 130 can be designed to act as a ground plane, a power plane, a mechanical
30 stiffener, an electromagnetic shielding plane, and/or a thermal conductor to aid in cooling of the package. The conductive layer may even be used to reduce noise.

[0035] Once assembled, the solder pads 112 on the die 110 are electrically coupled to the solder balls or bumps 160a, which are electrically coupled to the vias 144, which are electrically coupled to the trace layer 150, which is connected to solder balls or bumps (similar to 60b in Figure 1), which are used to couple the package to a PCB (not shown).

5 Therefore, in some embodiments, electrical paths are formed between the die 110 and the PCB (not shown). Accordingly, each electrical path extends through the thickness of the conductive layer 130 while being physically and/or electrically isolated from it.

[0036] The preceding description sets forth various implementations and embodiments. The implementations and embodiments described incorporate various
10 elements and/or operations recited in the appended claims. The implementations and embodiments are described with specificity in order to meet statutory requirements.

However, the description itself is not intended to limit the scope of this patent. Rather, the inventors have contemplated that the claimed invention might also be implemented in other ways, to include different elements and/or operations or combinations of elements and/or
15 operations similar to the ones described in this document, in conjunction with other present or future technologies.

WHAT IS CLAIMED IS:

1. A multi-layered memory package, comprising:

a die having an electrical connector;

a dielectric layer comprising a dielectric layer first side and an opposing dielectric
5 layer second side;

an electrical path extending through the dielectric layer from the dielectric layer first
side to the dielectric layer second side;

a conductive layer disposed between the die and the dielectric layer first side, wherein
the conductive layer defines a window there through for allowing the electrical connector to
10 electrically couple to the electrical path without contacting the conductive layer.

2. The package of claim 1, wherein the electrical connector is an input or output
connection to the die.

15 3. The package of claim 1, wherein the electrical connector is a contact pad.

4. The package of claim 1, further comprising an additional electrical connector
electrically coupling the electrical connector to the electrical path.

20 5. The package of claim 4, wherein the additional electrical connector is a solder ball or
bump.

6. The package of claim 1, wherein the die has multiple electrical connectors each
connected to a different electrical path through the dielectric layer.

25 7. The package of claim 1, wherein the conductive layer is electrically conductive.

8. The package of claim 1, wherein the conductive layer is thermally conductive.

9. The package of claim 1, wherein the conductive layer acts as a mechanical stiffener.

10. The package of claim 1, wherein the conductive layer is a foil layer.

11. The package of claim 1, wherein the conductive layer is made from a material selected from the group consisting of: alloy 42, FeNi36 (Invar), Cu, and Cu-Invar-Cu.

12. The package of claim 1, wherein the conductive layer is configured to act as a ground plane.

13. The package of claim 1, wherein the conductive layer is configured to act as a power plane.

14. The package of claim 1, wherein the window is disposed substantially at the center of the conductive layer.

15. The package of claim 1, wherein the window comprises a length of approximately 5mm to 15mm, and a width of approximately 0.10mm to 3.0mm, and the conductive layer comprises a thickness of approximately 5 microns to 150 microns.

16. The package of claim 1, wherein the window comprises a substantially rectangular shape.

17. The package of claim 16, wherein the die has multiple electrical connectors arranged in a row that is disposed along a length of the window.

18. The package of claim 1, further comprising a trace layer coupled to the dielectric layer second side.

19. The package of claim 18, wherein the electrical path comprises a via that extends through the dielectric layer.

20. The package of claim 1, further comprising additional layers.

21. The package of claim 20, wherein the electrical path comprises one or more traces, disposed on or in at least one of the layers of the package.

22. The package of claim 1, further comprising a solder ball coupled to the electrical path at the second side of the dielectric layer.

23. The package of claim 1, wherein the dielectric layer is a flex tape.

24. The package of claim 1, wherein the dielectric layer is made from a material selected from a group consisting of: polyimide, liquid crystal polymer, an FR-4 resin epoxy-based fiberglass composite, and a BT-based composite.

25. The package of claim 1, further comprising an underfill layer between the die and the conductive layer.

26. A semiconductor package, comprising:

a dielectric layer comprising a dielectric layer first side and an opposing dielectric layer second side;

multiple electrical paths extending through the dielectric layer from the dielectric layer first side to the dielectric layer second side;

multiple electrical connectors disposed at the dielectric layer second side, where each of the electrical connectors is electrically coupled to a different one of the electrical paths;

a die electrically coupled to the electrical connectors; and

a conductive layer disposed between the dielectric layer second side and the die, wherein the

conductive layer defines a window there through for allowing the electrical connectors to electrically couple to the electrical paths without contacting the conductive layer.

27. The package of claim 26, further comprising an underfill layer between the die and the conductive layer.

28. The package of claim 26, wherein the electrical connectors are solder balls.

29. The package of claim 28, further comprising a trace layer at the dielectric layer first side, where the trace layer is electrically coupled to the electrical paths.

30. The package of claim 29, further comprising additional solder balls coupled to the trace layer.

31. The package of claim 26, wherein the multiple electrical paths are vias through the dielectric layer.

32. A semiconductor package, comprising:

a non-conductive layer comprising a first side and an opposing second side;

multiple first means for conducting electricity, the first means extending through the non-conductive layer from the first side to the second side;

multiple second means for conducting electricity disposed at the second side, where each of the second means is electrically coupled to a different one of the first means;

a semiconductor device electrically coupled to the second means; and

a conductive layer disposed between the second side and the semiconductor device, wherein the conductive layer provides a means for allowing the second means to electrically couple to the first means without contacting the conductive layer.

33. A system comprising:

one or more semiconductor packages, each comprising:

a dielectric layer comprising a dielectric layer first side and an opposing dielectric layer second side;

multiple vias extending through the dielectric layer from the dielectric layer first side to the dielectric layer second side;

multiple solder balls disposed at the dielectric layer second side, where each of the solder balls is electrically coupled to a different one of the vias;

a die electrically coupled to the solder balls;

a conductive layer disposed between the dielectric layer second side and the die, wherein the conductive layer defines a window there through for allowing the solder balls to electrically couple to the vias without contacting the conductive layer; an underfill layer between the die and the conductive layer; and

a trace layer coupled to the dielectric layer first side, where the trace layer is electrically coupled to the vias.

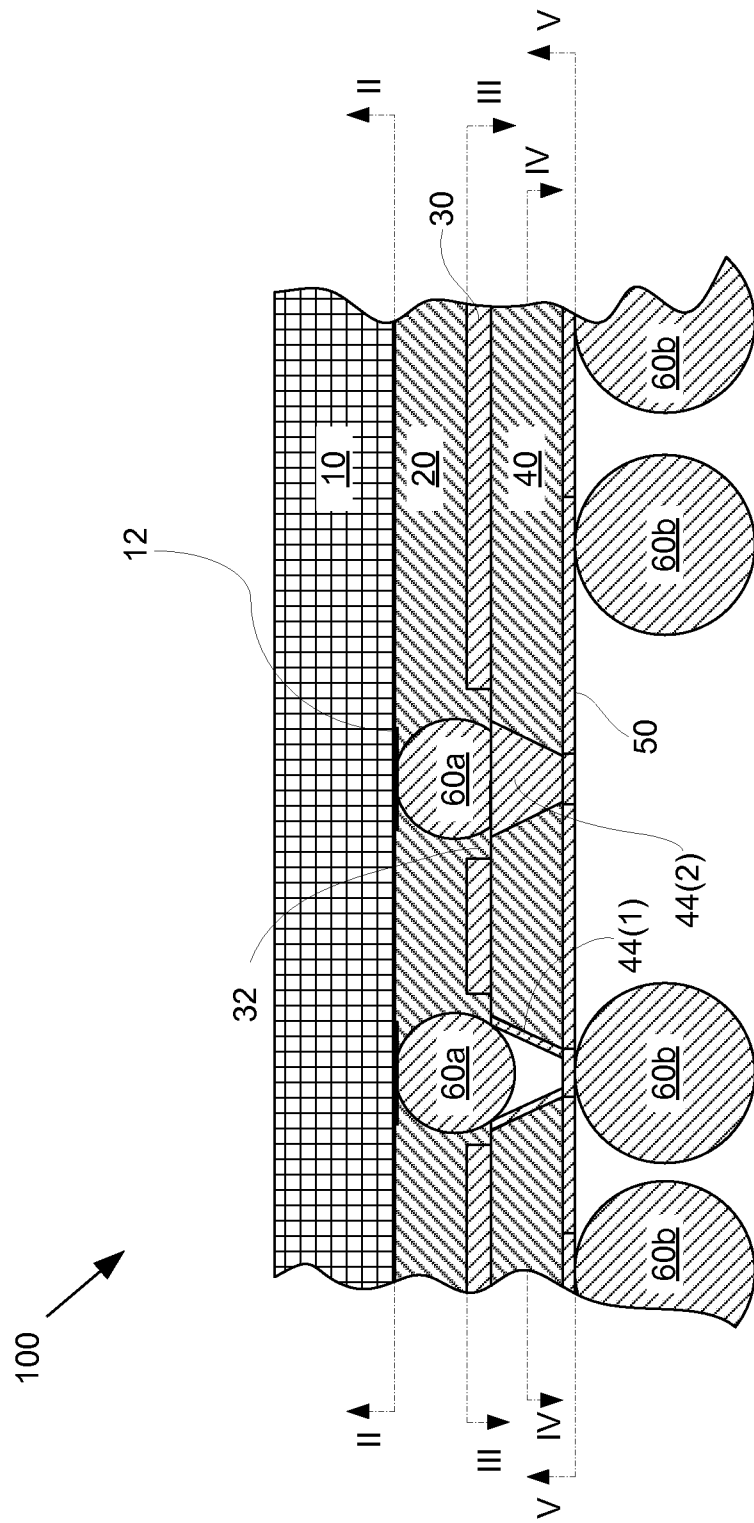


FIG. 1

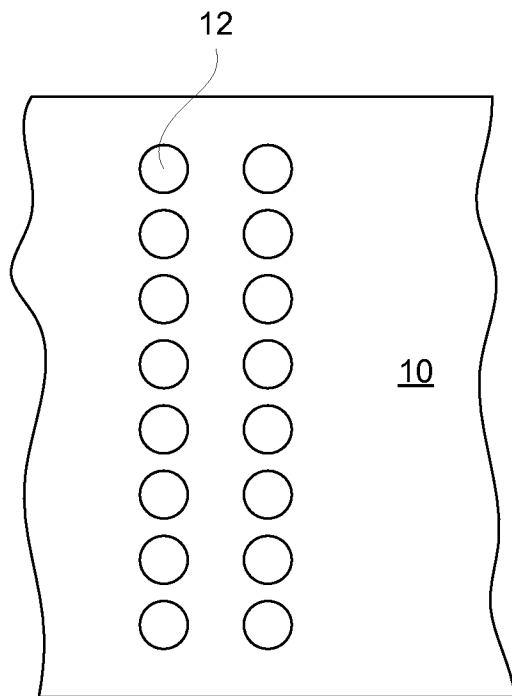


FIG. 2

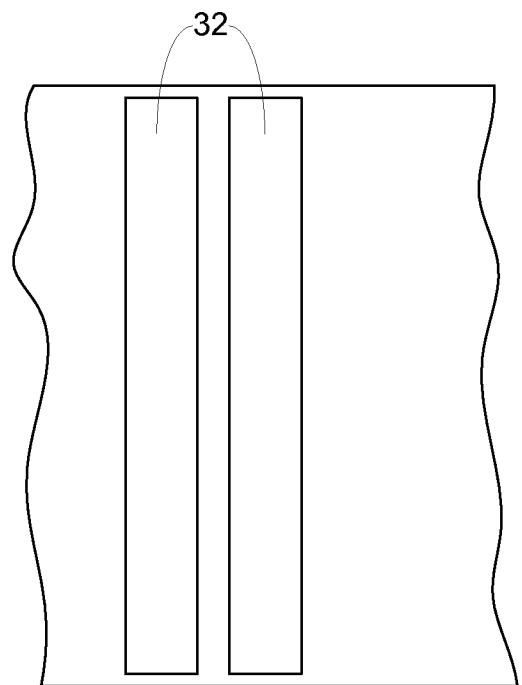


FIG. 3

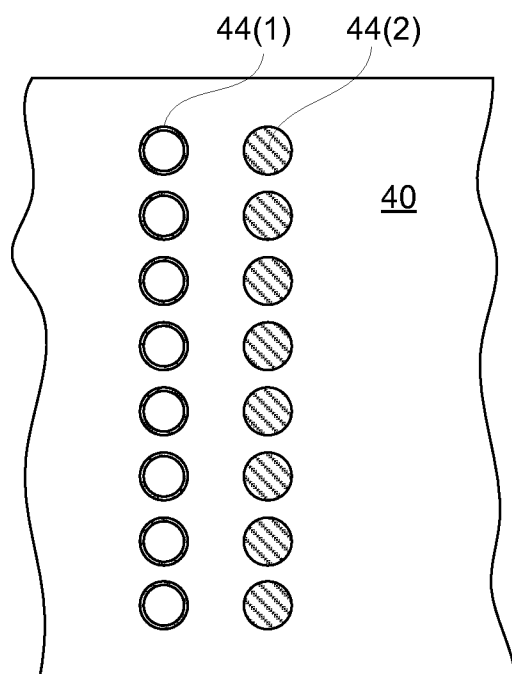


FIG. 4

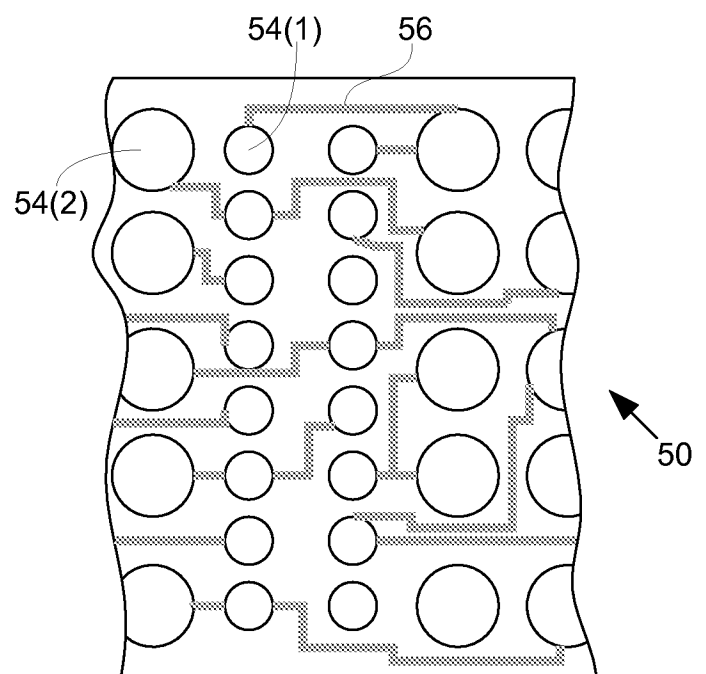


FIG. 5

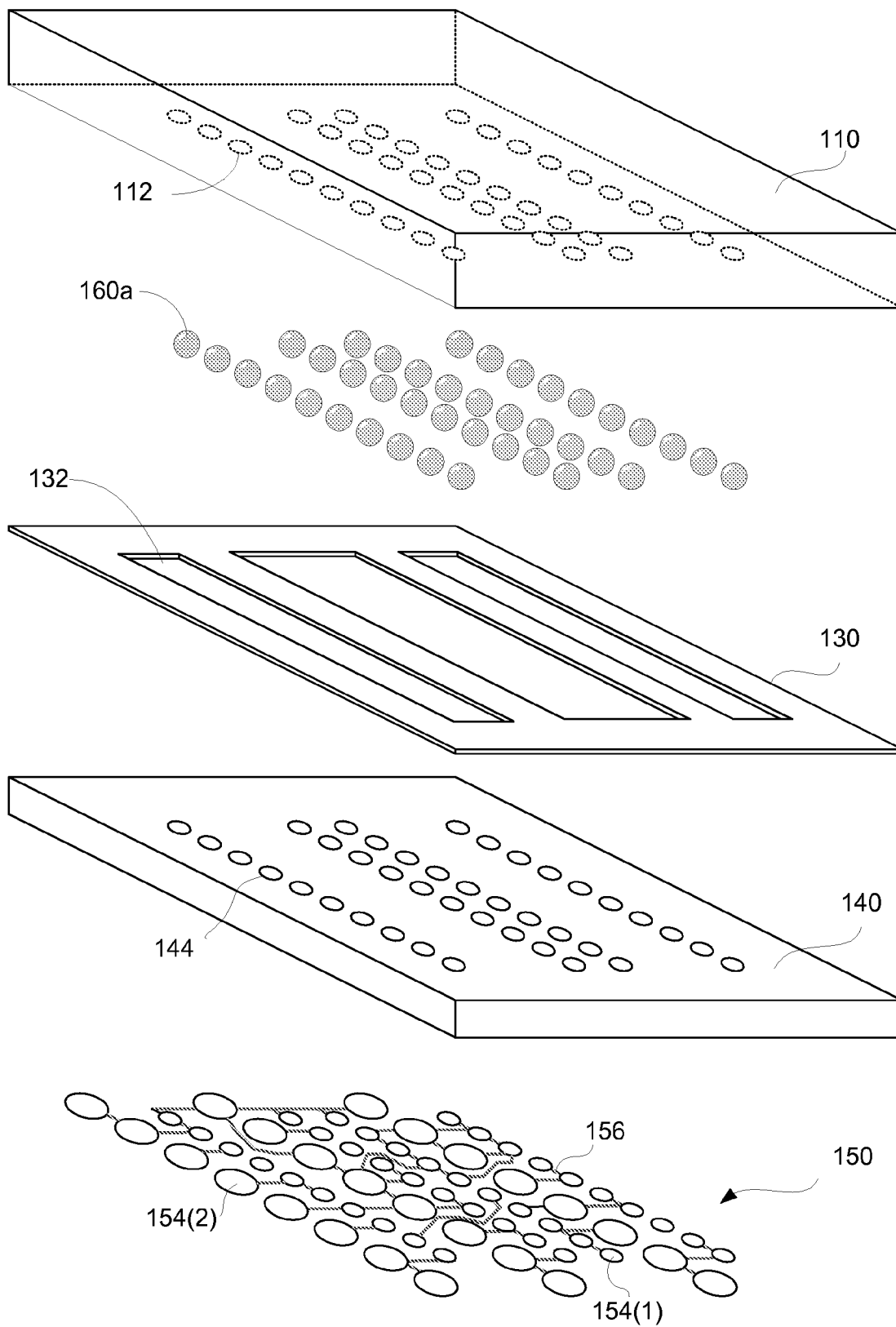


FIG. 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2008/054455

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L23/60

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 225 694 B1 (TERUI MAKOTO [JP]) 1 May 2001 (2001-05-01) column 2, line 1 - line 67 column 4, line 27 - column 5, line 14; figure 5	1-33
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A	EP 0 637 871 A (MATSUSHITA ELECTRIC IND CO LTD [JP]) 8 February 1995 (1995-02-08) column 5, line 22 - column 7, line 14; figure 1	1-33

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Date of the actual completion of the international search

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2008/054455

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