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**THREE-DIMENSIONAL MEMORY DEVICE AND METHOD OF MAKING
THEREOF USING DOUBLE PITCH WORD LINE FORMATION****RELATED APPLICATIONS**

[0001] This application claims the benefit of priority from U.S. Non-Provisional Patent Application No. 17/351,756, filed June 18, 2021; U.S. Non-Provisional Patent Application No. 17/351,789, filed June 18, 2021; U.S. Non-Provisional Patent Application No. 17/351,811, filed June 18, 2021, and U.S. Non-Provisional Patent Application No. 17/406,493, filed August 19, 2021; the entire contents of which are hereby incorporated by reference for all purposes.

FIELD

[0002] The present disclosure relates generally to the field of semiconductor devices, and particularly to a three-dimensional memory device and method of making thereof using double pitch word line formation.

BACKGROUND

[0003] Three-dimensional vertical NAND strings having one bit per cell are disclosed in an article by T. Endoh et al., titled “Novel Ultra High Density Memory With A Stacked-Surrounding Gate Transistor (S-SGT) Structured Cell”, IEDM Proc. (2001) 33-36.

SUMMARY

[0004] According to an aspect of the present disclosure, a three-dimensional memory device is provided, which comprises: a vertical repetition of multiple instances of a unit layer stack, wherein the unit layer stack comprises, from bottom to top or from top to bottom, a

cavity-free insulating layer that is free of any cavity therein, a first-type electrically conductive layer, a cavity-containing insulating layer including an encapsulated cavity therein, and a second-type electrically conductive layer; memory openings vertically extending through the vertical repetition; and memory opening fill structures located within the memory openings, wherein each of the memory opening fill structures comprises a respective vertical stack of memory elements.

[0005] According to another aspect of the present disclosure, a method of forming a three-dimensional memory device is provided, which comprises: forming a vertical repetition of multiple instances of a unit layer stack over a substrate, wherein the unit layer stack comprises a cavity-free insulating layer, a first nucleation seed liner, a sacrificial material layer, and a second nucleation seed liner; forming memory openings vertically extending through the vertical repetition; forming memory opening fill structures within the memory openings; forming backside trenches through the vertical repetition; removing the sacrificial material layers selective to the cavity-free insulating layers, the first nucleation seed layers, the second nucleation seed layers, and the memory opening fill structures, whereby backside recesses are formed in volumes from which the sacrificial material layers are removed; forming electrically conductive layers by nucleating a metal material on the first nucleation seed layers and the second nucleation seed layers while suppressing nucleation of the metal material on physically exposed sidewall segments of the memory opening fill structures and on physically exposed surfaces of the cavity-free insulating layers; and removing portions of the electrically conductive layers located outside of the backside recesses.

[0006] According to yet another aspect of the present disclosure, a method of forming a three-dimensional memory device is provided, which comprises: forming a vertical repetition of multiple instances of a unit layer stack over a substrate, wherein the unit layer stack

comprises a cavity-free insulating layer and a sacrificial material layer; forming memory openings vertically extending through the vertical repetition; forming memory opening fill structures comprising a respective dielectric metal oxide blocking dielectric layer within the memory openings; forming backside trenches through the vertical repetition; removing the sacrificial material layers selective to the cavity-free insulating layers and the memory opening fill structures, whereby backside recesses are formed in volumes from which the sacrificial material layers are removed, and wherein sidewalls of the dielectric metal oxide blocking dielectric layers are physically exposed to the backside recesses; forming nucleation seed layers comprising a nucleation seed material on physically exposed surfaces of the insulating layers while suppressing deposition of the nucleation seed material on the physically exposed sidewalls of the dielectric metal oxide blocking dielectric layers; forming electrically conductive layers by nucleating a metal material on the nucleation seed layers while suppressing nucleation of the metal material on the sidewalls of the dielectric metal oxide blocking dielectric layers; and removing portions of the electrically conductive layers located outside of the backside recesses.

[0007] According to an aspect of the present disclosure, a three-dimensional memory device is provided, which comprises: a vertical repetition of multiple instances of a unit layer stack, wherein the unit layer stack comprises, from bottom to top, a seamless insulating layer that is free of any seam therein, a first-type electrically conductive layer, a seamed insulating layer including a horizontally-extending seam therein, and a second-type electrically conductive layer; memory openings vertically extending through the vertical repetition; and memory opening fill structures located within the memory openings, wherein each of the memory opening fill structures comprises a respective vertical stack of memory elements.

[0008] According to another aspect of the present disclosure, a method of forming a three-dimensional memory device is provided, which comprises: forming a vertical repetition of multiple instances of a unit layer stack over a substrate, wherein the unit layer stack comprises an insulating layer and a sacrificial material layer; forming memory openings vertically extending through the vertical repetition; removing the sacrificial material layers selective to the insulating layers by introducing an isotropic etchant that etches a material of the sacrificial material layers selective to a material of the insulating layers into the memory openings, whereby lateral recesses are formed in volumes from which the sacrificial material layers are removed; depositing at least one conductive fill material at peripheral portions of the lateral recesses; depositing an insulating fill material over the at least one conductive fill material within remaining volumes of the lateral recesses; removing peripheral portions of the insulating fill material from inside the memory openings; and forming memory opening fill structures within volumes of the memory openings, wherein each of the memory opening fill structures comprises a respective vertical stack of memory elements.

[0009] According to yet another aspect of the present disclosure, a three-dimensional memory device is provided, which comprises: a vertical repetition of multiple instances of a unit layer stack, wherein the unit layer stack comprises, from bottom to top, a first-type insulating layer, a first-type electrically conductive layer, a second-type insulating layer, and a second-type electrically conductive layer; memory openings vertically extending through the vertical repetition; memory opening fill structures located within the memory openings, wherein each of the memory opening fill structures comprises a respective vertical stack of memory elements; and a laterally insulated contact structure comprising: a tubular contact via structure vertically extending through at least one instance of the unit layer stack and contacting an annular top surface of the second-type electrically conductive layer in an

underlying instance of the unit layer stack; and a cylindrical contact via structure laterally surrounded by the tubular contact via structure and contacting an annular top surface of the first-type electrically conductive layer in the underlying instance of the unit layer stack.

[0010] According to still another aspect of the present disclosure, a method of forming a three-dimensional memory device is provided, which comprises: forming a vertical repetition of multiple instances of a unit layer stack over a substrate, wherein the unit layer stack comprises an insulating layer and a sacrificial material layer; forming sacrificial memory opening fill structures vertically extending through the vertical repetition; forming contact via cavities having different depths through the vertical repetition, wherein a surface of a respective sacrificial material layer of the sacrificial material layers is physically exposed at a bottom of each of the contact via cavities; removing the sacrificial material layers selective to the insulating layers by isotropically etching a material of the sacrificial material layers selective to a material of the insulating layers, whereby lateral recesses are formed in volumes from which the sacrificial material layers are removed; depositing at least one conductive fill material at peripheral portions of the lateral recesses and the contact via cavities; depositing an insulating fill material over the at least one conductive fill material within remaining volumes of the lateral recesses and the contact via cavities; forming memory cavities by removing the sacrificial memory opening fill structures; removing proximal portions of the at least one conductive fill material from around the memory cavities; and forming memory opening fill structures within volumes of the memory cavities and additional volumes of voids formed by removal of the proximal portions of the at least one conductive fill material, wherein each of the memory opening fill structures comprises a vertical repetition of memory elements.

[0011] According to even another aspect of the present disclosure, a three-dimensional memory device is provided, which comprises: a vertical repetition of multiple instances of a unit layer stack, wherein the unit layer stack comprises, from bottom to top, a first-type insulating layer, a first-type electrically conductive layer comprising a first conductive barrier liner and a first conductive fill material layer, a second-type insulating layer, and a second-type electrically conductive layer comprising a second conductive fill material layer and a second conductive barrier liner; memory openings vertically extending through the vertical repetition; and memory opening fill structures located within the memory openings, wherein each of the memory opening fill structures comprises a respective vertical stack of memory elements. The first conductive fill material layer and the second conductive fill material layer are in direct contact with horizontal surfaces of the second-type insulating layer. The first conductive barrier liner is in direct contact with a horizontal surface of the first-type insulating layer. The second conductive barrier liner is in direct contact with a horizontal surface of another first-type insulating layer of an adjacent unit layer stack.

[0012] According to further another aspect of the present disclosure, a method of forming a three-dimensional memory device is provided, which comprises: forming a vertical repetition of multiple instances of a unit layer stack over a substrate, wherein the unit layer stack comprises an insulating layer and a sacrificial material layer; forming memory openings vertically extending through the vertical repetition; forming sacrificial memory opening fill structures within the memory openings; forming backside trenches through the vertical repetition; removing the sacrificial material layers selective to the insulating layers through the backside trenches, whereby lateral recesses are formed in volumes from which the sacrificial material layers are removed, and wherein the lateral recesses laterally surround remaining portions of the sacrificial memory opening fill structures; depositing at least one

conductive fill material at peripheral portions of the lateral recesses; depositing an insulating fill material over the at least one conductive fill material within remaining volumes of the lateral recesses; removing the sacrificial memory opening fill structures; removing proximal portions of the at least one conductive fill material from around memory cavities formed by removal of the sacrificial memory opening fill structures, wherein voids are formed within volumes of the memory openings; and forming memory opening fill structures within volumes of the memory openings, wherein each of the memory opening fill structures comprises a respective vertical stack of memory elements.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIG. 1 is a schematic vertical cross-sectional view of a first exemplary structure after formation of at least one peripheral device, a semiconductor material layer, and a gate dielectric layer according to a first embodiment of the present disclosure.

[0014] FIG. 2 is a schematic vertical cross-sectional view of the first exemplary structure after formation of a vertical repetition of a unit layer stack according to the first embodiment of the present disclosure.

[0015] FIG. 3 is a schematic vertical cross-sectional view of the first exemplary structure after formation of stepped terraces and a sacrificial retro-stepped dielectric material portion according to the first embodiment of the present disclosure.

[0016] FIG. 4A is a schematic vertical cross-sectional view of the first exemplary structure after formation of memory openings and support openings according to the first embodiment of the present disclosure.

[0017] FIG. 4B is a top-down view of the first exemplary structure of FIG. 4A. The vertical plane A – A' is the plane of the cross-section for FIG. 4A.

[0018] FIG. 5 is a schematic vertical cross-sectional view of the first exemplary structure after formation of sacrificial memory opening fill structures and sacrificial support opening fill structures according to the first embodiment of the present disclosure.

[0019] FIG. 6A is a schematic vertical cross-sectional view of the first exemplary structure after formation of backside trenches according to the first embodiment of the present disclosure.

[0020] FIG. 6B is a partial see-through top-down view of the first exemplary structure of FIG. 6A. The vertical plane A – A' is the plane of the schematic vertical cross-sectional view of FIG. 6A.

[0021] FIG. 7A is a schematic vertical cross-sectional view of the first exemplary structure after formation of sacrificial backside trench fill structures according to the first embodiment of the present disclosure.

[0022] FIG. 7B is a partial see-through top-down view of the first exemplary structure of FIG. 7A. The vertical plane A – A' is the plane of the schematic vertical cross-sectional view of FIG. 7A.

[0023] FIG. 8 is a schematic vertical cross-sectional view of the first exemplary structure after formation of voids within the volumes of the memory openings and the support openings according to the first embodiment of the present disclosure.

[0024] FIGS. 9A – 9J are sequential vertical cross-sectional views of a region between a memory opening and a sacrificial backside trench fill structure during formation of in-process electrically conductive layers according to the first embodiment of the present disclosure.

[0025] FIGS. 10A – 10F are sequential vertical cross-sectional views of a region around a memory opening and a backside trench fill structure during formation of memory opening fill structures according to the first embodiment of the present disclosure.

[0026] FIGS. 11A – 11D are sequential vertical cross-sectional views of a region around a memory opening and a backside trench during replacement of sacrificial backside trench fill structures with backside trench fill structures according to the first embodiment of the present disclosure.

[0027] FIG. 12 is a vertical cross-sectional view of a first alternative configuration of a region of the first exemplary structure according to the first embodiment of the present disclosure.

[0028] FIG. 13 is a vertical cross-sectional view of a second alternative configuration of a region of the first exemplary structure according to the first embodiment of the present disclosure.

[0029] FIG. 14 is a vertical cross-sectional view of a third alternative configuration of a region of the first exemplary structure according to the first embodiment of the present disclosure.

[0030] FIG. 15A is a vertical cross-sectional view of the first exemplary structure after replacement of the sacrificial backside trench fill structures with backside trench fill structures according to the first embodiment of the present disclosure.

[0031] FIG. 15B is a partial see-through top-down view of the first exemplary structure of FIG. 15A. The vertical plane A – A' is the plane of the schematic vertical cross-sectional view of FIG. 15A.

[0032] FIG. 16 is a vertical cross-sectional view of the first exemplary structure after removal of the sacrificial retro-stepped dielectric material portion according to the first embodiment of the present disclosure.

[0033] FIG. 17 is a vertical cross-sectional view of the first exemplary structure after removing vertically-connecting portions of the electrically conductive layers according to the first embodiment of the present disclosure.

[0034] FIG. 18A is a vertical cross-sectional view of the first exemplary structure after application and patterning of a photoresist layer and an anisotropic etch process according to the first embodiment of the present disclosure.

[0035] FIG. 18B is a partial see-through top-down view of the first exemplary structure of FIG. 18A. The vertical plane A – A' is the plane of the schematic vertical cross-sectional view of FIG. 18A.

[0036] FIG. 18C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 18B.

[0037] FIG. 19A is a vertical cross-sectional view of the first exemplary structure after formation of a retro-stepped dielectric material portion and a contact-level dielectric layer according to the first embodiment of the present disclosure.

[0038] FIG. 19B is a partial see-through top-down view of the first exemplary structure of FIG. 19A. The vertical plane A – A' is the plane of the schematic vertical cross-sectional view of FIG. 19A.

[0039] FIG. 19C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 19B.

[0040] FIG. 20A is a vertical cross-sectional view of the first exemplary structure after formation of contact via structures according to the first embodiment of the present disclosure.

[0041] FIG. 20B is a partial see-through top-down view of the first exemplary structure of FIG. 20A. The vertical plane A – A' is the plane of the schematic vertical cross-sectional view of FIG. 20A.

[0042] FIG. 20C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 20B.

[0043] FIG. 21 is a vertical cross-sectional view of an alternative embodiment of the first exemplary structure after formation of backside trenches and pillar cavities according to the first embodiment of the present disclosure.

[0044] FIG. 22A is a vertical cross-sectional view of the alternative embodiment of the first exemplary structure after formation of sacrificial backside trench fill structures and sacrificial pillar structures according to the first embodiment of the present disclosure.

[0045] FIG. 22B is a partial see-through top-down view of the first exemplary structure of FIG. 22A. The vertical plane A – A' is the plane of the schematic vertical cross-sectional view of FIG. 22A.

[0046] FIGS. 23A, 23B, 24A, 24B, 25A, 25B, 26A and 26B are sequential vertical cross-sectional view of a region of the alternative embodiment of the first exemplary structure during formation of memory opening fill structures at the steps that correspond to respective steps shown in FIGS. 9A – 9H according to the first embodiment of the present disclosure.

[0047] FIG. 27 is vertical cross-sectional view of a region of the alternative embodiment of the first exemplary structure at the step that corresponds to the step of FIG. 10A, according to the first embodiment of the present disclosure.

[0048] FIG. 28 is a vertical cross-sectional view of a second exemplary structure after formation of a vertical repetition of a unit layer stack according to a second embodiment of the present disclosure.

[0049] FIG. 29A is a schematic vertical cross-sectional view of the second exemplary structure after formation of memory openings and support openings according to the second embodiment of the present disclosure.

[0050] FIG. 29B is a top-down view of the first exemplary structure of FIG. 29A. The vertical plane A – A' is the plane of the cross-section for FIG. 29A.

[0051] FIG. 30 is a schematic vertical cross-sectional view of the second exemplary structure after laterally recessing the insulating layers selective to the sacrificial material layers according to the second embodiment of the present disclosure.

[0052] FIG. 31 is a schematic vertical cross-sectional view of the second exemplary structure after removal of the photoresist layer according to the second embodiment of the present disclosure.

[0053] FIG. 32 is a schematic vertical cross-sectional view of the second exemplary structure after formation of sacrificial memory opening fill structures and sacrificial support opening fill structures according to the second embodiment of the present disclosure.

[0054] FIG. 33A is a schematic vertical cross-sectional view of the second exemplary structure after formation of backside trenches according to the second embodiment of the present disclosure.

[0055] FIG. 33B is a top-down view of the second exemplary structure of FIG. 33A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 33A.

[0056] FIG. 34A is a schematic vertical cross-sectional view of the second exemplary structure after formation of sacrificial backside trench fill structures according to the second embodiment of the present disclosure.

[0057] FIG. 34B is a top-down view of the second exemplary structure of FIG. 34A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 34A.

[0058] FIG. 35A is a schematic vertical cross-sectional view of the second exemplary structure after formation of contact via cavities according to the second embodiment of the present disclosure.

[0059] FIG. 35B is a top-down view of the second exemplary structure of FIG. 35A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 35A.

[0060] FIG. 36 is a schematic vertical cross-sectional view of the second exemplary structure after formation of lateral recesses according to the second embodiment of the present disclosure.

[0061] FIG. 37 is a schematic vertical cross-sectional view of the second exemplary structure after formation of in-process electrically conductive layers according to the second embodiment of the present disclosure.

[0062] FIG. 38 is a schematic vertical cross-sectional view of the second exemplary structure after formation of insulating fill material layers and a sacrificial via fill material layer according to the second embodiment of the present disclosure.

[0063] FIG. 39 is a schematic vertical cross-sectional view of the second exemplary structure after a planarization process according to the second embodiment of the present disclosure.

[0064] FIG. 40 is a schematic vertical cross-sectional view of the second exemplary structure after removal of sacrificial backside trench fill structures according to the second embodiment of the present disclosure.

[0065] FIG. 41 is a schematic vertical cross-sectional view of the second exemplary structure after isotropically recessing the in-process electrically conductive layers around the backside trenches according to the second embodiment of the present disclosure.

[0066] FIG. 42A is a schematic vertical cross-sectional view of the second exemplary structure after formation of backside trench fill structures according to the second embodiment of the present disclosure.

[0067] FIG. 42B is a top-down view of the second exemplary structure of FIG. 42A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 42A.

[0068] FIG. 43 is a schematic vertical cross-sectional view of the second exemplary structure after removal of sacrificial memory opening fill structures and sacrificial support opening fill structures according to the second embodiment of the present disclosure.

[0069] FIG. 44 is a schematic vertical cross-sectional view of the second exemplary structure after isotropically etching the in-process electrically conductive layers according to the second embodiment of the present disclosure.

[0070] FIG. 45 is a schematic vertical cross-sectional view of the second exemplary structure after formation of memory opening fill structures according to the second embodiment of the present disclosure.

[0071] FIG. 46 is a schematic vertical cross-sectional view of the second exemplary structure after removal of sacrificial via fill material portions according to the second embodiment of the present disclosure.

[0072] FIG. 47 is a schematic vertical cross-sectional view of the second exemplary structure after isotropically recessing insulating fill material layers and in-process electrically conductive layers according to the second embodiment of the present disclosure.

[0073] FIG. 48 is a schematic vertical cross-sectional view of the second exemplary structure after anisotropically recessing the insulating fill material layers according to the second embodiment of the present disclosure.

[0074] FIG. 49 is a schematic vertical cross-sectional view of the second exemplary structure after formation of outer dielectric tubular spacers according to the second embodiment of the present disclosure.

[0075] FIG. 50 is a schematic vertical cross-sectional view of the second exemplary structure after formation of tubular contact via structures according to the second embodiment of the present disclosure.

[0076] FIG. 51 is a schematic vertical cross-sectional view of the second exemplary structure after anisotropically etching electrically conductive layers and insulating layers according to the second embodiment of the present disclosure.

[0077] FIG. 52A is a schematic vertical cross-sectional view of the second exemplary structure after formation of inner dielectric tubular spacers and cylindrical contact via structures according to the second embodiment of the present disclosure.

[0078] FIG. 52B is a top-down view of the second exemplary structure of FIG. 52A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 52A.

[0079] FIGS. 53A – 53F are schematic vertical cross-sectional view of an alternative embodiment of the second exemplary structure according to alternative configuration of the second embodiment.

[0080] FIG. 54A is a schematic vertical cross-sectional view of the third exemplary structure after formation of memory openings and support openings according to a third embodiment of the present disclosure.

[0081] FIG. 54B is a top-down view of the third exemplary structure of FIG. 54A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 54A.

[0082] FIG. 55 is a schematic vertical cross-sectional view of the third exemplary structure after formation of sacrificial memory opening fill structures and sacrificial support opening fill structures according to the third embodiment of the present disclosure.

[0083] FIG. 56A is a schematic vertical cross-sectional view of the third exemplary structure after formation of backside trenches according to the third embodiment of the present disclosure.

[0084] FIG. 56B is a top-down view of the third exemplary structure of FIG. 56A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 56A.

[0085] FIG. 57 is a schematic vertical cross-sectional view of the third exemplary structure after formation of lateral recesses according to the third embodiment of the present disclosure.

[0086] FIG. 58 is a schematic vertical cross-sectional view of the third exemplary structure after removing cylindrical regions of a first sacrificial fill material portion from each of the sacrificial memory opening fill structures and the sacrificial support opening fill structures according to the third embodiment of the present disclosure.

[0087] FIG. 59 is a schematic vertical cross-sectional view of the third exemplary structure after formation of an in-process electrically conductive layer according to the third embodiment of the present disclosure.

[0088] FIG. 60 is a schematic vertical cross-sectional view of the third exemplary structure after formation of an insulating fill material layer according to the third embodiment of the present disclosure.

[0089] FIG. 61 is a schematic vertical cross-sectional view of the third exemplary structure after formation of second-type insulating layers according to the third embodiment of the present disclosure.

[0090] FIG. 62 is a schematic vertical cross-sectional view of the third exemplary structure after isotropically recessing the in-process electrically conductive layer according to the third embodiment of the present disclosure.

[0091] FIG. 63 is a schematic vertical cross-sectional view of the third exemplary structure after formation of backside trench fill structures according to the third embodiment of the present disclosure.

[0092] FIG. 64 is a schematic vertical cross-sectional view of the third exemplary structure after removal of third sacrificial fill material portions from the sacrificial memory opening fill structures and the sacrificial support opening fill structures according to the third embodiment of the present disclosure.

[0093] FIG. 65 is a schematic vertical cross-sectional view of the third exemplary structure after removal of second sacrificial fill material portions from the sacrificial memory opening fill structures and the sacrificial support opening fill structures according to the third embodiment of the present disclosure.

[0094] FIG. 66 is schematic vertical cross-sectional view of the third exemplary structure after removal of first sacrificial fill material portions from the sacrificial memory opening fill structures and the sacrificial support opening fill structures according to the third embodiment of the present disclosure.

[0095] FIG. 67 is schematic vertical cross-sectional view of the third exemplary structure after removal of proximal portions of at least one conductive fill material from around the memory openings and the support openings according to the third embodiment of the present disclosure.

[0096] FIG. 68 is schematic vertical cross-sectional view of the third exemplary structure after formation of memory opening fill structures and support opening fill structures according to the third embodiment of the present disclosure.

[0097] FIG. 69 is a schematic vertical cross-sectional view of the third exemplary structure after removal of the sacrificial retro-stepped dielectric material portion according to the third embodiment of the present disclosure.

[0098] FIG. 70 is a schematic vertical cross-sectional view of the third exemplary structure after isotropic recessing of the in-process electrically conductive layers according to the third embodiment of the present disclosure.

[0099] FIG. 71A is a schematic vertical cross-sectional view of the third exemplary structure after formation of contact via structures according to the third embodiment of the present disclosure.

[0100] FIG. 71B is a top-down view of the third exemplary structure of FIG. 71A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 71A.

[0101] FIG. 72 is a schematic vertical cross-sectional view of an alternative configuration of the third exemplary structure according to the third embodiment of the present disclosure.

[0102] FIG. 73 is a schematic vertical cross-sectional view of a fourth exemplary structure after formation of a vertical repetition of a unit layer stack according to the fourth embodiment of the present disclosure.

[0103] FIG. 74 is a schematic vertical cross-sectional view of the fourth exemplary structure after formation of stepped terraces and a sacrificial retro-stepped dielectric material portion according to the fourth embodiment of the present disclosure.

[0104] FIG. 75A is a schematic vertical cross-sectional view of the fourth exemplary structure after formation of memory openings and support openings according to the fourth embodiment of the present disclosure.

[0105] FIG. 75B is a top-down view of the fourth exemplary structure of FIG. 75A. The vertical plane A – A' is the plane of the cross-section for FIG. 75A.

[0106] FIGS. 76A – 76H are sequential vertical cross-sectional views of a region between a memory opening and a sacrificial backside trench fill structure during formation of memory opening fill structures according to the fourth embodiment of the present disclosure.

[0107] FIG. 77 is a vertical cross-sectional view of the fourth exemplary structure after formation of memory opening fill structures and support pillar structures according to the fourth embodiment of the present disclosure.

[0108] FIG. 78A is a schematic vertical cross-sectional view of the fourth exemplary structure after formation of backside trenches and source regions according to the fourth embodiment of the present disclosure.

[0109] FIG. 78B is a top-down view of the fourth exemplary structure of FIG. 78A. The vertical plane A – A' is the plane of the cross-section for FIG. 78A.

[0110] FIG. 79A is a schematic vertical cross-sectional view of the fourth exemplary structure after formation of backside recesses according to the fourth embodiment of the present disclosure.

[0111] FIG. 79B is a magnified view of a region of the fourth exemplary structure of FIG. 79A.

[0112] FIGS. 80A – 80D are sequential vertical cross-sectional views of a region around a memory opening and a backside trench during formation of electrically conductive layers

and cavity-containing insulating layers according to the fourth embodiment of the present disclosure.

[0113] FIG. 81A is a schematic vertical cross-sectional view of the fourth exemplary structure after formation of backside trench fill structures according to the fourth embodiment of the present disclosure.

[0114] FIG. 81B is a magnified view of a region of the fourth exemplary structure of FIG. 81A.

[0115] FIG. 82A is a vertical cross-sectional view of the fourth exemplary structure after application and patterning of a photoresist layer and an anisotropic etch process according to the fourth embodiment of the present disclosure.

[0116] FIG. 82B is a partial see-through top-down view of the fourth exemplary structure of FIG. 82A. The vertical plane A – A' is the plane of the schematic vertical cross-sectional view of FIG. 82A.

[0117] FIG. 82C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 82B.

[0118] FIG. 83 is a schematic vertical cross-sectional view of a fifth exemplary structure after formation of a vertical repetition of a unit layer stack according to the fifth embodiment of the present disclosure.

[0119] FIG. 84 is a schematic vertical cross-sectional view of the fifth exemplary structure after formation of stepped terraces and a sacrificial retro-stepped dielectric material portion according to the fifth embodiment of the present disclosure.

[0120] FIG. 85A is a schematic vertical cross-sectional view of the fifth exemplary structure after formation of memory openings and support openings according to the fifth embodiment of the present disclosure.

[0121] FIG. 85B is a top-down view of the fifth exemplary structure of FIG. 85A. The vertical plane A – A' is the plane of the cross-section for FIG. 85A.

[0122] FIGS. 86A – 86H are sequential vertical cross-sectional views of a region between a memory opening and a sacrificial backside trench fill structure during formation of memory opening fill structures according to the fifth embodiment of the present disclosure.

[0123] FIG. 87 is a vertical cross-sectional view of the fifth exemplary structure after formation of memory opening fill structures and support pillar structures according to the fifth embodiment of the present disclosure.

[0124] FIG. 88A is a schematic vertical cross-sectional view of the fifth exemplary structure after formation of backside trenches and source regions according to the fifth embodiment of the present disclosure.

[0125] FIG. 88B is a top-down view of the fifth exemplary structure of FIG. 88A. The vertical plane A – A' is the plane of the cross-section for FIG. 88A.

[0126] FIG. 89A is a schematic vertical cross-sectional view of the fifth exemplary structure after formation of backside recesses according to the fifth embodiment of the present disclosure.

[0127] FIG. 89B is a magnified view of a region of the fifth exemplary structure of FIG. 89A.

[0128] FIGS. 90A – 90E are sequential vertical cross-sectional views of a region around a memory opening and a backside trench during formation of electrically conductive layers and cavity-containing insulating layers according to the fifth embodiment of the present disclosure.

[0129] FIG. 91A is a vertical cross-sectional view of the fifth exemplary structure after application and patterning of a photoresist layer and an anisotropic etch process according to the fifth embodiment of the present disclosure.

[0130] FIG. 91B is a partial see-through top-down view of the fifth exemplary structure of FIG. 91A. The vertical plane A – A' is the plane of the schematic vertical cross-sectional view of FIG. 91A.

[0131] FIG. 91C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 91B.

[0132] FIGS. 92A and 92B are sequential vertical cross-sectional views of a region around a memory opening and a backside trench during formation of electrically conductive layers and cavity-containing insulating layers in an alternative embodiment of the fifth exemplary structure according to the fifth embodiment of the present disclosure.

[0133] FIG. 93A is a vertical cross-sectional view of the alternative embodiment of the fifth exemplary structure after application and patterning of a photoresist layer and an anisotropic etch process according to the fifth embodiment of the present disclosure.

[0134] FIG. 93B is a partial see-through top-down view of the fifth exemplary structure of FIG. 93A. The vertical plane A – A' is the plane of the schematic vertical cross-sectional view of FIG. 93A.

[0135] FIG. 93C is a vertical cross-sectional view along the vertical plane C – C' of FIG. 93B.

DETAILED DESCRIPTION

[0136] As discussed above, the embodiments of the present disclosure are directed to three-dimensional memory devices and methods of making thereof using double pitch word

line formation, the various aspects of which are described below. The sacrificial material layers are thicker than insulating layers in the stack of sacrificial material layers and insulating layers. When the sacrificial layers are removed from the stack, the resulting recesses are wider than if the sacrificial material layers had the same thickness as the insulating layers. Therefore, it is easier to deposit word lines into the wider recesses. Two word lines may be deposited into each recess followed by depositing an insulating layer into the gap between the word lines. Thus, the double pitch word line formation with the wider recesses may reduce or overcome material clogging in the recesses between memory openings which leads to incomplete filling of the recesses by the word lines, without increasing the total height of the stack.

[0137] The embodiments of the disclosure can be employed to form various structures including a multilevel memory structure, non-limiting examples of which include semiconductor devices such as three-dimensional memory array devices comprising a plurality of NAND memory strings.

[0138] The drawings are not drawn to scale. Multiple instances of an element may be duplicated where a single instance of the element is illustrated, unless absence of duplication of elements is expressly described or clearly indicated otherwise. Ordinals such as “first,” “second,” and “third” are employed merely to identify similar elements, and different ordinals may be employed across the specification and the claims of the instant disclosure. The term “at least one” element refers to all possibilities including the possibility of a single element and the possibility of multiple elements.

[0139] The same reference numerals refer to the same element or similar element. Unless otherwise indicated, elements having the same reference numerals are presumed to have the same composition and the same function. Unless otherwise indicated, a “contact” between

elements refers to a direct contact between elements that provides an edge or a surface shared by the elements. If two or more elements are not in direct contact with each other or among one another, the two elements are “disjoined from” each other or “disjoined among” one another. As used herein, a first element located “on” a second element can be located on the exterior side of a surface of the second element or on the interior side of the second element. As used herein, a first element is located “directly on” a second element if there exist a physical contact between a surface of the first element and a surface of the second element. As used herein, a first element is “electrically connected to” a second element if there exists a conductive path consisting of at least one conductive material between the first element and the second element. As used herein, a “prototype” structure or an “in-process” structure refers to a transient structure that is subsequently modified in the shape or composition of at least one component therein.

[0140] As used herein, a “layer” refers to a material portion including a region having a thickness. A layer may extend over the entirety of an underlying or overlying structure, or may have an extent less than the extent of an underlying or overlying structure. Further, a layer may be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer may be located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer may extend horizontally, vertically, and/or along a tapered surface. A substrate may be a layer, may include one or more layers therein, or may have one or more layer thereupon, thereabove, and/or therebelow.

[0141] Generally, a semiconductor die, or a semiconductor package, can include a memory chip. Each semiconductor package contains one or more dies (for example one, two, or four). The die is the smallest unit that can independently execute commands or report

status. Each die contains one or more planes (typically one or two). Identical, concurrent operations can take place on each plane, although with some restrictions. Each plane contains a number of blocks, which are the smallest unit that can be erased by in a single erase operation. Each block contains a number of pages, which are the smallest unit that can be programmed, i.e., a smallest unit on which a read operation can be performed.

[0142] Referring to FIG. 1, a first exemplary structure according to a first embodiment of the present disclosure is illustrated, which can be employed, for example, to fabricate a device structure containing vertical NAND memory devices. The exemplary structure includes a substrate (9, 10), which can be a semiconductor substrate. The substrate can include a substrate semiconductor layer 9 and an optional semiconductor material layer 10. The substrate semiconductor layer 9 maybe a semiconductor wafer or a semiconductor material layer, and can include at least one elemental semiconductor material (e.g., single crystal silicon wafer or layer), at least one III-V compound semiconductor material, at least one II-VI compound semiconductor material, at least one organic semiconductor material, or other semiconductor materials known in the art. The substrate can have a major surface 7, which can be, for example, a topmost surface of the substrate semiconductor layer 9. The major surface 7 can be a semiconductor surface. In one embodiment, the major surface 7 can be a single crystalline semiconductor surface, such as a single crystalline semiconductor surface.

[0143] As used herein, a “semiconducting material” refers to a material having electrical conductivity in the range from 1.0×10^{-6} S/cm to 1.0×10^5 S/cm. As used herein, a “semiconductor material” refers to a material having electrical conductivity in the range from 1.0×10^{-6} S/cm to 1.0×10^5 S/cm in the absence of electrical dopants therein, and is capable of producing a doped material having electrical conductivity in a range from 1.0 S/cm to 1.0

$\times 10^5$ S/cm upon suitable doping with an electrical dopant. As used herein, an “electrical dopant” refers to a p-type dopant that adds a hole to a valence band within a band structure, or an n-type dopant that adds an electron to a conduction band within a band structure. As used herein, a “conductive material” refers to a material having electrical conductivity greater than 1.0×10^5 S/cm. As used herein, an “insulator material” or a “dielectric material” refers to a material having electrical conductivity less than 1.0×10^{-6} S/cm. As used herein, a “heavily doped semiconductor material” refers to a semiconductor material that is doped with electrical dopant at a sufficiently high atomic concentration to become a conductive material either as formed as a crystalline material or if converted into a crystalline material through an anneal process (for example, from an initial amorphous state), i.e., to have electrical conductivity greater than 1.0×10^5 S/cm. A “doped semiconductor material” may be a heavily doped semiconductor material, or may be a semiconductor material that includes electrical dopants (i.e., p-type dopants and/or n-type dopants) at a concentration that provides electrical conductivity in the range from 1.0×10^{-6} S/cm to 1.0×10^5 S/cm. An “intrinsic semiconductor material” refers to a semiconductor material that is not doped with electrical dopants. Thus, a semiconductor material may be semiconducting or conductive, and may be an intrinsic semiconductor material or a doped semiconductor material. A doped semiconductor material can be semiconducting or conductive depending on the atomic concentration of electrical dopants therein. As used herein, a “conductive material” refers to a conductive material including at least one conductive element therein. All measurements for electrical conductivities are made at the standard condition.

[0144] At least one semiconductor device 700 for a peripheral circuitry can be formed on a portion of the substrate semiconductor layer 9. The at least one semiconductor device can include, for example, field effect transistors. For example, at least one shallow trench

isolation structure 720 can be formed by etching portions of the substrate semiconductor layer 9 and depositing a dielectric material therein. A gate dielectric layer, at least one gate conductor layer, and a gate cap dielectric layer can be formed over the substrate semiconductor layer 9, and can be subsequently patterned to form at least one gate structure (750, 752, 754, 758), each of which can include a gate dielectric 750, a gate electrode (752, 754), and a gate cap dielectric 758. The gate electrode (752, 754) may include a stack of a first gate electrode portion 752 and a second gate electrode portion 754. At least one gate spacer 756 can be formed around the at least one gate structure (750, 752, 754, 758) by depositing and anisotropically etching a dielectric liner. Active regions 730 can be formed in upper portions of the substrate semiconductor layer 9, for example, by introducing electrical dopants employing the at least one gate structure (750, 752, 754, 758) as masking structures. Additional masks may be employed as needed. The active region 730 can include source regions and drain regions of field effect transistors. A first dielectric liner 761 and a second dielectric liner 762 can be optionally formed. Each of the first and second dielectric liners (761, 762) can comprise a silicon oxide layer, a silicon nitride layer, and/or a dielectric metal oxide layer. As used herein, silicon oxide includes silicon dioxide as well as non-stoichiometric silicon oxides having more or less than two oxygen atoms for each silicon atoms. Silicon dioxide is preferred. In an illustrative example, the first dielectric liner 761 can be a silicon oxide layer, and the second dielectric liner 762 can be a silicon nitride layer. The least one semiconductor device for the peripheral circuitry can contain a driver circuit for memory devices to be subsequently formed, which can include at least one NAND device.

[0145] A dielectric material such as silicon oxide can be deposited over the at least one semiconductor device, and can be subsequently planarized to form a planarization dielectric layer 770. In one embodiment the planarized top surface of the planarization dielectric layer

770 can be coplanar with a top surface of the dielectric liners (761, 762). Subsequently, the planarization dielectric layer 770 and the dielectric liners (761, 762) can be removed from an area to physically expose a top surface of the substrate semiconductor layer 9. As used herein, a surface is “physically exposed” if the surface is in physical contact with vacuum, or a gas phase material (such as air).

[0146] The optional semiconductor material layer 10, if present, can be formed on the top surface of the substrate semiconductor layer 9 prior to, or after, formation of the at least one semiconductor device 700 by deposition of a single crystalline semiconductor material, for example, by selective epitaxy. The deposited semiconductor material can be the same as, or can be different from, the semiconductor material of the substrate semiconductor layer 9. The deposited semiconductor material can be any material that can be employed for the semiconductor substrate layer 9 as described above. The single crystalline semiconductor material of the semiconductor material layer 10 can be in epitaxial alignment with the single crystalline structure of the substrate semiconductor layer 9. Portions of the deposited semiconductor material located above the top surface of the planarization dielectric layer 170 can be removed, for example, by chemical mechanical planarization (CMP). In this case, the semiconductor material layer 10 can have a top surface that is coplanar with the top surface of the planarization dielectric layer 770.

[0147] The region (i.e., area) of the at least one semiconductor device 700 is herein referred to as a peripheral device region 200. The region in which a memory array is subsequently formed is herein referred to as a memory array region 100. A contact region 300 for subsequently forming stepped terraces of electrically conductive layers can be provided between the memory array region 100 and the peripheral device region 200.

[0148] In one alternative embodiment, the peripheral device region 200 containing the at

least one semiconductor device 700 for a peripheral circuitry may be located under the memory array region 100 in a CMOS under array configuration. In another alternative embodiment, the peripheral device region 200 may be located on a separate substrate which is subsequently bonded to the memory array region 100.

[0149] Referring to FIG. 2, a vertical repetition of a unit layer stack (32, 42) can be formed over the semiconductor material layer 10. Multiple instances of the unit layer stack (32, 42) are repeated along the vertical direction. In one embodiment, the vertical repetition of the unit layer stack (32, 42) may comprise a periodic vertical repetition along the vertical direction, in which each unit layer stack (32, 42) has a same structure and a same set of material compositions. In one embodiment, each instance of the unit layer stack (32, 42) may include a first-type insulating layer 32 and a sacrificial material layer 42.

[0150] The first-type insulating layer 32 is an insulating layer that includes, and/or consists essentially of, a first insulating material such as undoped silicate glass (i.e., silicon oxide). The first-type insulating layer 32 can be free of any seam therein. The first-type insulating layers 32 may be deposited, for example, by chemical vapor deposition. The thickness of each first-type insulating layer 32 can be in a range from 15 nm to 50 nm, although lesser and greater thicknesses may also be employed.

[0151] The sacrificial material layers 42 includes a sacrificial material that can be removed selective to the material of the first-type insulating layers 32. For example, the sacrificial material layers 42 can include silicon nitride. The sacrificial material layers 42 may be deposited, for example, by chemical vapor deposition. The thickness of each sacrificial material layer 42 can be in a range from 45 nm to 150 nm, although lesser and greater thicknesses may also be employed. Generally, the thickness of the sacrificial material

layers 42 may be greater than the thickness of insulating layers 32 by a factor in a range from 2 to 6.

[0152] The total number of repetitions of a pair of a first-type insulating layer 32 and a sacrificial material layer 42 can be in a range from 8 to 1,024, such as from 64 to 256, although lesser and greater total number of repetitions may also be employed. A topmost first-type insulating layer 32 may be formed at the top of the vertically repetition of the first-type insulating layers 32 and the sacrificial material layers 42. Generally, a vertical repetition of multiple instances of a unit layer stack (32, 42) can be formed over a substrate (9, 10). The unit layer stack (32, 42) comprises a first-type insulating layer 32 and a sacrificial material layer 42.

[0153] Referring to FIG. 3, stepped surfaces can be formed in the contact region 300. As used herein, “stepped surfaces” refer to a set of surfaces that include at least two horizontal surfaces and at least two vertical surfaces such that each horizontal surface is adjoined to a first vertical surface that extends upward from a first edge of the horizontal surface, and is adjoined to a second vertical surface that extends downward from a second edge of the horizontal surface. A stepped cavity is formed within the volume from which portions of the vertical repetition (32, 42) are removed through formation of the stepped surfaces. A “stepped cavity” refers to a cavity having stepped surfaces.

[0154] The contact region 300 can be located between the memory array region 100 and the peripheral device region 200 containing the at least one semiconductor device for the peripheral circuitry. The stepped cavity can have various stepped surfaces such that the horizontal cross-sectional shape of the stepped cavity changes in steps as a function of the vertical distance from the top surface of the substrate (9, 10). In one embodiment, the stepped cavity can be formed by repetitively performing a set of processing steps. The set of

processing steps can include, for example, an etch process of a first type that vertically increases the depth of a cavity by one or more levels, and an etch process of a second type that laterally expands the area to be vertically etched in a subsequent etch process of the first type. As used herein, a “level” of a structure including alternating plurality is defined as the relative position of a pair of a first material layer and a second material layer within the structure.

[0155] Each sacrificial material layer 42 other than a topmost sacrificial material layer 42 within the vertical repetition (32, 42) laterally extends farther than any overlying sacrificial material layer 42 within the vertical repetition (32, 42) in the terrace region. The terrace region includes stepped surfaces of the vertical repetition (32, 42) that continuously extend from a bottommost layer within the vertical repetition (32, 42) to a topmost layer within the vertical repetition (32, 42).

[0156] Each vertical step of the stepped surfaces can have the height of one or more pairs of an insulating layer 32 and a sacrificial material layer. In one embodiment, each vertical step can have the height of a single pair of an insulating layer 32 and a sacrificial material layer 42. In another embodiment, multiple “columns” of staircases can be formed along a first horizontal direction $hd1$ such that each vertical step has the height of a plurality of pairs of an insulating layer 32 and a sacrificial material layer 42, and the number of columns can be at least the number of the plurality of pairs. Each column of staircase can be vertically offset among one another such that each of the sacrificial material layers 42 has a physically exposed top surface in a respective column of staircases. In the illustrative example, two columns of staircases are formed for each block of memory stack structures to be subsequently formed such that one column of staircases provide physically exposed top surfaces for odd-numbered sacrificial material layers 42 (as counted from the bottom) and

another column of staircases provide physically exposed top surfaces for even-numbered sacrificial material layers (as counted from the bottom). Configurations employing three, four, or more columns of staircases with a respective set of vertical offsets among the physically exposed surfaces of the sacrificial material layers 42 may also be employed. Each sacrificial material layer 42 has a greater lateral extent, at least along one direction, than any overlying sacrificial material layers 42 such that each physically exposed surface of any sacrificial material layer 42 does not have an overhang. In one embodiment, the vertical steps within each column of staircases may be arranged along the first horizontal direction hd1, and the columns of staircases may be arranged along a second horizontal direction hd2 that is perpendicular to the first horizontal direction hd1. In one embodiment, the first horizontal direction hd1 may be perpendicular to the boundary between the memory array region 100 and the contact region 300.

[0157] A sacrificial retro-stepped dielectric material portion 67 (i.e., an insulating fill material portion) can be formed in the stepped cavity by deposition of a sacrificial material that can provide an etch rate that is at least 100 times the etch rate of the first-type insulating layers 32. For example, if the first-type insulating layers 32 include undoped silicate glass, then organosilicate glass or borosilicate glass that provide an etch rate in dilute hydrofluoric acid that is at least 100 times the etch rate of undoped silicate glass in dilute hydrofluoric acid can be employed as the material of the sacrificial retro-stepped dielectric material portion 67. Excess portions of the deposited dielectric material can be removed from above the top surface of the topmost first-type insulating layer 32, for example, by chemical mechanical planarization (CMP). The remaining portion of the deposited dielectric material filling the stepped cavity constitutes the sacrificial retro-stepped dielectric material portion 67. As used herein, a “retro-stepped” element refers to an element that has stepped surfaces and a

horizontal cross-sectional area that increases monotonically as a function of a vertical distance from a top surface of a substrate on which the element is present.

[0158] Generally, stepped surfaces can be formed by patterning the vertical repetition in a staircase region which is located in the contact region 300. The stepped surfaces comprise vertically-extending surfaces including a sidewall of a respective instance of the unit layer stack (32, 42) that extends vertically from a bottommost surface of the respective instance of the unit layer stack (32, 42), such as a bottom surface of a first-type insulating layer 32, to a topmost surface of the respective instance of the unit layer stack (32, 42), such as a top surface of a sacrificial material layer 42. A sacrificial retro-stepped dielectric material portion 67 is formed over the stepped surfaces.

[0159] Referring to FIGS. 4A and 4B, a lithographic material stack (not shown) including at least a photoresist layer can be formed over the topmost first-type insulating layer 32 and the sacrificial retro-stepped dielectric material portion 67, and can be lithographically patterned to form openings therein. The openings include a first set of openings formed over the memory array region 100 and a second set of openings formed over the contact region 300. The pattern in the lithographic material stack can be transferred through the topmost first-type insulating layer 32 or the sacrificial retro-stepped dielectric material portion 67, and through the vertical repetition (32, 42) by at least one anisotropic etch that employs the patterned lithographic material stack as an etch mask. Portions of the vertical repetition (32, 42) underlying the openings in the patterned lithographic material stack are etched to form memory openings 49 and support openings 19. As used herein, a “memory opening” refers to a structure in which memory elements, such as a memory stack structure, is subsequently formed. As used herein, a “support opening” refers to a structure in which a support structure (such as a support pillar structure) that mechanically supports other elements is subsequently

formed. The memory openings 49 are formed through the topmost first-type insulating layer 32 and the entirety of the vertical repetition (32, 42) in the memory array region 100. The support openings 19 are formed through the sacrificial retro-stepped dielectric material portion 67 and the portion of the vertical repetition (32, 42) that underlie the stepped surfaces in the contact region 300.

[0160] The memory openings 49 extend through the entirety of the vertical repetition (32, 42). The support openings 19 extend through a subset of layers within the vertical repetition (32, 42). The chemistry of the anisotropic etch process employed to etch through the materials of the vertical repetition (32, 42) can alternate to optimize etching of the first and second materials in the vertical repetition (32, 42). The anisotropic etch can be, for example, a series of reactive ion etches. The sidewalls of the memory openings 49 and the support openings 19 can be substantially vertical, or can be tapered. The patterned lithographic material stack can be subsequently removed, for example, by ashing.

[0161] The memory openings 49 and the support openings 19 can extend from the top surface of the vertical repetition (32, 42) to at least the horizontal plane including the topmost surface of the semiconductor material layer 10. In one embodiment, an overetch into the semiconductor material layer 10 may be optionally performed after the top surface of the semiconductor material layer 10 is physically exposed at a bottom of each memory opening 49 and each support opening 19. The overetch may be performed prior to, or after, removal of the lithographic material stack. In other words, the recessed surfaces of the semiconductor material layer 10 may be vertically offset from the un-recessed top surfaces of the semiconductor material layer 10 by a recess depth. The recess depth can be, for example, in a range from 1 nm to 50 nm, although lesser and greater recess depths can also be employed. The overetch is optional, and may be omitted. If the overetch is not performed, the bottom

surfaces of the memory openings 49 and the support openings 19 can be coplanar with the topmost surface of the semiconductor material layer 10.

[0162] Each of the memory openings 49 and the support openings 19 may include a sidewall (or a plurality of sidewalls) that extends substantially perpendicular to the topmost surface of the substrate. A two-dimensional array of memory openings 49 can be formed in the memory array region 100. A two-dimensional array of support openings 19 can be formed in the contact region 300. The substrate semiconductor layer 9 and the semiconductor material layer 10 collectively constitutes a substrate (9, 10), which can be a semiconductor substrate. Alternatively, the semiconductor material layer 10 may be omitted, and the memory openings 49 and the support openings 19 can be extend to a top surface of the substrate semiconductor layer 9.

[0163] Referring to FIG. 5, a first sacrificial fill material that is different from the materials of the first-type insulating layers 32 and the sacrificial material layers 42 can be deposited in the memory openings 49 and the support openings 19. The first sacrificial fill material may include, for example, amorphous silicon, amorphous carbon, diamond-like carbon, germanium, or silicon-germanium. Excess portions of the first sacrificial fill material can be removed from the horizontal plane including the top surface of the topmost first-type insulating layer 32. Each remaining portion of the first sacrificial fill material located in a memory opening 49 constitutes a sacrificial memory opening fill structure 48. Each remaining portion of the first sacrificial fill material located in a support opening 19 constitutes a sacrificial support opening fill structure 18.

[0164] Referring to FIGS. 6A and 6B, a photoresist layer (not shown) can be applied over the vertical repetition (32, 42), the sacrificial retro-stepped dielectric material portion 67, the sacrificial memory opening fill structures 48, and the sacrificial support opening fill

structures 18, and can be lithographically patterned to form elongated openings in areas between clusters of the sacrificial memory opening fill structures 48. The pattern in the photoresist layer can be transferred through vertical repetition (32, 42) and/or the sacrificial retro-stepped dielectric material portion 67 employing an anisotropic etch to form backside trenches 79, which vertically extend from the top surface of the topmost first-type insulating layer 32 at least to the top surface of the substrate (9, 10), and laterally extend through the memory array region 100 and the contact region 300.

[0165] In one embodiment, the backside trenches 79 can laterally extend along a first horizontal direction (e.g., word line direction) hd1 and can be laterally spaced apart from each other along a second horizontal direction (e.g., bit line direction) hd2 that is perpendicular to the first horizontal direction hd1. The sacrificial memory opening fill structures 58 can be arranged in rows that extend along the first horizontal direction hd1. Each backside trench 79 can have a uniform width that is invariant along the lengthwise direction (i.e., along the first horizontal direction hd1). Multiple rows of sacrificial memory opening fill structures 48 can be located between a neighboring pair of backside trenches 79. The photoresist layer can be removed, for example, by ashing.

[0166] An optional source region 61 can be formed at a surface portion of the semiconductor material layer 10 under each backside trench 79 by implantation of electrical dopants into physically exposed surface portions of the semiconductor material layer 10. In one embodiment, the semiconductor material layer 10 may have a doping of the first conductivity type, and the source regions 61 may have a doping of a second conductivity type that is the opposite of the first conductivity type. A horizontal semiconductor channel 59 can be formed between each source region 61 and bottom surfaces of an adjacent set of sacrificial memory opening fill structures 48.

[0167] Referring to FIGS. 7A and 7B, an optional etch-stop spacer 75 may be formed at the periphery of each backside trench 79 by conformally depositing and anisotropically etching an etch-stop material. The etch-stop material comprises a material that is different from the material of the sacrificial material layers 42. For example, the optional etch stop spacer 75 may include silicon oxide. The thickness of each etch-stop spacer 75, as measured between an inner sidewall and an outer sidewall, can be in a range from 5 nm to 100 nm, such as from 10 nm to 50 nm, although lesser and greater thicknesses may also be employed.

[0168] A second sacrificial fill material can be deposited in remaining volumes of the backside trenches 79. The second sacrificial fill material can include any material that may be employed for the first sacrificial fill material. The second sacrificial fill material is preferably different from the first sacrificial fill material of the sacrificial memory opening fill structures 48 and the sacrificial support opening fill structure 18. Excess portions of the second sacrificial fill material can be removed from above the horizontal plane including the top surface of the topmost first-type insulating layers 32 by a planarization process, which may employ a chemical mechanical polishing (CMP) process and/or a recess etch process. Each remaining portion of the second sacrificial fill material located within a respective one of the backside trenches 79 constitutes a sacrificial trench fill material portion 77. In one embodiment, the sacrificial trench fill material portion 77 may comprise a carbon material. The optional etch-stop spacer 75 and the sacrificial trench fill material portion 77 located within a backside trench 79 are collectively referred to as a sacrificial backside trench fill structure (75, 77).

[0169] Referring to FIG. 8, the first sacrificial fill material of the sacrificial memory opening fill structures 48 and the sacrificial support opening fill structures 18 can be removed selective to the materials of the first-type insulating layers 32, the sacrificial material layers

42, and the sacrificial retro-stepped dielectric material portion 67. In case the first sacrificial fill material is different from the second sacrificial fill material, the first sacrificial fill material can be removed selective to the second sacrificial fill material. For example, if the first sacrificial fill material comprises amorphous silicon or silicon-germanium, then a wet etch process using hot trimethyl-2 hydroxyethyl ammonium hydroxide (“hot TMY”) or tetramethyl ammonium hydroxide (TMAH) may be used to remove the sacrificial memory opening fill structures 48 and the sacrificial support opening fill structures 18. Voids are formed within the volumes of the memory openings 49 and the support openings 19.

[0170] FIGS. 9A – 9J are sequential vertical cross-sectional views of a region between a memory opening 49 and a sacrificial backside trench fill structure (75, 77) during formation of in-process electrically conductive layers (44, 45’) according to the first embodiment of the present disclosure.

[0171] Referring to FIG. 9A, the region between the memory opening 49 and the sacrificial backside trench fill structure (75, 77) is illustrated at the processing steps of FIG. 8.

[0172] Referring to FIG. 9B, the sacrificial material layers 42 can be removed selective to the first-type insulating layers 32 by introducing an isotropic etchant that etches the material of the sacrificial material layers 42 selective to the material of the first-type insulating layers into the memory openings 49 and the support openings 19. Lateral recesses 43 are formed in volumes from which the sacrificial material layers 42 are removed. The removal of the second material of the sacrificial material layers 42 can be selective to the first material of the first-type insulating layers 32, the material of the sacrificial retro-stepped dielectric material portion 67, the semiconductor material of the semiconductor material layer 10, and the material of the optional etch-stop spacers 75 or the material of the sacrificial trench fill material portions 77. In one embodiment, the sacrificial material layers 42 can include

silicon nitride, and the materials of the first-type insulating layers 32 and the sacrificial retro-stepped dielectric material portion 67 can be selected from silicon oxide and dielectric metal oxides.

[0173] In an illustrative example, if the sacrificial material layers 42 include silicon nitride, then the etch process can be a wet etch process in which the exemplary structure is immersed within a wet etch tank including phosphoric acid, which etches silicon nitride selective to silicon oxide, silicon, and various other materials employed in the art. The sacrificial backside trench fill structures (75, 77) and the sacrificial retro-stepped dielectric material portion 67 provide structural support while the lateral recesses 43 are present within volumes previously occupied by the sacrificial material layers 42.

[0174] Each lateral recess 43 can be a laterally extending cavity having a lateral dimension that is greater than the vertical extent of the cavity. In other words, the lateral dimension of each lateral recess 43 can be greater than the height of the lateral recess 43. A plurality of lateral recesses 43 can be formed in the volumes from which the second material of the sacrificial material layers 42 is removed. Each of the plurality of lateral recesses 43 can extend substantially parallel to the top surface of the substrate (9, 10). A lateral recess 43 can be vertically bounded by a top surface of an underlying first-type insulating layer 32 and a bottom surface of an overlying first-type insulating layer 32. In one embodiment, each lateral recess 43 can have a uniform height throughout.

[0175] Referring to FIG. 9C, a liner 44 is formed at peripheral portions of the lateral recesses 43 by a conformal deposition method, such as area selective deposition (ASD). In one embodiment, the at least one electrically conductive material is deposited directly on physically exposed surfaces of instances of the first-type insulating layer 32 and on physically exposed sidewalls of the sacrificial backside trench fill structures (75, 77) to form

a conductive barrier liner 44. The conductive barrier liner 44 includes a metal or metal nitride conductive barrier material such as TiN, TaN, WN, MoN or Ru. Alternatively, the liner 44 may comprise a sacrificial liner, such as an amorphous silicon, which can be used as a sacrificial nucleation layer for deposition of tungsten word lines in a subsequent step. The thickness of the liner 44 may be in a range from 1 nm to 10 nm, such as from 1 nm to 5 nm, although lesser and greater thicknesses may also be employed.

[0176] Referring to FIG. 9D, a sacrificial masking material layer 41L may be deposited by a conformal deposition process within the lateral recesses 43. For example, a semiconductor material, such as amorphous silicon, germanium or silicon-germanium, or an insulating material, such as amorphous carbon or diamond-like carbon, or a conductive material, such as titanium nitride, may be deposited in the lateral recesses 43. For example, if the liner 44 comprises TiN or Ru, then layer 41L may comprise amorphous silicon. If the liner 44 comprises MoN, then layer 41L may comprise amorphous silicon or TiN. If the liner 44 comprises amorphous silicon, then layer 41L may comprise TiN. A memory cavity 49' may be present within a center portion of each memory opening 49 after deposition of the sacrificial masking material layer 41L.

[0177] Referring to FIG. 9E, the sacrificial masking material layer 41L can be recessed within each memory opening 49 and within each support opening, for example, employing an isotropic etch process or a combination of anisotropic and isotropic etch processes. Each remaining portion of the sacrificial masking material layer 41L constitutes a sacrificial masking material portion 41, which may have sidewalls that are laterally recessed outward from the sidewall of each memory opening 49 and from the sidewall of each support opening 19.

[0178] Referring to FIG. 9F, a selective etch process may be performed to remove physically exposed portions of the liner 44. Portions of the liner 44 overlying sidewalls of the first-type insulating layers 32 can be removed from around each of the memory openings 49 and from around each of the support openings 19. The liner 44 can be divided into a plurality of liners 44 located at a respective level of the sacrificial masking material portions 41.

[0179] Referring to FIG. 9G, the sacrificial masking material portions 41 can be removed selective to the liners 44 and the first-type insulating layers 32 by a selective etch process. For example, if the sacrificial masking material portions 41 include amorphous silicon and the liners 44 include TiN or MoN, then a wet etch process employing hot trimethyl-2 hydroxyethyl ammonium hydroxide (“hot TMY”) or tetramethyl ammonium hydroxide (TMAH) may be used to remove the sacrificial masking material portions 41.

[0180] Referring to FIG. 9H, a selective conductive material deposition process may be performed to grow a conductive fill material layer 45' directly from physically exposed surfaces of the liners 44. In one embodiment, a chemical vapor deposition process or an atomic layer deposition process employing a metal-containing precursor gas can be performed to selectively grow the conductive fill material layer 45' from each physically exposed surface of the liners 44. The conductive fill material layer 45' includes at least one conductive material such as W, Co, Ru, Mo, Cu, Al, etc. If the liners 44 comprise conductive barrier liners (e.g., metal nitride liners, such as TiN or MoN), then the liners 44 are retained in the exemplary structure. Alternatively, if the liners 44 comprise sacrificial liners, such as amorphous silicon, then they are consumed during the deposition of the conductive fill material, such as tungsten. In one embodiment, the liners 44 comprise TiN or Ru and the conductive fill material comprises W. In another embodiment, the liners 44 comprise MoN

and the conductive fill material comprises Mo. In another embodiment, the liners 44 comprise amorphous silicon sacrificial liners and the conductive fill material comprises W. In one embodiment, the thickness of each conductive fill material layer 45' can be in a range from 20 % to 45 %, such as from 25 % to 35 %, of the thickness of the sacrificial material layers 42. In one embodiment, the conductive fill material layer 45' may have a thickness that is about the same as the lateral recess distance of the liners 44 from the memory openings 49 and from the support openings 19. Lateral cavities 43' are present within volumes of the lateral recesses 43 that are not filled by the conductive fill material layers 45'.

[0181] Referring to FIG. 9I, an insulating fill material can be deposited over the at least one conductive fill material (44, 45') within remaining volumes of the lateral recesses 43 by a conformal deposition process. The insulating fill material includes an insulating material such as undoped silicate glass (i.e., silicon oxide) or a doped silicate glass. The thickness of the insulating fill material can be selected such that a horizontal seam 36S is formed at each levels of the lateral recesses 43. The deposited insulating fill material forms an insulating fill material layer 36L.

[0182] Referring to FIG. 9J, peripheral portions of the insulating fill material can be removed from inside the memory openings 49 and the support openings 19, for example, by performing an isotropic etch process or an anisotropic etch process. In one embodiment, the insulating fill material layer 36L comprises silicon oxide, and removal of the peripheral portions of the insulating fill material can be removed from inside the memory openings 49 and the support openings 19 employing an isotropic etch process such as a wet etch process employing dilute hydrofluoric acid. In one embodiment, an anisotropic etch process may be performed to etch peripheral portions of the conductive fill material layers 45' so that

cylindrical sidewalls of the conductive fill material layers 45' are physically exposed around each memory opening 49 and around each support opening 19.

[0183] Remaining portions of the insulating fill material that remain in volumes of the lateral recesses 43 after removing the peripheral portions of the insulating fill material from inside the memory openings comprise seamed insulating layers comprising a respective horizontally-extending seam 36S therein. The seamed insulating layers are herein referred to as second-type insulating layers 36. The second-type insulating layers 36 may include the same material as, or may include a material that is different from, the material of the first-type insulating layers 32. In one embodiment, the horizontally-extending seam 36S within each second-type insulating layer 36 can be equidistant from a horizontal plane including a top surface of the second-type insulating layer 36 and from a horizontal plane including a bottom surface of the second-type insulating layer 36.

[0184] FIGS. 10A – 10F are sequential vertical cross-sectional views of a region around a memory opening 49 and a backside trench fill structure (75, 77) during formation of memory opening fill structures according to the first embodiment of the present disclosure.

[0185] Referring to FIG. 10A, the region around the memory opening 49 and the backside trench fill structure (75, 77) is illustrated at a processing step that corresponds to the processing step of FIG. 9J.

[0186] Referring to FIG. 10B, a stack of layers including a blocking dielectric layer 52, a memory material layer 54, a tunneling dielectric layer 56, and an optional sacrificial cover material layer 601 can be sequentially deposited in the memory openings 49.

[0187] The blocking dielectric layer 52 can include a single dielectric material layer or a stack of a plurality of dielectric material layers. In one embodiment, the blocking dielectric layer can include a dielectric metal oxide layer consisting essentially of a dielectric metal

oxide. As used herein, a dielectric metal oxide refers to a dielectric material that includes at least one conductive element and at least oxygen. The dielectric metal oxide may consist essentially of the at least one conductive element and oxygen, or may consist essentially of the at least one conductive element, oxygen, and at least one non-conductive element such as nitrogen. In one embodiment, the blocking dielectric layer 52 can include a dielectric metal oxide having a dielectric constant greater than 7.9, i.e., having a dielectric constant greater than the dielectric constant of silicon nitride.

[0188] Non-limiting examples of dielectric metal oxides include aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), lanthanum oxide (LaO_2), yttrium oxide (Y_2O_3), tantalum oxide (Ta_2O_5), silicates thereof, nitrogen-doped compounds thereof, alloys thereof, and stacks thereof. The dielectric metal oxide layer can be deposited, for example, by chemical vapor deposition (CVD), atomic layer deposition (ALD), pulsed laser deposition (PLD), liquid source misted chemical deposition, or a combination thereof. The thickness of the dielectric metal oxide layer can be in a range from 1 nm to 20 nm, although lesser and greater thicknesses can also be employed. The dielectric metal oxide layer can subsequently function as a dielectric material portion that blocks leakage of stored electrical charges to control gate electrodes. In one embodiment, the blocking dielectric layer 52 includes aluminum oxide. In one embodiment, the blocking dielectric layer 52 can include multiple dielectric metal oxide layers having different material compositions.

[0189] Alternatively or additionally, the blocking dielectric layer 52 can include a dielectric semiconductor compound such as silicon oxide, silicon oxynitride, silicon nitride, or a combination thereof. In one embodiment, the blocking dielectric layer 52 can include silicon oxide. In this case, the dielectric semiconductor compound of the blocking dielectric layer 52 can be formed by a conformal deposition method such as low pressure chemical

vapor deposition, atomic layer deposition, or a combination thereof. The thickness of the dielectric semiconductor compound can be in a range from 1 nm to 20 nm, although lesser and greater thicknesses can also be employed. Alternatively, the blocking dielectric layer 52 can be omitted, and a backside blocking dielectric layer can be formed after formation of lateral recesses on surfaces of memory films to be subsequently formed.

[0190] Subsequently, the memory material layer 54 can be formed. In one embodiment, the memory material layer 54 can be a continuous layer or patterned discrete portions of a charge trapping (i.e., charge storage) material, such as a dielectric charge trapping material, which can be, for example, silicon nitride. Alternatively, the memory material layer 54 can include a continuous layer or patterned discrete portions of a conductive material such as doped polysilicon or a conductive material that is patterned into multiple electrically isolated portions (e.g., floating gates), for example, by being formed within lateral recesses into sacrificial material layers 42. In one embodiment, the memory material layer 54 includes a silicon nitride layer. Alternatively, the memory material layer 54 may comprise a ferroelectric material, such as orthorhombic phase hafnium oxide doped with Al, Si and/or Zr. The ferroelectric material stores data based on the direction of its ferroelectric polarization.

[0191] The memory material layer 54 can be formed as a single charge storage or ferroelectric layer of homogeneous composition, or can include a stack of multiple charge storage or ferroelectric layers. The multiple charge storage layers, if employed, can comprise a plurality of spaced-apart floating gate material layers that contain conductive materials (e.g., metal such as tungsten, molybdenum, tantalum, titanium, platinum, ruthenium, and alloys thereof, or a metal silicide such as tungsten silicide, molybdenum silicide, tantalum silicide, titanium silicide, nickel silicide, cobalt silicide, or a combination thereof) and/or

semiconductor materials (e.g., polycrystalline or amorphous semiconductor material including at least one elemental semiconductor element or at least one compound semiconductor material). Alternatively or additionally, the memory material layer 54 may comprise an insulating charge trapping material, such as one or more silicon nitride segments. Alternatively, the memory material layer 54 may comprise conductive nanoparticles such as metal nanoparticles, which can be, for example, ruthenium nanoparticles. The memory material layer 54 can be formed, for example, by chemical vapor deposition (CVD), atomic layer deposition (ALD), physical vapor deposition (PVD), or any suitable deposition technique for storing electrical charges therein. The thickness of the memory material layer 54 can be in a range from 2 nm to 20 nm, although lesser and greater thicknesses can also be employed.

[0192] The tunneling dielectric layer 56 includes a dielectric material through which charge tunneling can be performed under suitable electrical bias conditions. The charge tunneling may be performed through hot-carrier injection or by Fowler-Nordheim tunneling induced charge transfer depending on the mode of operation of the monolithic three-dimensional NAND string memory device to be formed. The tunneling dielectric layer 56 can include silicon oxide, silicon nitride, silicon oxynitride, dielectric metal oxides (such as aluminum oxide and hafnium oxide), dielectric metal oxynitride, dielectric metal silicates, alloys thereof, and/or combinations thereof. In one embodiment, the tunneling dielectric layer 56 can include a stack of a first silicon oxide layer, a silicon oxynitride layer, and a second silicon oxide layer, which is commonly known as an ONO stack. In one embodiment, the tunneling dielectric layer 56 can include a silicon oxide layer that is substantially free of carbon or a silicon oxynitride layer that is substantially free of carbon. The thickness of the tunneling dielectric layer 56 can be in a range from 2 nm to 20 nm, although lesser and

greater thicknesses can also be employed. The tunneling dielectric layer 56 may be omitted if the memory material layer 54 comprises a ferroelectric material.

[0193] The optional sacrificial cover material layer 601 includes a sacrificial material that can be subsequently removed selective to the material of the tunneling dielectric layer 56. In one embodiment, the sacrificial cover material layer 601 can include a semiconductor material such as amorphous silicon, or may include a carbon-based material such as amorphous carbon or diamond-like carbon (DLC). The sacrificial cover material layer 601 can be formed by a conformal deposition method such as low pressure chemical vapor deposition (LPCVD). The thickness of the sacrificial cover material layer 601 can be in a range from 2 nm to 10 nm, although lesser and greater thicknesses can also be employed. A memory cavity 49' is formed in the volume of each memory opening 49 that is not filled with the deposited material layers (52, 54, 56, 601).

[0194] Referring to FIG. 10C, the optional sacrificial cover material layer 601, the tunneling dielectric layer 56, the memory material layer 54, the blocking dielectric layer 52 are sequentially anisotropically etched employing at least one anisotropic etch process. The portions of the sacrificial cover material layer 601, the tunneling dielectric layer 56, the memory material layer 54, and the blocking dielectric layer 52 located above the top surface of the topmost first-type insulating layer 32 can be removed by the at least one anisotropic etch process. Further, the horizontal portions of the sacrificial cover material layer 601, the tunneling dielectric layer 56, the memory material layer 54, and the blocking dielectric layer 52 at a bottom of each memory cavity 49' can be removed to form openings in remaining portions thereof. Each of the sacrificial cover material layer 601, the tunneling dielectric layer 56, the memory material layer 54, and the blocking dielectric layer 52 can be etched by

a respective anisotropic etch process employing a respective etch chemistry, which may, or may not, be the same for the various material layers.

[0195] Each remaining portion of the sacrificial cover material layer 601 can have a tubular configuration. The memory material layer 54 can comprise a charge trapping material, a floating gate material or a ferroelectric material. In one embodiment, each memory material layer 54 can include a vertical repetition of charge storage regions that store electrical charges upon programming. In one embodiment, the memory material layer 54 can be a memory material layer in which each portion adjacent to the sacrificial material layers 42 constitutes a charge storage region. The physically exposed semiconductor surface at the bottom of each memory cavity 49' can be vertically recessed so that the recessed semiconductor surface underneath the memory cavity 49' is vertically offset from the topmost surface of the semiconductor material layer 10 by a recess distance. A tunneling dielectric layer 56 may be located over the memory material layer 54. A set of a blocking dielectric layer 52, a memory material layer 54, and a tunneling dielectric layer 56 in a memory opening 49 constitutes a memory film 50, which may include a plurality of charge storage regions (comprising portions of the memory material layer 54) that are insulated from surrounding materials by the blocking dielectric layer 52 and the tunneling dielectric layer 56. In one embodiment, the sacrificial cover material layer 601, the tunneling dielectric layer 56, the memory material layer 54, and the blocking dielectric layer 52 can have vertically coincident sidewalls. The sacrificial cover material layer 601 can be subsequently removed selective to the material of the tunneling dielectric layer 56. In case the sacrificial cover material layer 601 includes a semiconductor material, a wet etch process employing hot trimethyl-2 hydroxyethyl ammonium hydroxide ("hot TMY") or tetramethyl ammonium hydroxide (TMAH) can be performed to remove the sacrificial cover material layer 601.

Alternatively, the sacrificial cover material layer 601 may be retained if it comprises amorphous silicon or polysilicon.

[0196] Referring to FIG. 10D, a semiconductor channel layer 60L can be deposited directly on the semiconductor surface of the semiconductor material layer 10, and directly on the tunneling dielectric layer 56. The semiconductor channel layer 60L includes a semiconductor material such as at least one elemental semiconductor material, at least one III-V compound semiconductor material, at least one II-VI compound semiconductor material, at least one organic semiconductor material, or other semiconductor materials known in the art. In one embodiment, the semiconductor channel layer 60L includes amorphous silicon or polysilicon. The semiconductor channel layer 60L can have a doping of a first conductivity type, which is the same as the conductivity type of the semiconductor material layer 10. The semiconductor channel layer 60L can be formed by a conformal deposition method such as low pressure chemical vapor deposition (LPCVD). The thickness of the semiconductor channel layer 60L can be in a range from 2 nm to 10 nm, although lesser and greater thicknesses can also be employed. The semiconductor channel layer 60L may partially fill the memory cavity 49' in each memory opening, or may fully fill the cavity in each memory opening.

[0197] In case the memory cavity 49' in each memory opening is not completely filled by the semiconductor channel layer 60L, a dielectric core layer 62L can be deposited in the memory cavity 49' to fill any remaining portion of the memory cavity 49' within each memory opening. The dielectric core layer 62L includes a dielectric material such as silicon oxide or organosilicate glass. The dielectric core layer 62L can be deposited by a conformal deposition method such as low pressure chemical vapor deposition (LPCVD), or by a self-planarizing deposition process such as spin coating.

[0198] Referring to FIG. 10E, the horizontal portion of the dielectric core layer 62L can be removed, for example, by a recess etch process such that each remaining portions of the dielectric core layer 62L is located within a respective memory opening 49 and has a respective top surface below the horizontal plane including the top surface of the topmost cavity-free insulating layer 32. Each remaining portion of the dielectric core layer 62L constitutes a dielectric core 62.

[0199] Referring to FIG. 10F, a doped semiconductor material having a doping of a second conductivity type can be deposited within each recessed region above the dielectric cores 62. The deposited semiconductor material can have a doping of a second conductivity type that is the opposite of the first conductivity type. For example, if the first conductivity type is p-type, the second conductivity type is n-type, and vice versa. The dopant concentration in the deposited semiconductor material can be in a range from $5.0 \times 10^{18}/\text{cm}^3$ to $2.0 \times 10^{21}/\text{cm}^3$, although lesser and greater dopant concentrations can also be employed. The doped semiconductor material can be, for example, doped polysilicon.

[0200] Excess portions of the deposited semiconductor material having a doping of the second conductivity type and a horizontal portion of the semiconductor channel layer 60L can be removed from above the horizontal plane including the top surface of the topmost cavity-free insulating layer 32, for example, by chemical mechanical planarization (CMP) or a recess etch process. Each remaining portion of the doped semiconductor material having a doping of the second conductivity type constitutes a drain region 63. Each remaining portion of the semiconductor channel layer 60L (which has a doping of the first conductivity type) constitutes a vertical semiconductor channel 60.

[0201] A tunneling dielectric layer 56 is surrounded by a memory material layer 54, and laterally surrounds a portion of the vertical semiconductor channel 60. Each adjoining set of

a blocking dielectric layer 52, a memory material layer 54, and a tunneling dielectric layer 56 collectively constitute a memory film 50, which can store electrical charges or electrical polarization with a macroscopic retention time. In some embodiments, a blocking dielectric layer 52 may not be present in the memory film 50 at this step, and a blocking dielectric layer may be subsequently formed after formation of lateral recesses. As used herein, a macroscopic retention time refers to a retention time suitable for operation of a memory device as a permanent memory device such as a retention time in excess of 24 hours.

[0202] Each combination of a memory film 50 and a vertical semiconductor channel 60 within a memory opening 49 constitutes a memory stack structure 55. The memory stack structure 55 is a combination of a semiconductor channel, a tunneling dielectric layer, a plurality of memory elements comprising portions of the memory material layer 54, and an optional blocking dielectric layer 52. An entire set of material portions (e.g., memory stack structure 55, dielectric core 63 and drain region 63) filling a memory opening 49 is herein referred to as a memory opening fill structure 58. An entire set of material portion filling a support opening 19 is herein referred to as a support opening fill structure. Each of the memory opening fill structures 58 contacts a closed periphery of a respective horizontally-extending seam in each of the seamed insulating layers, i.e., the second-type insulating layers 36.

[0203] FIGS. 11A – 11D are sequential vertical cross-sectional views of a region around a memory opening 49 and a backside trench 79 during replacement of sacrificial backside trench fill structures (75, 77) with backside trench fill structures (74, 76) according to the first embodiment of the present disclosure.

[0204] Referring to FIG. 11A, the sacrificial backside trench fill structures (75, 77) can be removed selective to the first-type insulating layers 32, the second-type insulating layers

36, and the in-process electrically conductive layers (44, 45'). If the liners 44 comprise the sacrificial liners (e.g., amorphous silicon), then the liners 44 are not present in the in-process electrically conductive layers. For example, a first etch process (or an ashing process if portion 77 comprises carbon) can be performed to etch the sacrificial trench fill material portion 77 selective to the etch-stop spacer 75, and a second etch process can be performed to etch the etch-stop spacer 75.

[0205] Referring to FIG. 11B, proximal portions of the at least one conductive fill material of the in-process electrically conductive layers (44, 45') can be recessed around the backside trenches 79 by performing an isotropic etch process that etches the conductive materials of the in-process electrically conductive layers (44, 45'). In one embodiment, the isotropic etch process may be a wet etch process that etches the conductive materials of the in-process electrically conductive layers (44, 45') selective to the materials of the insulating layers (32, 36). The duration of the isotropic etch process can be selected such that each vertically-extending portion of the in-process electrically conductive layers (44, 45') located between a vertically neighboring pair of first-type insulating layers 32 is removed by the isotropic etch process.

[0206] Each portion of the at least one conductive fill material filling a respective one of the lateral recesses 43 (i.e., each in-process electrically conductive layers (44, 45')) is divided into a respective pair of a first-type electrically conductive layer 46A and a second-type electrically conductive layer 46B that are disjoined from, and are vertically spaced from, each other. A second-type insulating layer 36 is located between a vertically-neighboring pair of a first-type electrically conductive layer 46A and a second-type electrically conductive layer 46B. Each first-type electrically conductive layer 46A comprises, from bottom to top, an optional first conductive barrier liner 44 and a first conductive fill material layer 45A. Each

second-type electrically conductive layer 46B comprises, from bottom to top, a second conductive fill material layer 45B and an optional second conductive barrier liner 44. The first conductive fill material layer 45A and the second conductive fill material 45B are in direct contact with horizontal surfaces of the second-type insulating layer 36.

[0207] A vertical repetition of multiple instances of a unit layer stack (32, 46A, 36, 46B) can be formed over the substrate (9, 10). The unit layer stack comprises, from bottom to top, a seamless insulating layer (such as a first-type insulating layer 32) that is free of any seam therein, a first-type electrically conductive layer 46A, a seamed insulating layer (such as a second-type insulating layer 36) including a horizontally-extending seam therein 36S, and a second-type electrically conductive layer 46B.

[0208] Referring to FIG. 11C, an insulating spacer layer 74L can be deposited in peripheral portions of the backside trenches 79 and over the vertical repetition (32, 46A, 36, 46B). The insulating spacer layer 74L includes an insulating material such as silicon oxide. Lateral protrusions of the backside trenches 79 at levels of the first-type electrically conductive layers 46A, the second-type insulating layers 36, and the second-type electrically conductive layers 46B can be filled with the insulating spacer layer 74L.

[0209] Referring to FIG. 11D, an anisotropic etch process can be performed to remove horizontally-extending portions of the insulating spacer layer 74L. An insulating spacer 74 can be formed in peripheral volumes of each backside trench 79. At least one conductive material can be deposited in unfilled volumes of the backside trenches 79. For example, a backside conductive barrier liner 76A and a backside conductive fill material portion 76B can be formed within each backside trench 79 by deposition and planarization of a conductive barrier material (such as TiN, TaN, or WN) and a conductive fill material such as W, Ru, Mo, Co, etc. Each combination of a backside conductive barrier liner 76A and a backside

conductive fill material portion 76B is herein referred to as a backside contact via structure 76. Alternatively, the above described insulating spacer layer 74L can be deposited to completely fill the entire volume of a backside trench 79 and may consist essentially of at least one dielectric material. In this alternative embodiment, the source region 61 and the backside contact via structure 76 may be omitted, and a horizontal source line (e.g., direct strap contact) may contact a side of the lower portion of the semiconductor channel 60.

[0210] Generally, a first backside trench fill structure (74, 76) and a second backside trench fill structure (74, 76) can be formed on sidewalls of each vertical repetition of instances of a unit layer stack (32, 46A, 36, 46B). A first backside trench fill structure (74, 76) comprising a first dielectric surface can contact first sidewalls of each layer within the vertically stack, and can laterally extend along a first horizontal direction. A second backside trench fill structure (74, 76) comprising a second dielectric surface can contact second sidewalls of each layer within the vertical repetition, can laterally extend along the second horizontal direction, and can be laterally spaced from the first backside trench fill structure (74, 76) along a second horizontal direction.

[0211] In one embodiment, vertical interfaces between an insulating spacer 74 and a contiguous set of a first-type electrically conductive layers 46A, a second-type insulating layers 36, and a second-type electrically conductive layers 46B can be laterally offset from vertical interfaces between the insulating spacer 74 and the first-type insulating layers 32. In this case, each of the first backside trench fill structure (74, 76) and the second backside trench fill structure (74, 76) has a respective laterally-undulating vertical cross-sectional profile in a vertical plane that is perpendicular to the first horizontal direction, and each of the first backside trench fill structure (74, 76) and the second backside trench fill structure (74, 76) has a greater width at levels of the first-type electrically conductive layers 46A, the

seamed insulating layers (comprising the second-type insulating layers 36), and the second-type electrically conductive layers 46B than at levels of the seamless insulating layers (comprising the first-type insulating layers 32).

[0212] In one embodiment, each horizontally-extending seam within the seamed insulating layers (comprising the second-type insulating layers 36) may be laterally spaced from, and does not contact, any of the first backside trench fill structure (74, 76) and the second backside trench fill structure (74, 76). In one embodiment, each of the first backside trench fill structure (74, 76) and the second backside trench fill structure (74, 76) comprises: a backside contact via structure 76 contacting a respective source region 61 in the substrate (9, 10); and an insulating spacer 74 laterally surrounding the backside contact via structure 76 and comprising a respective one of the first dielectric surface and the second dielectric surface as an outer surface. In one embodiment, each of the memory opening fill structures 58 comprises a respective straight outer sidewall that extends through each layer within the vertical repetition and contacts each layer within the vertical repetition.

[0213] Referring to FIG. 12, a first alternative configuration of a region of the first exemplary structure is illustrated at a processing step that is equivalent to the processing step of FIG. 11D. The first alternative configuration can be derived from the first exemplary structure illustrated in FIG. 11D by employing a non-conformal deposition process at the processing step of FIG. 9 to deposit an insulating fill material layer 36L. In this case, at least one instance, or each instance, of the seamed insulating layers (i.e., the second-type insulating layers 36) comprises an air gap 39 (e.g., an encapsulated cavity that is free of any solid phase material and is encapsulated by the second-type insulating layer 36). The dielectric material layer has an upper horizontally-extending portion and a lower horizontally-extending portion that are adjoined to each other at a periphery of the air gap 39 at a respective horizontally-

extending seam (which contact the memory opening fill structures 58 and the support pillar structures).

[0214] Referring to FIG. 13, a second alternative configuration of a region of the first exemplary structure is illustrated at a processing step that is equivalent to the processing step of FIG. 11D. The first exemplary structure illustrated in FIG. 10A can be modified prior to the processing steps of FIG. 10B by laterally recessing the conductive fill material layers 45' selective to the first-type insulating layers 32 and selective to the second-type insulating layers 36. In this embodiment, the memory opening fill structures 58 comprise a respective laterally-undulating outer sidewall that extends through each layer within the vertical repetition (32, 46A, 36, 46B) and laterally protrudes outward at levels of the first-type electrically conductive layers 46A and the second-type electrically conductive layers 46B relative to levels of the first-type insulating layers and the second-type (seamed) insulating layers 36, as shown in FIG. 13.

[0215] FIG. 14 is a vertical cross-sectional view of a third alternative configuration of a region of the first exemplary structure is illustrated at a processing step that is equivalent to the processing step of FIG. 11D. A non-conformal deposition process at the processing step of FIG. 9 to deposit an insulating fill material layer 36L. Further, the first exemplary structure illustrated in FIG. 10A can be modified prior to the processing steps of FIG. 10B by laterally recessing the conductive fill material layers 45' selective to the first-type insulating layers 32 and selective to the second-type insulating layers 36. In this embodiment, each of the memory opening fill structures 58 comprises a respective laterally-undulating outer sidewall, and the second-type insulating layers 36 include air gaps 39.

[0216] Referring to FIGS. 15A and 15B, the first exemplary structure is illustrated after replacement of the sacrificial backside trench fill structures (75, 77) with backside trench fill

structures (74, 76). Memory opening fill structures 58 are located within the memory openings 49, and support pillar structures 20 are located within the support openings 19.

[0217] Referring to FIG. 16, the sacrificial retro-stepped dielectric material portion 67 can be removed selective to the materials of the first-type insulating layers 32, the electrically conductive layers (46A, 46B), the memory opening fill structures 58, and the support pillar structures 20. For example, if the sacrificial retro-stepped dielectric material portion 67 comprises organosilicate glass or a doped silicate glass, a wet etch process employing dilute hydrofluoric acid may be performed to remove the sacrificial retro-stepped dielectric material portion 67. A retro-stepped cavity 69 can be formed in the volume from which the sacrificial retro-stepped dielectric material portion 67 is removed. In one embodiment, each first-type electrically conductive layer 46A can be connected to a respective second-type electrically conductive layer 46B by a vertically-connecting electrically conductive material portion (i.e., vertical conductive strap) 46V including the same material as the first-type electrically conductive layers 46A and the second-type electrically conductive layers 46B and located underneath the stepped surfaces within the contact region 300.

[0218] Referring to FIG. 17, an isotropic etch process can be performed to remove proximal portions of the at least one conductive fill material of the electrically conductive layers (46A, 46B) from the staircase region (i.e., contact region 300). Vertically-extending portions (i.e., portions 46V) of the at least one conductive fill material are removed from sidewalls of the second-type insulating layers 36 located within the staircase region. Specifically, the vertically-connecting electrically conductive material portions 46V of the at least one conductive fill material located underneath the stepped surfaces within the contact region 300 can be removed by the isotropic etch process. Each pair of a first-type electrically conductive layer 46A and a second-type electrically conductive layer 46B connected by a

respective vertically-connecting electrically conductive material portion 46V can be physically detached from each other, and can be electrically isolated from each other, upon removal of the vertically-connecting electrically conductive material portions 46V. In one embodiment, a wet etch process that etches the conductive materials of the vertically-connecting electrically conductive material portions 46V selective to the materials of the first-type insulating layers 32 and the second-type insulating layers 36 can be employed to etch the vertically-connecting electrically conductive material portions 46V. Sidewalls of the second-type insulating layers 36 can be physically exposed after the isotropic etch process.

[0219] Referring to FIGS. 18A – 18C, an optional etch mask layer 57 can be applied over the exemplary structure, and can be lithographically patterned to cover first areas within the contact region 300 without covering second areas of the contact region 300. In one embodiment, the etch mask layer 57 may be a patterned photoresist layer. In one embodiment, a first subset of the support pillar structures 20 can be covered by the etch mask layer 57, while a second subset of the support pillar structures 20 is not covered by the etch mask layer 57. The second areas of the staircase region that are not covered with the etch mask layer 57 can optionally be anisotropically etched such that a second-type insulating layer 36 and a first-type electrically conductive layer 46A are etched within the second areas. In this case, portions of the stepped surfaces within the second area are vertically recessed at least by a sum of the thickness of an instance of the second-type insulating layer 36 and the thickness of a first-type electrically conductive layer 46A that includes a horizontally-extending portion of the at least one conductive fill material. The etch mask layer 57 can be subsequently removed.

[0220] Referring to FIGS. 19A – 19C, at least one dielectric material can be deposited in the retro-stepped cavity 69 and over the vertical repetition (32, 46A, 36, 46B). The at least

one dielectric material can include, for example, undoped silicate glass, a doped silicate glass, and/or organosilicate glass. The portion of the at least one dielectric material that fills the retro-stepped cavity 69 constitutes a retro-stepped dielectric material portion 65. The portion of the at least one dielectric material that overlies the horizontal plane including the topmost surface of the vertical repetition (32, 46A, 36, 46B) constitutes a contact-level dielectric layer 80.

[0221] Referring to FIGS. 20A – 20C, via cavities can be formed through the contact-level dielectric layer 80 and the retro-stepped dielectric material portion 65. The via cavities can vertically extend down to a top surface of a respective one of the drain regions 63 or to a top surface of a respective one of the first-type electrically conductive layers 46A and the second-type electrically conductive layers 46B. At least one conductive material, such as at least one conductive material, can be deposited in the via cavities. Drain contact via structures 88 can be formed on the top surfaces of the drain regions 63, and layer contact via structures (e.g., word line contact via structures) 86 can be formed on the top surfaces of the electrically conductive layers 46. The layer contact via structures 86 can include first layer contact via structures 86A contacting a top surface of a respective one of the first-type electrically conductive layers 46A, and second layer contact via structures 86B contacting a top surface of a respective one of the second-type electrically conductive layers 46B.

[0222] Drain-select-level dielectric isolation structures 72 can be formed along the first horizontal direction hd1 that is parallel to the lengthwise direction of the backside trench fill structures (74, 76) at drain select levels, which are levels of a topmost subset of the electrically conductive layers 46 (i.e., the levels of the drain side select gate electrodes). Each drain-select-level dielectric isolation structure 72 can vertically extend through at least a

topmost electrically conductive layer 46B of the first-type electrically conductive layer 46A and the second-type electrically conductive layer 46B.

[0223] Referring to FIG. 21, an alternative embodiment of the first exemplary structure is illustrated at a processing step corresponding to the processing steps of FIGS. 6A and 6B. In the alternative embodiment, pillar cavities 149 are formed concurrently with formation of the backside trenches 79. In one embodiment, the pillar cavities 149 may be formed as cylindrical cavities located between laterally neighboring pairs of backside trenches 79. The pillar cavities 149 may be formed in the memory array region 100 and in the contact region 300 between respective memory openings 49 and the support openings 19.

[0224] Referring to FIGS. 22A and 22B, sacrificial pillar structures (175, 177) can be formed in the pillar cavities 149 concurrently with formation of sacrificial backside trench fill structures (75, 77). Each sacrificial pillar structure (175, 177) may include an optional cylindrical etch-stop spacer 175 including a same material as the optional etch-stop spacers 75, and a sacrificial pillar fill material portion 177 including a same material as the sacrificial trench fill material portions 77.

[0225] FIGS. 23A, 23B, 24A, 24B, 25A, 25B, 26A and 26B are sequential vertical cross-sectional views of a region between a memory opening 49 and a sacrificial pillar structure (175, 177) during formation of in-process electrically conductive layers (44, 45') according to the alternative embodiment of the first exemplary structure of first embodiment of the present disclosure. The steps in FIGS. 23A, 23B, 24A, 24B, 25A, 25B, 26A and 26B correspond to respective steps shown in FIGS. 9A – 9H of the first embodiment of the present disclosure.

[0226] Referring to FIG. 23A, the processing steps of FIG. 8 and 9A can be performed to remove the sacrificial memory opening fill structures 48 and the sacrificial support opening

fill structures 18 from the memory openings 49 and from the support openings 19, respectively.

[0227] Referring to FIGS. 23B, 24A, 24B and 25A, the steps described above with respect to FIGS. 9B – 9E are performed with any needed changes. Specifically, the sacrificial pillar structures (175, 177) provide additional support for the insulating layers 32 during formation of the backside recesses 43.

[0228] Referring to FIG. 25B the sacrificial pillar structures (175, 177) are removed from the pillar cavities 149 without removing the sacrificial backside trench fill structures (75, 77). For example, the sacrificial pillar structures (175, 177) can be removed by selective etching while the sacrificial backside trench fill structures (75, 77) are covered with a mask (e.g., hard mask or photoresist). At this step, the exposed pillar cavities 149 can function as additional memory openings 49. Subsequently, the recess of layer 41 is performed through the memory openings 49 and the pillar cavities 149 as described above with respect to FIG. 9F.

[0229] Referring to FIGS. 26A and 26B, the steps described above with respect to FIGS. 9G – 9H are performed with any needed changes. The steps described above with respect to FIGS. 9I and 9J are then performed.

[0230] FIG. 27 is vertical cross-sectional view of a region of the alternative embodiment of the first exemplary structure at the step that corresponds to the step of FIG. 10A, according to the first embodiment of the present disclosure. The steps described above with respect to FIGS. 10B – 10F and 11A – 11D are then performed with any needed changes. Specifically, the memory opening fill structures 58 are formed in both the memory openings 49 and the pillar cavities 149 to form the structure of FIGS. 11D, 12, 13 or 14. The steps described above with respect to FIGS. 15A – 20C are then performed with any needed changes

[0231] Referring to all drawings related to the first embodiment of the present disclosure, a three-dimensional memory device is provided, which comprises: a vertical repetition of multiple instances of a unit layer stack, wherein the unit layer stack comprises, from bottom to top, a seamless insulating layer 32 that is free of any seam therein, a first-type electrically conductive layer 46A, a seamed insulating layer 36 including a horizontally-extending seam therein, and a second-type electrically conductive layer 46B, memory openings 49 vertically extending through the vertical repetition; and memory opening fill structures 58 located within the memory openings 49, wherein each of the memory opening fill structures 58 comprises a respective vertical stack of memory elements.

[0232] In one embodiment, each of the memory opening fill structures 58 contacts a closed periphery of a respective horizontally-extending seam in each of the seamed insulating layers 36, and each of the memory opening fill structures 58 comprises a vertical semiconductor channel 60 and a memory film 50 containing the vertical stack of memory elements

[0233] In one embodiment, the horizontally-extending seam within the seamed insulating layer 36 is equidistant from a horizontal interface between the seamed insulating layer 36 and the second-type electrically conductive layer 46B, and from a horizontal interface between the seamed insulating layer 36 and the first-type electrically conductive layer 46A.

[0234] In one embodiment, the three-dimensional memory device comprises: a first backside trench fill structure (74, 76) comprising a first dielectric surface contacting first sidewalls of each layer within the vertical repetition and laterally extending along a first horizontal direction hd1; and a second backside trench fill structure (74, 76) comprising a second dielectric surface contacting second sidewalls of each layer within the vertical

repetition laterally extending along the first horizontal direction hd1, and laterally spaced from the first backside trench fill structure (74, 76) along a second horizontal direction hd1.

[0235] In one embodiment, each of the first backside trench fill structure (74, 76) and the second backside trench fill structure (74, 76) has a respective laterally-undulating vertical cross-sectional profile in the second horizontal direction hd2; and each of the first backside trench fill structure (74, 76) and the second backside trench fill structure (74, 76) has a greater width at levels of the first-type electrically conductive layers 46A, the seamed insulating layers 36, and the second-type electrically conductive layers 46B than at levels of the seamless insulating layers 32.

[0236] In one embodiment, each horizontally-extending seam within the seamed insulating layers 36 is laterally spaced from, and does not contact, any of the first backside trench fill structure (74, 76) and the second backside trench fill structure (74, 76).

[0237] In one embodiment, each of the first backside trench fill structure (74, 76) and the second backside trench fill structure (74, 76) comprises: a backside contact via structure 76 contacting a respective source region 61 in the substrate (9, 10); and an insulating spacer 74 laterally surrounding the backside contact via structure 76 and comprising a respective one of the first dielectric surface and the second dielectric surface as an outer surface.

[0238] In one embodiment, at least one instance of the seamed insulating layers 36 comprises an air gap 39 encapsulated by a dielectric material layer having an upper horizontally-extending portion and a lower horizontally-extending portion that are adjoined to each other at a periphery of the air gap at a respective horizontally-extending seam.

[0239] In one embodiment, within each instance of the unit layer stack: the first-type electrically conductive layer 46A comprises, from bottom to top, a first conductive barrier liner 44 and a first conductive fill material layer 45A; and the second-type electrically

conductive layer 46B comprises, from bottom to top, a second conductive fill material layer 45B and a second conductive barrier liner 44, wherein the first conductive fill material layer 45A and the second conductive fill material layer 45B are in direct contact with horizontal surfaces of the second-type insulating layer 36.

[0240] In one embodiment shown in FIG. 12, each of the memory opening fill structures 58 comprises a respective straight outer sidewall that extends through each layer within the vertical repetition and contacts each layer within the vertical repetition. In another embodiment shown in FIG. 13, each of the memory opening fill structures 58 comprises a respective laterally-undulating outer sidewall that extends through each layer within the vertical repetition and laterally protrudes outward at levels of the first-type electrically conductive layers 45A and the second-type electrically conductive layers 45B relative to levels of the seamless insulating layers 32 and the seamed insulating layers 36.

[0241] Referring to FIG. 28, a second exemplary structure according to a second embodiment of the present disclosure is illustrated, which may be the same as the first exemplary structure illustrated in FIG. 2.

[0242] Referring to FIGS. 29A and 29B, the processing steps of FIGS. 4A and 4B can be performed to form memory openings 49 and support openings 19. For example, a photoresist layer 17 can be applied over the vertical repetition (32, 42), and can be lithographically patterned with the same pattern as the pattern of the memory openings 49 and the support openings 19 illustrated in FIGS. 4A and 4B. An anisotropic etch process can be performed to transfer the pattern of the openings in the photoresist layer 17 through the vertical repetition (32, 42), thereby forming the memory openings 49 and the support openings 19.

[0243] Referring to FIG. 30, an optional isotropic etch process can be performed to laterally recess sidewalls of the first-type insulating layers 32 selective to the sacrificial

material layers 42. For example, if the sacrificial material layers 42 comprise silicon nitride and if the first-type insulating layers 32 comprise silicon oxide, a wet etch process employing dilute hydrofluoric acid can be performed to laterally recess the sidewalls of the first-type insulating layers 32 without recessing the sacrificial material layers 42 around each of the memory openings 49 and the support openings 19. The lateral recess distance may be in a range from 5 nm to 100 nm, although lesser and greater lateral recess distances may also be employed.

[0244] Referring to FIG. 31, the photoresist layer 17 can be removed, for example, by ashing.

[0245] Referring to FIG. 32, a first sacrificial fill material can be deposited in the memory openings 49 and the support openings 19. The first sacrificial fill material comprises a material that is different from the materials of the first-type insulating layers 32 and the sacrificial material layers 42. For example, the first sacrificial fill material may include, for example, amorphous silicon, amorphous carbon, diamond-like carbon, germanium, or silicon-germanium. Excess portions of the first sacrificial fill material can be removed from the horizontal plane including the top surface of the topmost first-type insulating layer 32. Each remaining portion of the first sacrificial fill material located in a memory opening 49 constitutes a sacrificial memory opening fill structure 48. Each remaining portion of the first sacrificial fill material located in a support opening 19 constitutes a sacrificial support opening fill structure 18. Optionally, each of the sacrificial memory opening fill structures 48 and the sacrificial support opening fill structures 18 may comprise laterally-protruding fins (48F, 18F) at each level of the first-type insulating layers 32.

[0246] Referring to FIGS. 33A and 33B, the processing steps of FIGS. 6A and 6B can be performed to form backside trenches 79 and source regions 61. The pattern of the backside trenches 79 may be the same as in the first exemplary structure.

[0247] Referring to FIGS. 34A and 34B, the processing steps of FIGS. 7A and 7B can be performed to form a sacrificial backside trench fill structure (75, 77) within each of the backside trenches 79.

[0248] Referring to FIGS. 35A and 35B, an etch mask layer 171 can be formed over the vertical repetition (32, 42), the sacrificial memory opening fill structures 48, the sacrificial support opening fill structures 18, and the sacrificial backside trench fill structures (75, 77), and can be lithographically patterned to form an array of openings in the contact region 300. The etch mask layer 171 can include an etch-resistant material, such as a hard mask comprising a conductive material or a dielectric metal oxide material. In one embodiment, the array of openings may comprise a rectangular array of circular or elliptical openings having a periodicity along the first horizontal direction $hd1$ and the second horizontal direction $hd2$.

[0249] A trimmable mask layer (not shown) can be applied over the etch mask layer 171, and can be patterned to cover the entirety of the memory array region 100 and a predominant portion of the contact region 300. Specifically, the trimmable mask layer can be patterned such that the trimmable mask layer covers all openings within the array of openings in the etch mask layer 171 other than a most distal column of openings in the etch mask layer 171 from the memory array region 100. An anisotropic etch process can be performed to transfer the pattern of a most distal column of openings in the etch mask layer 171 through a topmost first-type insulating layer 32 and a topmost sacrificial material layer 42. The trimmable mask layer can be trimmed to physically expose a second most distal column of openings in the

etch mask layer 171. Another anisotropic etch process can be performed to etch through a pair of a first-type insulating layer 32 and a sacrificial material layer 42 underneath each unmasked opening in the etch mask layer 171. A trimming process that physically exposes a new column of openings in the etch mask layer 171 and an anisotropic etch that recesses areas of unmasked openings in the etch mask layer 171 by a thickness of a first-tier insulating layer 32 and a thickness of a sacrificial material layer 42 can be iteratively performed to form a two-dimensional array of contact via cavities 81 having different depths. A set of contact via cavities 81 can be formed such that each sacrificial material layer 42 is physically exposed to at least one contact via cavity 81 that does not extend below the respective sacrificial material layer 42. The trimmable mask layer can be subsequently removed. Generally, contact via cavities 81 having different depths can be formed through the vertical repetition (32, 42). A surface of a respective sacrificial material layer 42 of the sacrificial material layers 42 of the vertical repetition (32, 42) is physically exposed at a bottom of each of the contact via cavities 81.

[0250] Referring to FIG. 36, the sacrificial material layers 42 can be removed selective to the first-type insulating layers 32 by introducing an isotropic etchant that etches the material of the sacrificial material layers 42 selective to the material of the first-type insulating layers into the contact via cavities 81. Lateral recesses 43 are formed in volumes from which the sacrificial material layers 42 are removed. The removal of the second material of the sacrificial material layers 42 can be selective to the first material of the first-type insulating layers 32, the material of the sacrificial memory opening fill structures 48 and the sacrificial support opening fill structures 18, and the material of the optional etch-stop spacers 75 or the material of the sacrificial trench fill material portions 77. In one embodiment, the sacrificial material layers 42 can include silicon nitride, and the materials of the first-type insulating

layers 32 and the etch-stop spacers 75 can be selected from silicon oxide and dielectric metal oxides.

[0251] In an illustrative example, if the sacrificial material layers 42 include silicon nitride, the etch process can be a wet etch process in which the exemplary structure is immersed within a wet etch tank including phosphoric acid, which etches silicon nitride selective to silicon oxide, silicon, and various other materials employed in the art. The sacrificial backside trench fill structures (75, 77), the sacrificial memory opening fill structures 48, and the sacrificial support opening fill structures 18 provide structural support while the lateral recesses 43 are present within volumes previously occupied by the sacrificial material layers 42.

[0252] Each lateral recess 43 can be a laterally extending cavity having a lateral dimension that is greater than the vertical extent of the cavity. In other words, the lateral dimension of each lateral recess 43 can be greater than the height of the lateral recess 43. A plurality of lateral recesses 43 can be formed in the volumes from which the second material of the sacrificial material layers 42 is removed. Each of the plurality of lateral recesses 43 can extend substantially parallel to the top surface of the substrate (9, 10). A lateral recess 43 can be vertically bounded by a top surface of an underlying first-type insulating layer 32 and a bottom surface of an overlying first-type insulating layer 32. In one embodiment, each lateral recess 43 can have a uniform height throughout.

[0253] Referring to FIG. 37, at least one conductive fill material can be deposited at peripheral portions of the lateral recesses 43. In one embodiment, the above described liner 44 is deposited directly on physically exposed surfaces of instances of the first-type insulating layer 32 and on physically exposed sidewalls of the sacrificial backside trench fill structures (75, 77).

[0254] Conductive fill material layers 45' can be deposited on the liners 44, as described above with respect to the first embodiment. If the liners 44 comprise the sacrificial material liners, then they are consumed during the deposition of the conductive fill material layers 45'. In one embodiment, the thickness of each conductive fill material layer 45' can be in a range from 20 % to 45 %, such as from 25 % to 35 %, of the thickness of the sacrificial material layers 42. In one embodiment, the conductive fill material layer 45' may have a thickness that is about the same as the lateral recess distance of the liners 44 from the memory openings 49 and from the support openings 19. Lateral cavities 43' are present within volumes of the lateral recesses 43 that are not filled by the conductive fill material layers 45'.

[0255] Referring to FIG. 38, an insulating fill material can be deposited over the at least one conductive fill material of the in-process electrically conductive layers (44, 45') within remaining volumes of the lateral recesses 43 by a conformal deposition process. The insulating fill material includes an insulating material such as undoped silicate glass or a doped silicate glass. The thickness of the insulating fill material can be selected such that a horizontal seam 36S is formed at each levels of the lateral recesses 43. The deposited insulating fill material forms an insulating fill material layer 36L.

[0256] A sacrificial via fill material layer 83L can be deposited in remaining volumes of the contact via cavities 81 and over a topmost surface of the insulating fill material layer 36L. The sacrificial via fill material layer 83L includes a sacrificial fill material such as borosilicate glass, organosilicate glass, amorphous carbon, diamond-like carbon, amorphous silicon, germanium, or silicon-germanium.

[0257] Referring to FIG. 39, a planarization process such as a chemical mechanical polishing (CMP) process and/or a recess etch process can be performed to remove excess portions of the sacrificial via fill material layer 83L, the insulating fill material layer 36L, and

the in-process electrically conductive layers (44, 45'). Each remaining portion of the sacrificial via fill material layer 83L that remains within a respective contact via cavity 81 constitutes a sacrificial via fill material portion 83.

[0258] Referring to FIG. 40, a first photoresist layer 277 can be applied over the second exemplary structure, and can be lithographically patterned to form elongated openings over the areas of the sacrificial backside trench fill structures (75, 77). At least one etch process can be performed to remove the sacrificial backside trench fill structures (75, 77). Backside voids are formed within volumes from which the sacrificial backside trench fill structures (75, 77) are removed. A horizontal semiconductor channel 59 can be formed between each source region 61 and bottom surfaces of an adjacent set of sacrificial memory opening fill structures 48.

[0259] Referring to FIG. 41, proximal portions of the at least one conductive fill material of the in-process electrically conductive layers (44, 45') can be removed from around the backside voids by performing an isotropic etch process that etches the conductive materials of the in-process electrically conductive layers (44, 45'). In one embodiment, the isotropic etch process may be a wet etch process that etches the conductive materials of the in-process electrically conductive layers (44, 45') selective to the materials of the insulating layers (32, 36). The duration of the isotropic etch process can be selected such that each vertically-extending portion of the in-process electrically conductive layers (44, 45') located between a vertically neighboring pair of first-type insulating layers 32 is removed by the isotropic etch process.

[0260] Each portion of the at least one conductive fill material filling a respective one of the lateral recesses 43 (i.e., each in-process electrically conductive layers (44, 45')) is divided into a respective pair of a first-type electrically conductive layer 46A and a second-type

electrically conductive layer 46B that are disjoined from, and are vertically spaced from, each other. A second-type insulating layer 36 is located between a vertically-neighboring pair of a first-type electrically conductive layer 46A and a second-type electrically conductive layer 46B. Each first-type electrically conductive layer 46A comprises, from bottom to top, an optional first conductive barrier liner 44 and a first conductive fill material layer 45A. Each second-type electrically conductive layer 46B comprises, from bottom to top, a second conductive fill material layer 45B and an optional second conductive barrier liner 44. The first conductive fill material layer 46A and the second conductive fill material 46B are in direct contact with horizontal surfaces of the second-type insulating layer 36.

[0261] A vertical repetition of multiple instances of a unit layer stack (32, 46A, 36, 46B) can be formed over the substrate (9, 10). The unit layer stack comprises, from bottom to top, a seamless insulating layer (such as a first-type insulating layer 32) that is free of any seam therein, a first-type electrically conductive layer 46A, a seamed insulating layer (such as a second-type insulating layer 36) including a horizontally-extending seam 36S therein, and a second-type electrically conductive layer 46B. The first photoresist layer 277 can be subsequently removed, for example, by ashing.

[0262] Referring to FIGS. 42A and 42B, a backside trench fill structure (74, 76) can be formed in each backside trench 79 as described above with respect to the first embodiment.

[0263] Referring to FIG. 43, an optional second photoresist layer 275 can be applied over the second exemplary structure, and can be lithographically patterned to cover the backside trench fill structures (74, 76) and the sacrificial via fill material portions 83. An isotropic etch process can be patterned to remove the sacrificial memory opening fill structures 48 and the sacrificial support opening fill structures 18. A memory cavity 49' is formed in each volume from which a sacrificial memory opening fill structure 48 is removed, and a support

cavity 19' is formed in each volume from which the sacrificial support opening fill structure 18 is removed. Alternatively, if the sacrificial via fill material portions 83 comprise a different material than the sacrificial memory opening fill structures 48 and the sacrificial support opening fill structures 18, then the sacrificial memory opening fill structures 48 and the sacrificial support opening fill structures 18 can be removed by selective etching without forming the second photoresist layer 275.

[0264] Referring to FIG. 44, proximal portions of the at least one conductive fill material in the electrically conductive layers (46A, 46B) can be removed from around the memory cavities 49' and the support cavities 19' to re-form the memory openings 49 and support openings 19. Remaining portions of the at least one conductive fill material of the electrically conductive layers (46A, 46B) and the insulating fill material of the second-type insulating layers 36 after removal of the proximal portions of the at least one conductive fill material from around the memory cavities 49' comprise layer stacks (32, 46A, 36, 46B) located within a volume of a respective one of the lateral recesses 43. The volume of the respective one of the lateral recesses 43 is filled with material portions comprising, from bottom to top, a first-type electrically conductive layer 46A, a seamed insulating layer (comprising the second-type insulating layer 36) including a horizontally-extending seam 36S therein, and a second-type electrically conductive layer 46B. Cylindrical surfaces of the second-type insulating layers 36 can be physically exposed around each of the memory openings 49 and the support openings 19. The second photoresist layer 275 (if present) can be subsequently removed, for example, by ashing.

[0265] Referring to FIG. 45, the processing steps of FIGS. 10B – 10F can be performed to form a memory opening fill structure 58 within each memory opening 49, and to form a support pillar structure 20 within each support opening 19. Generally, the volume of each

memory opening fill structure 58 may be greater than the volume of a memory cavity 49'. In one embodiment, the memory opening fill structures 58 can be formed within volumes of the memory cavities 49' and additional volumes of voids formed by removal of the proximal portions of the at least one conductive fill material. In one embodiment, the memory opening fill structures 58 may be formed by forming a memory film 50 including a respective vertical stack of memory elements within each of the memory cavities 49, forming a vertical semiconductor channel 60 over the memory film 50 within each of the memory cavities 49, and forming a drain region 63 at a top end of the vertical semiconductor channel 60 within each of the memory cavities 49.

[0266] Referring to FIG. 46, an optional third photoresist layer 273 can be applied over the second exemplary structure, and can be lithographically patterned to form openings in areas of the sacrificial via fill material portions 83. An etch process such as a wet etch process can be performed to remove the sacrificial via fill material portions 83 selective to the materials of the second-type insulating layers 36 and the electrically conductive layers 46. Alternatively, the third photoresist layer 273 may be omitted and the sacrificial via fill material portions 83 can be removed by selective etching.

[0267] Referring to FIG. 47, a first isotropic etch process can be performed to remove physically exposed portions of the second-type insulating layer 36 from around the contact via cavities 81. A second isotropic etch process can be performed to remove physically exposed portions of the electrically conductive layers (46A, 46B) from around the contact via cavities 81. Alternatively, an anisotropic etch process may be performed using the third photoresist layer as a mask. Vertically-extending portions of the at least one conductive fill material of the electrically conductive layers (46A, 46B) are removed from the periphery of the contact via cavities 81. A top surface of a respective underlying second-type electrically

conductive layer 46B can be physically exposed underneath each of the contact via cavities 81.

[0268] Each adjoined pair of a first-type electrically conductive layer 46A and a second-type electrically conductive layer 46B are physically disjoined from each other upon removal of the vertically-extending portions of the at least one conductive fill material from the periphery of the contact via cavities 81. Within each instance of a unit layer stack (32, 46A, 36, 46B), an entirety of a bottom surface of the second-type insulating layer 36 is in direct contact with a top surface of the first conductive fill material layer 45A, and an entirety of a bottom surface of the second conductive fill material layer 45B is in direct contact with a top surface of the second-type insulating layer 36.

[0269] In one embodiment, within each instance of the unit layer stack, an entirety of a bottom surface of the first conductive fill material layer 45A is in direct contact with a top surface of the first conductive barrier liner 44 of the first electrically conductive layer 46A, and an entirety of a bottom surface of the second conductive barrier liner 44 is in direct contact with a top surface of the second conductive fill material layer 45B of the second electrically conductive layer 46B. In one embodiment, each instance of the first conductive fill material layer 45A and the second conductive fill material layer 45B has a same material composition (which is herein referred to as a conductive fill material composition) and a same thickness (which is herein referred to as a conductive fill material thickness). In one embodiment, each instance of the first conductive barrier liner 44 and the second conductive barrier liner 44 has a same material composition (which is herein referred to as a conductive liner composition) and a same thickness (which is herein referred to as a conductive liner thickness).

[0270] Referring to FIG. 48, an anisotropic etch process can be performed to vertically recess insulating fill material layers at the bottom of each of the contact via cavities 81. Physically exposed portions of the first-type insulating layers 32 can be removed from underneath each of the contact via cavities 81, and a top surface of a second-type electrically conductive layer 46B can be physically exposed at the bottom of the contact via cavities 81. The third photoresist layer 273 can be subsequently removed, for example, by ashing.

[0271] Referring to FIG. 49, a first conformal dielectric material layer can be conformally deposited and anisotropically etched using a sidewall spacer etch process to form outer dielectric tubular spacers 85O in peripheral regions of the contact via cavities 81. Each outer dielectric tubular spacer 85O contacts an annular top surface of a second-type electrically conductive layer 46B.

[0272] Referring to FIG. 50, a first conformal conductive material layer can be conformally deposited and anisotropically etched to form tubular contact via structures 86O on inner sidewalls of the outer dielectric tubular spacers 85O. In one embodiment, at least one tubular contact via structure 86O can vertically extend through at least one instance of a unit layer stack (32, 46A, 36, 46B), and can contact an annular top surface of a second-type electrically conductive layer 46B in an underlying instance of the unit layer stack (32, 46A, 36, 46B). In one embodiment, a tubular contact via structure 86O contacts a second conductive barrier liner 44 of an underlying instance of the unit layer stack (32, 46A, 36, 46B), and does not contact the second conductive fill material layer 45B of the underlying instance of the unit layer stack (32, 46A, 36, 46B).

[0273] Referring to FIG. 51, a pair of a second-type electrically conductive layer 46B and a second-type insulating layer 36 can be anisotropically etched underneath each unfilled portion of the contact via cavities 81. A respective one of the second-type electrically

conductive layers 46B and a respective one of the seamed insulating layers (i.e., the second-type insulating layers 36) can be removed underneath an opening within each of the tubular contact via structures 86O. A top surface of a first-type electrically conductive layer 46A can be physically exposed underneath each contact via cavity 81.

[0274] Referring to FIGS. 52A and 52B, a second conformal dielectric material layer can be conformally deposited and anisotropically etched to form inner dielectric tubular spacers 85I on inner sidewalls of the tubular contact via structures 86O and on an annular top surface segment of a respective one of the first-type electrically conductive layers 45A.

[0275] A second conformal conductive material layer can be conformally deposited to form cylindrical contact via structures 86I on inner sidewalls of the inner dielectric tubular spacers 85I. In one embodiment, at least one cylindrical contact via structure 86I can vertically extend through at least one instance of a unit layer stack (32, 46A, 36, 46B), and can contact a top surface of a first-type electrically conductive layer 46A in an underlying instance of the unit layer stack (32, 46A, 36, 46B). The tubular contact via structure 86O contacts a second conductive fill material layer 45B of an underlying instance of the unit layer stack (32, 46A, 36, 46B). The tubular contact via structure 86O surrounds the inner dielectric tubular spacers 85I, and the inner dielectric tubular spacers 85I surround the cylindrical contact via structures 86I. Therefore, the cylindrical contact via structures 86I do not contact the respective tubular contact via structures 86O.

[0276] FIGS. 53A – 53F are schematic vertical cross-sectional view of an alternative embodiment of the second exemplary structure according to alternative configuration of the second embodiment.

[0277] Referring to FIG. 53A, the outer dielectric tubular spacers 85O are formed in peripheral regions of the contact via cavities 81 of the second exemplary structure of FIG. 47

without performing the anisotropic etch of FIG. 48. The outer dielectric tubular spacers 85O may be formed using the process described above with respect to FIG. 49. Each outer dielectric tubular spacer 85O contacts an annular top surface of a first-type insulating layer 32.

[0278] Referring to FIG. 53B, an anisotropic etch is performed to vertically recess one pair of a respective first-type insulating layer 32 and a respective second-type electrically conductive layer 46B using the outer dielectric tubular spacers 85O as a mask to form first extension regions 81F. A respective second-type insulating layer 36 is exposed at the bottom of the first extension regions 81F of the contact via cavities 81. Sidewalls of the respective second-type electrically conductive layer 46B are exposed at the sidewall of the first extension regions 81F of the contact via cavities 81. The first extension regions 81F are narrower than the respective contact via cavities 81 by about two times the thickness of the outer dielectric tubular spacer 85O.

[0279] Referring to FIG. 53C, a first conformal conductive material layer 86L can be conformally deposited on inner sidewalls of the outer dielectric tubular spacers 85O and on the sidewalls of the first extension regions 81F. The first conformal conductive material layer 86L contacts the sidewalls of the respective second-type electrically conductive layer 46B which are exposed at the sidewall of the respective first extension regions 81F below the outer dielectric tubular spacers 85O. A middle conformal dielectric layer 85L, such as a silicon oxide layer, is deposited on the first conformal conductive material layer 86L.

[0280] Referring to FIG. 53D, the middle conformal dielectric layer 85L and the first conformal conductive material layer 86L are anisotropically etched using a sidewall spacer etch to form respective middle dielectric tubular spacers 85M and the outer tubular contact via structure 86O. The anisotropic etch may be extended after forming the spacers to punch

through the respective underlying second-type insulating layer 36 to form second extension regions 81S of the contact via cavities 81. The second extension regions 81S extend through the respective underlying second-type insulating layer 36 and expose a respective first-type electrically conductive layer 46A.

[0281] Referring to FIG. 53E, a third conformal dielectric material layer can be conformally deposited on the middle dielectric tubular spacers 85M and anisotropically etched to form inner dielectric tubular spacers 85I on inner sidewalls of the middle dielectric tubular spacers 85M and on an annular top surface segment of a respective one of the first-type electrically conductive layers 46A.

[0282] Referring to FIG. 53F, a second conformal conductive material layer can be conformally deposited into the remaining space in the contact via cavities 81 to form cylindrical contact via structures 86I on inner sidewalls of the inner dielectric tubular spacers 85I. In one embodiment, at least one cylindrical contact via structure 86I can vertically extend through at least one instance of a unit layer stack (32, 46A, 36, 46B), and can contact a surface of a first-type electrically conductive layer 46A exposed in the contact via cavity 81 in an underlying instance of the unit layer stack (32, 46A, 36, 46B).

[0283] In this embodiment, a tubular contact via structure 86O contacts a sidewall of a second conductive fill material layer 45B of an underlying instance of the unit layer stack (32, 46A, 36, 46B). Thus, the current can flow from the tubular contact via structure 86O through the sidewall of the second conductive fill material layer 45B (i.e., the second-type electrically conductive layer 46B). The middle and inner dielectric tubular spacers (85M, 85I) surround the cylindrical contact via structures 86I. Therefore, the cylindrical contact via structures 86I do not contact the respective tubular contact via structures 86O.

[0284] Referring to all drawings related to the second embodiment of the present disclosure, a three-dimensional memory device is provided, which comprises: a vertical repetition of multiple instances of a unit layer stack, wherein the unit layer stack comprises, from bottom to top, a first-type insulating layer 32, a first-type electrically conductive layer 46A, a second-type insulating layer 36, and a second-type electrically conductive layer 46B; memory openings 49 vertically extending through the vertical repetition; memory opening fill structures 58 located within the memory openings 49, wherein each of the memory opening fill structures 58 comprises a respective vertical stack of memory elements; and a laterally insulated contact structure (86I, 85I, 86O, 85O) comprising: a tubular contact via structure 86O vertically extending through at least one instance of the unit layer stack and contacting an annular top surface of the second-type electrically conductive layer 46B in an underlying instance of the unit layer stack; and a cylindrical contact via structure 86I laterally surrounded by the tubular contact via structure 86O and contacting an annular top surface of the first-type electrically conductive layer 46A in the underlying instance of the unit layer stack.

[0285] In one embodiment, the first-type electrically conductive layer 46A comprises a first conductive barrier liner 44 and a first conductive fill material layer 45A that overlies the first conductive barrier liner 44; and the second-type electrically conductive layer 46B comprises a second conductive fill material layer 45B and a second conductive barrier liner 44 that overlies the second conductive fill material layer.

[0286] In one embodiment, the cylindrical contact via structure 86I contacts the first conductive fill material layer 45A of the underlying instance of the unit layer stack and does not contact the first conductive barrier liner 44 of the underlying instance of the unit layer stack. The tubular contact via structure 86O contacts the second conductive barrier liner 44

of the underlying instance of the unit layer stack and does not contact the second conductive fill material layer 45B of the underlying instance of the unit layer stack.

[0287] In one embodiment, the laterally insulated contact structure (86I, 85I, 86O, 85O) comprises an outer dielectric tubular spacer 85O laterally surrounding the tubular contact via structure 86O and contacting an additional annular top surface of the second-type electrically conductive layer 48B in the underlying instance of the unit layer stack.

[0288] In one embodiment, the laterally-insulated contact structure (86I, 85I, 86O, 85O) comprises an inner dielectric tubular spacer 85I laterally surrounded by the tubular contact via structure 86O, laterally surrounding the cylindrical contact via structure 86I, and contacting a sidewall of the second-type electrically conductive layer 46B in the underlying instance of the unit layer stack, a sidewall of the second-type insulating layer 36 in the underlying instance of the unit layer stack, and an annular top surface of the first-type electrically conductive layer 46A in the underlying instance of the unit layer stack.

[0289] In one embodiment, within each instance of the unit layer stack, an entirety of a bottom surface of the second-type insulating layer 36 is in direct contact with a top surface of the first conductive fill material layer 45A; and an entirety of a bottom surface of the second conductive fill material layer 45B is in direct contact with a top surface of the second-type insulating layer 36. In one embodiment, within each instance of the unit layer stack: an entirety of a bottom surface of the first conductive fill material layer 45A is in direct contact with a top surface of the first conductive barrier liner 44; and an entirety of a bottom surface of the second conductive barrier liner 44 is in direct contact with a top surface of the second conductive fill material layer 45B.

[0290] In one embodiment, each of the memory opening fill structures 58 comprises a vertical semiconductor channel 60 and a memory film 50 containing the vertical stack of

memory elements. In one embodiment, at least one of the tubular contact via structure 86O and the cylindrical contact via structure 86I comprises a conductive material having a different material composition than the conductive fill material composition of the instances of the first conductive fill material layer 45A and the second conductive fill material layer 45B.

[0291] In one embodiment, within each instance of the unit layer stack, the first-type insulating layer 32 comprises a seamless insulating layer that is free of any seam therein; and the second-type insulating layer 36 comprises a seamed insulating layer including a horizontally-extending seam therein.

[0292] In one embodiment, each of the memory opening fill structures 58 is laterally spaced from the horizontally-extending seams of instances of the seamed insulating layers by a respective seamless portion of the seamed insulating layers 36.

[0293] In one embodiment, the horizontally-extending seam within the seamed insulating layer 36 is equidistant from a horizontal interface between the seamed insulating layer 36 and the second-type electrically conductive layer 46B; and from a horizontal interface between the seamed insulating layer 36 and the first-type electrically conductive layer 46A.

[0294] In one embodiment, the three-dimensional memory device comprises: a first backside trench fill structure (74, 76) comprising a first dielectric surface contacting first sidewalls of each layer within the vertical repetition and laterally extending along a first horizontal direction hd1; and a second backside trench fill structure (74, 76) comprising a second dielectric surface contacting second sidewalls of each layer within the vertical repetition laterally extending along the first horizontal direction hd1, and laterally spaced from the first backside trench fill structure (74, 76) along a second horizontal direction hd1.

[0295] Referring to FIGS. 54A and 54B, a third exemplary structure according to a third embodiment of the present disclosure is illustrated, which can be the same as the first exemplary structure illustrated in FIGS. 4A and 4B. Specifically, memory openings 49 and support openings 19 can be formed in the same manner as in the first embodiment.

[0296] Referring to FIG. 55, at least one sacrificial fill material can be deposited in each of the memory openings 49 and the support openings 19. For example, a first sacrificial fill material layer, a second sacrificial fill material layer, and a third sacrificial fill material layer can be sequentially deposited in the memory openings 49 and the support openings 19, and excess portions of the first sacrificial fill material layer, the second sacrificial fill material layer, and the third sacrificial fill material layer can be removed from the horizontal plane including a top surface of a topmost first-type insulating layer 32 by a planarization process, which may employ a chemical mechanical polishing (CMP) process or a recess etch process. In one embodiment, the material of the first sacrificial fill material layer may include a material that can be removed selective to the material of the second sacrificial fill material layer. Further, the material of the third sacrificial fill material layer may include a material that can be removed selective to the material of the second sacrificial fill material layer.

[0297] Each remaining portion of the at least one sacrificial fill material in a memory opening 49 constitutes a sacrificial memory opening fill structure 48. Each remaining portion of the at least one sacrificial fill material in a support opening 19 constitutes a sacrificial support opening fill structure 18. In one embodiment, each of the sacrificial memory opening fill structures 48 and the support opening fill structures 18 can comprise a respective set of a first sacrificial fill material portion 481 that is a remaining portion of the first sacrificial fill material layer, a second sacrificial fill material portion 482 that is a remaining portion of the second sacrificial fill material layer, and a third sacrificial fill material portion 483 that is a

remaining portion of the third sacrificial fill material layer. Alternatively, only two sacrificial fill material portions may be included.

[0298] In an illustrative example, the first sacrificial fill material portions 481 may comprise a semiconductor material such as amorphous silicon, the second sacrificial fill material portions 482 may comprise a dielectric material such as silicon oxide, and the third sacrificial fill material portions 483 may comprise a carbon material such as amorphous carbon or diamond-like carbon. In one embodiment, the lateral thickness between an inner sidewall and an outer sidewall of each first sacrificial fill material portion 481 may be the same as, or may be about the same as, the thickness of at least one conductive fill material to be subsequently deposited to form electrically conductive layers.

[0299] Generally, each of the sacrificial memory opening fill structures 48 may comprise a first sacrificial fill material portion 481 comprising a first sacrificial fill material and having a tubular shape, a second sacrificial fill material portion 482 comprising a second sacrificial fill material and laterally surrounded by the first sacrificial fill material portion 481, and a third sacrificial fill material portion 483 having a cylindrical shape and comprising a third sacrificial fill material and laterally surrounded by the second sacrificial fill material portion 482.

[0300] In an alternative embodiment, each of the sacrificial memory opening fill structures 48 and the support opening fill structures 18 can comprise a single sacrificial material. For example, each of the sacrificial memory opening fill structures 48 and the support opening fill structures 18 can consist essentially of amorphous silicon.

[0301] Referring to FIGS. 56A and 56B, the processing steps of FIGS. 6A and 6B can be performed to form backside trenches 79 and source regions 61. Sidewalls of the multiple instances of the unit layer stack (32, 42) are physically exposed to the backside trenches 79.

[0302] Referring to FIG. 57, the sacrificial material layers 42 can be removed selective to the first-type insulating layers 32 by introducing an isotropic etchant that etches the material of the sacrificial material layers 42 selective to the material of the first-type insulating layers into the backside trenches 79. Lateral recesses 43 are formed in volumes from which the sacrificial material layers 42 are removed. The removal of the second material of the sacrificial material layers 42 can be selective to the first material of the first-type insulating layers 32, the material of the sacrificial retro-stepped dielectric material portion 67, the semiconductor material of the semiconductor material layer 10, and the material of the sacrificial memory opening fill structures 48 and the support opening fill structures 18 (e.g., the material of the first sacrificial fill material portions 481). In one embodiment, the sacrificial material layers 42 can include silicon nitride, the materials of the first-type insulating layers 32 and the sacrificial retro-stepped dielectric material portion 67 can be selected from silicon oxide and dielectric metal oxides, and the materials of the sacrificial memory opening fill structures 48 and the support opening fill structures 18 (e.g., the material of the first sacrificial fill material portions 481) can include amorphous silicon.

[0303] In an illustrative example, if the sacrificial material layers 42 include silicon nitride, the etch process can be a wet etch process in which the exemplary structure is immersed within a wet etch tank including phosphoric acid, which etches silicon nitride selective to silicon oxide, silicon, and various other materials employed in the art. The sacrificial retro-stepped dielectric material portion 67, the sacrificial memory opening fill structures 48, and the sacrificial support opening fill structures 18 provide structural support while the lateral recesses 43 are present within volumes previously occupied by the sacrificial material layers 42.

[0304] Referring to FIG. 58, cylindrical portions of the sacrificial memory opening fill structures 48 and the sacrificial support opening fill structure 18 are recessed around each of the lateral recesses 43. In one embodiment, cylindrical regions of each first sacrificial fill material portion 481 exposed in the backside recesses 43 can be removed from each of the sacrificial memory opening fill structures 48 and the sacrificial support opening fill structures 18 through each backside recess 43 by performing an isotropic etch process that etches the material of the first sacrificial fill material portions 481 selective to the material of the second sacrificial fill material portions 482. In one embodiment, an isotropic etchant that etches the first sacrificial fill material selective to the second sacrificial fill material can be performed to remove the cylindrical regions of each first sacrificial fill material portion 481 selective to the second sacrificial fill material portions 482. In an illustrative example, the first sacrificial fill material can include amorphous silicon, the second sacrificial fill material can include silicon oxide, and the isotropic etchant can include hot trimethyl-2 hydroxyethyl ammonium hydroxide (“hot TMY”) or tetramethyl ammonium hydroxide (TMAH).

[0305] Alternatively, if the sacrificial memory opening fill structures 48 and the sacrificial support opening fill structures 18 comprise a single material (e.g., amorphous silicon), then a timed lateral selective etch may be performed to etch (i.e., recess) only the outer portions of the sacrificial memory opening fill structures 48 and the sacrificial support opening fill structures 18.

[0306] Referring to FIG. 59, the optional liner 44 and the conductive fill material layer 45' can be deposited at peripheral portions of the lateral recesses 43, as described above with respect to FIGS 9C and 9H. In this embodiment, the steps of FIGS. 9D to 9G may be omitted. The deposited at least one conductive fill material constitutes an in-process electrically conductive layer (44, 45'). In one embodiment, proximal portions of the at least

one conductive fill material of the in-process electrically conductive layer (44, 45') can be deposited within volumes from which a material of the sacrificial memory opening fill structures 48 and the support opening fill structures 18 (such as the material of the cylindrical portions of the first sacrificial fill material portions 481) is removed.

[0307] Referring to FIG. 60, an insulating fill material can be deposited over the at least one conductive fill material (44, 45') within remaining volumes of the lateral recesses 43 by a conformal deposition process, as described above with respect to FIG. 9I. The insulating fill material includes an insulating material, such as undoped silicate glass or a doped silicate glass. The thickness of the insulating fill material can be selected such that a horizontal seam 36S is formed at each levels of the lateral recesses 43. The deposited insulating fill material forms an insulating fill material layer 36L.

[0308] Referring to FIG. 61, an etch-back process can be performed to recess the insulating fill material layer 36L, as described above with respect to FIG. 9J. Remaining portions of the insulating fill material that remain in volumes of the lateral recesses 43 after recessing the insulating fill material from inside the backside trenches 79 comprise seamed insulating layers comprising a respective horizontally-extending seam 36S therein. The seamed insulating layers are herein referred to as second-type insulating layers 36. The second-type insulating layers 36 may include the same material as, or may include a material that is different from, the material of the first-type insulating layers 32. In one embodiment, the horizontally-extending seam 36S within each second-type insulating layer 36 can be equidistant from a horizontal plane including a top surface of the second-type insulating layer 36 and from a horizontal plane including a bottom surface of the second-type insulating layer 36.

[0309] Referring to FIG. 62, proximal portions of the at least one conductive fill material of the in-process electrically conductive layers (44, 45') can be removed from around the backside trenches 79 by performing an isotropic etch process that etches the conductive materials of the in-process electrically conductive layers (44, 45'). In one embodiment, the isotropic etch process may be a wet etch process that etches the conductive materials of the in-process electrically conductive layers (44, 45') selective to the materials of the insulating layers (32, 36). The duration of the isotropic etch process can be selected such that each vertically-extending portion of the in-process electrically conductive layers (44, 45') located between a vertically neighboring pair of first-type insulating layers 32 is removed by the isotropic etch process.

[0310] Each portion of the at least one conductive fill material filling a respective one of the lateral recesses 43 (i.e., each in-process electrically conductive layers (44, 45')) is divided into a respective pair of a first-type electrically conductive layer 46A and a second-type electrically conductive layer 46B that are disjoined from, and are vertically spaced from, each other. A second-type insulating layer 36 is located between a vertically-neighboring pair of a first-type electrically conductive layer 46A and a second-type electrically conductive layer 46B. Each first-type electrically conductive layer 46A comprises, from bottom to top, a first conductive barrier liner 44 and a first conductive fill material layer 45A. Each second-type electrically conductive layer 46B comprises, from bottom to top, a second conductive fill material layer 45B and a second conductive barrier liner 44. The first conductive fill material layer 46A and the second conductive fill material 46B are in direct contact with horizontal surfaces of the second-type insulating layer 36.

[0311] A vertical repetition of multiple instances of a unit layer stack (32, 46A, 36, 46B) can be formed over the substrate (9, 10). The unit layer stack comprises, from bottom to top,

a seamless insulating layer (such as a first-type insulating layer 32) that is free of any seam therein, a first-type electrically conductive layer 46A, a seamed insulating layer including a horizontally-extending seam 36S therein (such as a second-type insulating layer 36), and a second-type electrically conductive layer 46B.

[0312] Referring to FIG. 63, the backside trench fill structure (74, 76) can be formed in each respective backside trench 79, as described above with respect to the first embodiment. In one embodiment, each of the first backside trench fill structure (74, 76) and the second backside trench fill structure (74, 76) has a respective laterally-undulating vertical cross-sectional profile in a vertical plane that is perpendicular to the first horizontal direction hd1, and each of the first backside trench fill structure (74, 76) and the second backside trench fill structure (74, 76) has a greater width at levels of the first-type electrically conductive layers 46A, the seamless insulating layers (i.e., the first-type insulating layers 32), and the second-type electrically conductive layers 46B than at levels of the seamed insulating layers (i.e., the second-type insulating layers 36).

[0313] In one embodiment, each horizontally-extending seam 36S within the seamed insulating layers 36 is in direct contact with a respective one of the first dielectric surface and the second dielectric surface. In one embodiment, each of the first backside trench fill structure (74, 76) and the second backside trench fill structure (74, 76) comprises a backside contact via structure 76 contacting a respective source region 61 in the substrate (9, 10), and an insulating spacer 74 laterally surrounding the backside contact via structure 76 and comprising a respective one of the first dielectric surface and the second dielectric surface as an outer surface.

[0314] Referring to FIG. 64, the third sacrificial fill material portions 483 can be removed from the sacrificial memory opening fill structures 48 and the sacrificial support opening fill

structures 18. For example, an isotropic removal process can be performed to remove the material of the third sacrificial fill material portions 483 in the sacrificial memory opening fill structures 48 and the sacrificial support opening fill structures 18 selective to the material of the second sacrificial fill material portions 482. In an illustrative example, if the third sacrificial fill material portions 483 comprise amorphous carbon, an ashing process can be employed to remove the third sacrificial fill material portions 483. A memory cavity 49' or a support cavity 19' is formed in each volume from which a third sacrificial fill material portion 483 is removed.

[0315] Referring to FIG. 65, the second sacrificial fill material portions 482 of the sacrificial memory opening fill structures 48 and the sacrificial support opening fill structures 18 can be removed. For example, if second sacrificial fill material portions 482 comprise silicon oxide, a wet etch process employing dilute hydrofluoric acid can be performed to remove the second sacrificial fill material portions 482.

[0316] Referring to FIG. 66, the first sacrificial fill material portions 481 of the sacrificial memory opening fill structures 48 and the sacrificial support opening fill structures 18 can be removed. For example, if first sacrificial fill material portions 481 comprise amorphous silicon, a wet etch process employing hot trimethyl-2 hydroxyethyl ammonium hydroxide ("hot TMY") or tetramethyl ammonium hydroxide (TMAH) can be performed to remove the first sacrificial fill material portions 481. The entirety of the sacrificial memory opening fill structures 48 and the support opening fill structures 18 can be removed. Voids are formed within the volumes of the memory cavities 49 and the support cavities 19.

[0317] In the alternative embodiment in which the sacrificial memory opening fill structures 48 and the support opening fill structures 18 include only one material, such as amorphous silicon, the steps of FIGS. 64 and 65 may be omitted. Instead, the entire

remaining portions of the sacrificial memory opening fill structures 48 and the support opening fill structures 18 are removed in one etching step described above with respect to FIG. 66.

[0318] Referring to FIG. 67, an etch process that etches the materials of the electrically conductive layers (46A, 46B) selective to the materials of the insulating layers (32, 36) and the sacrificial retro-stepped dielectric material portion 67 can be performed. Proximal portions of the at least one conductive fill material of the first-type electrically conductive layers 46A and the second-type electrically conductive layers 46B can be removed from around the memory cavities 49 and the support cavities 19. In one embodiment, voids are formed within volumes of the memory openings 49 and within volumes of the support openings 19. In other words, the volumes of the memory cavities 49 can include the volumes of the memory openings 49 as formed at the processing steps of FIGS. 54A and 54B, and the volumes of the support cavities 19 can include the volumes of the support openings 19 as formed at the processing steps of FIGS. 54A and 54B. Sidewalls of the second-type insulating layers 36 (which include the deposited insulating fill material) are physically exposed after removing the proximal portions of the at least one conductive fill material from around the memory cavities 49.

[0319] Referring to FIG. 68, the processing steps of FIGS. 10B – 10F can be performed to form a memory opening fill structure 58 within each memory opening 49, and to form a support pillar structure 20 within each support cavities 19. In one embodiment, the memory opening fill structures 58 can be formed within volumes of the memory cavities 49, and the support pillars 20 can be formed within the volumes of the support openings 19. In one embodiment, the memory opening fill structures 58 may be formed by forming a memory film 50 including a respective vertical stack of memory elements within each of the memory

cavities 49, forming a vertical semiconductor channel 60 over the memory film 50 within each of the memory cavities 49, and forming a drain region 63 at a top end of the vertical semiconductor channel 60 within each of the memory cavities 49.

[0320] Referring to FIG. 69, the processing steps of FIG. 16 can be performed to remove the sacrificial retro-stepped dielectric material portion 67 selective to the materials of the first-type insulating layers 32, the electrically conductive layers (46A, 46B), the memory opening fill structures 58, and the support pillar structures 20.

[0321] Referring to FIG. 70, the processing steps of FIG. 17 can be performed.

[0322] Referring to FIGS. 71A and 71B, the processing steps of FIGS. 18A – 18C, 19A – 19C, and 20A – 20C can be performed to pattern the stepped surfaces in the contact region 300, to form a retro-stepped dielectric material portion 65, and to form various contact via structures (88, 85A, 85B). The three-dimensional memory device may comprise a retro-stepped dielectric material portion 65 overlying stepped surfaces of the vertically repetition of a unit layer stack (32, 46A, 36, 46B), first-type contact via structures 86A vertically extending through the retro-stepped dielectric material portion 65 and contacting a top surface of a respective instance of the first-type electrically conductive layer 46A, and second-type contact via structures 86B vertically extending through the retro-stepped dielectric material portion 65 and contacting a top surface of a respective instance of the second-type electrically conductive layer 86B.

[0323] Referring to FIG. 72, an alternative configuration of the third exemplary structure according to the third embodiment of the present disclosure can be derived from the third exemplary structure by employing a non-conformal deposition process at the processing step of FIG. 60 to deposit an insulating fill material layer 36L. In this case, at least one instance, or each instance, of the seamed insulating layers (i.e., the second-type insulating layers 36)

comprises the air gap 39 that is free of any solid phase material and is encapsulated by a dielectric material layer (i.e., one of the second-type insulating layers 36). The dielectric material layer has an upper horizontally-extending portion and a lower horizontally-extending portion that are adjoined to each other at a periphery of the air gap 39 at a respective horizontally-extending seam 36S.

[0324] In one alternative configuration of the third exemplary structure, the memory opening fill structures 58 comprises a respective laterally-undulating outer sidewall that extends through each layer within the vertical repetition (32, 46A, 36, 46B) and laterally protrudes outward at levels of the first-type electrically conductive layers 46A, the second-type electrically conductive layers 46B, and the levels of the first-type insulating layers 32 relative to levels of the second-type (seamed) insulating layers 36, similar to that shown in FIG. 13. In other words, the second-type (seamed) insulating layers 36 protrude inwards into the laterally-undulating outer sidewall of the memory opening fill structures 58. This decreases neighboring word line interference.

[0325] In another alternative configuration of the third exemplary structure, the second-type (seamed) insulating layers 36 have a different thickness than the first-type insulating layers 32. For example, the second-type (seamed) insulating layers 36 are thinner (e.g., 20 to 100% thinner) than the first-type insulating layers 32. This decreases the overall thickness of the vertical repetition.

[0326] Referring to all drawings related to the third embodiment of the present disclosure, a three-dimensional memory device is provided, which comprises: a vertical repetition of multiple instances of a unit layer stack, wherein the unit layer stack comprises, from bottom to top, a first-type insulating layer 32, a first-type electrically conductive layer 46A comprising a first conductive barrier liner 44 and a first conductive fill material layer

45A, a second-type insulating layer 36, and a second-type electrically conductive layer 46B comprising a second conductive fill material layer 45B and a second conductive barrier liner 44; memory openings 49 vertically extending through the vertical repetition; and memory opening fill structures 58 located within the memory openings 49, wherein each of the memory opening fill structures 58 comprises a respective vertical stack of memory elements. The first conductive fill material layer 45A and the second conductive fill material layer 45B are in direct contact with horizontal surfaces of the second-type insulating layer 36. The first conductive barrier liner 44 is in direct contact with a horizontal surface of the first-type insulating layer 32. The second conductive barrier liner 44 is in direct contact with a horizontal surface of another first-type insulating layer 32 of an adjacent unit layer stack.

[0327] In one embodiment, within each instance of the unit layer stack: an entirety of a bottom surface of the second-type insulating layer 36 is in direct contact with a top surface of the first conductive fill material layer 45A; and an entirety of a bottom surface of the second conductive fill material layer 45B is in direct contact with a top surface of the second-type insulating layer 36.

[0328] In one embodiment, within each instance of the unit layer stack: an entirety of a bottom surface of the first conductive fill material layer 45A is in direct contact with a top surface of the first conductive barrier liner 44; and an entirety of a bottom surface of the second conductive barrier liner 44 is in direct contact with a top surface of the second conductive fill material layer 45B.

[0329] In one embodiment, each instance of the first conductive fill material layer 45A and the second conductive fill material layer 45B has a same conductive fill material composition and a same conductive fill material thickness. In one embodiment, each instance

of the first conductive barrier liner 44 and the second conductive barrier liner 44 has a same conductive liner composition and a same conductive liner thickness.

[0330] In one embodiment, within each instance of the unit layer stack: the first-type insulating layer 32 comprises a seamless insulating layer that is free of any seam therein; and the second-type insulating layer 36 comprises a seamed insulating layer including a horizontally-extending seam 36S therein.

[0331] In one embodiment, each of the memory opening fill structures 58 is laterally spaced from the horizontally-extending seams 36S by a respective seamless portion of the seamed insulating layers 36.

[0332] In one embodiment, the horizontally-extending seam within the seamed insulating layer 36 in each instance of the unit layer stack is equidistant from a horizontal interface between the seamed insulating layer 36 and the second-type electrically conductive layer 46B; and from a horizontal interface between the seamed insulating layer 36 and the first-type electrically conductive layer 46A.

[0333] In one embodiment, the three-dimensional memory device comprises: a first backside trench fill structure (74, 76) comprising a first dielectric surface contacting first sidewalls of each layer within the vertical repetition and laterally extending along a first horizontal direction hd1; and a second backside trench fill structure (74, 76) comprising a second dielectric surface contacting second sidewalls of each layer within the vertical repetition laterally extending along the first horizontal direction hd1, and laterally spaced from the first backside trench fill structure (74, 76) along a second horizontal direction hd2.

[0334] In one embodiment, each of the first backside trench fill structure (74, 76) and the second backside trench fill structure (74, 76) has a respective laterally-undulating vertical cross-sectional profile in the second horizontal direction hd2; and each of the first backside

trench fill structure (74, 76) and the second backside trench fill structure (74, 76) has a greater width at levels of the first-type electrically conductive layers 46A, the seamless insulating layers 32, and the second-type electrically conductive layers 46B than at levels of the seamed insulating layers 36.

[0335] In one embodiment, each horizontally-extending seam 36S within the seamed insulating layers 36 is in direct contact with a respective one of the first dielectric surface and the second dielectric surface.

[0336] In one embodiment, each of the first backside trench fill structure (74, 76) and the second backside trench fill structure (74, 76) comprises: a backside contact via structure 76 contacting a respective source region 61 in the substrate (9, 10); and an insulating spacer 74 laterally surrounding the backside contact via structure 76 and comprising a respective one of the first dielectric surface and the second dielectric surface as an outer surface.

[0337] In one embodiment, at least one instance of the seamed insulating layers 36 comprises an air gap 39 encapsulated by a dielectric material layer having an upper horizontally-extending portion and a lower horizontally-extending portion that are adjoined to each other at a periphery of the air gap at a respective horizontally-extending seam 36S. In one embodiment, the seams may be spaced from the retro-stepped dielectric material portion 65 in a first area of a staircase region, and may contact the retro-stepped dielectric material portion 65 in a second area of the staircase region.

[0338] The various exemplary structures can include a three-dimensional memory device. In one embodiment, the three-dimensional memory device comprises a three-dimensional NAND memory device. The electrically conductive layers 46 can comprise, or can be electrically connected to, a respective word line of the three-dimensional NAND memory device.

[0339] Referring to FIG. 73, a fourth exemplary structure according to the fourth embodiment of the present disclosure may be derived from the first exemplary structure illustrated in FIG. 2 by modifying a unit layer stack of the first exemplary structure. Specifically, the unit layer stack as modified in the fourth exemplary structure includes, from bottom to top or from top to bottom, a cavity-free insulating layer 32, a first nucleation seed liner 47, a sacrificial material layer 42, and a second nucleation seed liner 47. Each cavity-free insulating layer 32 can be the same as a first-type insulating layer 32 in the first exemplary structure. Each sacrificial material layer 42 can be the same as a sacrificial material layer 42 in the first exemplary structure.

[0340] According to an aspect of the present disclosure, each of the first nucleation seed layers 47 and the second nucleation seed layers 47 comprises a non-metallic material that can be subsequently employed as a nucleation layer for the purpose of deposition of electrically conductive layers which include a metal material. For example, each of the first nucleation seed layers 47 and the second nucleation seed layers 47 comprises a non-metallic material that can be subsequently employed as a nucleation layer for deposition of a transition metal that may be deposited by a selective metal deposition process that grows the transition metal from nucleation seed layer surfaces and suppresses deposition of the transition metal from dielectric surfaces, such as the surfaces of the cavity-free insulating layers 32. In an illustrative example, the transition metal may be tungsten, ruthenium, or molybdenum. In one embodiment, the non-metallic material of the first nucleation seed layers 47 and the second nucleation seed layers 47 may comprise, and/or may consist essentially of, at least one material selected from silicon, germanium, and boron. For example, the first nucleation seed layers 47 and the second nucleation seed layers 47 may comprise, and/or may consist essentially of, amorphous silicon, amorphous germanium, boron, an amorphous silicon-

germanium alloy, boron-doped silicon, boron-doped germanium, or a boron-doped silicon-germanium alloy. The thickness of each of the first nucleation seed layers 47 and the second nucleation seed layers 47 may be in a range from 0.3 nm to 3.0 nm, such as from 0.6 nm to 2.0 nm, although lesser and greater thicknesses may also be employed. The first nucleation seed layers 47 and the second nucleation seed layers 47 may be deposited, for example, by chemical vapor deposition.

[0341] Referring to FIG. 74, the processing steps of FIG. 3 can be performed with needed changes to form stepped surfaces and a sacrificial retro-stepped dielectric material portion 67. In this case, the anisotropic etch process that form the stepped surfaces can be modified to etch the first nucleation seed layers 47 and the second nucleation seed layers 47 in addition to the cavity-free insulating layers 32 and the sacrificial material layers 42.

[0342] Referring to FIGS. 75A and 75B, the processing steps of FIGS. 4A and 4B can be performed with any needed changes to form memory openings 49 and support openings 19. The steps of the anisotropic etch process may be modified to etch through the first nucleation seed layers 47 and the second nucleation seed layers 47 in addition to the cavity-free insulating layers 32 and the sacrificial material layers 42.

[0343] FIGS. 76A – 76H are sequential vertical cross-sectional views of a region between a memory opening and a sacrificial backside trench fill structure during formation of memory opening fill structures according to the fourth embodiment of the present disclosure.

[0344] Referring to FIG. 76A, a memory openings 49 is illustrated after the processing steps of FIGS. 75A and 75B.

[0345] Referring to FIG. 76B, a surface oxidation process can be performed to convert physically exposed portions of the sacrificial material layers 42 into tubular dielectric oxide liners 421. A thermal oxidation process or a plasma oxidation process may be performed to

convert surface portions of the sacrificial material layers 42 into the tubular dielectric oxide liners 421. In an illustrative example, if the sacrificial material layers 42 comprise, and/or consists essentially of, silicon nitride, the tubular dielectric oxide liners 421 may comprise silicon oxide or silicon oxynitride liners. The lateral thickness of the tubular dielectric oxide liners 421 (as measured between an outer cylindrical sidewall and an inner cylindrical sidewall) may be in a range from 0.5 nm to 4 nm, such as from 1 nm to 3 nm, although lesser and greater thicknesses may also be employed.

[0346] Referring to FIG. 76C, a stack of layers including a dielectric metal oxide blocking dielectric layer 51, a silicon oxide blocking dielectric layer 52, a memory material layer 54, a dielectric material liner 56, and an optional sacrificial cover material layer 601 can be sequentially deposited in the memory openings 49 by a respective conformal deposition process.

[0347] The dielectric metal oxide blocking dielectric layer 51 can be formed employing a conformal deposition process. The dielectric metal oxide blocking dielectric layer 51 consists essentially of at least one dielectric metal oxide material. The thickness of the dielectric metal oxide blocking dielectric layer 51 can be in a range from 1 nm to 20 nm, although lesser and greater thicknesses can also be employed. The dielectric metal oxide blocking dielectric layer 51 can subsequently function as a dielectric material portion that blocks leakage of stored electrical charges to control gate electrodes. In one embodiment, the dielectric metal oxide blocking dielectric layer 51 includes aluminum oxide. In one embodiment, the dielectric metal oxide blocking dielectric layer 51 can include multiple dielectric metal oxide layers having different material compositions.

[0348] The silicon oxide blocking dielectric layer 52 can include silicon oxide. The thickness of the silicon oxide blocking dielectric layer 52 can be in a range from 1 nm to 20

nm, although lesser and greater thicknesses can also be employed.

[0349] Subsequently, the memory material layer 54 can be deposited as a continuous material layer by a conformal deposition process such as a chemical vapor deposition process or an atomic layer deposition process. The memory material layer 54 includes a memory material, i.e., a material that can store data by selecting a state of the material. For example, the memory material layer 54 may include a charge storage material such as silicon nitride, polysilicon, or a metallic material, a ferroelectric material that can store information in the form of ferroelectric polarization direction, or any other memory material that can store data by altering electrical resistivity.

[0350] The memory material layer 54 can be formed as a single memory material layer of homogeneous composition, or can include a stack of multiple memory material layers. In one embodiment, the memory material layer 54 may comprise an insulating charge trapping material, such as one or more silicon nitride segments. The memory material layer 54 can be formed, for example, by chemical vapor deposition (CVD), atomic layer deposition (ALD), physical vapor deposition (PVD), or any suitable deposition technique for storing electrical charges therein. The thickness of the memory material layer 54 can be in a range from 2 nm to 20 nm, although lesser and greater thicknesses can also be employed.

[0351] The dielectric material liner 56 includes a dielectric material. The dielectric material liner 56 can be formed on the memory material layer 54 employing a conformal deposition process. In one embodiment, the dielectric material liner 56 comprises a tunneling dielectric layer through which charge tunneling can be performed under suitable electrical bias conditions. The charge tunneling may be performed through hot-carrier injection or by Fowler-Nordheim tunneling induced charge transfer depending on the mode of operation of the monolithic three-dimensional NAND string memory device to be formed. The dielectric

material liner 56 can include silicon oxide, silicon nitride, silicon oxynitride, dielectric metal oxides (such as aluminum oxide and hafnium oxide), dielectric metal oxynitride, dielectric metal silicates, alloys thereof, and/or combinations thereof. In one embodiment, the dielectric material liner 56 can include a stack of a first silicon oxide layer, a silicon oxynitride layer, and a second silicon oxide layer, which is commonly known as an ONO stack. In one embodiment, the dielectric material liner 56 can include a silicon oxide layer that is substantially free of carbon or a silicon oxynitride layer that is substantially free of carbon. The thickness of the dielectric material liner 56 can be in a range from 2 nm to 20 nm, although lesser and greater thicknesses can also be employed.

[0352] The optional sacrificial cover material layer 601 includes a sacrificial material that can be subsequently removed selective to the material of the dielectric material liner 56. In one embodiment, the sacrificial cover material layer 601 can include a semiconductor material such as amorphous silicon, or may include a carbon-based material such as amorphous carbon or diamond-like carbon (DLC). The sacrificial cover material layer 601 can be formed by a conformal deposition method such as low pressure chemical vapor deposition (LPCVD). The thickness of the sacrificial cover material layer 601 can be in a range from 2 nm to 10 nm, although lesser and greater thicknesses can also be employed. A memory cavity 49' is formed in the volume of each memory opening 49 that is not filled with the deposited material layers (52, 54, 56, 601).

[0353] Referring to FIG. 76D, horizontal portions of the optional sacrificial cover material layer 601, the dielectric material liner 56, the memory material layer 54, the silicon oxide blocking dielectric layer 52, and the dielectric metal oxide blocking dielectric layer 51 are sequentially anisotropically etched by performing at least one anisotropic etch process. The portions of the sacrificial cover material layer 601, the dielectric material liner 56, the

memory material layer 54, the silicon oxide blocking dielectric layer 52, and the dielectric metal oxide blocking dielectric layer 51 located above the top surface of the topmost cavity-free insulating layer 32 can be removed by the at least one anisotropic etch process. Further, the horizontal portions of the sacrificial cover material layer 601, the dielectric material liner 56, the memory material layer 54, the silicon oxide blocking dielectric layer 52, and the dielectric metal oxide blocking dielectric layer 51 at a bottom of each memory cavity 49' can be removed to form openings in remaining portions thereof. Each of the sacrificial cover material layer 601, the dielectric material liner 56, the memory material layer 54, the silicon oxide blocking dielectric layer 52, and the dielectric metal oxide blocking dielectric layer 51 can be etched by a respective anisotropic etch process employing a respective etch chemistry, which may, or may not, be the same for the various material layers.

[0354] Each remaining portion of the sacrificial cover material layer 601 can have a tubular configuration. The memory material layer 54 can comprise a charge trapping material, a floating gate material, a ferroelectric material, a resistive memory material that can provide at least two different levels of resistivity (such as a phase change material), or any other memory material that can store information by a change in state. In one embodiment, each memory material layer 54 can include a vertical stack of charge storage regions that store electrical charges upon programming. In one embodiment, the memory material layer 54 can be a memory material layer in which each portion adjacent to the sacrificial material layers 42 constitutes a charge storage region.

[0355] Optionally, the physically exposed semiconductor surface at the bottom of each memory cavity 49' can be vertically recessed so that the recessed semiconductor surface underneath the memory cavity 49' is vertically offset from the topmost surface of the semiconductor material layer 10 by a recess distance. A set of a dielectric metal oxide

blocking dielectric layer 51, a silicon oxide blocking dielectric layer 52, a memory material layer 54, and a dielectric material liner 56 in a memory opening 49 constitutes a memory film 50, which includes a vertical stack of memory elements (comprising the memory material layer 54) that are insulated from surrounding materials by a dielectric metal oxide blocking dielectric layer 51, a silicon oxide blocking dielectric layer 52, and a dielectric material liner 56. In one embodiment, the sacrificial cover material layer 601, the dielectric material liner 56, the memory material layer 54, the silicon oxide blocking dielectric layer 52, and the dielectric metal oxide blocking dielectric layer 51 can have vertically coincident sidewalls. The sacrificial cover material layer 601 can be subsequently removed selective to the material of the dielectric material liner 56. In case the sacrificial cover material layer 601 includes a semiconductor material, a wet etch process employing hot trimethyl-2 hydroxyethyl ammonium hydroxide (“hot TMY”) or tetramethyl ammonium hydroxide (TMAH) can be performed to remove the sacrificial cover material layer 601.

[0356] Referring to FIG. 76E, a semiconductor channel layer 60L can be deposited directly on the semiconductor surface of the semiconductor material layer 10, and directly on the dielectric material liner 56. The semiconductor channel layer 60L includes a semiconductor material such as at least one elemental semiconductor material, at least one III-V compound semiconductor material, at least one II-VI compound semiconductor material, at least one organic semiconductor material, or other semiconductor materials known in the art. In one embodiment, the semiconductor channel layer 60L includes amorphous silicon or polysilicon. The semiconductor channel layer 60L can have a doping of a first conductivity type, which is the same as the conductivity type of the semiconductor material layer 10. The semiconductor channel layer 60L can be formed by a conformal deposition method such as low pressure chemical vapor deposition (LPCVD). The thickness

of the semiconductor channel layer 60L can be in a range from 2 nm to 10 nm, although lesser and greater thicknesses can also be employed. The semiconductor channel layer 60L may partially fill the memory cavity 49' in each memory opening, or may fully fill the cavity in each memory opening.

[0357] Referring to FIG. 76F, in case the memory cavity 49' in each memory opening is not completely filled by the semiconductor channel layer 60L, a dielectric core layer 62L can be deposited in the memory cavity 49' to fill any remaining portion of the memory cavity 49' within each memory opening. The dielectric core layer 62L includes a dielectric material such as silicon oxide or organosilicate glass. The dielectric core layer 62L can be deposited by a conformal deposition method such as low pressure chemical vapor deposition (LPCVD), or by a self-planarizing deposition process such as spin coating.

[0358] Referring to FIG. 76G, the horizontal portion of the dielectric core layer 62L can be removed, for example, by a recess etch process such that each remaining portions of the dielectric core layer 62L is located within a respective memory opening 49 and has a respective top surface below the horizontal plane including the top surface of the topmost cavity-free insulating layer 32. Each remaining portion of the dielectric core layer 62L constitutes a dielectric core 62.

[0359] Referring to FIG. 76H, a doped semiconductor material having a doping of a second conductivity type can be deposited within each recessed region above the dielectric cores 62. The deposited semiconductor material can have a doping of a second conductivity type that is the opposite of the first conductivity type. For example, if the first conductivity type is p-type, the second conductivity type is n-type, and vice versa. The dopant concentration in the deposited semiconductor material can be in a range from $5.0 \times 10^{18}/\text{cm}^3$ to $2.0 \times 10^{21}/\text{cm}^3$, although lesser and greater dopant concentrations can also be employed.

The doped semiconductor material can be, for example, doped polysilicon.

[0360] Excess portions of the deposited semiconductor material having a doping of the second conductivity type and a horizontal portion of the semiconductor channel layer 60L can be removed from above the horizontal plane including the top surface of the topmost cavity-free insulating layer 32, for example, by chemical mechanical planarization (CMP) or a recess etch process. Each remaining portion of the doped semiconductor material having a doping of the second conductivity type constitutes a drain region 63. Each remaining portion of the semiconductor channel layer 60L (which has a doping of the first conductivity type) constitutes a vertical semiconductor channel 60. The vertical semiconductor channel 60 is formed directly on the dielectric material liner 56.

[0361] A dielectric material liner 56 is surrounded by a memory material layer 54, and laterally surrounds a portion of the vertical semiconductor channel 60. Each adjoining set of a dielectric metal oxide blocking dielectric layer 51, a silicon oxide blocking dielectric layer 52, a memory material layer 54, and a dielectric material liner 56 collectively constitute a memory film 50, which can store electrical charges or ferroelectric polarization with a macroscopic retention time. As used herein, a macroscopic retention time refers to a retention time suitable for operation of a memory device as a permanent memory device such as a retention time in excess of 24 hours.

[0362] Each combination of a memory film 50 and a vertical semiconductor channel 60 within a memory opening 49 constitutes a memory stack structure 55. The memory stack structure 55 is a combination of a semiconductor channel, a dielectric material liner, a plurality of memory elements comprising portions of the memory material layer 54, and optional blocking dielectric layers (51, 52). An entire set of material portions that fills a memory opening 49 is herein referred to as a memory opening fill structure 58. An entire set

of material portions that fills a support opening 19 constitutes a support pillar structure.

[0363] Generally, a memory opening fill structure 58 can be formed in each memory opening 49. The memory opening fill structure 58 comprises a dielectric metal oxide blocking dielectric layer 51, a silicon oxide blocking dielectric layer 52, a memory material layer 54, an optional dielectric material liner 56, and a vertical semiconductor channel 60. A dielectric material liner 56 may laterally surround the vertical semiconductor channel 60. The memory material layer 54 can laterally surround the dielectric material liner 56.

[0364] Referring to FIG. 77, the fourth exemplary structure is illustrated after formation of memory opening fill structures 58 and support pillar structure 20 within the memory openings 49 and the support openings 19, respectively. An instance of a memory opening fill structure 58 can be formed within each memory opening 49 of the structure of FIGS. 75A and 75B. An instance of the support pillar structure 20 can be formed within each support opening 19 of the structure of FIGS. 75A and 75B.

[0365] Each memory stack structure 55 includes a vertical semiconductor channel 60 and a memory film 50. While the present disclosure is described employing the illustrated configuration for the memory stack structure 55, the methods of the present disclosure can be applied to alternative memory stack structures including different layer stacks or structures for the memory film 50 and/or for the vertical semiconductor channel 60.

[0366] Referring to FIGS. 78A and 78B, the processing steps of FIGS. 6A and 6B can be performed to form backside trenches 79 and source regions 61.

[0367] Referring to FIGS. 79A and 79B, an etchant that selectively etches the second material of the sacrificial material layers 42 with respect to the materials of the cavity-free insulating layers 32, the first nucleation seed layers 47, the second nucleation seed layers 47, and the tubular dielectric oxide liners 421 can be introduced into the backside trenches 79, for

example, employing an isotropic etch process. Backside recesses 43 are formed in volumes from which the sacrificial material layers 42 are removed. The removal of the second material of the sacrificial material layers 42 can be selective to the material of the cavity-free insulating layers 32, the material of the sacrificial retro-stepped dielectric material portion 67, the semiconductor material of the semiconductor material layer 10, and the material of the tubular dielectric oxide liners 421 (which may include, for example, silicon oxide). In one embodiment, the sacrificial material layers 42 can include silicon nitride, and the materials of the cavity-free insulating layers 32 and the sacrificial retro-stepped dielectric material portion 67 can be selected from silicon oxide and dielectric metal oxides.

[0368] The etch process that removes the second material selective to the cavity-free insulating layers 32 and the tubular dielectric oxide liners 421 can be a wet etch process employing a wet etch solution, or can be a gas phase (dry) etch process in which the etchant is introduced in a vapor phase into the backside trenches 79. For example, if the sacrificial material layers 42 include silicon nitride, the etch process can be a wet etch process in which the fourth exemplary structure is immersed within a wet etch tank including phosphoric acid, which etches silicon nitride selective to silicon oxide, silicon, and various other materials employed in the art. The support pillar structure 20, the sacrificial retro-stepped dielectric material portion 67, and the memory opening fill structures 58 provide structural support while the backside recesses 43 are present within volumes previously occupied by the sacrificial material layers 42.

[0369] Each backside recess 43 can be a laterally extending cavity having a lateral dimension that is greater than the vertical extent of the cavity. In other words, the lateral dimension of each backside recess 43 can be greater than the height of the backside recess 43. A plurality of backside recesses 43 can be formed in the volumes from which the sacrificial

material layers 42 are removed. In one embodiment, the memory array region 100 comprises an array of monolithic three-dimensional NAND strings having a plurality of device levels disposed above the substrate (9, 10). In this case, each backside recess 43 can define a space for receiving a respective word line of the array of monolithic three-dimensional NAND strings.

[0370] Each of the plurality of backside recesses 43 can extend substantially parallel to the top surface of the substrate (9, 10). A backside recess 43 can be vertically bounded by a top surface of an underlying first nucleation seed layer 47 and a bottom surface of an overlying nucleation seed layer 47. In one embodiment, each backside recess 43 can have a uniform height throughout.

[0371] FIGS. 80A – 80D are sequential vertical cross-sectional views of a region around a memory opening 49 and a backside trench 79 during formation of electrically conductive layers 46 and cavity-containing insulating layers 36 according to the fourth embodiment of the present disclosure.

[0372] Referring to FIG. 80A, an isotropic etch process can be performed to remove the tubular dielectric oxide liners 421 selective to the dielectric metal oxide blocking dielectric layers 51, the first nucleation seed layers 47, and the second nucleation seed layers 47. For example, if the tubular dielectric oxide liners 421 comprise silicon oxide and if the dielectric metal oxide blocking dielectric layers 51 comprise aluminum oxide, a wet etch process employing dilute hydrofluoric acid can be performed to etch the tubular dielectric oxide liners 421 selective to the dielectric metal oxide blocking dielectric layers 51, the first nucleation seed layers 47, and the second nucleation seed layers 47.

[0373] Referring to FIG. 80B, a selective metal deposition process can be performed to grow electrically conductive layers 46 from the first nucleation seed layers 47 and the second

nucleation seed layers 47. According to an aspect of the present disclosure, the materials of the first nucleation seed layers 47 and the second nucleation seed layers 47 can be employed as a nucleation material that induces nucleation of the metal of the electrically conductive layers 46. The selective metal deposition grows metal only from surfaces of a pre-existing metallic material or from surfaces of the nucleation seed layers 47. Thus, the selective metal deposition does not grow the metal from the physically exposed surfaces of the memory opening fill structures 58 or the support pillar structures 20, or from the sidewalls of the cavity-free insulating layers 32 that are not covered with any nucleation seed layer 47. The precursor gas for deposition of the metal can be selected such that the precursor gas does not form a metal film directly on dielectric surfaces (such as the surfaces of the cavity-free insulating layers 32) in the absence of a nucleation material (such as the material of the nucleation seed layers 47) or a pre-existing metallic material.

[0374] In an illustrative example, each of the first nucleation seed layers 47 and the second nucleation seed layers 47 comprises at least one material selected from silicon, germanium, or boron. The metal within the electrically conductive layers 46 may comprise, and/or may consist essentially of, tungsten, molybdenum, ruthenium, or cobalt. The first nucleation seed layers 47 and the second nucleation seed layers 47 function as catalysts for inducing nucleation of the metal of the electrically conductive layer 46. At the same time, the first nucleation seed layers 47 and the second nucleation seed layers 47 may form volatile compounds such as SiF_4 , GeF_4 , or B_2F_6 during exposure to the metal precursor gas that decomposes into the metal of the electrically conductive layers 46. Thus, a predominant fraction of the material of the nucleation seed layers 47 may be removed during the nucleation process.

[0375] According to an aspect of the present disclosure, the thicknesses of the first nucleation seed layers 47 and the second nucleation seed layers 47 can be selected such that a predominant fraction (such as more than 50 % and/or more than 90 % and/or more than 95 %) of the first nucleation seed layers 47 and the second nucleation seed layers 47 is removed during the growth process that forms the electrically conductive layers 46. Thus, the metallic material of the electrically conductive layers 46 is in direct contact with the horizontal surfaces and the sidewalls of the cavity-free insulating layers 32. The total atomic percentage of silicon, germanium, and boron in the surface portions of the electrically conductive layers 46 that contact the horizontal surfaces of the cavity-free insulating layers 32 may be in a range from 0.1 % to 5 %, such as from 0.2 % to 2 %, although lesser and greater atomic percentages may also be employed. The total atomic percentage of silicon, germanium, and boron in the surface portions of the electrically conductive layers 46 that contact the sidewalls of the cavity-free insulating layers 32 may be less than 1 part per million, i.e., less than 0.0001 %.

[0376] Generally, the electrically conductive layers 46 can be formed by nucleating a metallic material on the first nucleation seed layers 47 and the second nucleation seed layers 47 while suppressing nucleation of the metallic material on physically exposed sidewall segments of the memory opening fill structures 58 and on physically exposed surfaces of the cavity-free insulating layers 32. The thickness of the electrically conductive layers 46 can be in a range from 20 % to 45 %, such as from 30 % to 40 %, of the height of the backside recesses 43 as provided at the processing steps of FIG. 80A. For example, the thickness of the electrically conductive layers 46 may be about 33 % of the height of the backside recesses 43 as provided at the processing steps of FIG. 80A.

[0377] Referring to FIG. 80C, an anisotropic etch process can be performed to remove portions of the electrically conductive layers 46 located outside of the volumes of the backside recesses 43 as formed at the processing steps of FIG. 80A. In other words, portions of the electrically conductive layers 46 overlying the topmost cavity-free insulating layer 32 or located within the volumes of the backside trenches 79 as formed at the processing steps of 78A and 78B. Remaining portions of the electrically conductive layers 46 comprise first-type electrically conductive layers 46A that fill a lower portion of a respective backside cavity 43, and second-type electrically conductive layers 46B that fill an upper portion of a respective backside cavity 43.

[0378] Referring to FIG. 80D, an insulating fill material such as silicon oxide or organosilicate glass can be anisotropically deposited within remaining volumes of the backside recesses 43. The anisotropic deposition of the insulating fill material can form encapsulated cavities (i.e., air gaps) 39 that are encapsulated by a respective horizontally-extending portion of the insulating fill material that fill a respective remaining volume of the backside trenches 43, and form a cavity-containing insulating layer 36. Each of the cavity-containing insulating layers 36 includes in an encapsulated cavity 39 therein. Each encapsulated cavity (i.e., air gap) 39 laterally surrounds a plurality of memory opening fill structures 58, and is laterally spaced from the memory opening fill structures 58 by tubular portions of a respective one of the cavity-containing insulating layers 36.

[0379] An anisotropic etch process can be performed to anisotropically etch the insulating fill material. Horizontally-extending portions of the insulting fill material can be removed from above the topmost cavity-free insulating layer 32 and from above the source regions 61. Remaining portions of the insulating fill material that remain in the backside

trenches 79 comprise insulating spacers 74. The insulating spacers 74 are connected to each of the cavity-containing insulating layers 36.

[0380] In one embodiment, each of the encapsulated cavities 39 is free of any solid phase material. Generally, an insulating material portion (such as the insulating spacers 74) comprising the same dielectric material as the cavity-containing insulating layers 36 can be formed at peripheral regions of the backside trenches 79. The insulating material portion can be connected to each of the cavity-containing insulating layers 36 without an interface between the insulating material portion and each of the cavity-containing insulating layers 36. In one embodiment, the insulating material portion comprises an insulating spacer 74.

[0381] A vertical repetition of a unit layer stack is formed over the substrate (9, 10). The unit layer stack includes a cavity-free insulating layer 32, a first-type electrically conductive layer 46A, a cavity-containing insulating layer 36, and a second-type electrically conductive layer 46B. The insulating spacer 74 can vertically extend through each layer within the vertical repetition of the unit layer stack (32, 46A, 36, 46B), and contacts a top surface of the substrate, which may be a top surface of a respective one of the source regions 61.

[0382] The anisotropic deposition process that forms the cavity-containing insulating layers 36 may form laterally-extending seams 36S at each interface at which a downward-growing portion of the insulating fill material and an upward-growing portion of the insulating fill material merge. Thus, each of the cavity-containing insulating layers 36 may comprise a respective laterally-extending seam 36S that may continuously extend from a respective one of the encapsulated cavities 36 through an insulating spacer 74 to inner sidewalls of the insulating spacers 74 (that are physically exposed to a void in the backside trenches 79 at this processing step).

[0383] In one embodiment, an insulating material portion (such as an insulating spacer 74) comprises a plurality of sidewalls that contact sidewalls of each of the cavity-free insulating layers 32, each of the first-type electrically conductive layers 46A, and each of the second-type electrically conductive layers 46B within the vertical repetition. In one embodiment, the first-type electrically conductive layers 46A and the second-type electrically conductive layers 46B consist essentially of a single metal, and each of the first-type dielectrically conductive layers 46A and the second-type electrically conductive layers 46B contact a horizontal surface of a respective one of the cavity-free insulating layers 32 and a horizontal surface of a respective one of the cavity-containing insulating layers 36.

[0384] In one embodiment, each of the memory opening fill structures 58 comprises: a dielectric metal oxide blocking dielectric layer 51 in contact with each layer within the vertical repetition (32, 46A, 36, 46B); and a silicon oxide blocking dielectric layer 52 surrounded by the dielectric metal oxide blocking dielectric layer 51 and laterally enclosing a respective vertical stack of memory elements (such as portions of a memory material layer 54 located at levels of the electrically conductive layers (46A, 46B)).

[0385] In one embodiment, the dielectric metal oxide blocking dielectric layer 51 comprises a straight sidewall that vertically extends from a top surface of a topmost layer within the vertical repetition (32, 46A, 36, 46B) to a bottom surface of a bottommost layer within the vertical repetition (32, 46A, 36, 46B).

[0386] Referring to FIGS. 81A and 81B, the processing steps of FIG. 11D can be performed to form a backside contact via structure 76 within each unfilled volume of the backside trenches 79. In this case, each insulating spacer 74 can laterally surround a backside contact via structure 76. Each backside contact via structure 76 can vertically extend through each layer within the vertical repetition (32, 46A, 36, 46B), and can a top surface of the

substrate such as a top surface of a source region 61. In one embodiment, each of the cavity-containing insulating layers 36 comprises a respective laterally-extending seam 36S that continuously extends from a respective one of the encapsulated cavities 36 through an insulating spacer 74 and to a backside contact via structure 76.

[0387] Referring to FIGS. 82A – 82C, the processing steps of FIGS. 16, 17, 18A – 18C, 19A – 19C can be performed to remove the sacrificial retro-stepped dielectric material portion 67, to pattern additional steps in the vertically repetition of the unit layer stack (32, 46A, 36, 46B) to physically exposed edge portions of the top surfaces of the first-type electrically conductive layers 46A, and to form a retro-stepped dielectric material portion 65. The retro-stepped dielectric material portion 65 overlies, and contacts, stepped surface of the vertical repetition. The first-type electrically conductive layers 46A, the second-type electrically conductive layers 46B, and the cavity-free insulating layers 32 are free of lateral recesses and contact the retro-stepped dielectric material portion 65. Upon removal of the sacrificial retro-stepped material portion 67, at least one of the encapsulated cavities 39 may become connected to the void formed by removal of the sacrificial retro-stepped dielectric material portion 67. In this case, the retro-stepped dielectric material portion 65 may fill a peripheral region of at least one encapsulated cavity 39. In this case, the cavity-containing insulating layers 36 may comprise lateral recesses into which a dielectric material of the retro-stepped dielectric material portion 65 laterally protrude.

[0388] Subsequently, the processing steps of FIGS. 20A – 20C can be performed to form various contact via structures (88, 86A, 86B).

[0389] A fifth exemplary structure can be derived from the fourth exemplary structure by omitting formation of nucleation seed layers 47 in the unit layer stack, and instead depositing the nucleation seed layers physically exposed surfaces of the cavity-free insulating layers 32

in the backside recesses 43 while suppressing formation of the nucleation seed layers from physically exposed surfaces of the dielectric metal oxide blocking dielectric layers 51 of the memory opening fill structures 58 or the support pillar structures 20.

[0390] Referring to FIG. 83, the fifth exemplary structure according to the fifth embodiment of the present disclosure may be the same as the first exemplary structure illustrated in FIG. 2.

[0391] Referring to FIG. 84, the processing steps of FIG. 3 can be performed to form stepped surfaces and a sacrificial retro-stepped dielectric material portion 67. The fifth exemplary structure of FIG. 84 may be the same as the first exemplary structure of FIG. 3.

[0392] Referring to FIGS. 85A and 85B, the processing steps of FIGS. 4A and 4B can be performed to form memory openings 49 and support openings 19. The fifth exemplary structure of FIGS. 85A and 85B may be the same as the first exemplary structure of FIGS. 4A and 4B.

[0393] FIGS. 86A – 86H are sequential vertical cross-sectional views of a region between a memory opening and a sacrificial backside trench fill structure during formation of memory opening fill structures according to the fifth embodiment of the present disclosure. The processing steps of FIGS. 76A – 76H may be performed with any needed changes to form a memory opening fill structure 58 within each memory opening 49 and to form a support pillar structure 20 within each support opening 19. Changes in the processing steps may be due to the absence of the nucleation seed layers 47 in the fifth exemplary structure relative to the fourth exemplary structure.

[0394] Referring to FIG. 87, the fifth exemplary structure is illustrated after formation of memory opening fill structures 58 and support pillar structure 20 within the memory openings 49 and the support openings 19, respectively. An instance of a memory opening fill

structure 58 can be formed within each memory opening 49 of the structure of FIGS. 85A and 85B. An instance of the support pillar structure 20 can be formed within each support opening 19 of the structure of FIGS. 85A and 85B.

[0395] Each memory stack structure 55 includes a vertical semiconductor channel 60 and a memory film 50. While the present disclosure is described employing the illustrated configuration for the memory stack structure 55, the methods of the present disclosure can be applied to alternative memory stack structures including different layer stacks or structures for the memory film 50 and/or for the vertical semiconductor channel 60.

[0396] Referring to FIGS. 88A and 88B, the processing steps of FIGS. 6A and 6B can be performed to form backside trenches 79 and source regions 61.

[0397] Referring to FIGS. 89A and 89B, an etchant that selectively etches the second material of the sacrificial material layers 42 with respect to the materials of the cavity-free insulating layers 32, and the tubular dielectric oxide liners 421 can be introduced into the backside trenches 79, for example, employing an isotropic etch process. Backside recesses 43 are formed in volumes from which the sacrificial material layers 42 are removed. The removal of the second material of the sacrificial material layers 42 can be selective to the material of the cavity-free insulating layers 32, the material of the sacrificial retro-stepped dielectric material portion 67, the semiconductor material of the semiconductor material layer 10, and the material of the tubular dielectric oxide liners 421 (which may include, for example, silicon oxide). In one embodiment, the sacrificial material layers 42 can include silicon nitride, and the materials of the cavity-free insulating layers 32 and the sacrificial retro-stepped dielectric material portion 67 can be selected from silicon oxide and dielectric metal oxides.

[0398] The etch process that removes the second material selective to the cavity-free

insulating layers 32 and the tubular dielectric oxide liners 421 can be a wet etch process employing a wet etch solution, or can be a gas phase (dry) etch process in which the etchant is introduced in a vapor phase into the backside trenches 79. For example, if the sacrificial material layers 42 include silicon nitride, the etch process can be a wet etch process in which the fifth exemplary structure is immersed within a wet etch tank including phosphoric acid, which etches silicon nitride selective to silicon oxide, silicon, and various other materials employed in the art. The support pillar structure 20, the sacrificial retro-stepped dielectric material portion 67, and the memory opening fill structures 58 provide structural support while the backside recesses 43 are present within volumes previously occupied by the sacrificial material layers 42.

[0399] FIGS. 90A – 90E are sequential vertical cross-sectional views of a region around a memory opening 49 and a backside trench 79 during formation of electrically conductive layers 46 and cavity-containing insulating layers 36 according to the fifth embodiment of the present disclosure.

[0400] Referring to FIG. 90A, an isotropic etch process can be performed to remove the tubular dielectric oxide liners 421 selective to the dielectric metal oxide blocking dielectric layers 51 and the cavity-free insulating layers 32. For example, if the cavity-free insulating layers 32 and the tubular dielectric oxide liners 421 comprise silicon oxide and if the dielectric metal oxide blocking dielectric layers 51 comprise aluminum oxide, a wet etch process employing dilute hydrofluoric acid can be performed to etch the tubular dielectric oxide liners 421 selective to the dielectric metal oxide blocking dielectric layers 51, the first nucleation seed layers 47, and the second nucleation seed layers 47.

[0401] Referring to FIG. 90B and according to an aspect of the present disclosure, an area selective deposition process is performed, which deposits a nucleation seed material on

physically exposed surfaces of the cavity-free insulating layers 32 while suppressing deposition of the nucleation seed material on the physically exposed surfaces of the dielectric metal oxide blocking dielectric layers 51. In one embodiment, aluminum oxide blocking dielectric layers 51 may have a fluorine terminated surface when silicon nucleation seed layers are deposited by plasma enhanced chemical vapor deposition using an argon/SiF₄/H₂ mixture. The fluorine terminated aluminum oxide surfaces inhibit silicon deposition. In contrast silicon oxide cavity-free insulating layers 32 may have exposed surfaces which are not terminated with fluorine or are terminated with a lower concentration of fluorine than the aluminum oxide surfaces. Thus, the nucleation seed layers 147 are selectively deposited on the exposed surfaces of the silicon oxide cavity-free insulating layers 32.

[0402] In one embodiment, the area selective deposition process utilizes different nucleation times that a deposition process has on different types of surfaces. Specifically, for the purpose of deposition of a nucleation seed material such as silicon, the insulating material (such as silicon oxide) of the cavity-free insulating layers 32 may have a shorter incubation time than the dielectric metal oxide material of the dielectric metal oxide blocking dielectric layers 51.

[0403] In one embodiment, a precursor gas for deposition of the nucleation seed material is flowed into a process chamber including the fifth exemplary structure for a duration of time that is greater than the incubation time of the nucleation seed material on the surfaces of the cavity-free insulating layers 32, and is shorter than the incubation time of the nucleation seed material on the surfaces of the dielectric metal oxide blocking dielectric layers 51. Optionally, a pulse of an etchant gas may be flowed into the process chamber to remove any atom of the nucleation seed material from the physically exposed surfaces of the dielectric metal oxide blocking dielectric layers 51 without etching a predominant fraction (such as

more than 50 %) of the nucleation seed material from the surfaces of the cavity-free insulating layers 32. The cycle of an exposure to the precursor gas for the nucleation seed material for a duration less than the incubation time of the nucleation seed material on the surfaces of the dielectric metal oxide blocking dielectric layers 51 and an exposure to a pulse of an etchant gas may be repeated multiple times to form a nucleation seed layer 147 on each physically exposed surface of the cavity-free insulating layers 32 while preventing formation of the nucleation seed layer 147 on surfaces of the dielectric metal oxide blocking dielectric layers 51.

[0404] The nucleation seed layers 147 comprise a non-metallic material that can be subsequently employed as a nucleation layer for the purpose of deposition of electrically conductive layers including a metallic material. For example, each of the nucleation seed layers 147 comprises a non-metallic material that can be subsequently employed as a nucleation layer for deposition of a transition metal that may be deposited by a selective metal deposition process that grows the transition metal from metallic surfaces and suppresses deposition of the transition metal from dielectric surfaces such as the surfaces of the cavity-free insulating layers 32. In an illustrative example, the transition metal may be tungsten, ruthenium, cobalt or molybdenum. In one embodiment, the non-metallic material of the nucleation seed layers 147 may comprise, and/or may consist essentially of, at least one material selected from silicon, germanium, and boron. For example, the nucleation seed layers 147 may comprise, and/or may consist essentially of, amorphous silicon, amorphous germanium, boron, an amorphous silicon-germanium alloy, boron-doped silicon, boron-doped germanium, or a boron-doped silicon-germanium alloy. The thickness of each of the nucleation seed layers 147 may be in a range from 0.3 nm to 3.0 nm, such as from 0.6 nm to 2.0 nm, although lesser and greater thicknesses may also be employed.

[0405] Referring to FIG. 90C, a selective metal deposition process can be performed to grow electrically conductive layers 46 from the nucleation seed layers 147. According to an aspect of the present disclosure, the materials of the nucleation seed layers 147 can be employed as a nucleation material that induces nucleation of the metal in the electrically conductive layers 46. The selective metal deposition grows metal only from surfaces of a pre-existing metallic material or from surfaces of the nucleation seed layers 147. Thus, the selective metal deposition does not grow the metal from the physically exposed surfaces of the memory opening fill structures 58 or the support pillar structures 20, or from the sidewalls of the cavity-free insulating layers 32 that are not covered with any nucleation seed layer 147. The precursor gas for deposition of the metal can be selected such that the precursor gas does not form a metal film directly on dielectric surfaces (such as the surfaces of the cavity-free insulating layers 32) in the absence of a nucleation material (such as the material of the nucleation seed layers 147) or a pre-existing metallic material.

[0406] In an illustrative example, each of the nucleation seed layers 147 comprises at least one material selected from silicon, germanium, or boron. The metal within the electrically conductive layers 46 may comprise, and/or may consist essentially of, tungsten, molybdenum, ruthenium, or cobalt. The nucleation seed layers 147 function as catalysts for inducing nucleation of the metal of the electrically conductive layer 46. At the same time, the nucleation seed layers 147 may form volatile compounds such as SiF_4 , GeF_4 , or B_2F_6 during exposure to the metal precursor gas that decomposes into the metal of the electrically conductive layers 46. Thus, a predominant fraction of the material of the nucleation seed layers 147 may be removed during the nucleation process.

[0407] According to an aspect of the present disclosure, the thicknesses of the nucleation seed layers 147 can be selected such that a predominant fraction (such as more than 50 %

and/or more than 90 % and/or more than 95 %) of the nucleation seed layers 147 is removed during the growth process that forms the electrically conductive layers 46. Thus, the metallic material of the electrically conductive layers 46 is in direct contact with the horizontal surfaces and the sidewalls of the cavity-free insulating layers 32. The total atomic percentage of silicon, germanium, and boron in the surface portions of the electrically conductive layers 46 that contact the horizontal surfaces of the cavity-free insulating layers 32 may be in a range from 0.1 % to 5 %, such as from 0.2 % to 2 %, although lesser and greater atomic percentages may also be employed.

[0408] Generally, the electrically conductive layers 46 can be formed by nucleating a metallic material on the nucleation seed layers 147 while suppressing nucleation of the metallic material on physically exposed sidewall segments of the memory opening fill structures 58. The thickness of the electrically conductive layers 46 can be in a range from 20 % to 45 %, such as from 30 % to 40 %, of the height of the backside recesses 43 as provided at the processing steps of FIG. 90A. For example, the thickness of the electrically conductive layers 46 may be about 33 % of the height of the backside recesses 43 as provided at the processing steps of FIG. 90A.

[0409] Referring to FIG. 90D, an anisotropic etch process can be performed to remove portions of the electrically conductive layers 46 located outside of the volumes of the backside recesses 43 as formed at the processing steps of FIG. 90A. In other words, portions of the electrically conductive layers 46 overlying the topmost cavity-free insulating layer 32 or located within the volumes of the backside trenches as formed at the processing steps of 78A and 78B. Remaining portions of the electrically conductive layers 46 comprise first-type electrically conductive layers 46A that fills a lower portion of a respective backside cavity 43 as formed at the processing steps of FIG. 90A and second-type electrically conductive layers

46B that fills an upper portion of a respective backside cavity 43 as formed at the processing steps of FIG. 90A.

[0410] Referring to FIG. 90E, an insulating fill material such as silicon oxide or organosilicate glass can be anisotropically deposited within remaining volumes of the backside recesses 43. The anisotropic deposition of the insulating fill material can form the encapsulated cavities (i.e., air gaps) 39 that are encapsulated by a respective horizontally-extending portion of the insulating fill material that fill a respective remaining volume of the backside trenches 43, and form the cavity-containing insulating layer 36.

[0411] An anisotropic etch process can be performed to anisotropically etch the insulating fill material. Horizontally-extending portions of the insulating fill material can be removed from above the topmost cavity-free insulating layer 32 and from above the source regions 61. Remaining portions of the insulating fill material that remain in the backside trenches 79 comprise insulating spacers 74. The insulating spacers 74 are connected to each of the cavity-containing insulating layers 36.

[0412] A vertical repetition of a unit layer stack is formed over the substrate (9, 10). The unit layer stack includes a cavity-free insulating layer 32, a first-type electrically conductive layer 46A, a cavity-containing insulating layer 36, and a second-type electrically conductive layer 46B. The insulating spacer 74 can vertically extend through each layer within the vertical repetition of the unit layer stack (32, 46A, 36, 46B), and contacts a top surface of the substrate, which may be a top surface of a respective one of the source regions 61.

[0413] Referring to FIGS. 91A – 91C, the processing steps of FIG. 11D can be performed to form a backside contact via structure 76 within each unfilled volume of the backside trenches 79. In this case, each insulating spacer 74 can laterally surround a backside contact via structure 76. Each backside contact via structure 76 can vertically extend through each

layer within the vertical repetition (32, 46A, 36, 46B), and can a top surface of the substrate such as a top surface of a source region 61. In one embodiment, each of the cavity-containing insulating layers 36 comprises a respective laterally-extending seam that continuously extends from a respective one of the encapsulated cavities 36 through an insulating spacer 74 and to a backside contact via structure 76.

[0414] Subsequently, the processing steps of FIGS. 16, 17, 18A – 18C, 19A – 19C can be performed to remove the sacrificial retro-stepped dielectric material portion 67, to pattern additional steps in the vertically repetition of the unit layer stack (32, 46A, 36, 46B) to physically exposed edge portions of the top surfaces of the first-type electrically conductive layers 46A, and to form a retro-stepped dielectric material portion 65. The retro-stepped dielectric material portion 65 overlies, and contacts, stepped surface of the vertical repetition. The first-type electrically conductive layers 46A, the second-type electrically conductive layers 46B, and the cavity-free insulating layers 32 are free of lateral recesses and contact the retro-stepped dielectric material portion 65. Upon removal of the sacrificial retro-stepped material portion 67, at least one of the encapsulated cavities 39 may become connected to the void formed by removal of the sacrificial retro-stepped dielectric material portion 67. In this case, the retro-stepped dielectric material portion 65 may fill a peripheral region of at least one encapsulated cavity 39. In this case, the cavity-containing insulating layers 36 may comprise lateral recesses into which a dielectric material of the retro-stepped dielectric material portion 65 laterally protrude.

[0415] Subsequently, the processing steps of FIGS. 20A – 20C can be performed to form various contact via structures (88, 86A, 86B).

[0416] Referring to FIG. 92A, an alternative embodiment of the fifth exemplary structure can be derived from the fifth exemplary structure of FIG. 90C by omitting the processing

steps of FIG. 90D and by depositing an insulating fill material to form an insulating fill material layer 36L. The insulating fill material layer 36L may include the same material as the cavity-containing insulating layers 36 and the insulating spacers 74 of the fifth exemplary structure illustrated in FIG. 90E.

[0417] Referring to FIG. 92B, an anisotropic etch process can be performed to remove portions of the electrically conductive layers 46 and the insulating fill material layer 36L from inside the backside trenches 79 and from above a topmost cavity-free insulating layer 32.

[0418] Referring to FIGS. 93A – 93C, an insulating material (such as silicon oxide) can be conformally deposited in the backside trenches 79 and can be anisotropically etched to form an insulating spacer 174 in each backside trench 79. The processing steps of FIG. 11D can be performed to form a backside contact via structure 76 within each unfilled volume of the backside trenches 79. In this case, each insulating spacer 74 can laterally surround a backside contact via structure 76. Each backside contact via structure 76 can vertically extend through each layer within the vertical repetition (32, 46A, 36, 46B), and can a top surface of the substrate such as a top surface of a source region 61. In one embodiment, each of the cavity-containing insulating layers 36 comprises a respective laterally-extending seam that continuously extends from a respective one of the encapsulated cavities 36 to an outer sidewall of an insulating spacer 74.

[0419] Subsequently, the processing steps of FIGS. 16, 17, 18A – 18C, 19A – 19C can be performed to remove the sacrificial retro-stepped dielectric material portion 67, to pattern additional steps in the vertically repetition of the unit layer stack (32, 46A, 36, 46B) to physically exposed edge portions of the top surfaces of the first-type electrically conductive layers 46A, and to form a retro-stepped dielectric material portion 65. The retro-stepped

dielectric material portion 65 overlies, and contacts, stepped surface of the vertical repetition. The first-type electrically conductive layers 46A, the second-type electrically conductive layers 46B, and the cavity-free insulating layers 32 are free of lateral recesses and contact the retro-stepped dielectric material portion 65. Upon removal of the sacrificial retro-stepped material portion 67, at least one of the encapsulated cavities 39 may become connected to the void formed by removal of the sacrificial retro-stepped dielectric material portion 67. In this case, the retro-stepped dielectric material portion 65 may fill a peripheral region of at least one encapsulated cavity 39. In this case, the cavity-containing insulating layers 36 may comprise lateral recesses into which a dielectric material of the retro-stepped dielectric material portion 65 laterally protrude.

[0420] Subsequently, the processing steps of FIGS. 20A – 20C can be performed to form various contact via structures (88, 86A, 86B).

[0421] According to various embodiments of the present disclosure, a three-dimensional memory device is provided, which comprises: a vertical repetition of multiple instances of a unit layer stack (32, 46A, 36, 46B), wherein the unit layer stack (32, 46A, 36, 46B) comprises, from bottom to top or from top to bottom, a cavity-free insulating layer 32 that is free of any cavity therein, a first-type electrically conductive layer 46A, a cavity-containing insulating layer 35 including an encapsulated cavity 39 therein, and a second-type electrically conductive layer 46A; memory openings 49 vertically extending through the vertical repetition; and memory opening fill structures 58 located within the memory openings 49, wherein each of the memory opening fill structures 58 comprises a respective vertical stack of memory elements.

[0422] The various embodiments of the present disclosure can be employed to provide vertical scaling of three-dimensional memory device including a vertical stack of insulating layers and electrically conductive layers.

[0423] Although the foregoing refers to particular preferred embodiments, it will be understood that the disclosure is not so limited. It will occur to those of ordinary skill in the art that various modifications may be made to the disclosed embodiments and that such modifications are intended to be within the scope of the disclosure. Compatibility is presumed among all embodiments that are not alternatives of one another. The word “comprise” or “include” contemplates all embodiments in which the word “consist essentially of” or the word “consists of” replaces the word “comprise” or “include,” unless explicitly stated otherwise. Where an embodiment employing a particular structure and/or configuration is illustrated in the present disclosure, it is understood that the present disclosure may be practiced with any other compatible structures and/or configurations that are functionally equivalent provided that such substitutions are not explicitly forbidden or otherwise known to be impossible to one of ordinary skill in the art. All of the publications, patent applications and patents cited herein are incorporated herein by reference in their entirety.

WHAT IS CLAIMED IS:

1. A three-dimensional memory device, comprising:

a vertical repetition of multiple instances of a unit layer stack, wherein the unit layer stack comprises, from bottom to top or from top to bottom, a cavity-free insulating layer that is free of any cavity therein, a first-type electrically conductive layer, a cavity-containing insulating layer including an encapsulated cavity therein, and a second-type electrically conductive layer;

memory openings vertically extending through the vertical repetition; and

memory opening fill structures located within the memory openings, wherein each of the memory opening fill structures comprises a respective vertical stack of memory elements.

2. The three-dimensional memory device of Claim 1, wherein each of the encapsulated cavity is laterally spaced from the memory opening fill structures by tubular portions of a respective one of the cavity-containing insulating layers.

3. The three-dimensional memory device of Claim 1, wherein each of the encapsulated cavities comprises an air gap which is free of any solid phase material.

4. The three-dimensional memory device of Claim 1, further comprising an insulating material portion comprising a same dielectric material as the cavity-containing insulating layers and connected to each of the cavity-containing insulating layers.

5. The three-dimensional memory device of Claim 4, wherein the insulating material portion

comprises an insulating spacer laterally surrounding a backside contact via structure that vertically extends through each layer within the vertical repetition.

6. The three-dimensional memory device of Claim 5, wherein each of the cavity-containing insulating layers comprises a respective laterally-extending seam that continuously extends from a respective one of the encapsulated cavities through the insulating spacer and to the backside contact via structure.

7. The three-dimensional memory device of Claim 4, wherein the insulating material portion comprises a plurality of sidewalls that contact sidewalls of each of the cavity-free insulating layers, each of the first-type electrically conductive layers, and each of the second-type electrically conductive layers within the vertical repetition.

8. The three-dimensional memory device of Claim 1, wherein:

the first-type electrically conductive layers and the second-type electrically conductive layers consist essentially of a single metal; and

each of the first-type dielectrically conductive layers and the second-type electrically conductive layers contacts a horizontal surface of a respective one of the cavity-free insulating layers and a horizontal surface of a respective one of the cavity-containing insulating layers.

9. The three-dimensional memory device of Claim 1, wherein each of the memory opening fill structures comprises:

a dielectric metal oxide blocking dielectric layer in contact with each layer within the

vertical repetition;

a silicon oxide blocking dielectric layer surrounded by the dielectric metal oxide blocking dielectric layer and laterally enclosing a respective vertical stack of memory elements; and

a vertical semiconductor channel surrounded by the vertical stack of memory elements.

10. The three-dimensional memory device of Claim 9, wherein the dielectric metal oxide blocking dielectric layer comprises a straight sidewall that vertically extends from a top surface of a topmost layer within the vertical repetition to a bottom surface of a bottommost layer within the vertical repetition.

11. The three-dimensional memory device of Claim 1, further comprising a retro-stepped dielectric material portion overlying, and contacting, stepped surface of the vertical repetition, wherein:

the first-type electrically conductive layers, the second-type electrically conductive layers, and the cavity-free insulating layers are free of lateral recesses and contact the retro-stepped dielectric material portion; and

the cavity-containing insulating layers comprises lateral recesses into which a dielectric material of the retro-stepped dielectric material portion laterally protrude.

12. A method of forming a three-dimensional memory device, comprising:

forming a vertical repetition of multiple instances of a unit layer stack over a substrate, wherein the unit layer stack comprises a cavity-free insulating layer, a first

nucleation seed liner, a sacrificial material layer, and a second nucleation seed liner;
forming memory openings vertically extending through the vertical repetition;
forming memory opening fill structures within the memory openings;
forming backside trenches through the vertical repetition;
removing the sacrificial material layers selective to the cavity-free insulating layers, the first nucleation seed layers, the second nucleation seed layers, and the memory opening fill structures, whereby backside recesses are formed in volumes from which the sacrificial material layers are removed;

forming electrically conductive layers by nucleating a metal material on the first nucleation seed layers and the second nucleation seed layers while suppressing nucleation of the metal material on physically exposed sidewall segments of the memory opening fill structures and on physically exposed surfaces of the cavity-free insulating layers; and

removing portions of the electrically conductive layers located outside of the backside recesses.

13. The method of Claim 12, further comprising depositing an insulating fill material within remaining volumes of the backside recesses, wherein portions of the insulating fill material that are deposited in the remaining volumes of the backside recesses to form cavity-containing insulating layers.

14. The method of Claim 13, further comprising anisotropically etching the insulating fill material, wherein remaining portions of the insulating fill material that remain in the backside trenches comprise insulating spacers that are connected to each of the cavity-containing insulating layers.

15. The method of Claim 14, wherein:

each of the cavity-containing insulating layers comprises an encapsulated cavity that laterally surrounds the memory opening fill structures and is laterally spaced from the memory opening fill structures by tubular portions of a respective one of the cavity-containing insulating layers; and

each of the cavity-containing insulating layers comprises a seam that continuously extends horizontally from a respective encapsulated cavity through the insulating spacers to inner sidewalls of the insulating spacers.

16. The method of Claim 12, wherein:

each of the memory opening fill structures comprises a dielectric metal oxide blocking dielectric layer in contact with each layer within the vertical repetition, a silicon oxide blocking dielectric layer surrounded by the dielectric metal oxide blocking dielectric layer and laterally enclosing a respective vertical stack of memory elements, and a vertical semiconductor channel surrounded by the vertical stack of memory elements; and

each of the first nucleation seed layers and the second nucleation seed layers comprises at least one material selected from silicon, germanium or boron, and is consumed during nucleation of the metal material such that the metal material is in direct contact with the insulating layers.

17. A method of forming a three-dimensional memory device, comprising:

forming a vertical repetition of multiple instances of a unit layer stack over a substrate, wherein the unit layer stack comprises a cavity-free insulating layer and a

sacrificial material layer;

forming memory openings vertically extending through the vertical repetition;

forming memory opening fill structures comprising a respective dielectric metal oxide

blocking dielectric layer within the memory openings;

forming backside trenches through the vertical repetition;

removing the sacrificial material layers selective to the cavity-free insulating layers and the memory opening fill structures, whereby backside recesses are formed in volumes from which the sacrificial material layers are removed, and wherein sidewalls of the dielectric metal oxide blocking dielectric layers are physically exposed to the backside recesses;

forming nucleation seed layers comprising a nucleation seed material on physically exposed surfaces of the insulating layers while suppressing deposition of the nucleation seed material on the physically exposed sidewalls of the dielectric metal oxide blocking dielectric layers;

forming electrically conductive layers by nucleating a metal material on the nucleation seed layers while suppressing nucleation of the metal material on the sidewalls of the dielectric metal oxide blocking dielectric layers; and

removing portions of the electrically conductive layers located outside of the backside recesses.

18. The method of Claim 17, further comprising depositing an insulating fill material within remaining volumes of the backside recesses, wherein portions of the insulating fill material that are deposited in the remaining volumes of the backside recesses to form cavity-containing insulating layers.

19. The method of Claim 18, further comprising:

anisotropically etching the insulating fill material, wherein remaining portions of the insulating fill material that remain in the backside trenches comprise insulating spacers that are connected to each of the cavity-containing insulating layers; and

forming backside contact via structures within remaining volumes of the backside trenches on physically exposed surface segments of the substrate and on inner sidewalls of the insulating spacers.

20. The method of Claim 17, wherein:

each of the memory opening fill structures further comprises a silicon oxide blocking dielectric layer surrounded by the dielectric metal oxide blocking dielectric layer and laterally enclosing a respective vertical stack of memory elements, and a vertical semiconductor channel surrounded by the vertical stack of memory elements; and

each of the first nucleation seed layers and the second nucleation seed layers comprises at least one material selected from silicon, germanium or boron, and is consumed during nucleation of the metal material such that the metal material is in direct contact with the insulating layers.

21. A three-dimensional memory device, comprising:

a vertical repetition of multiple instances of a unit layer stack, wherein the unit layer stack comprises, from bottom to top, a seamless insulating layer that is free of any seam therein, a first-type electrically conductive layer, a seamed insulating layer including a horizontally-extending seam therein, and a second-type electrically conductive layer;

memory openings vertically extending through the vertical repetition; and

memory opening fill structures located within the memory openings, wherein each of the memory opening fill structures comprises a respective vertical stack of memory elements.

22. The three-dimensional memory device of Claim 21, wherein:

each of the memory opening fill structures contacts a closed periphery of a respective horizontally-extending seam in each of the seamed insulating layers; and

each of the memory opening fill structures comprises a vertical semiconductor channel and a memory film containing the vertical stack of memory elements.

23. The three-dimensional memory device of Claim 21, wherein the horizontally-extending seam within the seamed insulating layer is equidistant from a horizontal interface between the seamed insulating layer and the second-type electrically conductive layer, and from a horizontal interface between the seamed insulating layer and the first-type electrically conductive layer.

24. The three-dimensional memory device of Claim 21, further comprising:

a first backside trench fill structure comprising a first dielectric surface contacting first sidewalls of each layer within the vertical repetition and laterally extending along a first horizontal direction; and

a second backside trench fill structure comprising a second dielectric surface contacting second sidewalls of each layer within the first vertical repetition, laterally extending along the first horizontal direction, and laterally spaced from the first backside trench fill structure along a second horizontal direction.

25. The three-dimensional memory device of Claim 24, wherein:

each of the first backside trench fill structure and the second backside trench fill structure has a respective laterally-undulating vertical cross-sectional profile in the second horizontal direction; and

each of the first backside trench fill structure and the second backside trench fill structure has a greater width at levels of the first-type electrically conductive layers, the seamed insulating layers, and the second-type electrically conductive layers than at levels of the seamless insulating layers.

26. The three-dimensional memory device of Claim 24, wherein each horizontally-extending seam within the seamed insulating layers is laterally spaced from, and does not contact, any of the first backside trench fill structure and the second backside trench fill structure.

27. The three-dimensional memory device of Claim 24, wherein each of the first backside trench fill structure and the second backside trench fill structure comprises:

a backside contact via structure contacting a respective source region in a substrate;
and

an insulating spacer laterally surrounding the backside contact via structure and comprising a respective one of the first dielectric surface and the second dielectric surface as an outer surface.

28. The three-dimensional memory device of Claim 21, wherein the seamed insulating layer comprises an air gap.

29. The three-dimensional memory device of Claim 28, wherein the air gap is encapsulated by a dielectric material layer having an upper horizontally-extending portion and a lower horizontally-extending portion that are adjoined to each other at a periphery of the air gap at a respective horizontally-extending seam.

30. The three-dimensional memory device of Claim 21, wherein within each instance of the unit layer stack:

the first-type electrically conductive layer comprises, from bottom to top, a first conductive barrier liner and a first conductive fill material layer; and

the second-type electrically conductive layer comprises, from bottom to top, a second conductive fill material layer and a second conductive barrier liner.

31. The three-dimensional memory device of Claim 30, wherein the first conductive fill material layer and the second conductive fill material layer are in direct contact with horizontal surfaces of the seamed insulating layer.

32. The three-dimensional memory device of Claim 21, wherein each of the memory opening fill structures comprises a respective straight outer sidewall that extends through each layer within the vertical repetition and contacts each layer within the vertical repetition.

33. The three-dimensional memory device of Claim 21, wherein each of the memory opening fill structures comprises a respective laterally-undulating outer sidewall that extends through each layer within the vertical repetition and laterally protrudes outward at levels of

the first-type electrically conductive layers and the second-type electrically conductive layers relative to levels of the seamed insulating layers and the seamless insulating layers.

34. A method of forming a three-dimensional memory device, comprising:

- forming a vertical repetition of multiple instances of a unit layer stack over a substrate, wherein the unit layer stack comprises an insulating layer and a sacrificial material layer;

- forming memory openings vertically extending through the vertical repetition;

- removing the sacrificial material layers selective to the insulating layers by introducing an isotropic etchant that etches a material of the sacrificial material layers selective to a material of the insulating layers into the memory openings, whereby lateral recesses are formed in volumes from which the sacrificial material layers are removed;

- depositing at least one conductive fill material at peripheral portions of the lateral recesses;

- depositing an insulating fill material over the at least one conductive fill material within remaining volumes of the lateral recesses;

- removing peripheral portions of the insulating fill material from inside the memory openings; and

- forming memory opening fill structures within volumes of the memory openings, wherein each of the memory opening fill structures comprises a respective vertical stack of memory elements.

35. The method of Claim 34, further comprising:

- forming backside trenches through the vertical repetition;

forming sacrificial backside trench fill structures within the backside trenches prior to formation of the lateral recesses;

removing the sacrificial backside trench fill structures after depositing the insulating fill material; and

laterally recessing proximal portions of the at least one conductive fill material from around the backside trenches, wherein each portion of the at least one conductive fill material filling a respective one of the lateral recesses is divided into a respective pair of a first-type electrically conductive layer and a second-type electrically conductive layer that are disjoined from and are vertically spaced from each other.

36. The method of Claim 35, wherein the at least one conductive fill material comprises:

a conductive barrier liner that is deposited directly on physically exposed surfaces of the insulating layers and on physically exposed sidewalls of the sacrificial backside trench fill structures; and

a conductive fill material layer that is deposited directly on the conductive barrier liner.

37. The method of Claim 35, wherein:

remaining portions of the insulating fill material that remain in volumes of the lateral recesses after removing the peripheral portions of the insulating fill material from inside the memory openings comprise seamed insulating layers that include a respective horizontally-extending seam therein;

each of the first-type electrically conductive layers is formed directly on a bottom surface of a respective one of the seamed insulating layers; and

each of the second-type electrically conductive layers is formed directly on a top surface of a respective one of the seamed insulating layers.

38. The method of Claim 35, further comprising:

forming support openings through the vertical repetition;

forming sacrificial support pillar structures within the support openings prior to formation of the lateral recesses;

removing the sacrificial support pillar structures after depositing the insulating fill material; and

laterally recessing portions of the at least one conductive fill material from around the support openings, wherein portions of the at least one conductive fill material that are proximal to the support openings are removed and sidewalls of portions of the insulating fill material that are deposited in the lateral recesses are physically exposed.

39. The method of Claim 34, further comprising:

forming stepped surfaces by patterning the vertical repetition in a staircase region, wherein the stepped surfaces comprise vertically-extending surfaces including a sidewall of a respective instance of the unit layer stack that extends vertically from a bottommost surface of the respective instance of the unit layer stack to a topmost surface of the respective instance of the unit layer stack;

forming a sacrificial retro-stepped dielectric material portion over the stepped surfaces prior to removing the sacrificial material layers;

removing the sacrificial retro-stepped dielectric material portion after depositing the insulating fill material layer; and

removing proximal portions of the at least one conductive fill material from the staircase region, wherein vertically-extending portions of the at least one conductive fill material are removed from sidewalls of the deposited insulating fill material located within the staircase region.

40. The method of Claim 34, wherein:

the sacrificial material layer is thicker than the insulating layer; and

the memory opening fill structures each comprise a vertical semiconductor channel and a memory film containing the vertical stack of memory elements.

41. A three-dimensional memory device, comprising:

a vertical repetition of multiple instances of a unit layer stack, wherein the unit layer stack comprises, from bottom to top, a first-type insulating layer, a first-type electrically conductive layer, a second-type insulating layer, and a second-type electrically conductive layer;

memory openings vertically extending through the vertical repetition;

memory opening fill structures located within the memory openings, wherein each of the memory opening fill structures comprises a respective vertical stack of memory elements; and

a laterally insulated contact structure comprising:

a tubular contact via structure vertically extending through at least one instance of the unit layer stack and contacting an annular top surface of the second-type electrically conductive layer in an underlying instance of the unit layer stack; and

a cylindrical contact via structure laterally surrounded by the tubular contact via structure and contacting an annular top surface of the first-type electrically conductive layer in the underlying instance of the unit layer stack.

42. The three-dimensional memory device of Claim 41, wherein:

the first-type electrically conductive layer comprises a first conductive barrier liner and a first conductive fill material layer that overlies the first conductive barrier liner; and

the second-type electrically conductive layer comprises a second conductive fill material layer and a second conductive barrier liner that overlies the second conductive fill material layer.

43. The three-dimensional memory device of Claim 42, wherein:

the cylindrical contact via structure contacts the first conductive fill material layer of the underlying instance of the unit layer stack and does not contact the first conductive barrier liner of the underlying instance of the unit layer stack; and

the tubular contact via structure contacts the second conductive barrier liner of the underlying instance of the unit layer stack and does not contact the second conductive fill material layer of the underlying instance of the unit layer stack.

44. The three-dimensional memory device of Claim 41, wherein the laterally insulated contact structure comprises an outer dielectric tubular spacer laterally surrounding the tubular contact via structure and contacting an additional annular top surface of the second-type electrically conductive layer in the underlying instance of the unit layer stack.

45. The three-dimensional memory device of Claim 44, wherein the laterally-insulated contact structure further comprises an inner dielectric tubular spacer laterally surrounded by the tubular contact via structure, laterally surrounding the cylindrical contact via structure, and contacting a sidewall of the second-type electrically conductive layer in the underlying instance of the unit layer stack, a sidewall of the second-type insulating layer in the underlying instance of the unit layer stack, and an annular top surface of the first-type electrically conductive layer in the underlying instance of the unit layer stack.

46. The three-dimensional memory device of Claim 42, wherein within each instance of the unit layer stack:

- an entirety of a bottom surface of the second-type insulating layer is in direct contact with a top surface of the first conductive fill material layer; and

- an entirety of a bottom surface of the second conductive fill material layer is in direct contact with a top surface of the second-type insulating layer.

47. The three-dimensional memory device of Claim 42, wherein within each instance of the unit layer stack:

- an entirety of a bottom surface of the first conductive fill material layer is in direct contact with a top surface of the first conductive barrier liner; and

- an entirety of a bottom surface of the second conductive barrier liner is in direct contact with a top surface of the second conductive fill material layer.

48. The three-dimensional memory device of Claim 41, wherein each of the memory opening fill structures comprises a vertical semiconductor channel and a memory film containing the vertical stack of memory elements.

49. The three-dimensional memory device of Claim 42, wherein:

each instance of the first conductive fill material layer and the second conductive fill material layer has a same conductive fill material composition and a same conductive fill material thickness; and

each instance of the first conductive barrier liner and the second conductive barrier liner has a same conductive liner composition and a same conductive liner thickness.

50. The three-dimensional memory device of Claim 49, wherein at least one of the tubular contact via structure and the cylindrical contact via structure comprises a conductive material having a different material composition than the same conductive fill material composition of the instances of the first conductive fill material layer and the second conductive fill material layer.

51. The three-dimensional memory device of Claim 41, wherein within each instance of the unit layer stack:

the first-type insulating layer comprises a seamless insulating layer that is free of any seam therein; and

the second-type insulating layer comprises a seamed insulating layer including a horizontally-extending seam therein.

52. The three-dimensional memory device of Claim 51, wherein each of the memory opening fill structures is laterally spaced from the horizontally-extending seams of the seamed insulating layers by a respective seamless portion of the seamed insulating layers.

53. The three-dimensional memory device of Claim 51, wherein the horizontally-extending seam within the seamed insulating layer is equidistant from a horizontal interface between the seamed insulating layer and the second-type electrically conductive layer, and from a horizontal interface between the seamed insulating layer and the first-type electrically conductive layer.

54. The three-dimensional memory device of Claim 51, further comprising:

a first backside trench fill structure comprising a first dielectric surface contacting first sidewalls of each layer within the vertical repetition and laterally extending along a first horizontal direction; and

a second backside trench fill structure comprising a second dielectric surface contacting second sidewalls of each layer within the first vertical repetition, laterally extending along the first horizontal direction, and laterally spaced from the first backside trench fill structure along a second horizontal direction.

55. A method of forming a three-dimensional memory device, comprising:

forming a vertical repetition of multiple instances of a unit layer stack over a substrate, wherein the unit layer stack comprises an insulating layer and a sacrificial material layer;

forming sacrificial memory opening fill structures vertically extending through the vertical repetition;

forming contact via cavities having different depths through the vertical repetition, wherein a surface of a respective sacrificial material layer of the sacrificial material layers is physically exposed at a bottom of each of the contact via cavities;

removing the sacrificial material layers selective to the insulating layers by isotropically etching a material of the sacrificial material layers selective to a material of the insulating layers, whereby lateral recesses are formed in volumes from which the sacrificial material layers are removed;

depositing at least one conductive fill material at peripheral portions of the lateral recesses and the contact via cavities;

depositing an insulating fill material over the at least one conductive fill material within remaining volumes of the lateral recesses and the contact via cavities;

forming memory cavities by removing the sacrificial memory opening fill structures;

removing proximal portions of the at least one conductive fill material from around the memory cavities; and

forming memory opening fill structures within volumes of the memory cavities and additional volumes of voids formed by removal of the proximal portions of the at least one conductive fill material, wherein each of the memory opening fill structures comprises a vertical repetition of memory elements.

56. The method of Claim 55, wherein:

remaining portions of the at least one conductive fill material and the insulating fill material after removal of the proximal portions of the at least one conductive fill material

from around the memory cavities comprise layer stacks located within a volume of a respective one of the lateral recesses; and

a volume of the respective one of the lateral recesses is filled with, from bottom to top, a first-type electrically conductive layer, a seamed insulating layer including a horizontally-extending seam therein, and a second-type electrically conductive layer.

57. The method of Claim 56, further comprising:

removing the insulating fill material and the at least one conductive fill material from inside the contact via cavities;

forming an outer dielectric tubular spacer within each of the contact via cavities by depositing and anisotropically etching a first conformal dielectric material layer; and

forming a tubular contact via structure on an inner sidewall of the outer dielectric tubular spacer within each of the contact via cavities by depositing and anisotropically etching a first conformal conductive material layer.

58. The method of Claim 57, further comprising:

anisotropically etching a respective one of the second-type electrically conductive layers and a respective one of the seamless insulating layers underneath an opening within each of the outer dielectric tubular spacers;

forming an inner dielectric tubular spacer on an inner sidewall of the tubular contact via structure within each of the contact via cavities by depositing and anisotropically etching a second conformal dielectric material layer; and

forming a cylindrical contact via structure on an inner sidewall of the inner dielectric tubular spacer within each of the contact via cavities by depositing and planarizing a second conformal conductive material layer.

59. The method of Claim 55, further comprising:

forming backside trenches through the vertical repetition, wherein sidewalls of the multiple instances of the unit layer stack are physically exposed to the backside trenches;

forming sacrificial backside trench fill structures in the backside trenches, wherein the sacrificial material layers are removed after formation of the sacrificial backside trench fill structures and the at least one conductive fill material is deposited directly on sidewalls of the sacrificial backside trench fill structures;

removing the sacrificial backside trench fill structures, wherein backside voids are formed within volumes from which the sacrificial backside trench fill structures are removed;

removing portions of the at least one conductive fill material that are proximal to the backside trenches from around the backside voids; and

forming backside trench fill structures in the backside voids.

60. The method of Claim 55, wherein the memory opening fill structures are formed by:

forming a memory film including a respective vertical stack of memory elements within each of the memory cavities;

forming a vertical semiconductor channel over the memory film within each of the memory cavities; and

forming a drain region at a top end of the vertical semiconductor channel within each of the memory cavities.

61. A three-dimensional memory device comprising:

a vertical repetition of multiple instances of a unit layer stack, wherein the unit layer stack comprises, from bottom to top, a first-type insulating layer, a first-type electrically conductive layer comprising a first conductive barrier liner and a first conductive fill material layer, a second-type insulating layer, and a second-type electrically conductive layer comprising a second conductive fill material layer and a second conductive barrier liner;

memory openings vertically extending through the vertical repetition; and

memory opening fill structures located within the memory openings, wherein each of the memory opening fill structures comprises a respective vertical stack of memory elements.

wherein:

the first conductive fill material layer and the second conductive fill material layer are in direct contact with horizontal surfaces of the second-type insulating layer;

the first conductive barrier liner is in direct contact with a horizontal surface of the first-type insulating layer; and

the second conductive barrier liner is in direct contact with a horizontal surface of another first-type insulating layer of an adjacent unit layer stack.

62. The three-dimensional memory device of Claim 61, wherein within each instance of the unit layer stack:

an entirety of a bottom surface of the second-type insulating layer is in direct contact with a top surface of the first conductive fill material layer; and

an entirety of a bottom surface of the second conductive fill material layer is in direct contact with a top surface of the second-type insulating layer.

63. The three-dimensional memory device of Claim 61, wherein, within each instance of the unit layer stack:

an entirety of a bottom surface of the first conductive fill material layer is in direct contact with a top surface of the first conductive barrier liner; and

an entirety of a bottom surface of the second conductive barrier liner is in direct contact with a top surface of the second conductive fill material layer.

64. The three-dimensional memory device of Claim 61, wherein each instance of the first conductive fill material layer and the second conductive fill material layer has a same conductive fill material composition and a same conductive fill material thickness.

65. The three-dimensional memory device of Claim 64, wherein each instance of the first conductive barrier liner and the second conductive barrier liner has a same conductive liner composition and a same conductive liner thickness.

66. The three-dimensional memory device of Claim 61, wherein within each instance of the unit layer stack:

the first-type insulating layer comprises a seamless insulating layer that is free of any seam therein; and

the second-type insulating layer comprises a seamed insulating layer including a horizontally-extending seam therein.

67. The three-dimensional memory device of Claim 66, wherein each of the memory opening fill structures is laterally spaced from the horizontally-extending seams by a respective seamless portion of the seamed insulating layers.

68. The three-dimensional memory device of Claim 66, wherein the horizontally-extending seam within the seamed insulating layer in each instance of the unit layer stack is equidistant from a horizontal interface between the seamed insulating layer and the second-type electrically conductive layer, and from a horizontal interface between the seamed insulating layer and the first-type electrically conductive layer.

69. The three-dimensional memory device of Claim 66, further comprising:

a first backside trench fill structure comprising a first dielectric surface contacting first sidewalls of each layer within the vertical repetition and laterally extending along a first horizontal direction; and

a second backside trench fill structure comprising a second dielectric surface contacting second sidewalls of each layer within the first vertical repetition, laterally extending along the first horizontal direction, and laterally spaced from the first backside trench fill structure along a second horizontal direction.

70. The three-dimensional memory device of Claim 69, wherein:

each of the first backside trench fill structure and the second backside trench fill structure has a respective laterally-undulating vertical cross-sectional profile in the second horizontal direction; and

each of the first backside trench fill structure and the second backside trench fill structure has a greater width at levels of the first-type electrically conductive layers, the seamless insulating layers, and the second-type electrically conductive layers than at levels of the seamed insulating layers.

71. The three-dimensional memory device of Claim 69, wherein each horizontally-extending seam within the seamed insulating layers is in direct contact with a respective one of the first dielectric surface and the second dielectric surface.

72. The three-dimensional memory device of Claim 69, wherein each of the first backside trench fill structure and the second backside trench fill structure comprises:

- a backside contact via structure contacting a respective source region a substrate; and
- an insulating spacer laterally surrounding the backside contact via structure and comprising a respective one of the first dielectric surface and the second dielectric surface as an outer surface.

73. The three-dimensional memory device of Claim 61, wherein the seamed insulating layer comprises an air gap encapsulated by a dielectric material layer having an upper horizontally-extending portion and a lower horizontally-extending portion that are adjoined to each other at a periphery of the air gap at the horizontally-extending seam.

74. The three-dimensional memory device of Claim 61, further comprising:

- a retro-stepped dielectric material portion overlying stepped surfaces of the vertical repetition;

first-type contact via structures vertically extending through the retro-stepped dielectric material portion and contacting a top surface of a respective instance of the first-type electrically conductive layer; and

second-type contact via structures vertically extending through the retro-stepped dielectric material portion and contacting a top surface of a respective instance of the second-type electrically conductive layer.

75. A method of forming a three-dimensional memory device, comprising:

forming a vertical repetition of multiple instances of a unit layer stack over a substrate, wherein the unit layer stack comprises an insulating layer and a sacrificial material layer;

forming memory openings vertically extending through the vertical repetition;

forming sacrificial memory opening fill structures within the memory openings;

forming backside trenches through the vertical repetition;

removing the sacrificial material layers selective to the insulating layers through the backside trenches, whereby lateral recesses are formed in volumes from which the sacrificial material layers are removed, and wherein the lateral recesses laterally surround remaining portions of the sacrificial memory opening fill structures;

depositing at least one conductive fill material at peripheral portions of the lateral recesses;

depositing an insulating fill material over the at least one conductive fill material within remaining volumes of the lateral recesses;

removing the sacrificial memory opening fill structures;

removing proximal portions of the at least one conductive fill material from around memory cavities formed by removal of the sacrificial memory opening fill structures, wherein voids are formed within volumes of the memory openings; and

forming memory opening fill structures within volumes of the memory openings, wherein each of the memory opening fill structures comprises a respective vertical stack of memory elements.

76. The method of Claim 75, further comprising:

introducing an isotropic etchant that etches a material of the sacrificial material layers selective to a material of the insulating layers into the backside trenches, whereby the sacrificial material layers are removed selective to the insulating layers; and

removing peripheral portions of the insulating fill material and the at least one conductive fill material from peripheral regions of the backside trenches.

77. The method of Claim 76, further comprising:

forming insulating spacers at peripheral portions of backside trenches by conformally depositing and anisotropically etching an insulating material layer; and

forming a backside contact via structure within each remaining volume of the backside trenches after formation of the insulating spacers.

78. The method of Claim 75, further comprising isotropically recessing cylindrical portions of the sacrificial memory opening fill structures around each of the lateral recesses,

wherein:

the proximal portions of the at least one conductive fill material are deposited within volumes from which a material of the sacrificial memory opening fill structures is removed; and

sidewalls of the deposited insulating fill material are physically exposed after removing the proximal portions of the at least one conductive fill material from around the memory cavities.

79. The method of Claim 78, wherein:

each of the sacrificial memory opening fill structures comprises a first sacrificial fill material portion comprising a first sacrificial fill material and having a tubular shape and a second sacrificial fill material portion comprising a second sacrificial fill material and laterally surrounded by the first sacrificial fill material portion; and

said isotropically recessing of the cylindrical portions of the sacrificial memory opening fill structures comprises isotropically etching cylindrical portions of the first sacrificial fill material portions by providing an isotropic etchant that etches the first sacrificial fill material selective to the second sacrificial fill material.

80. The method of Claim 75, further comprising:

forming stepped surfaces by patterning the vertical repetition in a staircase region, wherein the stepped surfaces comprise vertically-extending surfaces including a sidewall of a respective instance of the unit layer stack that extends vertically from a bottommost surface of the respective instance of the unit layer stack to a topmost surface of the respective instance of the unit layer stack;

forming a sacrificial retro-stepped dielectric material portion over the stepped surfaces prior to removing the sacrificial material layers;

removing the sacrificial retro-stepped dielectric material portion after depositing the insulating fill material layer; and

removing proximal portions of the at least one conductive fill material from the staircase region, wherein vertically-extending portions of the at least one conductive fill material are removed from sidewalls of the deposited insulating fill material located within the staircase region.

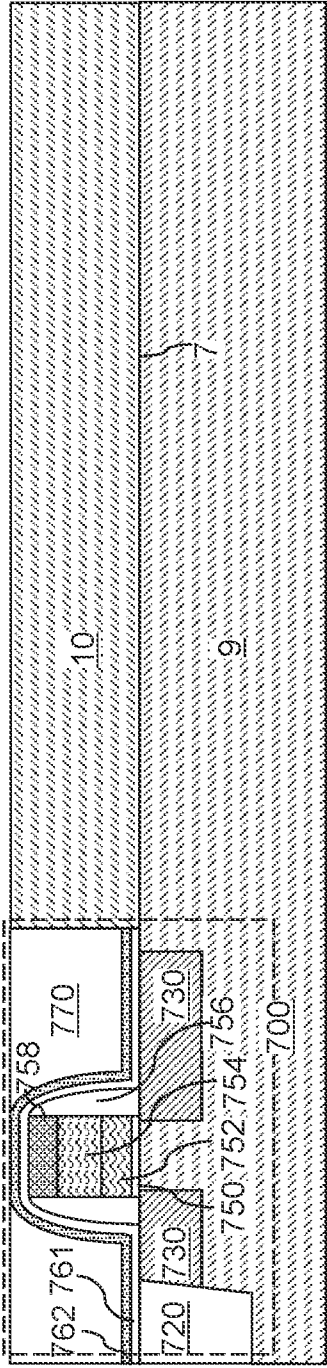


FIG. 1

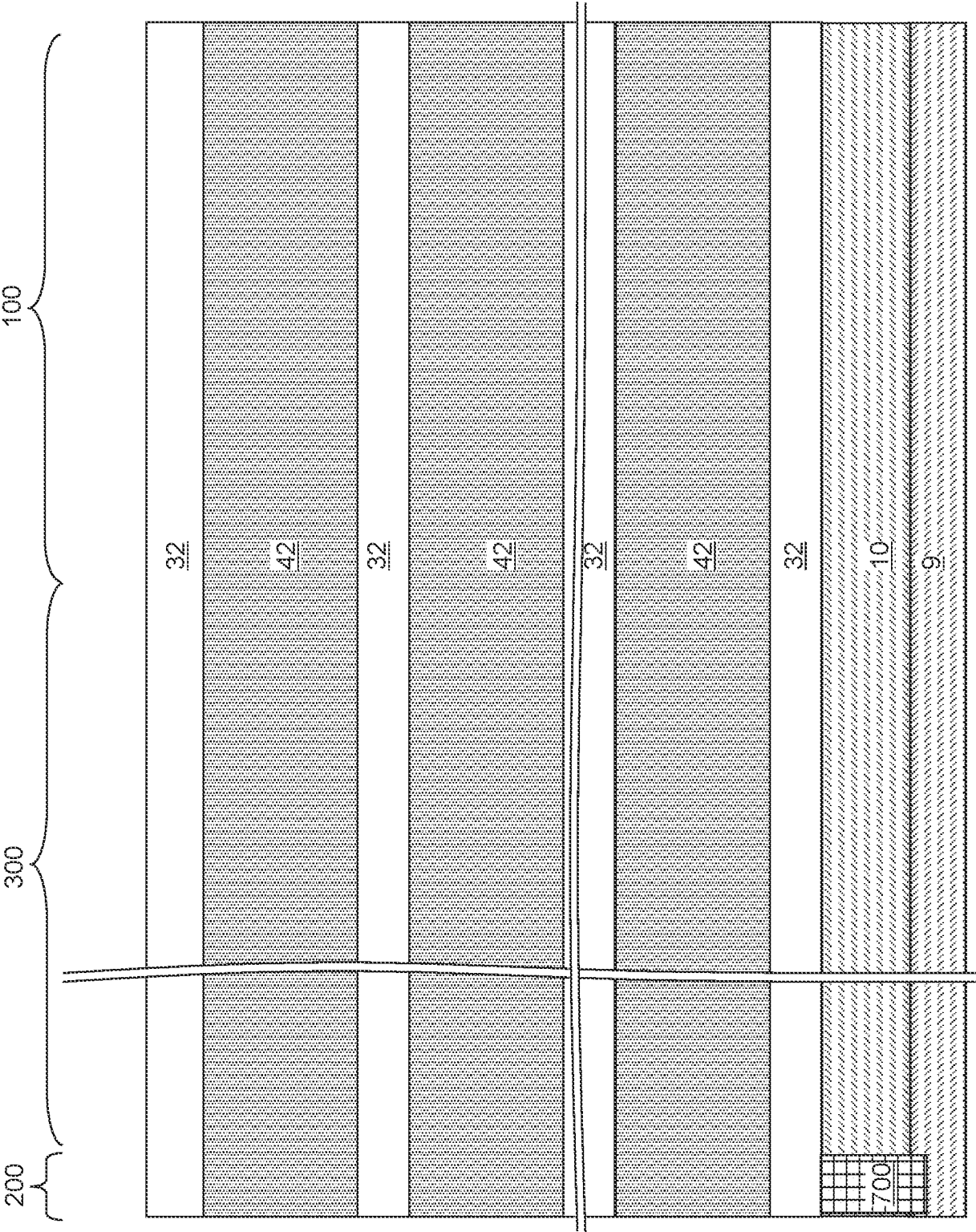


FIG. 2

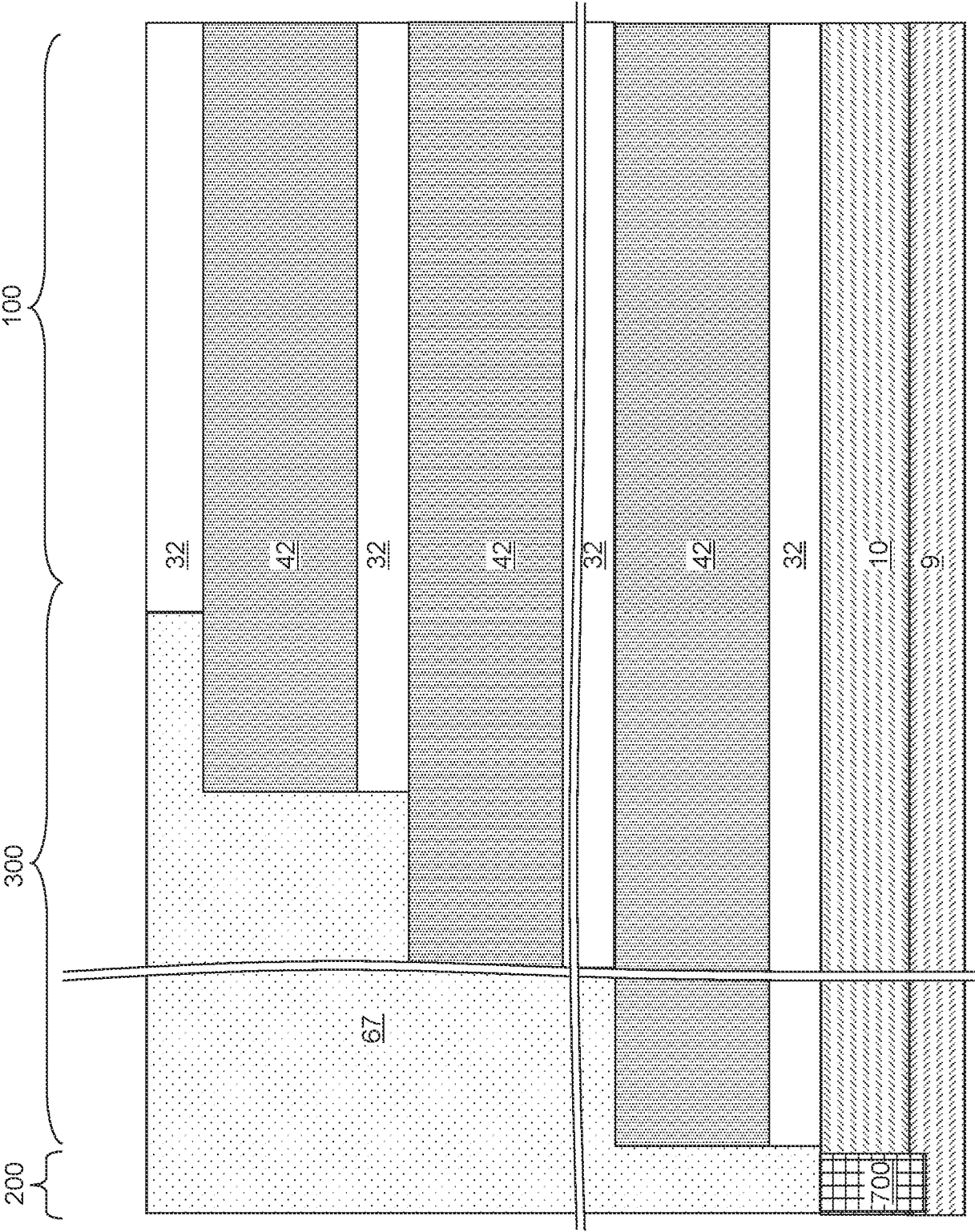


FIG. 3

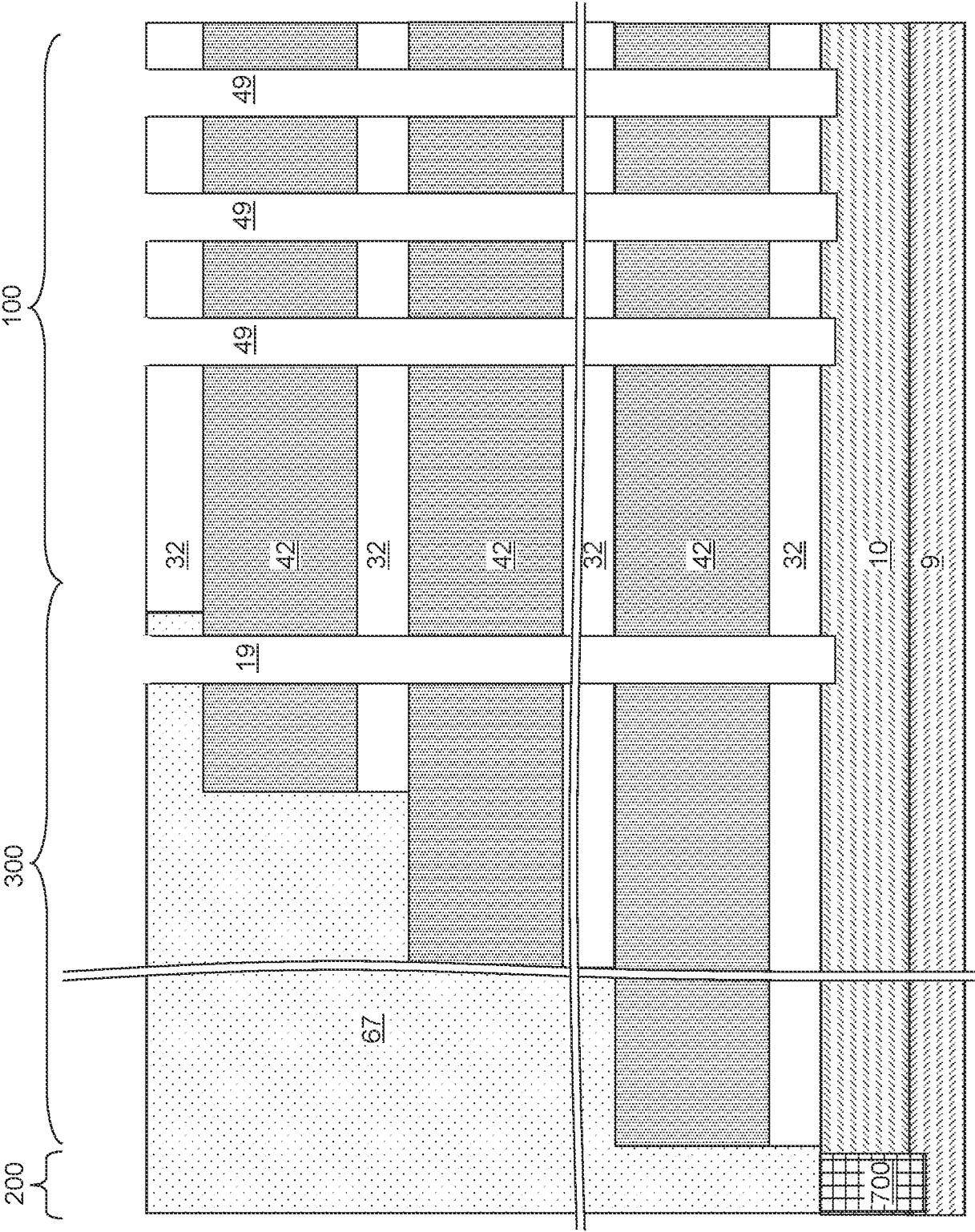
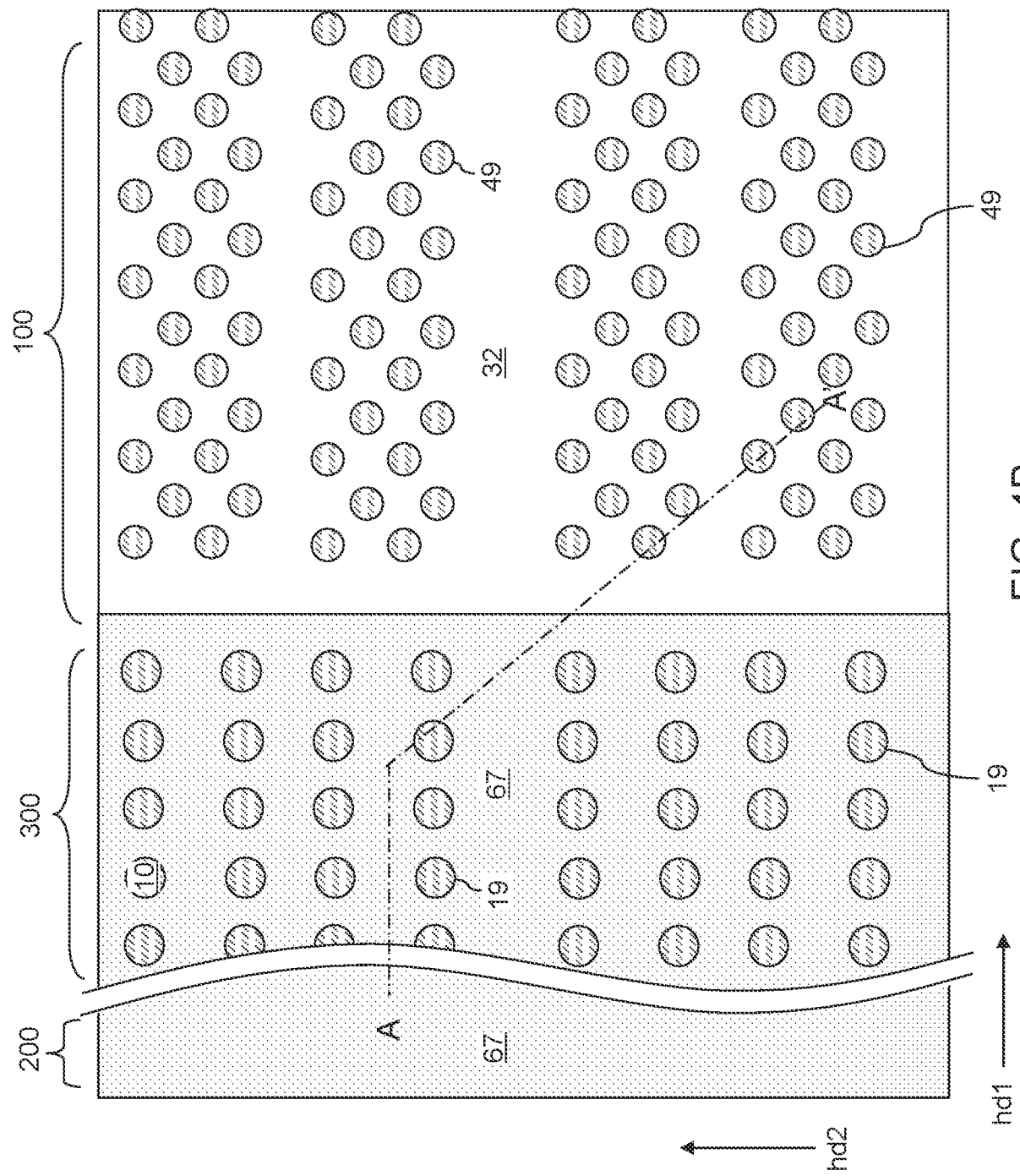


FIG. 4A



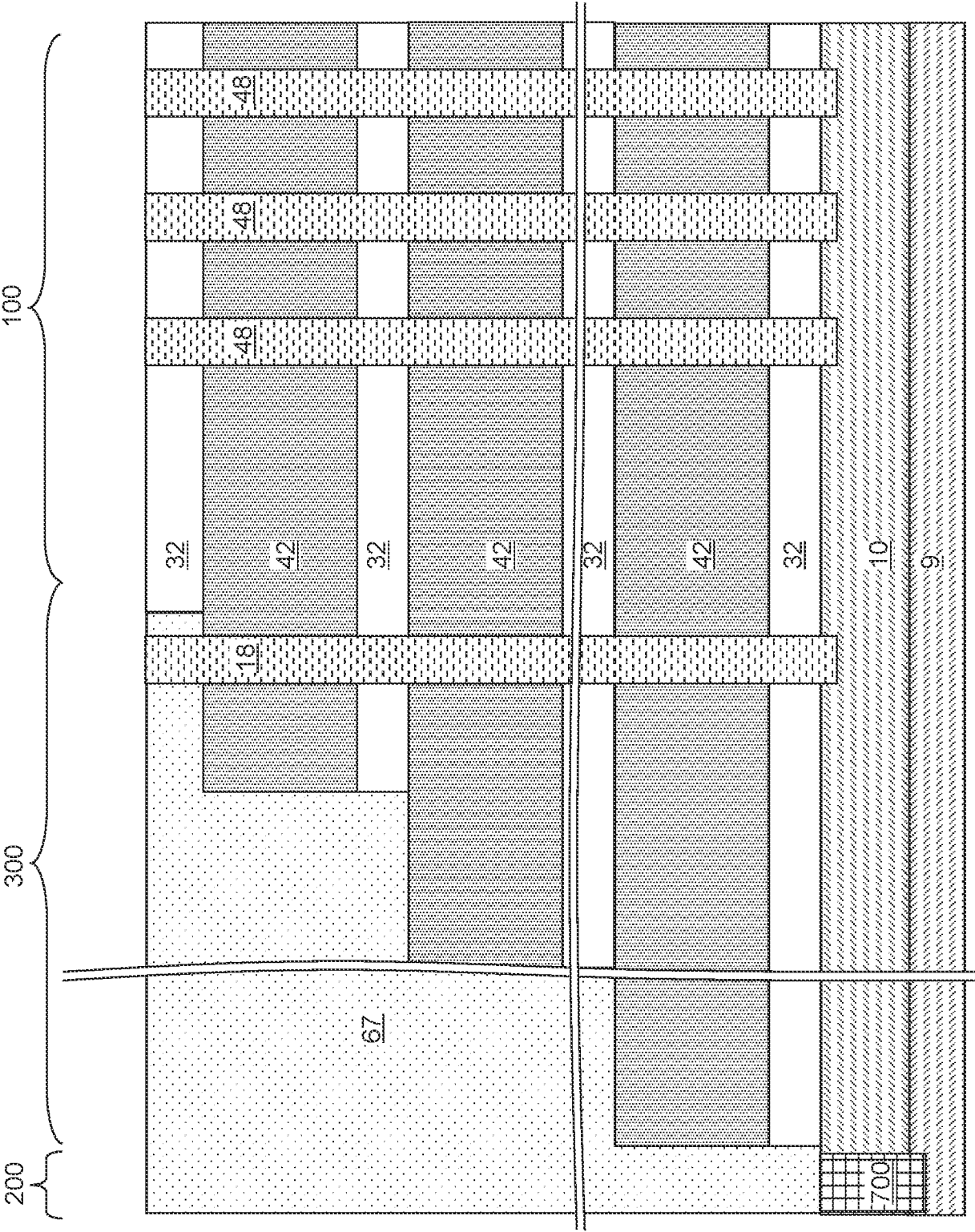


FIG. 5

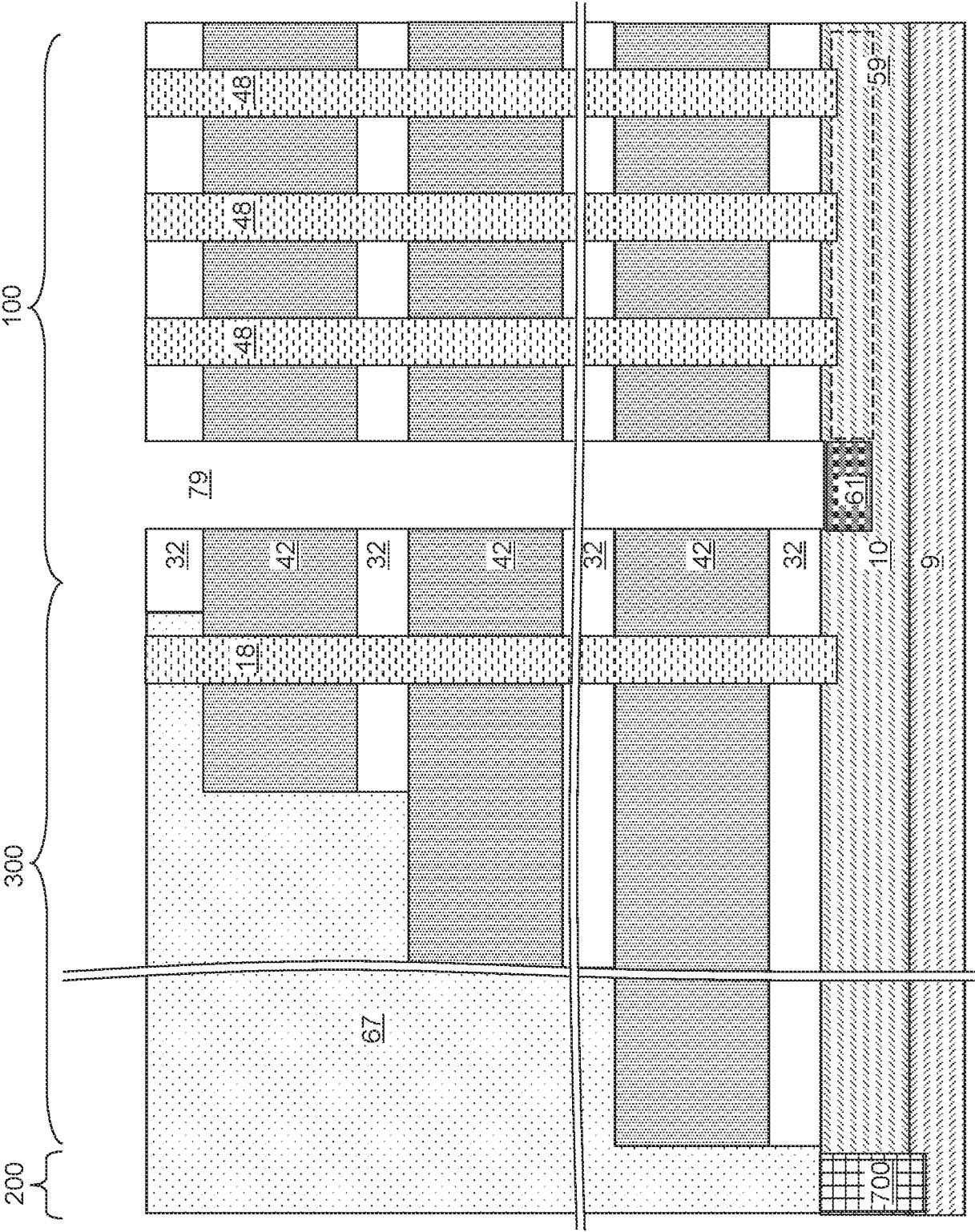


FIG. 6A

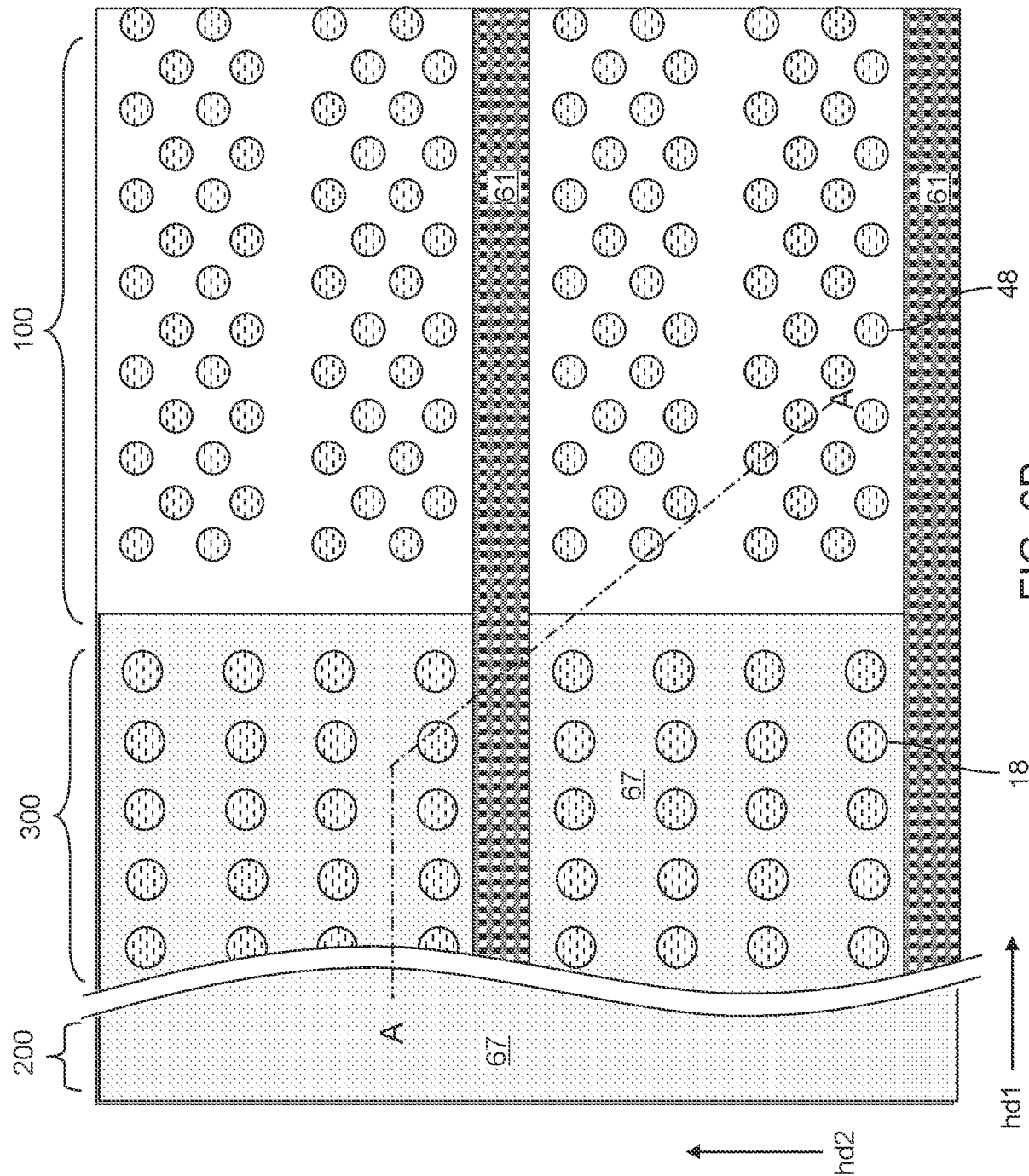


FIG. 6B

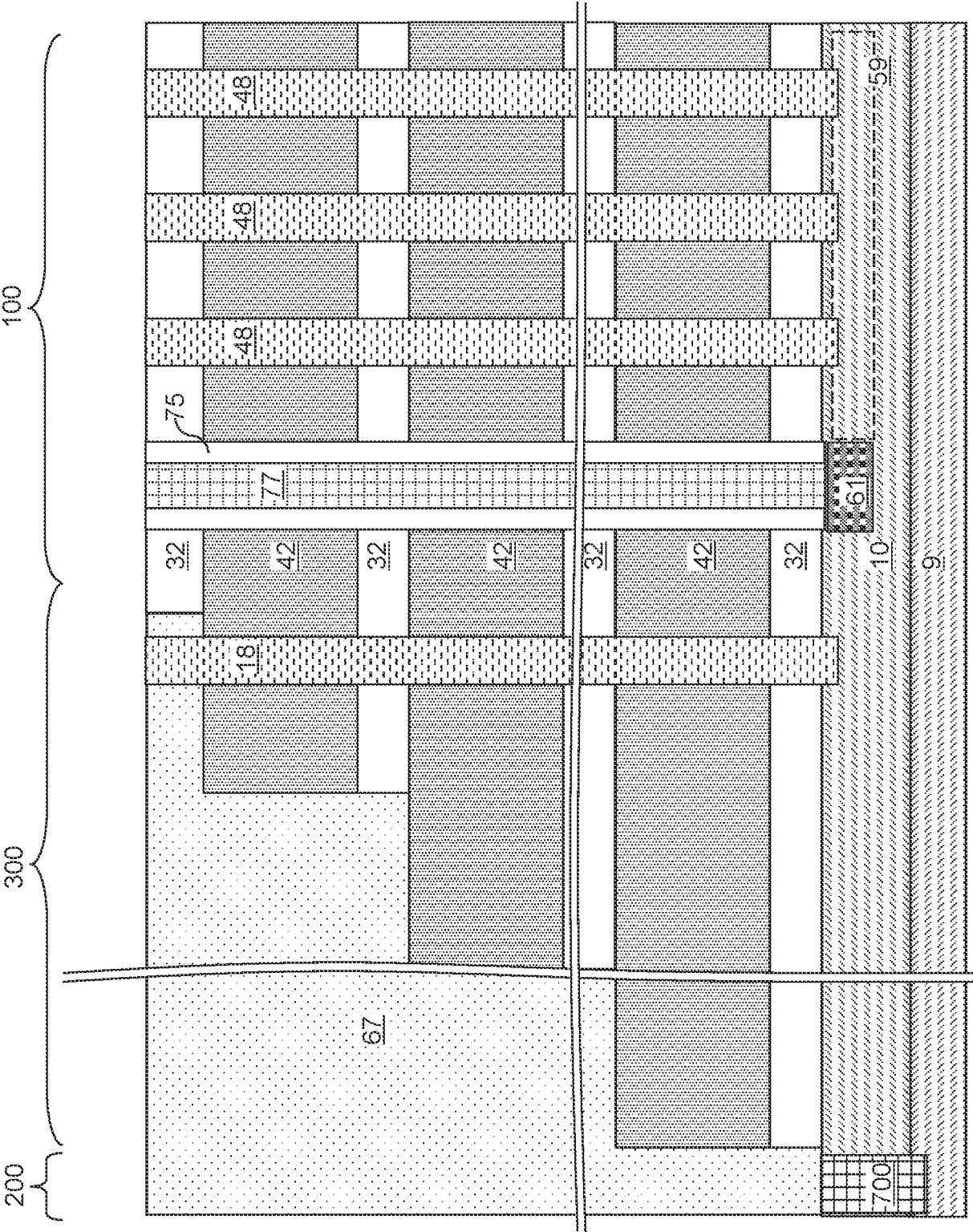
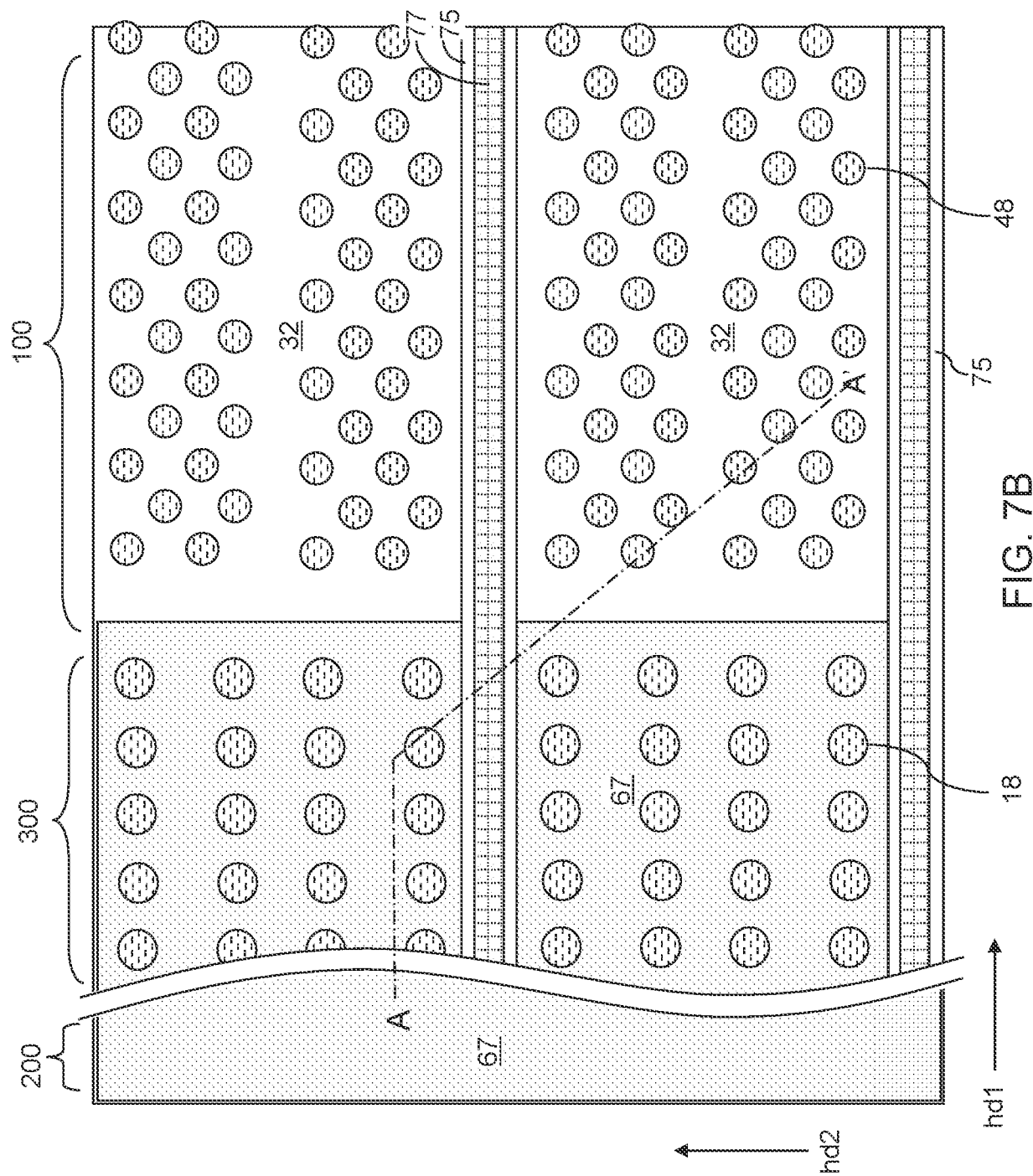


FIG. 7A



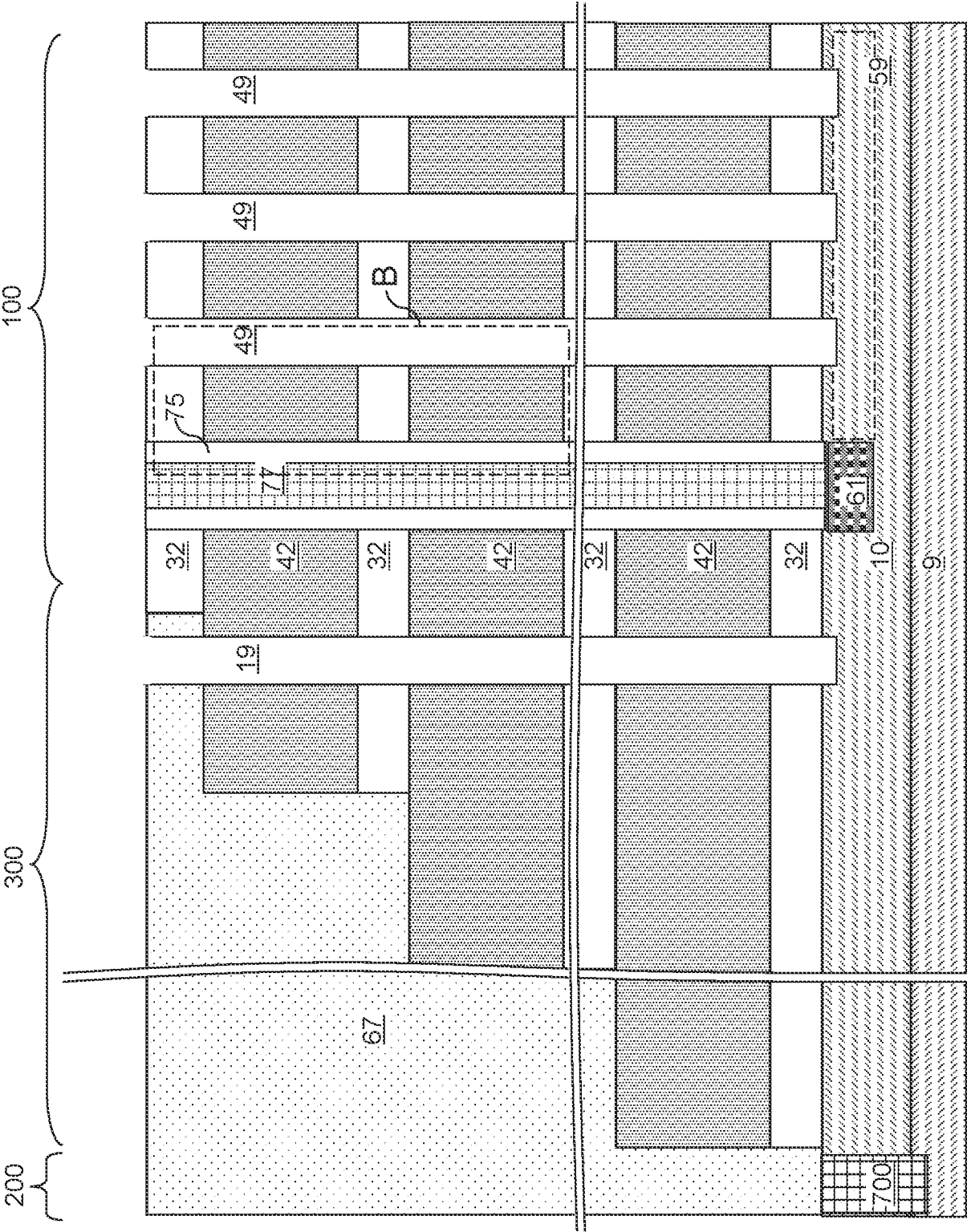


FIG. 8

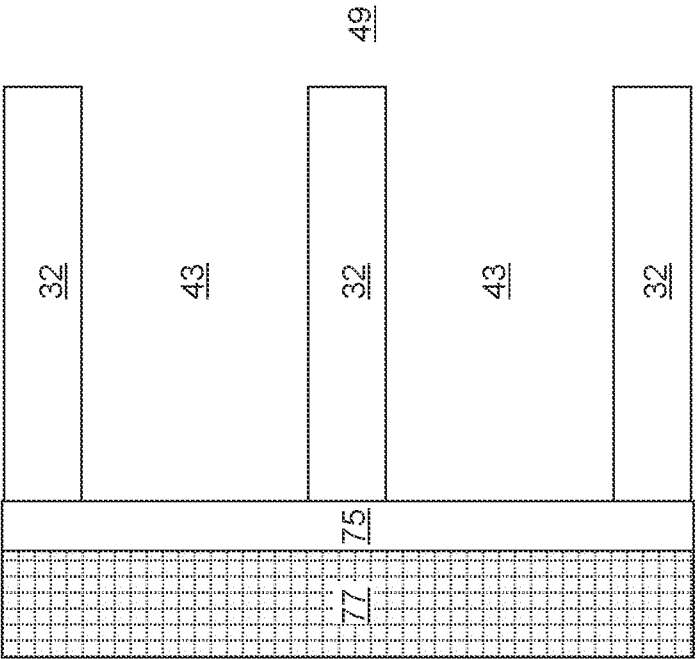


FIG. 9A

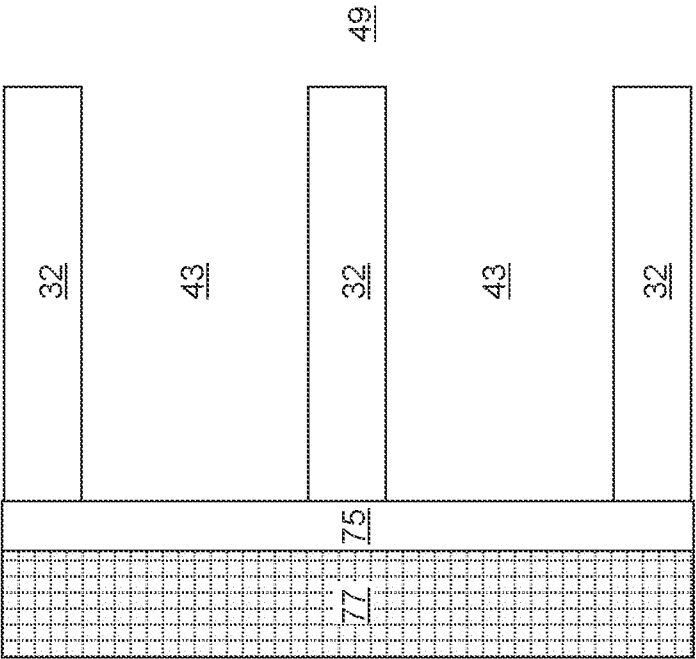


FIG. 9B

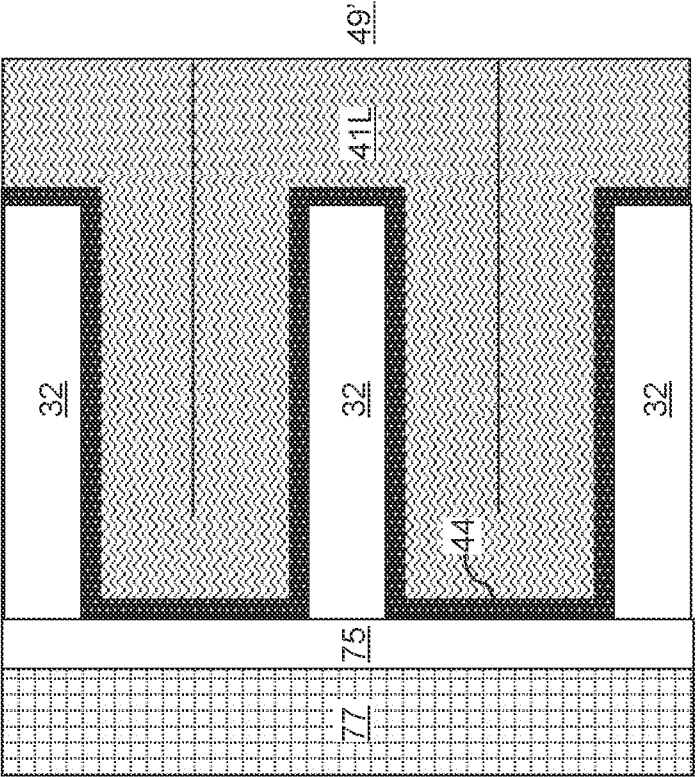


FIG. 9D

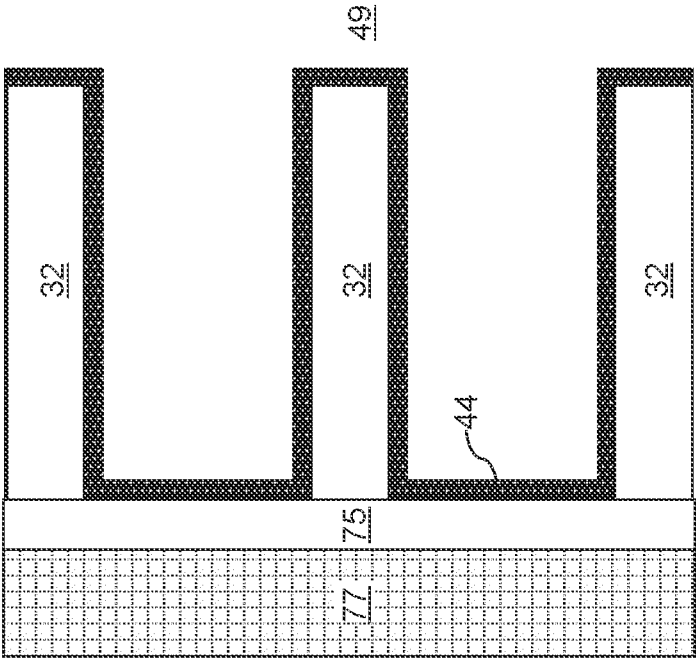


FIG. 9C

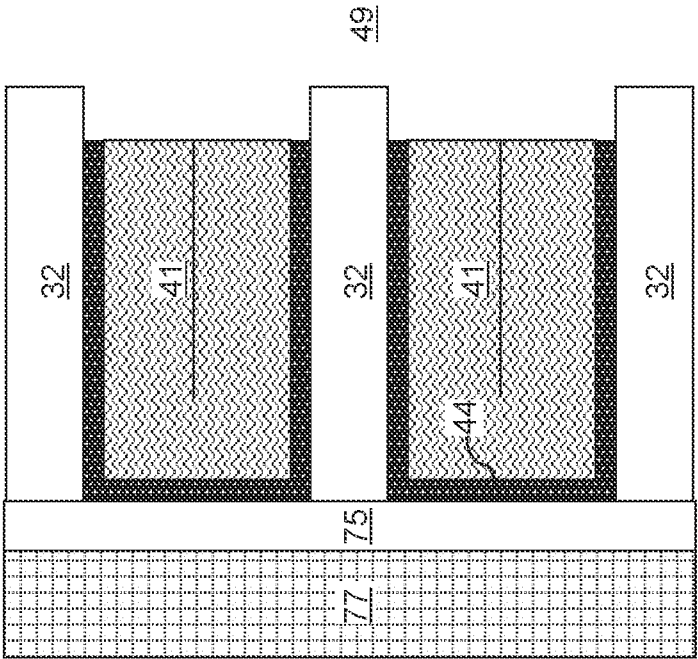


FIG. 9F

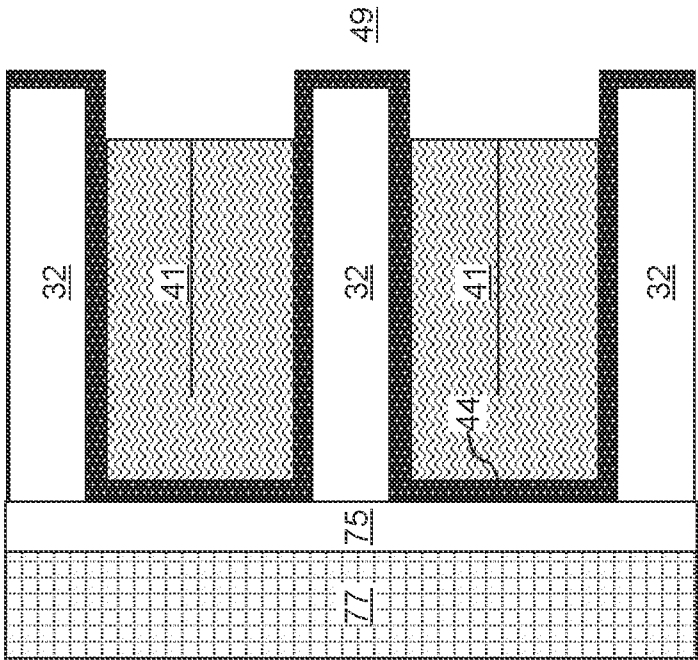


FIG. 9E

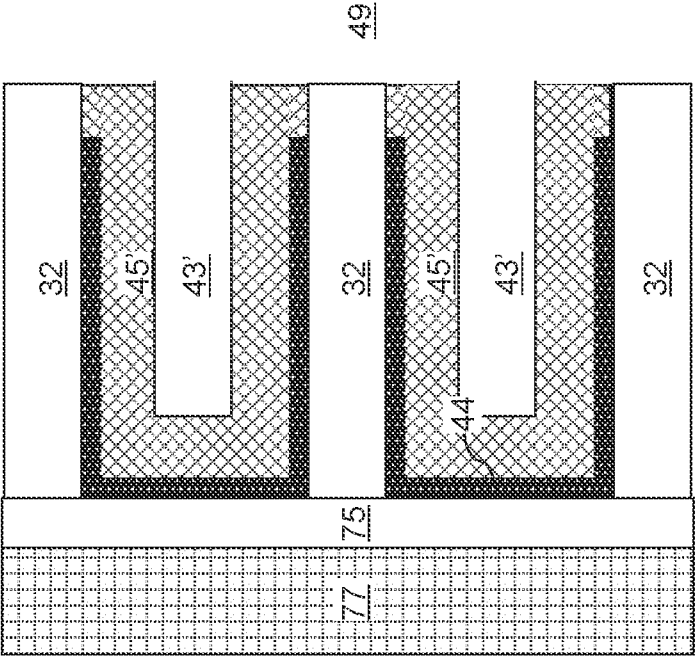


FIG. 9H

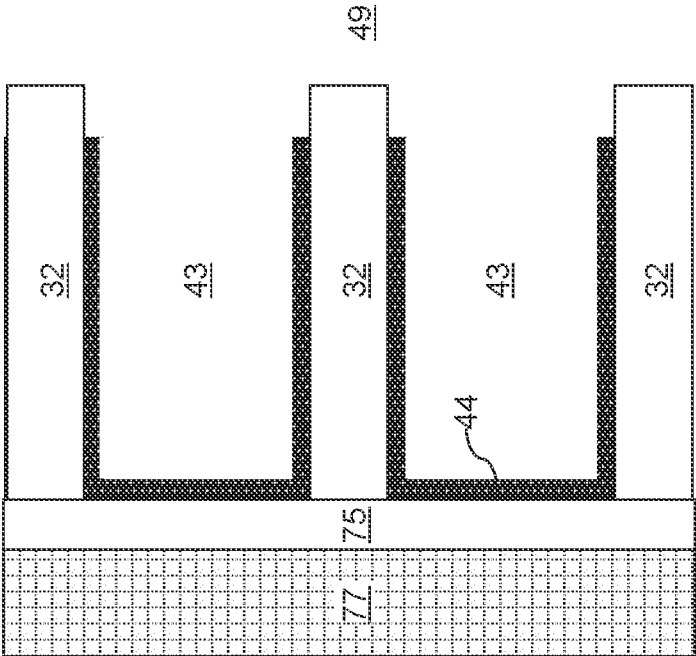


FIG. 9G

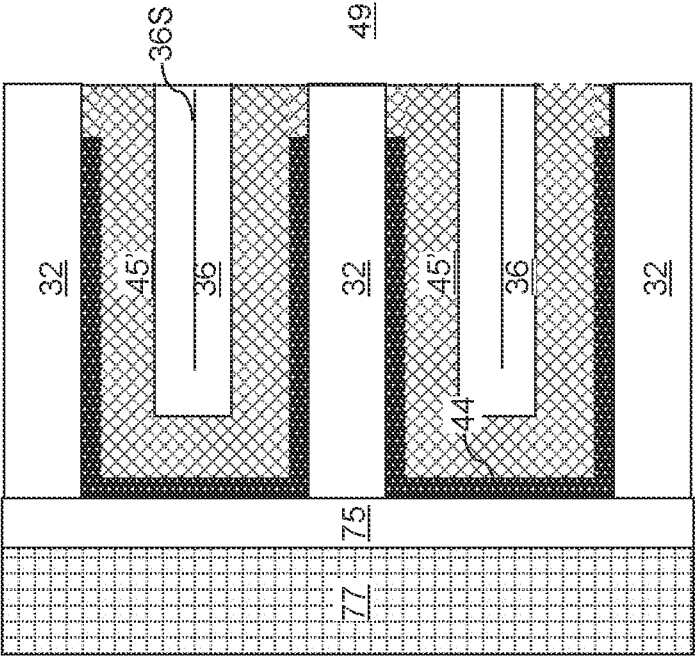


FIG. 9I

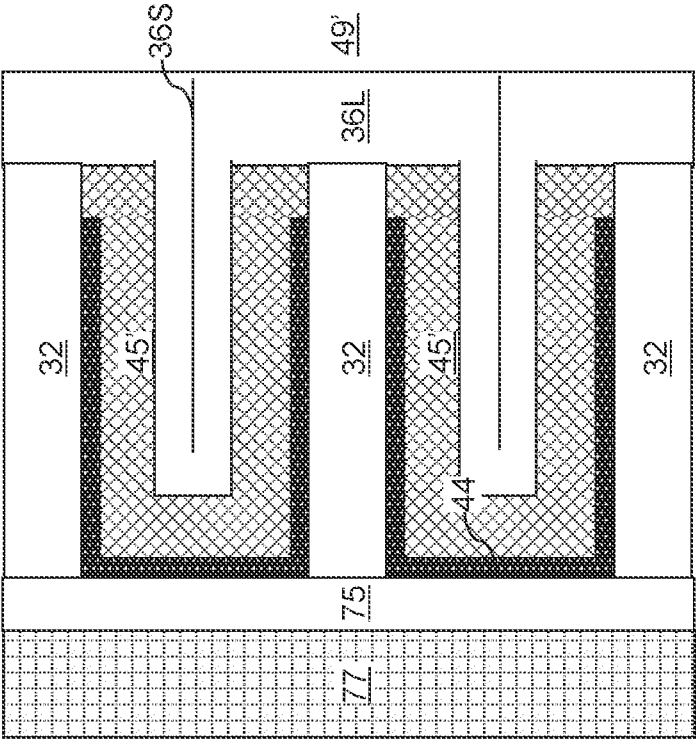


FIG. 9J

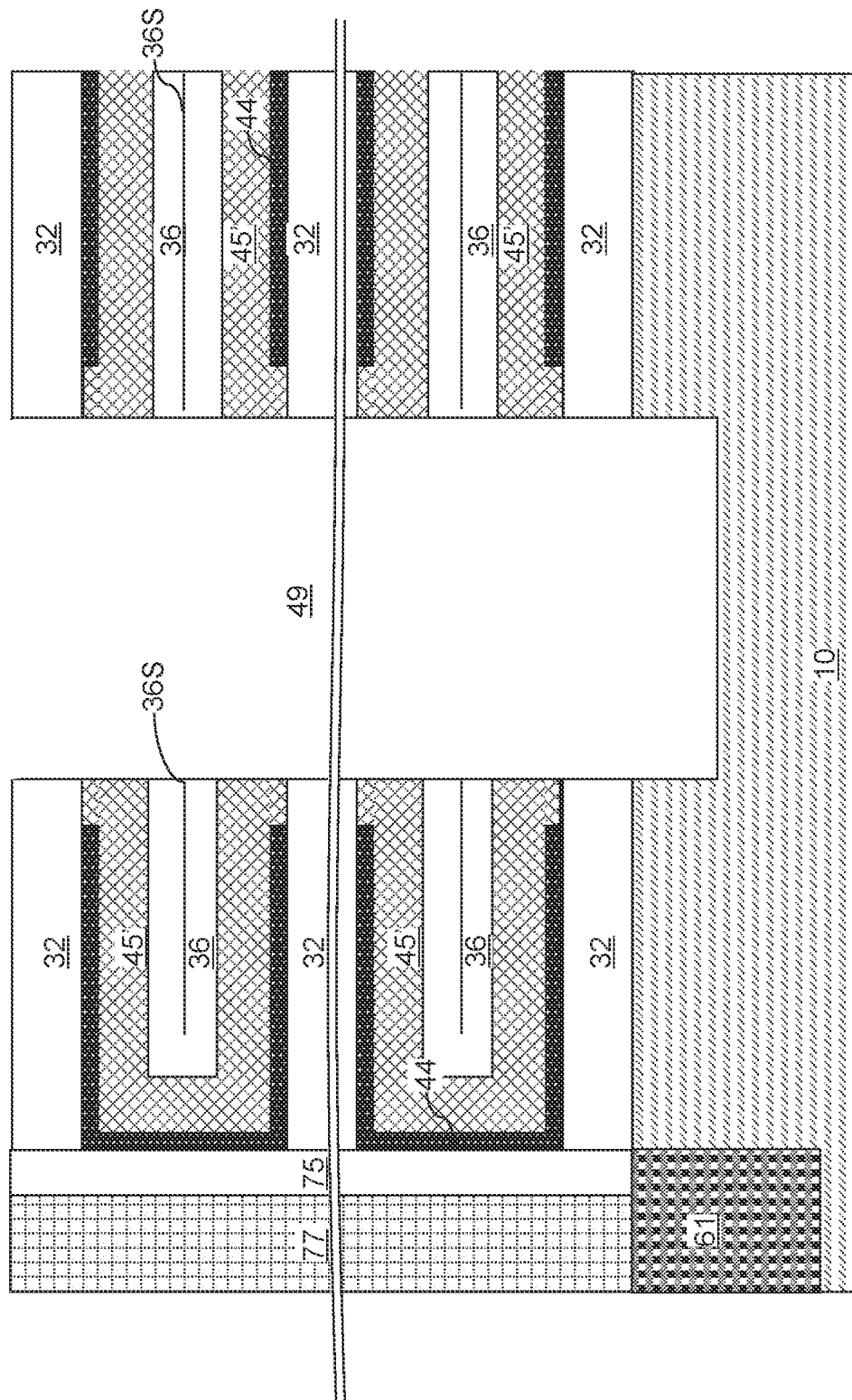
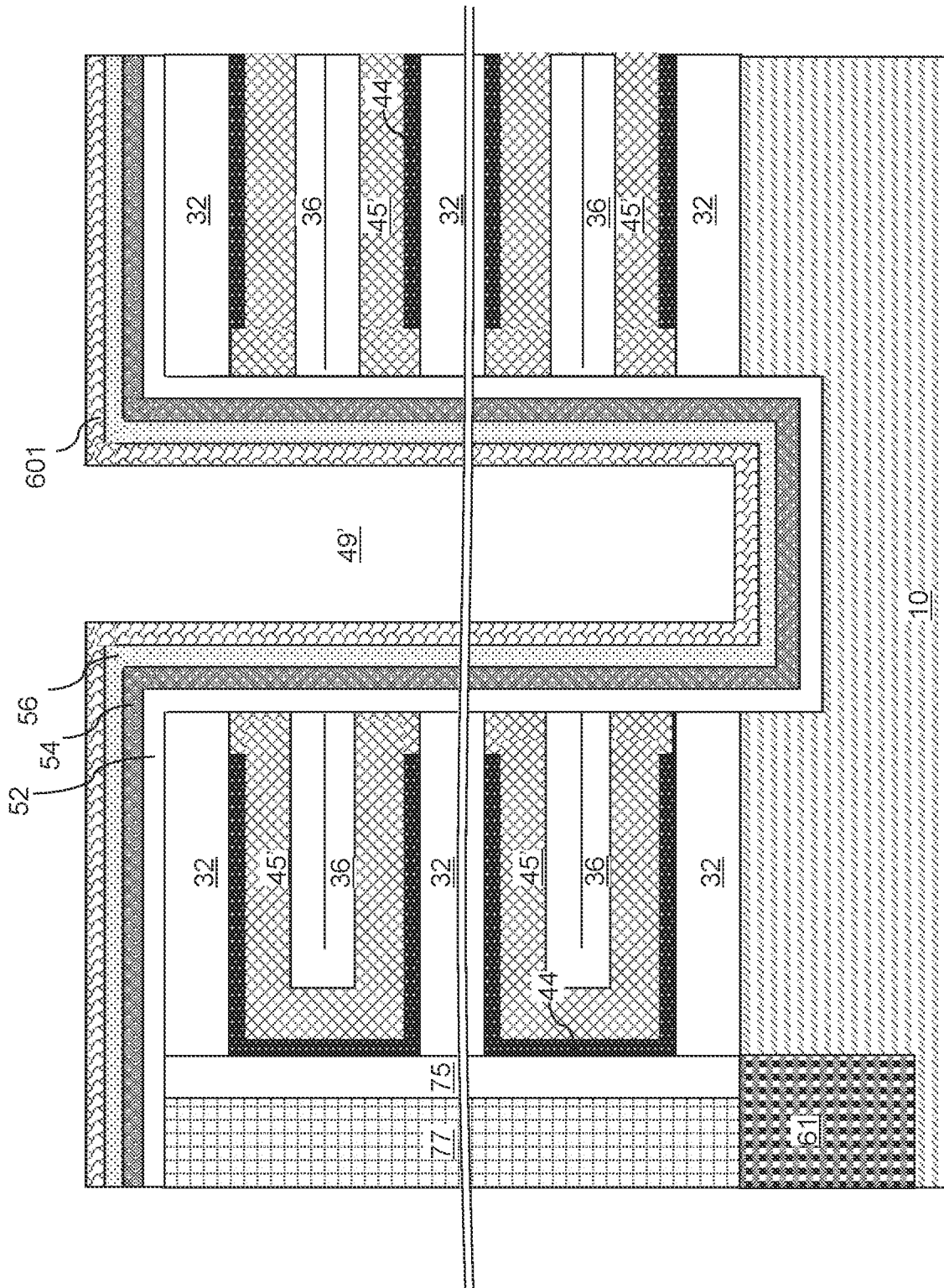


FIG. 10A



103B

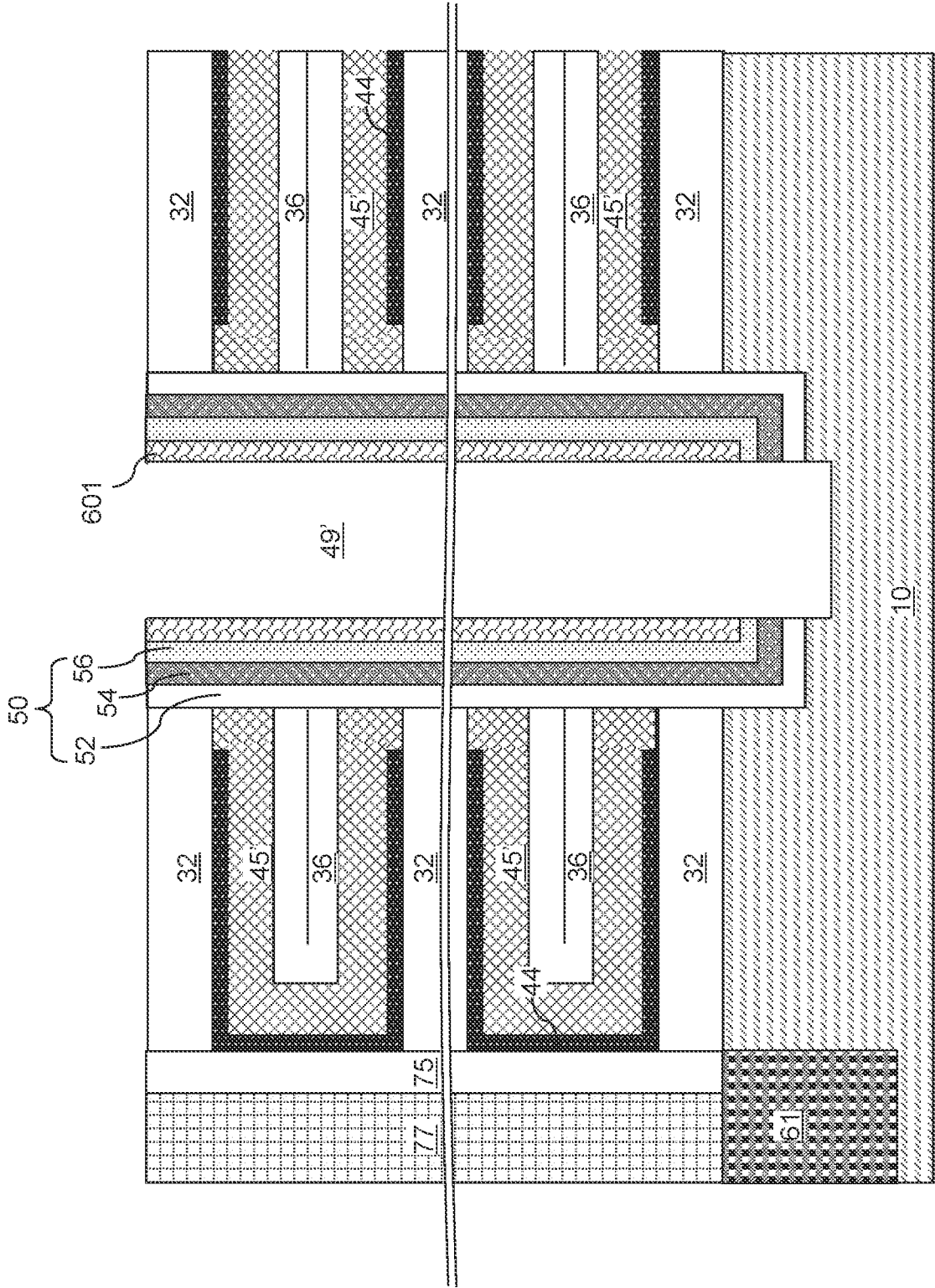


FIG. 10C

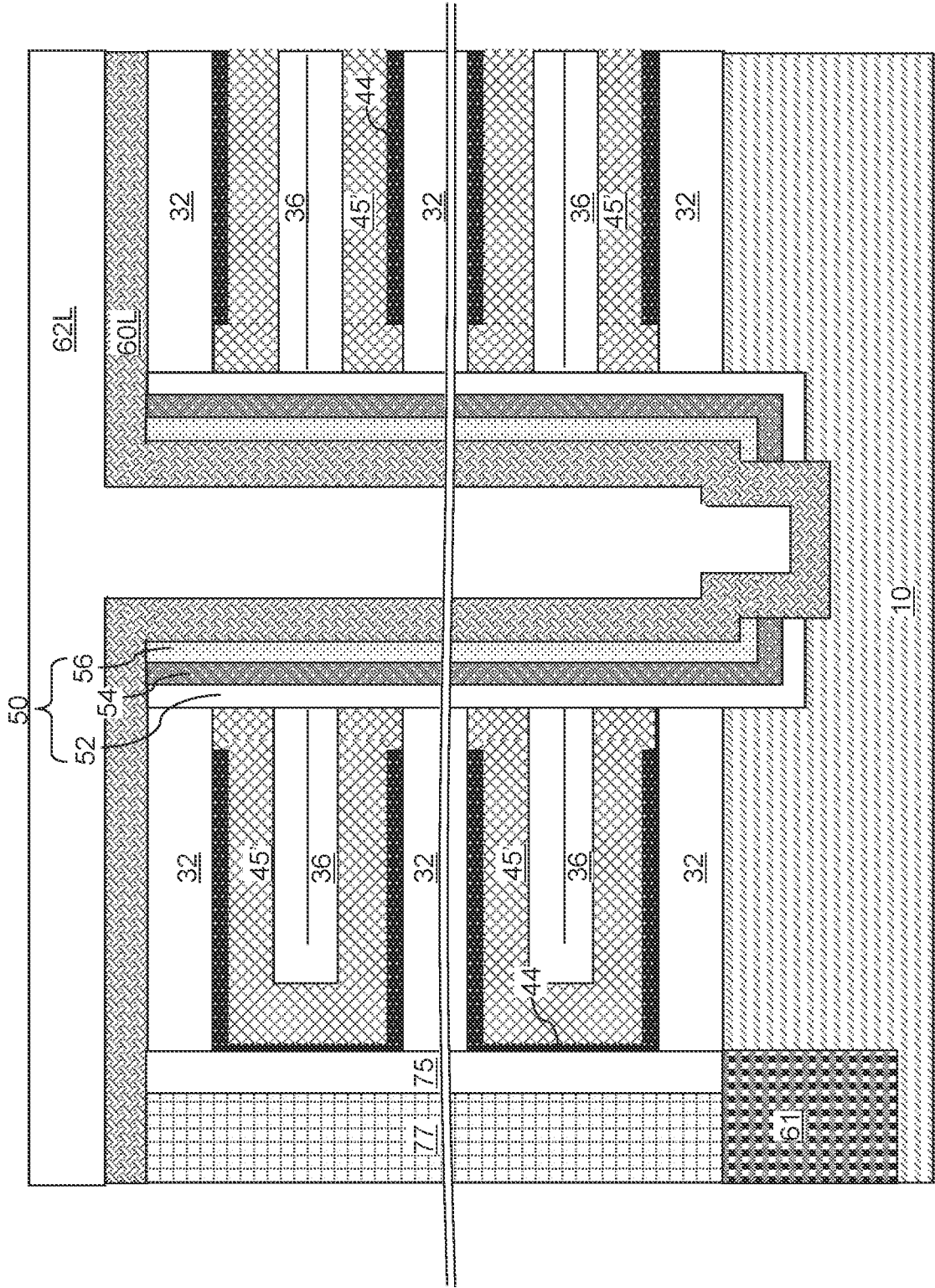


FIG. 10D

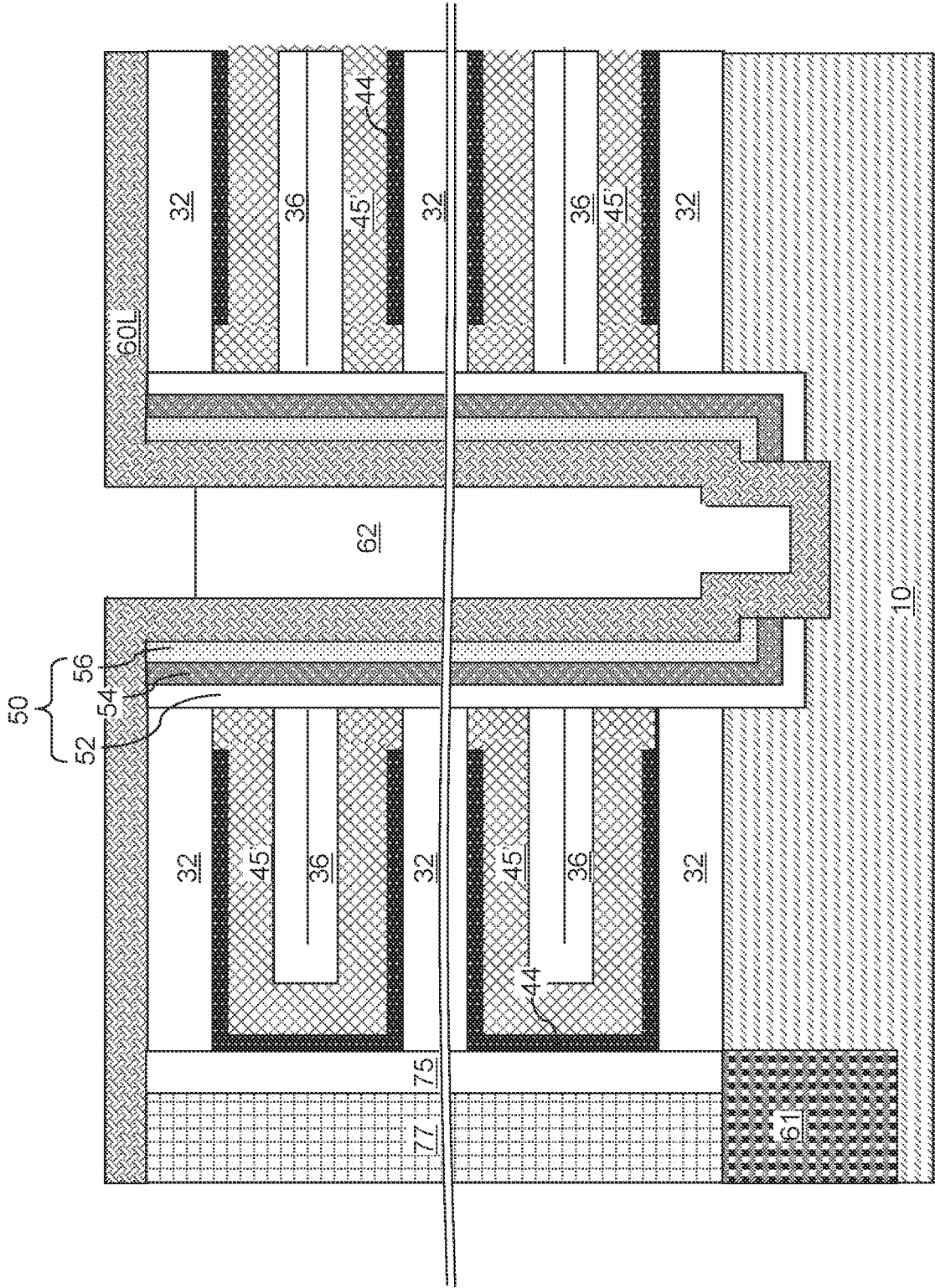


FIG. 10E

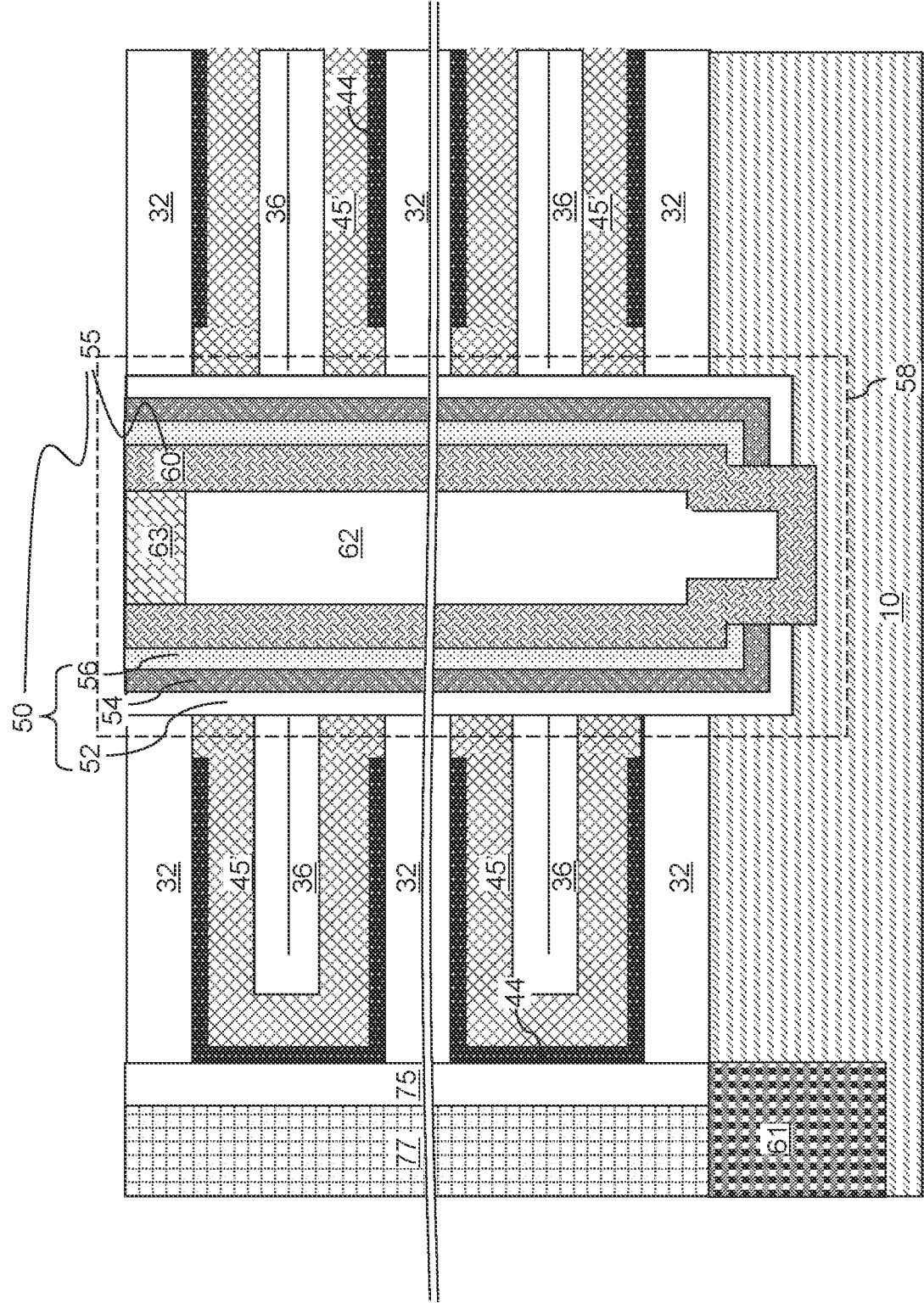
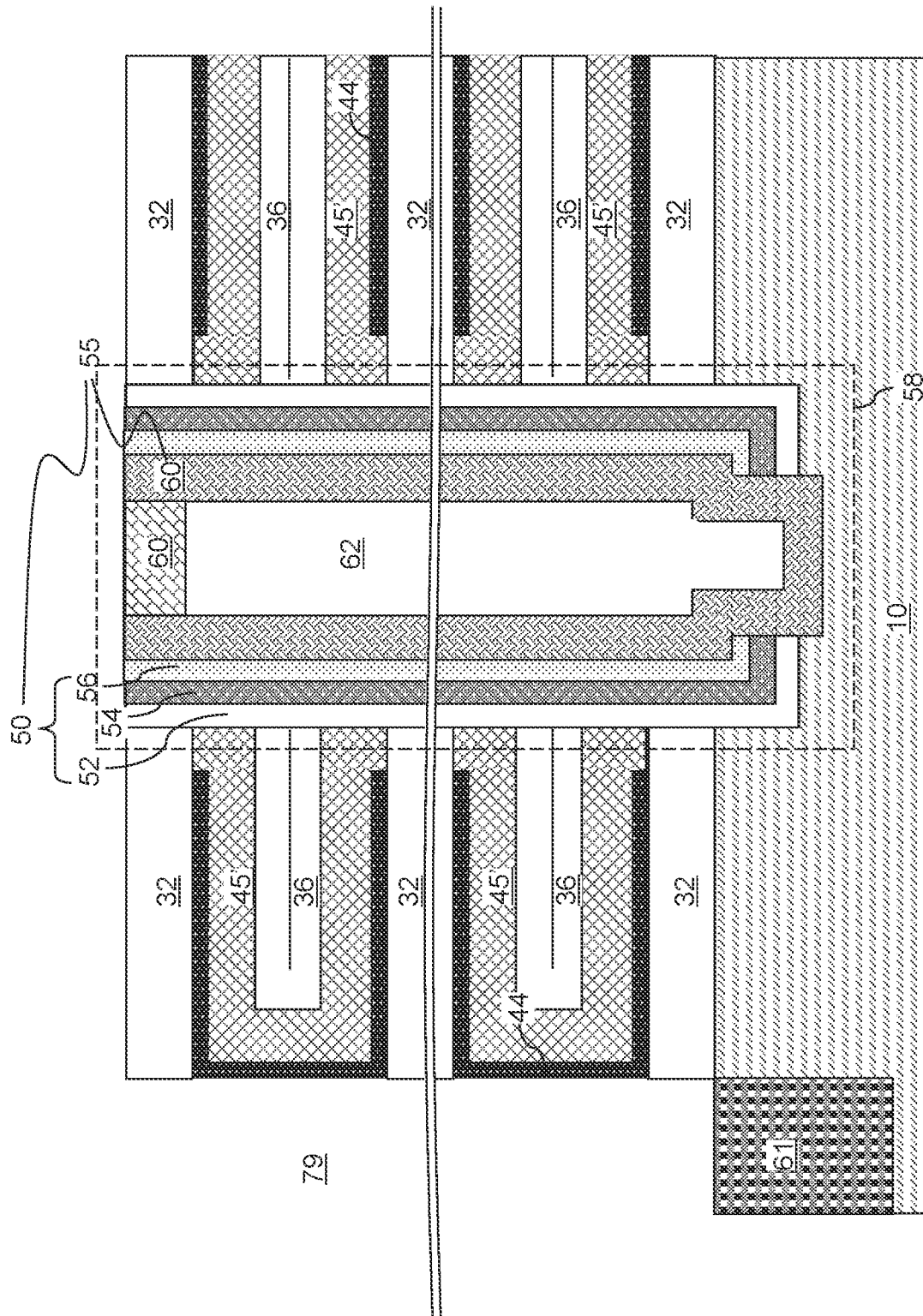
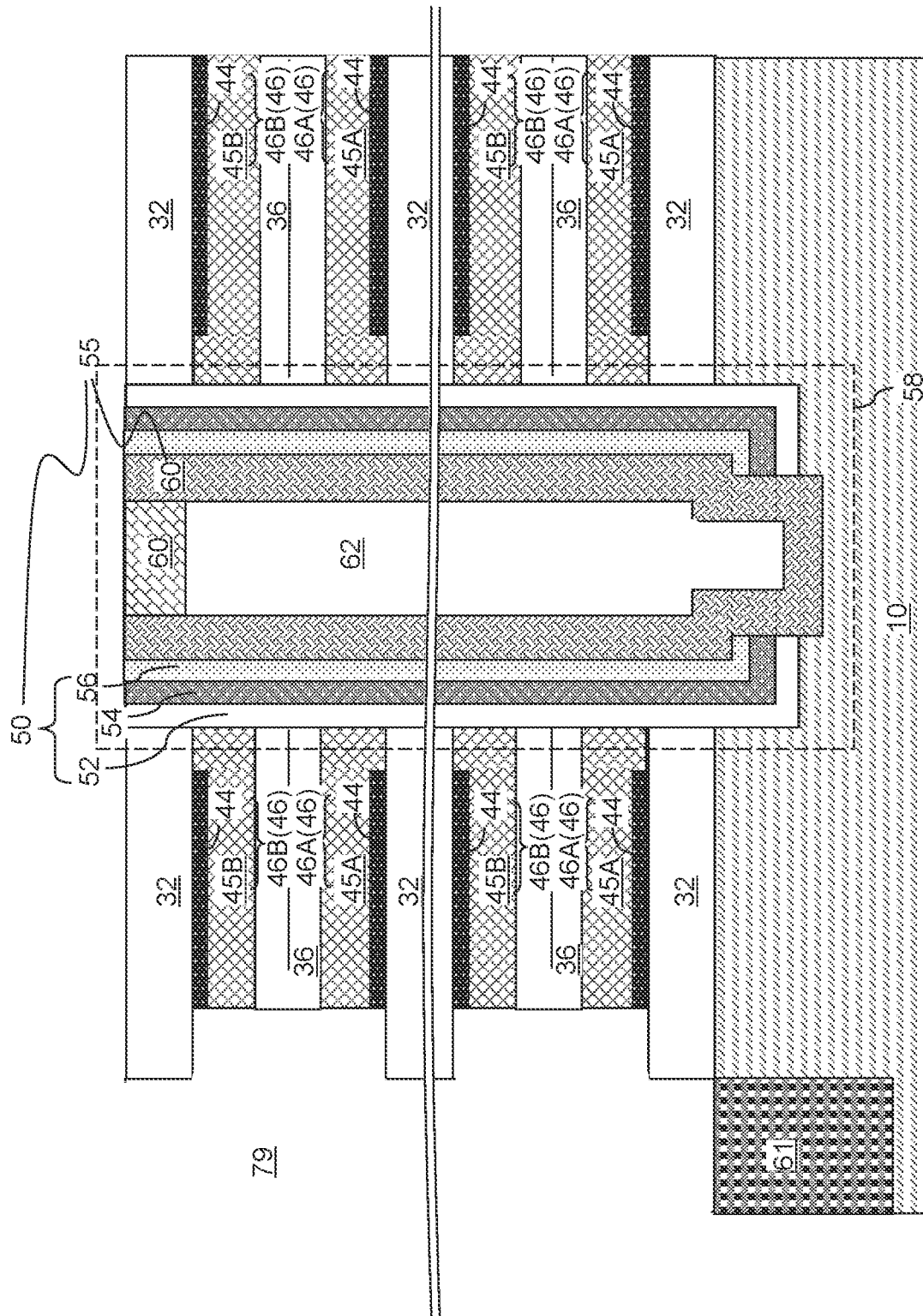
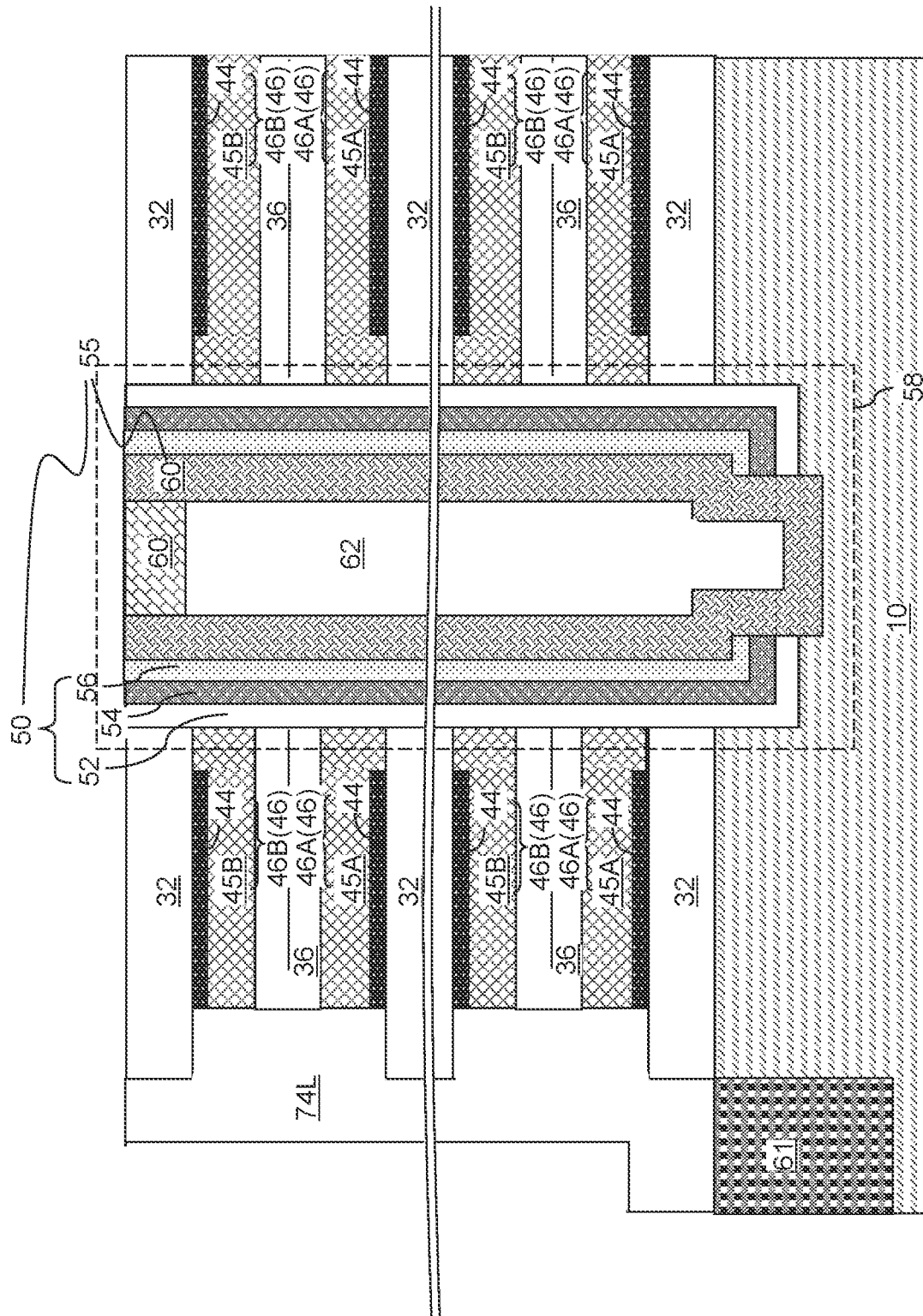


FIG. 10F







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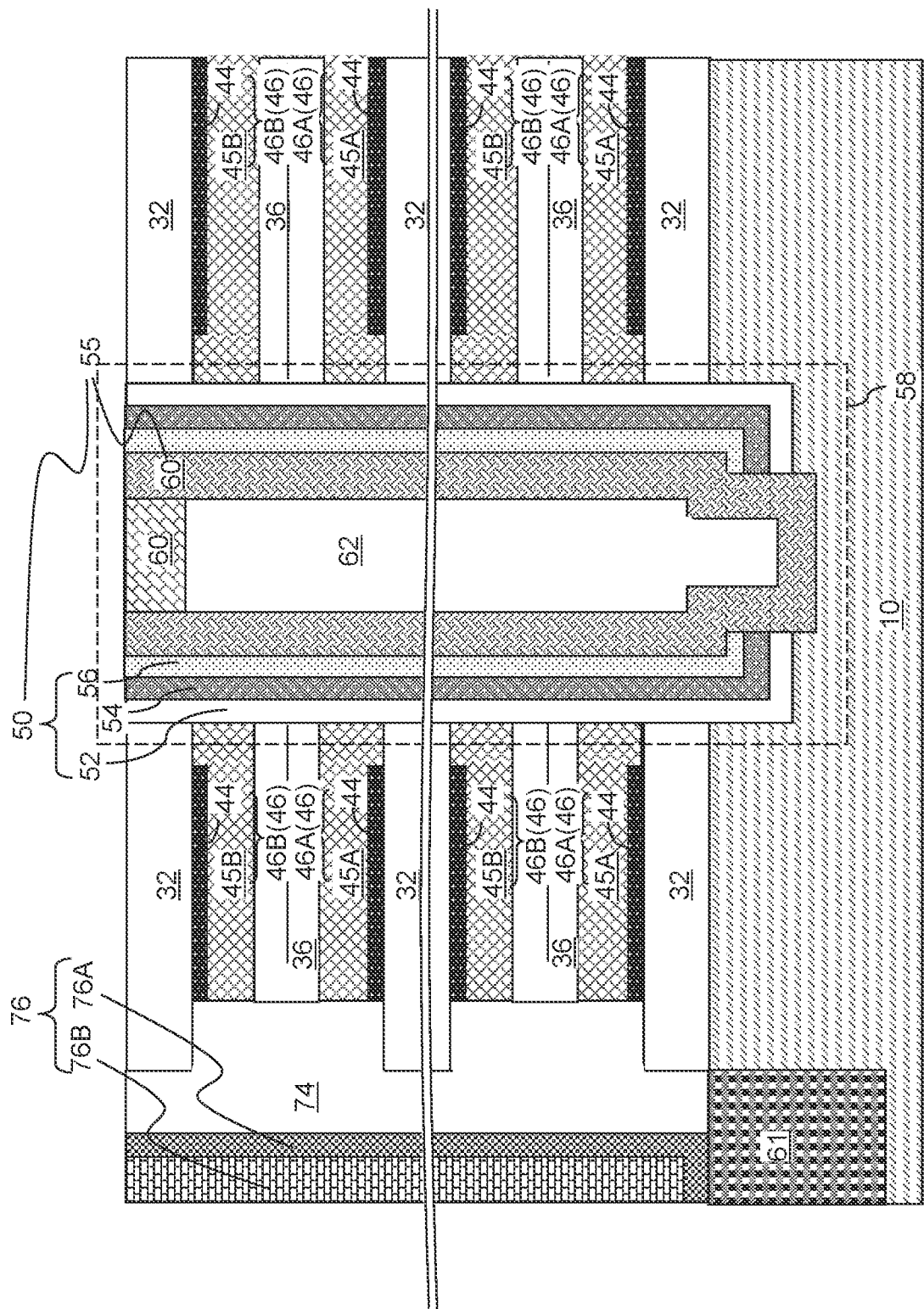
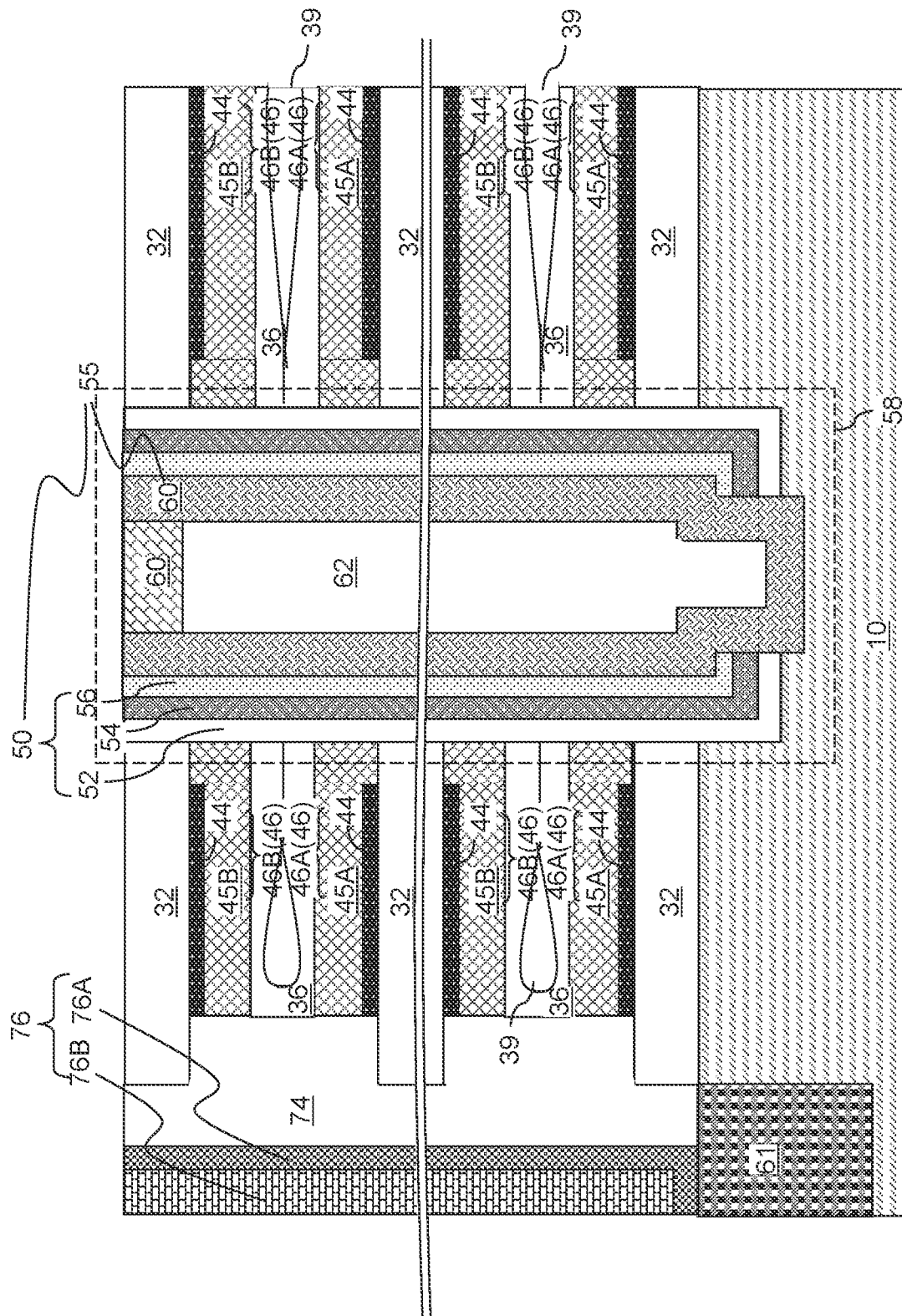
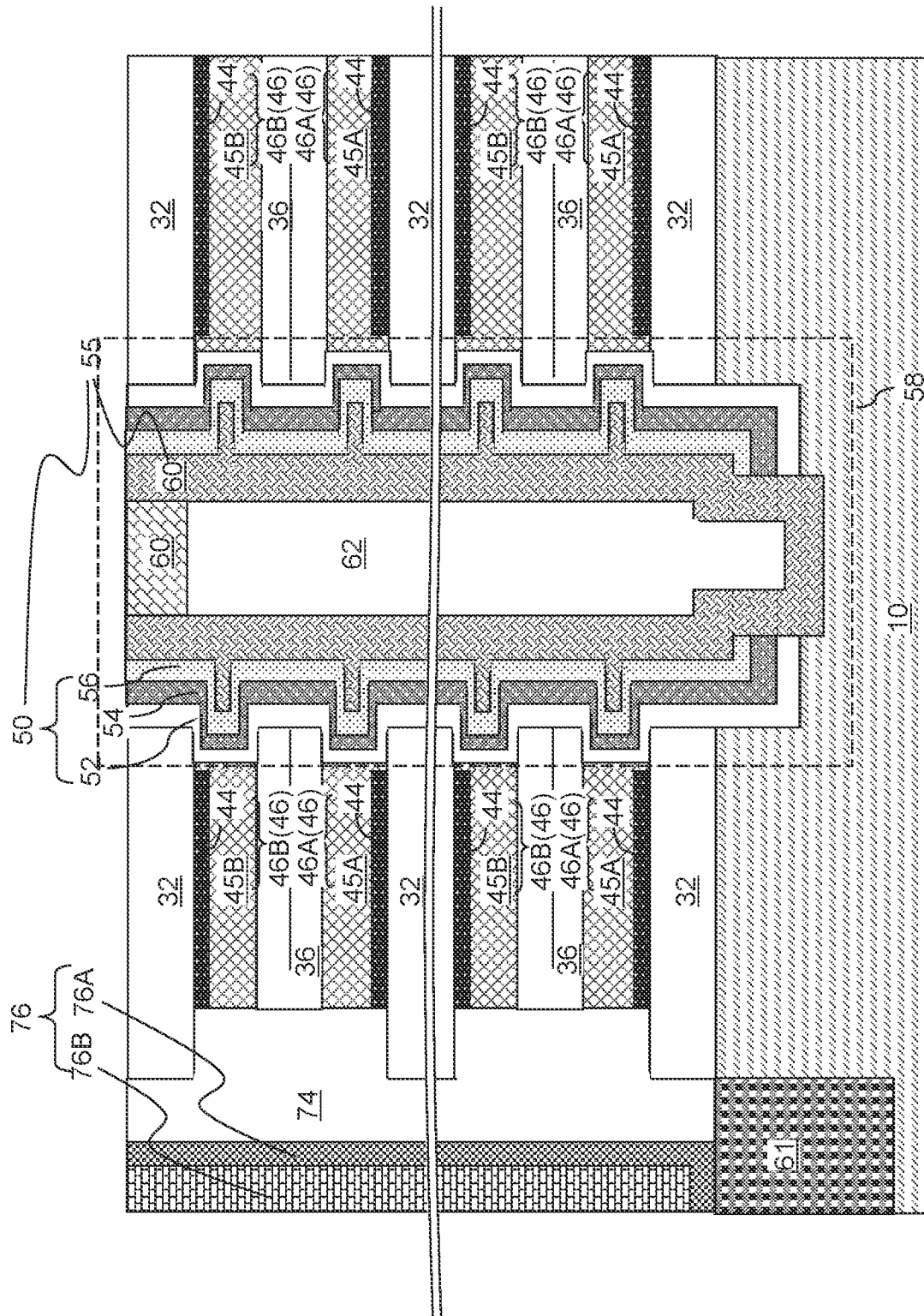


FIG. 11D



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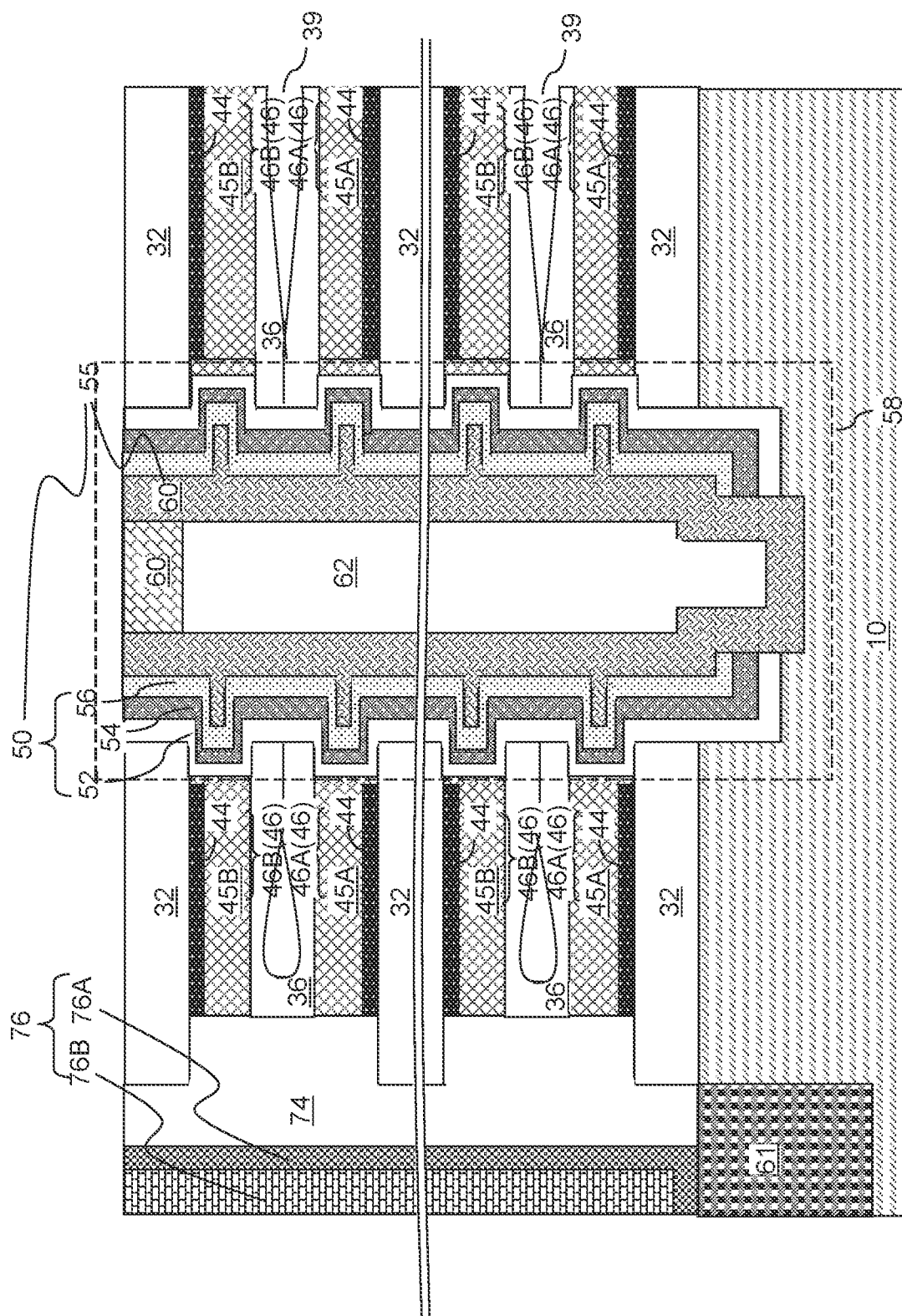
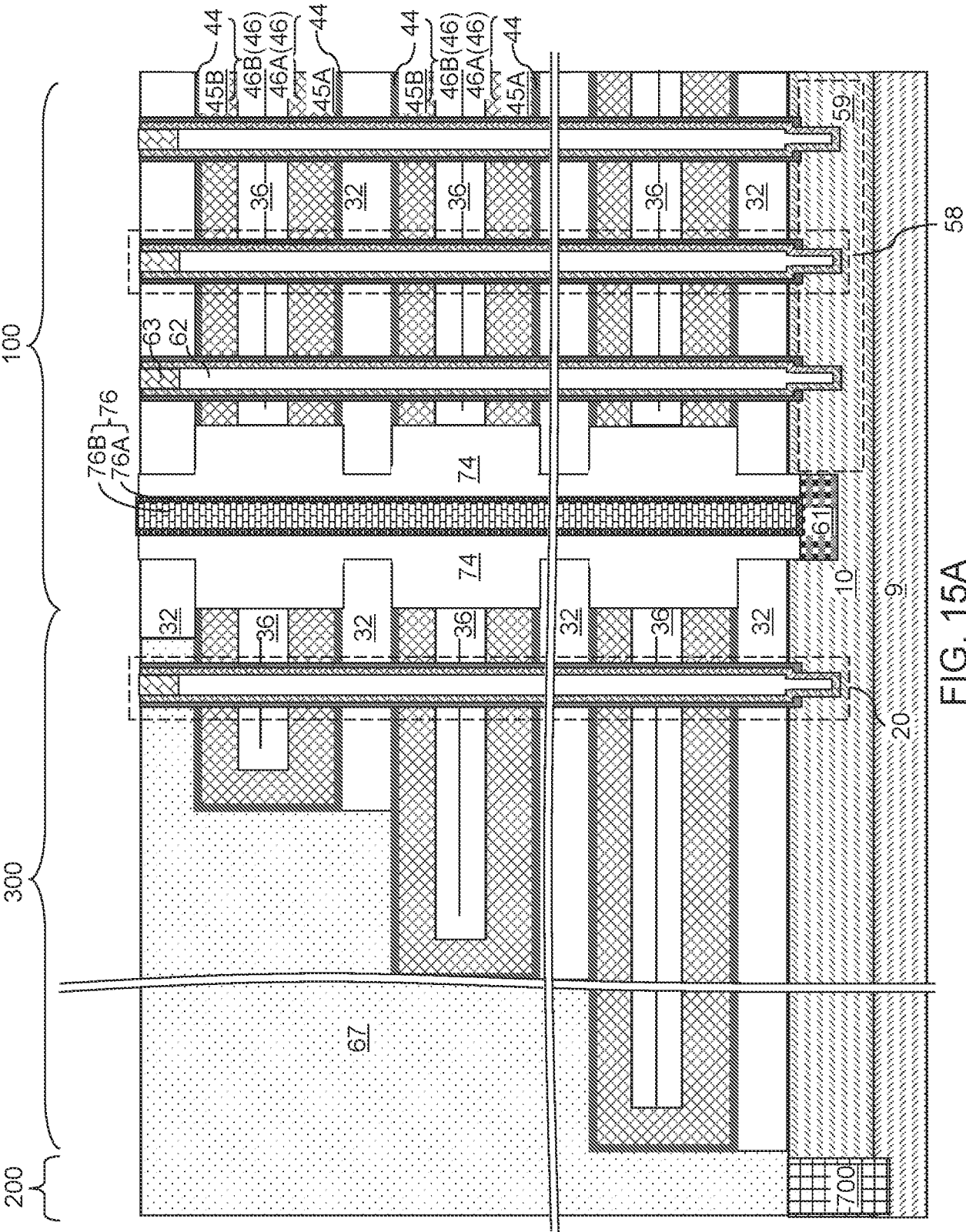
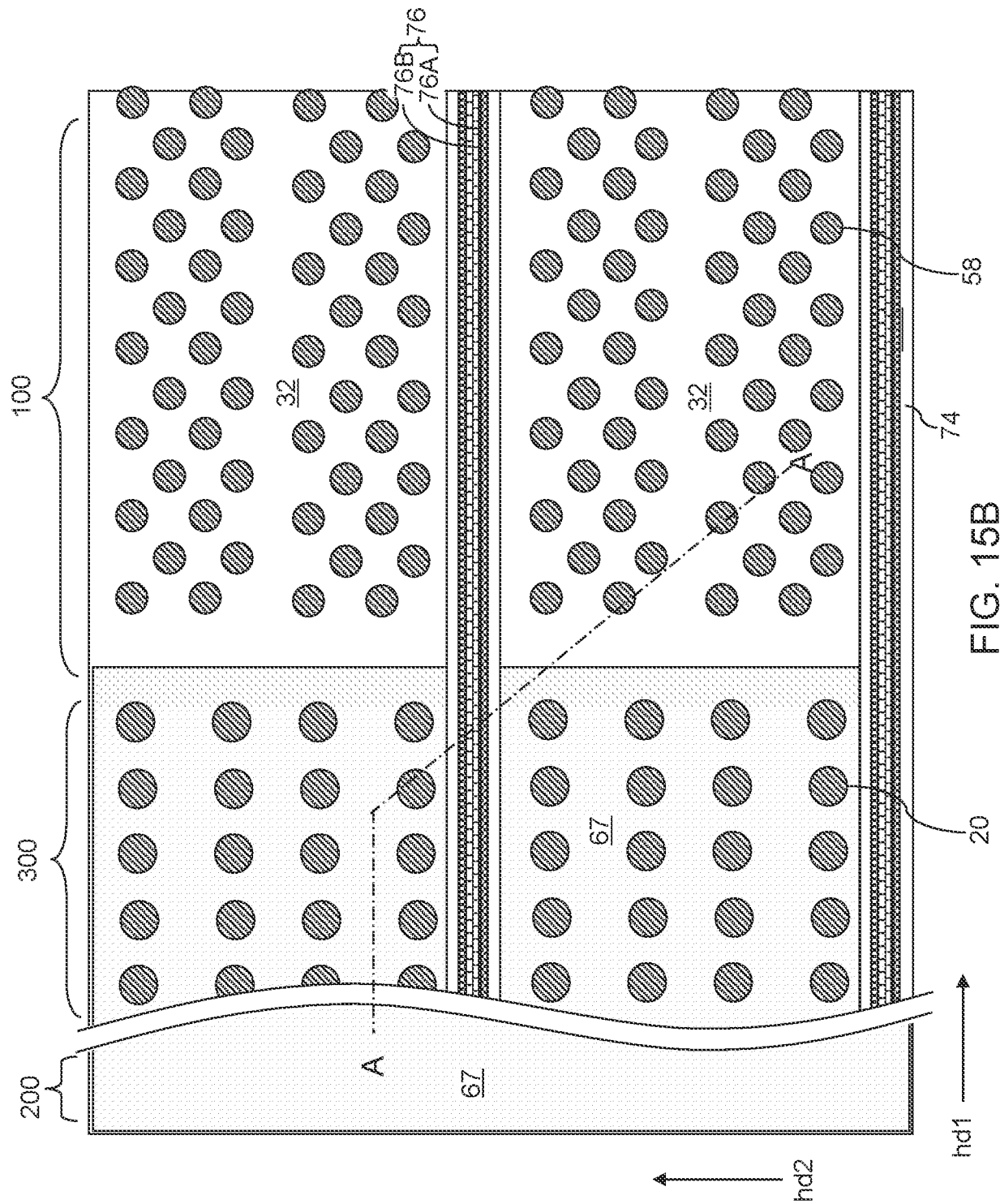


FIG. 14





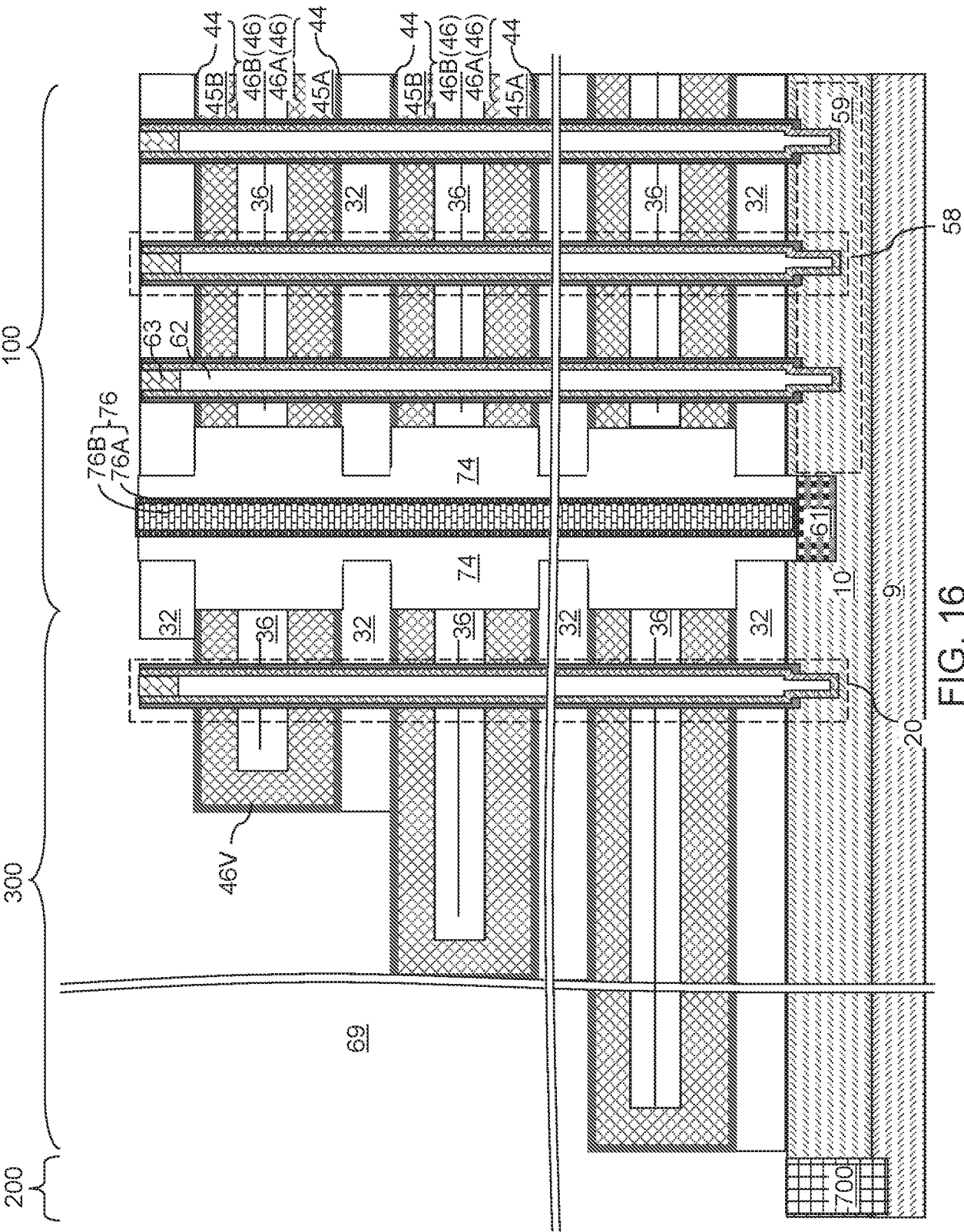
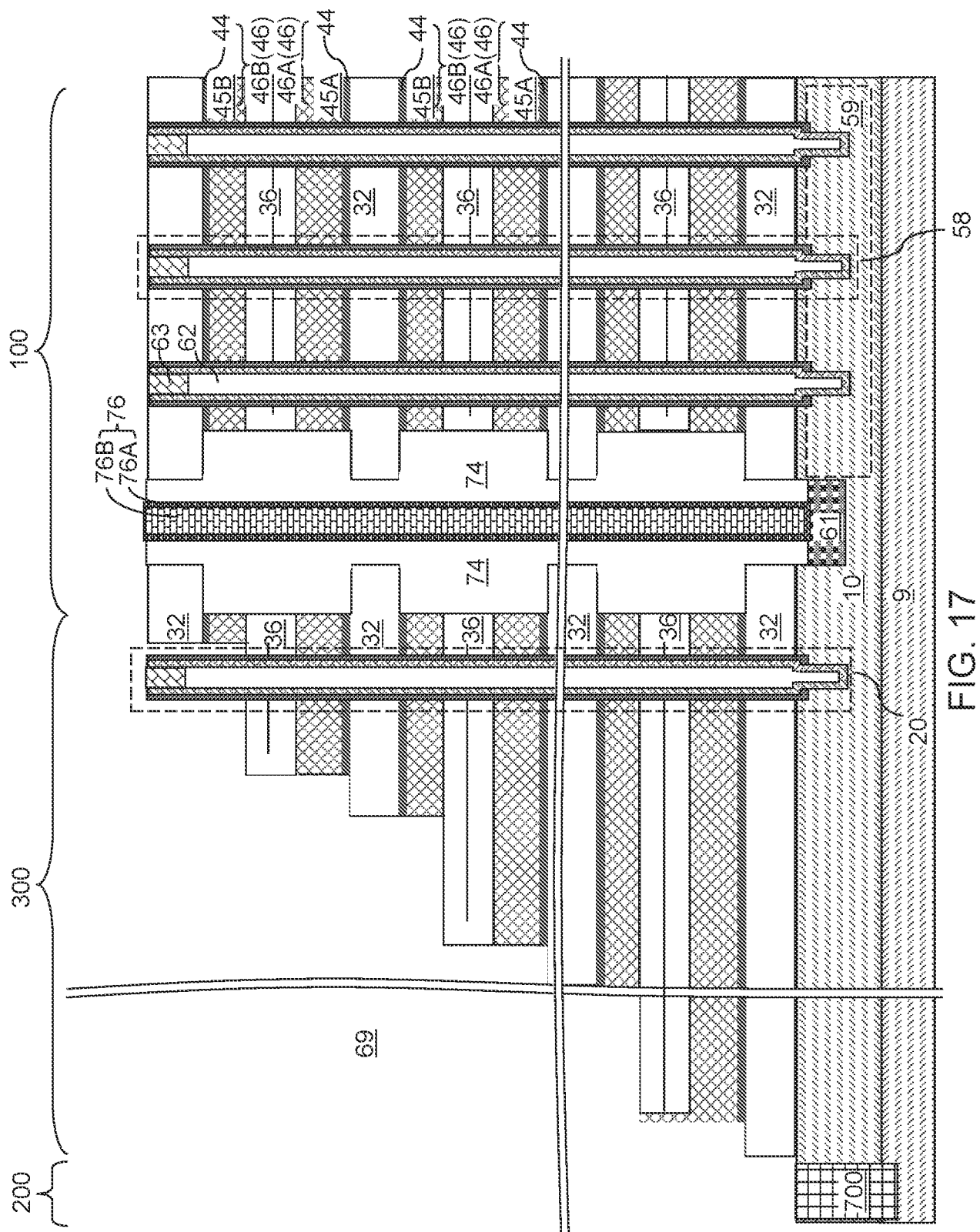
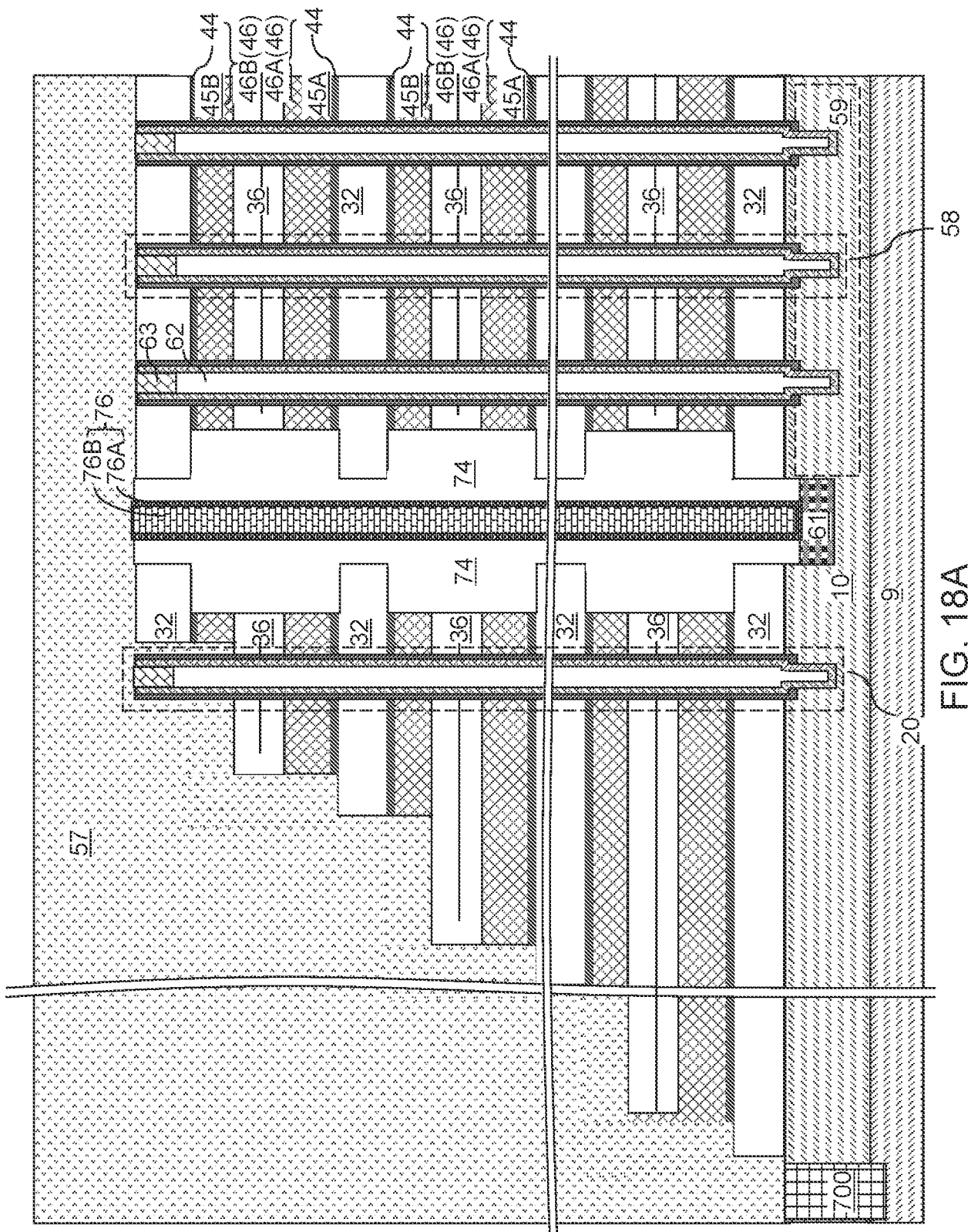
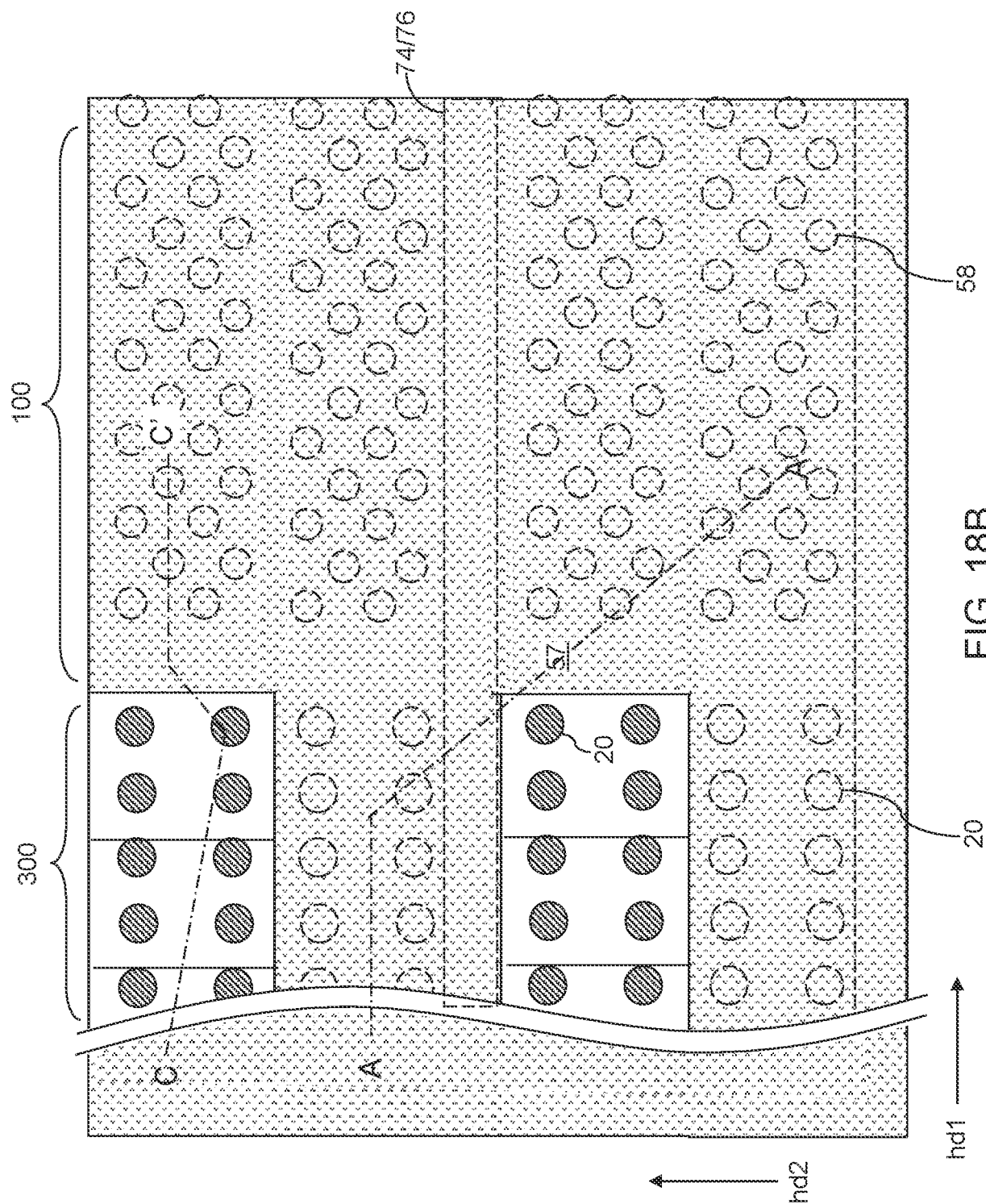
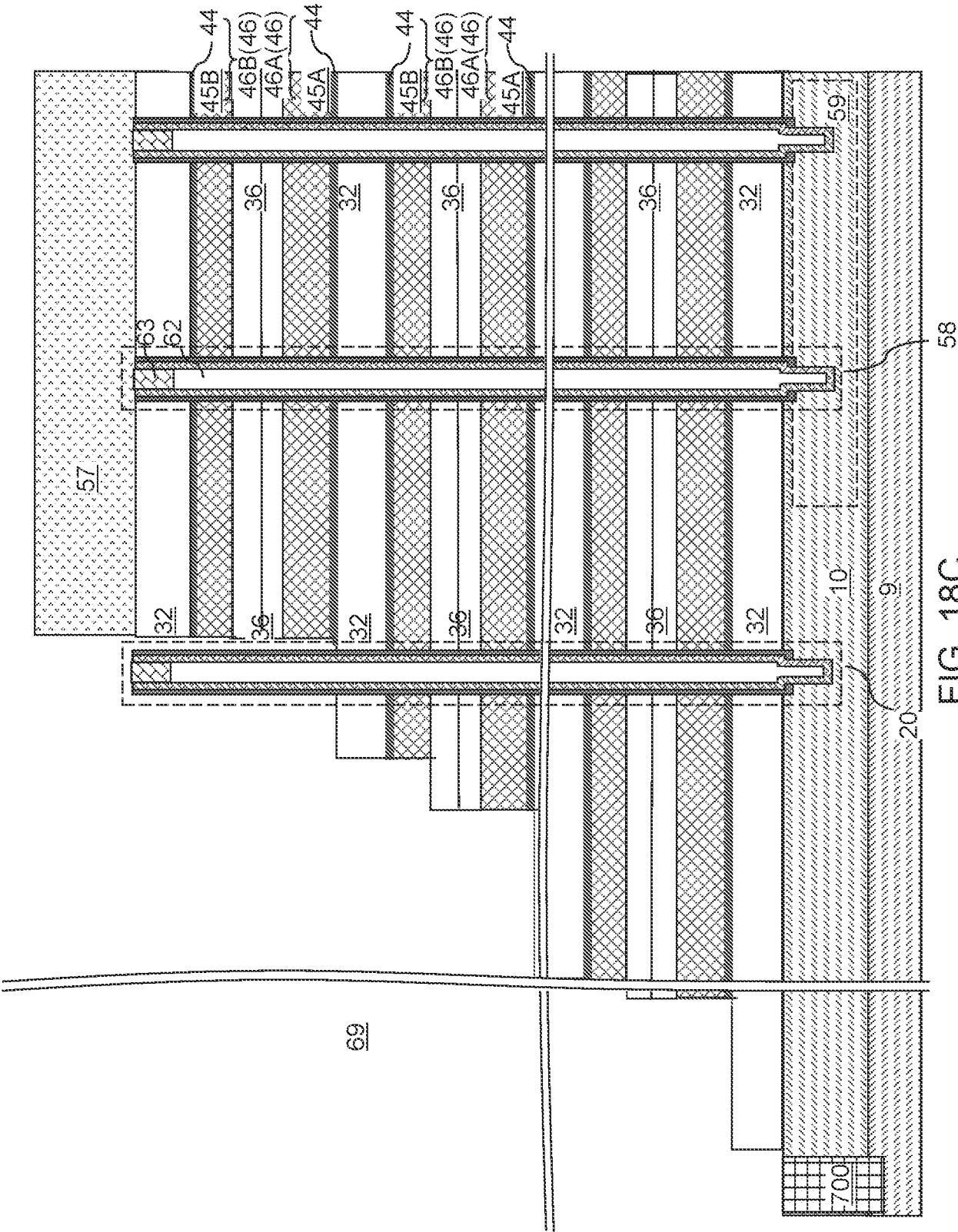


FIG. 16









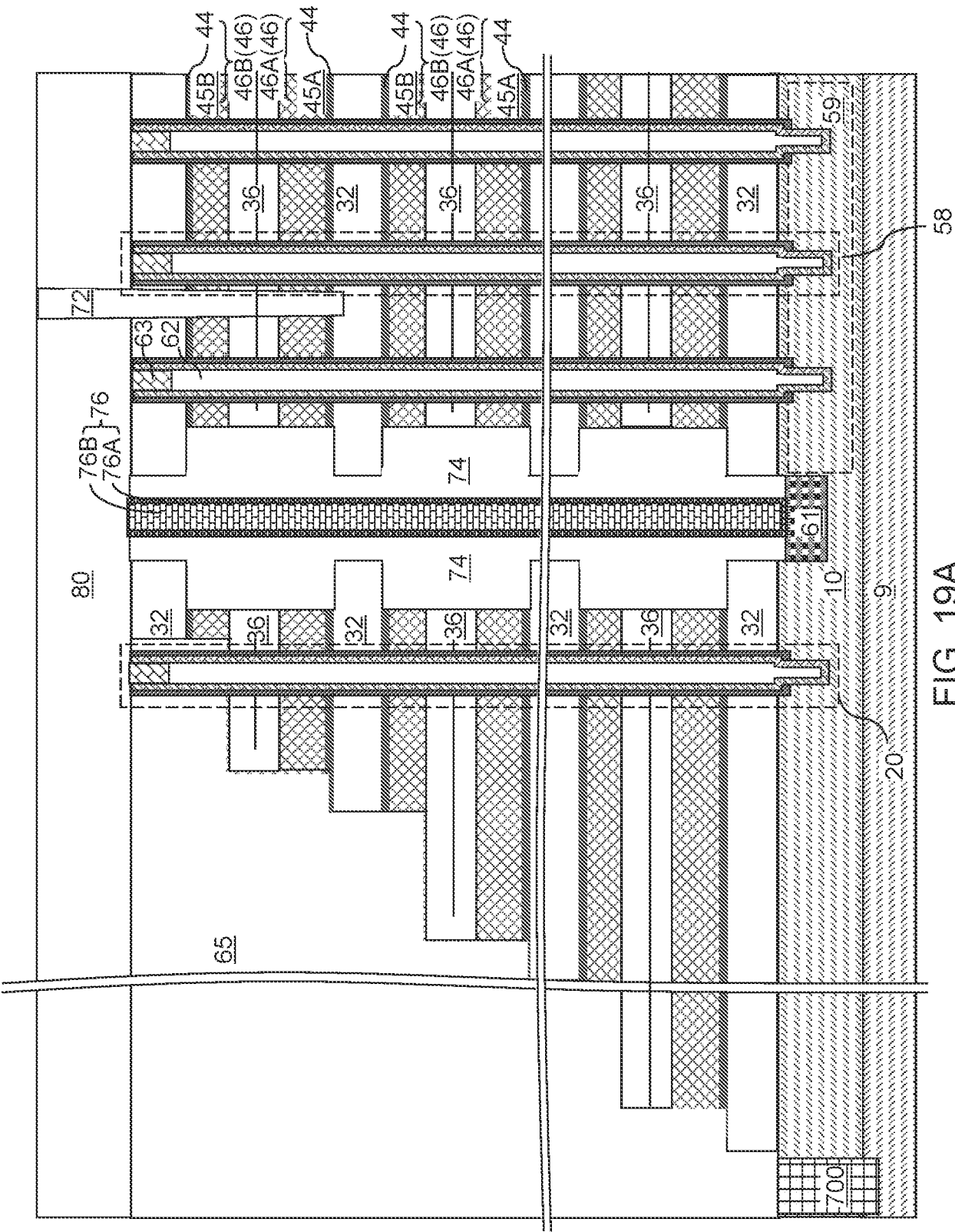
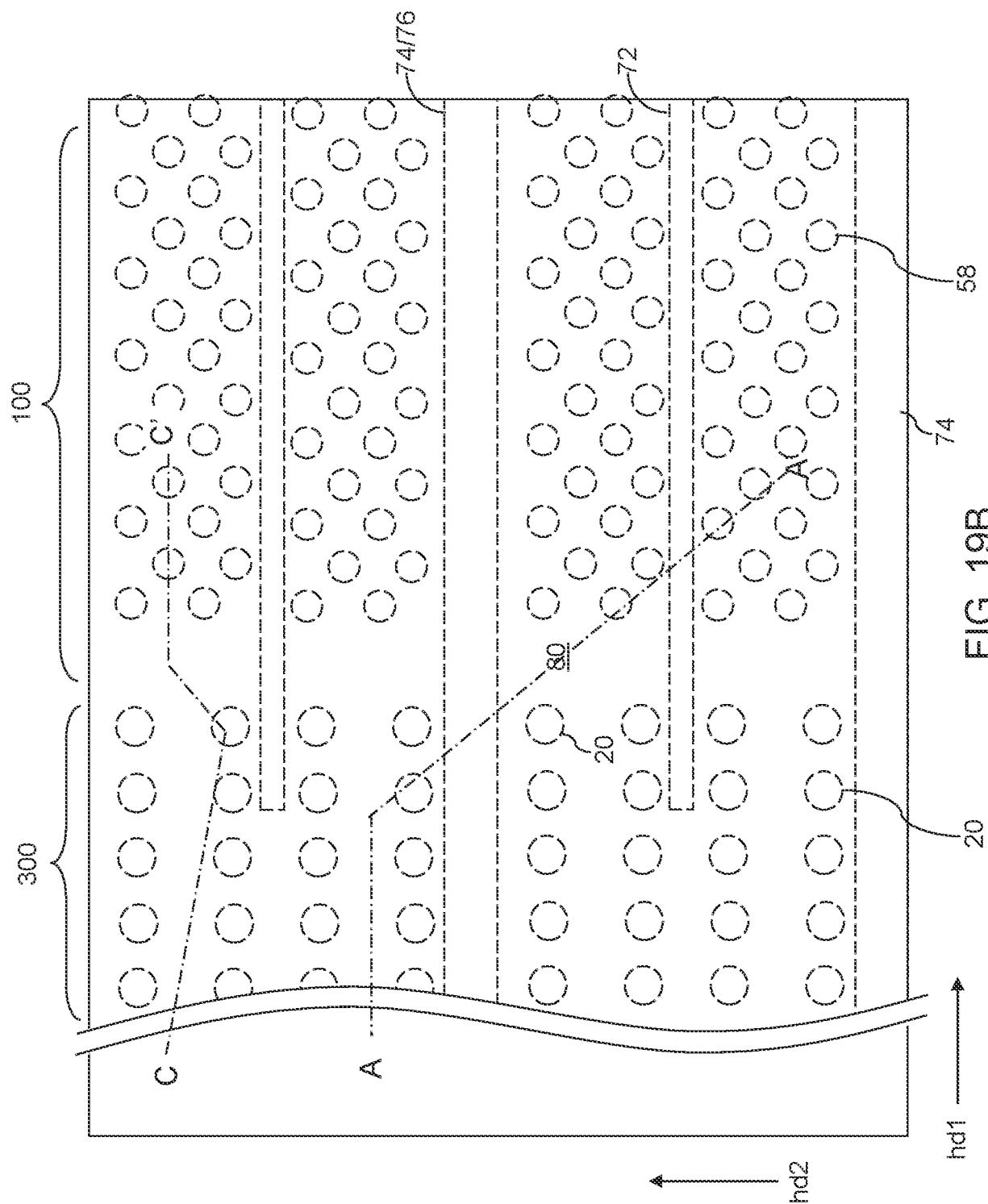
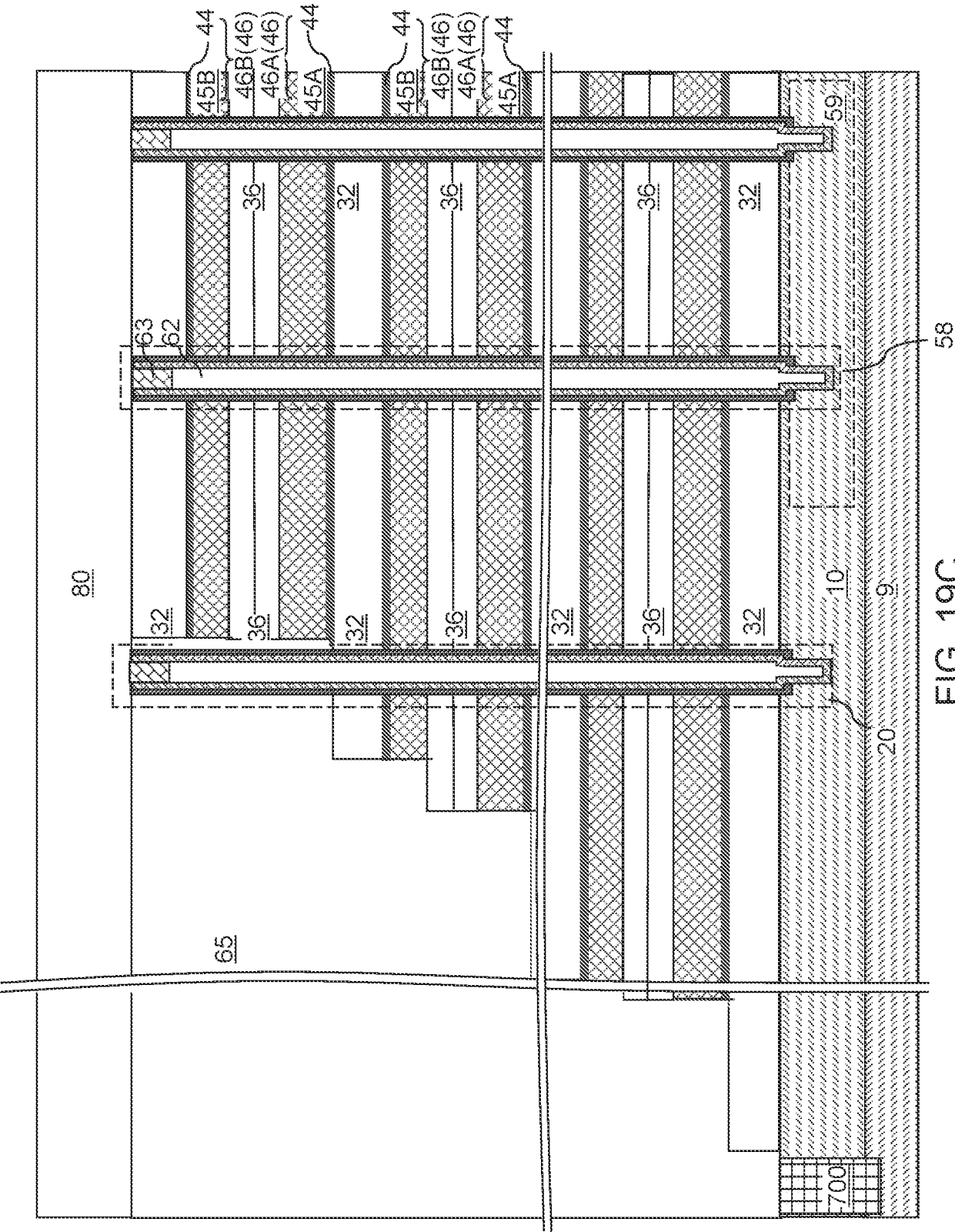


FIG. 19A





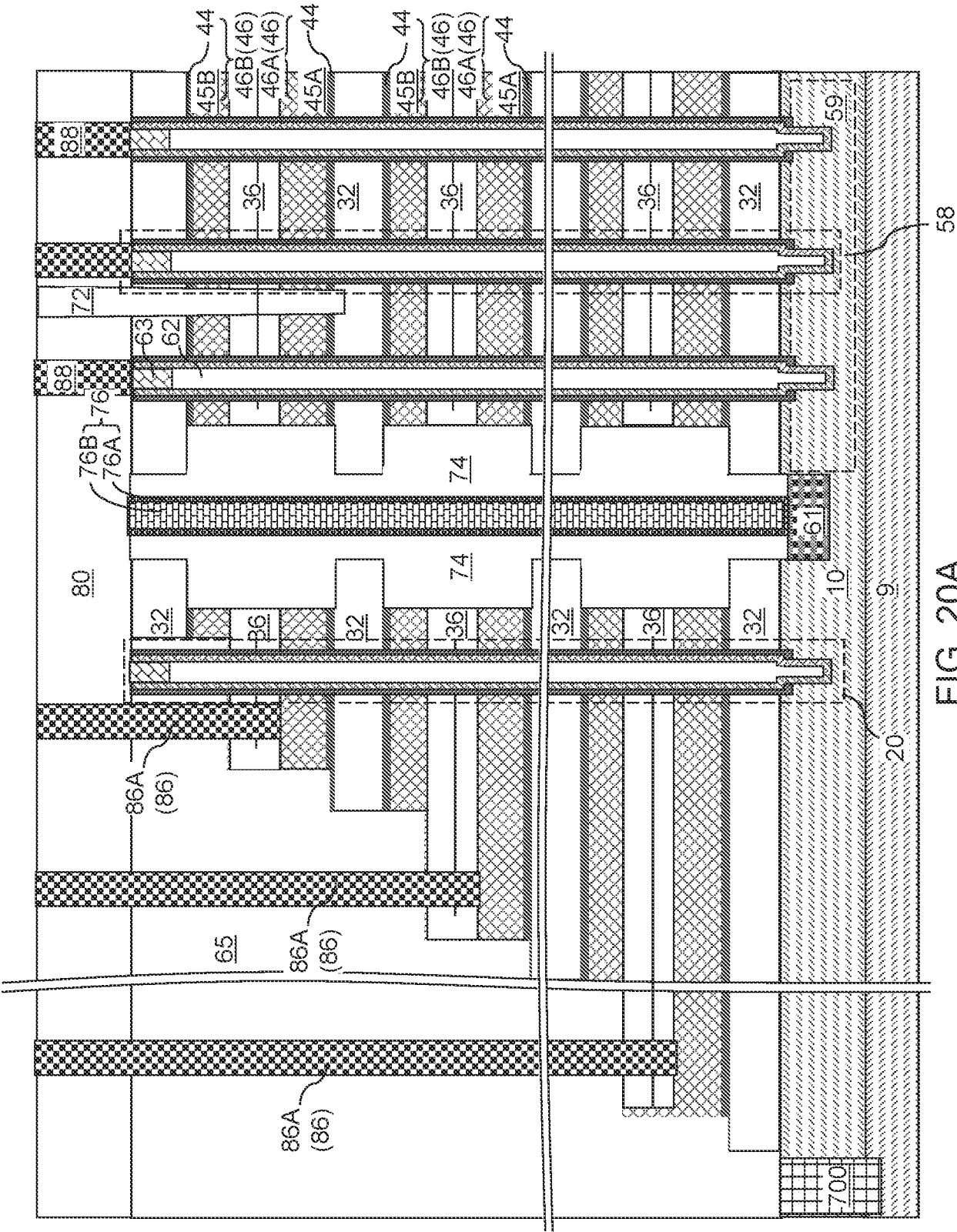
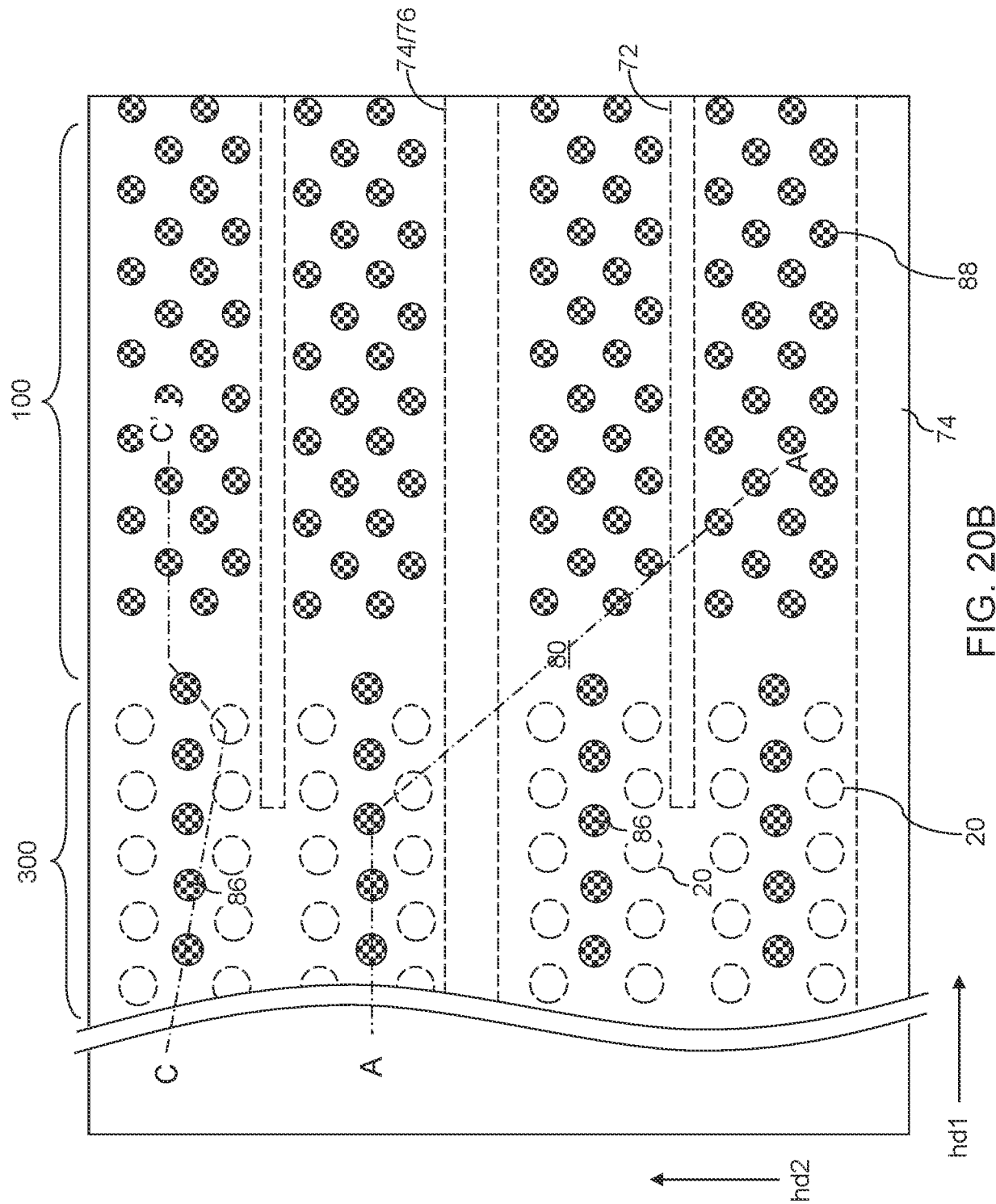
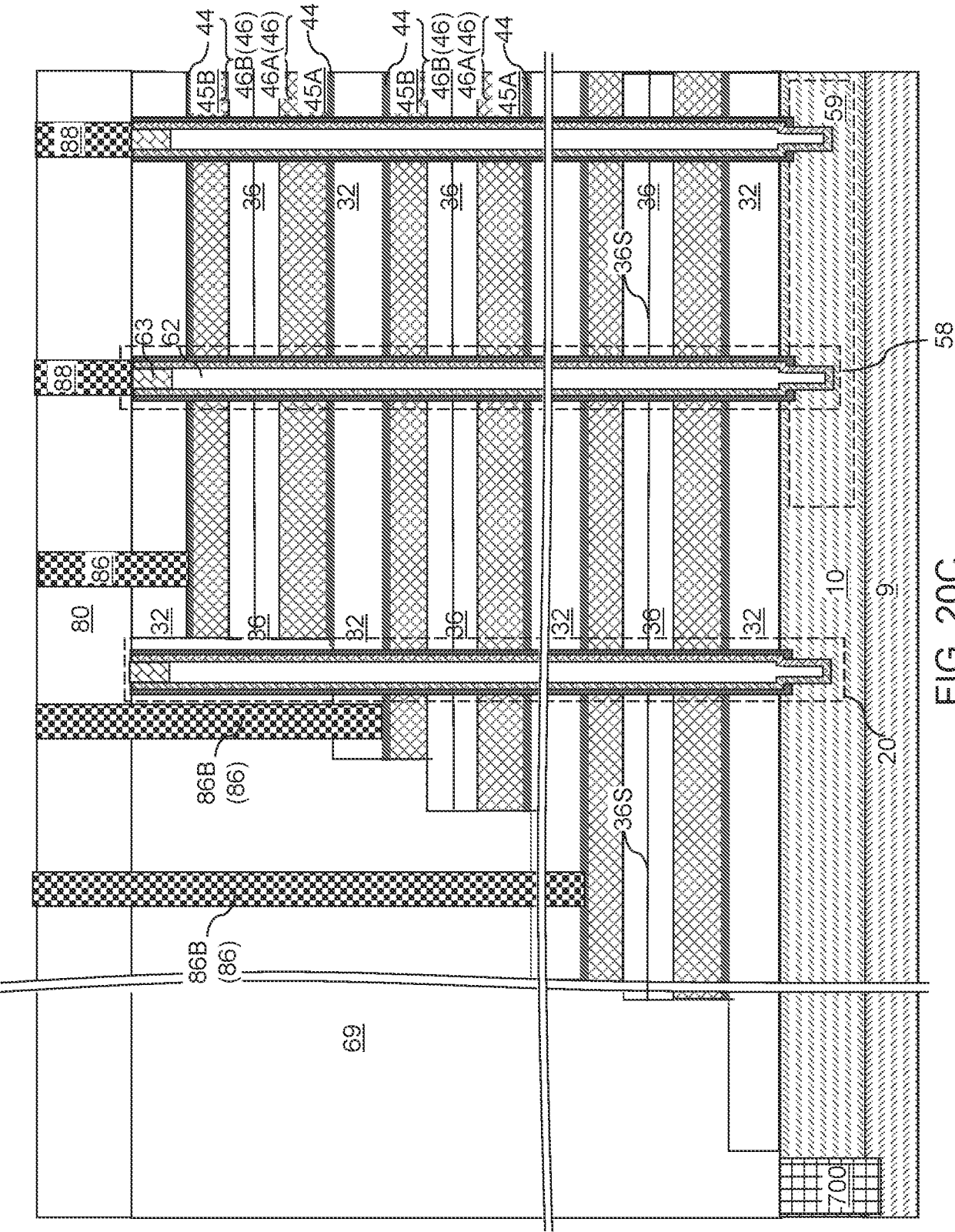


FIG. 20A





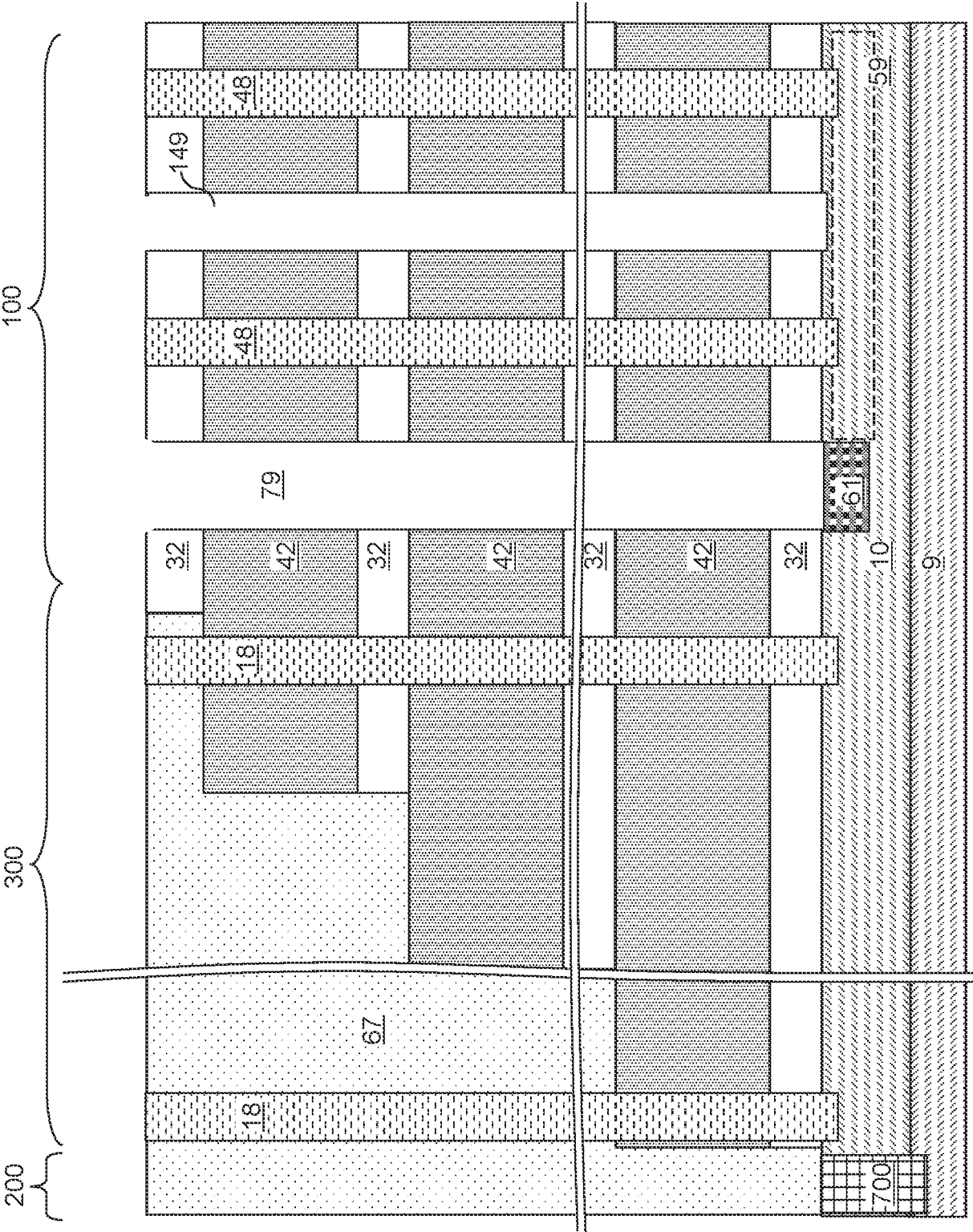


FIG. 21

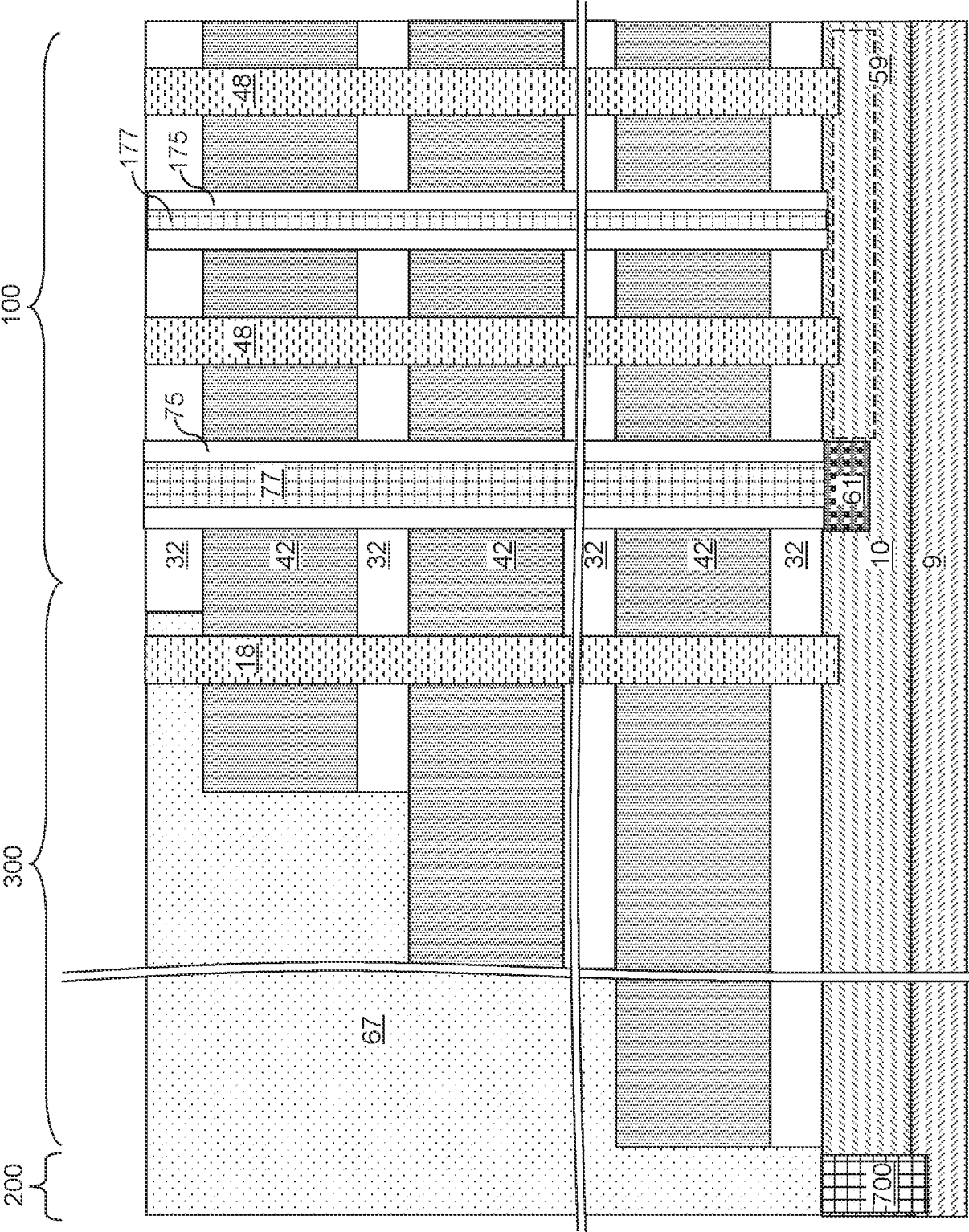


FIG. 22A

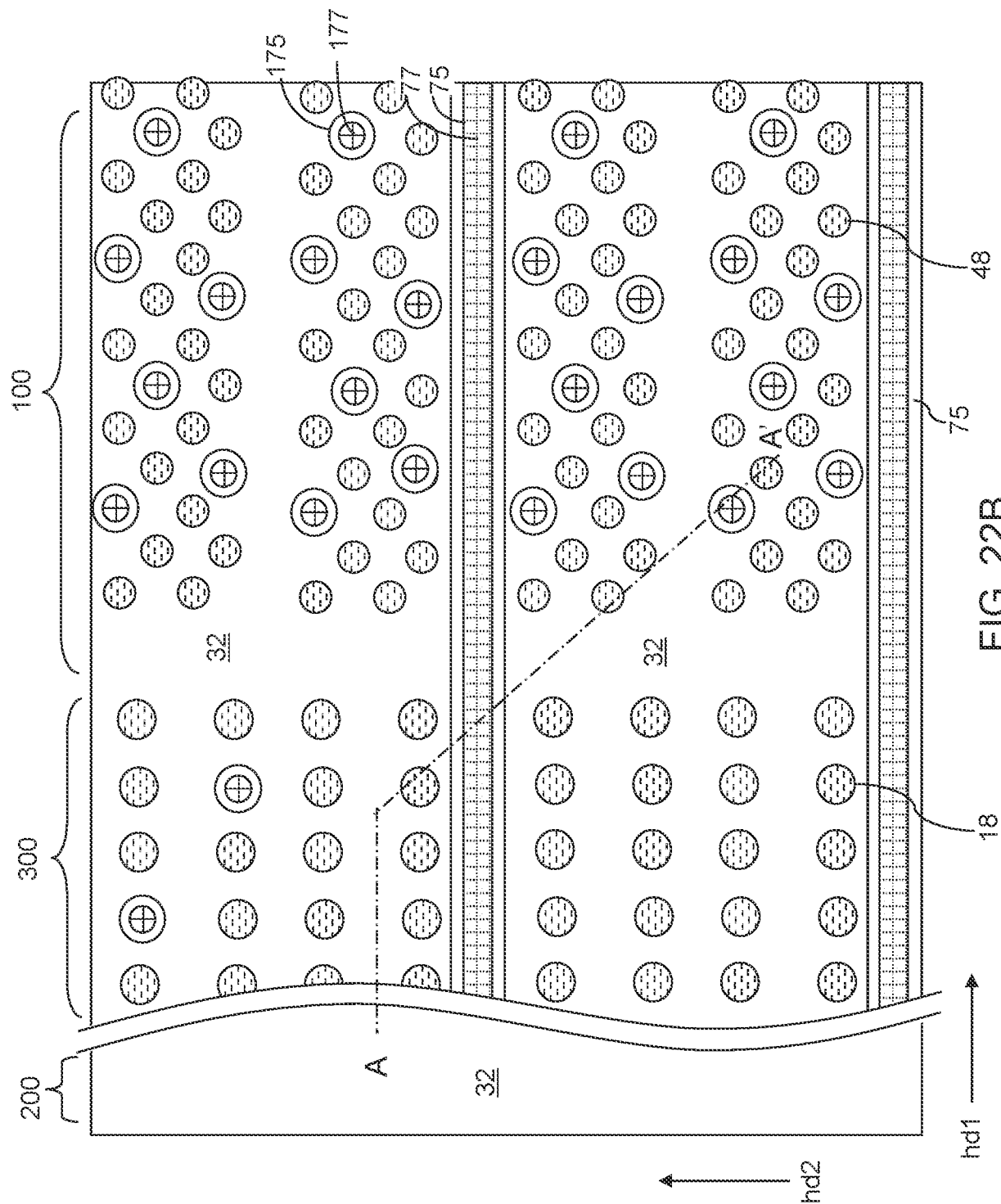


FIG. 22B

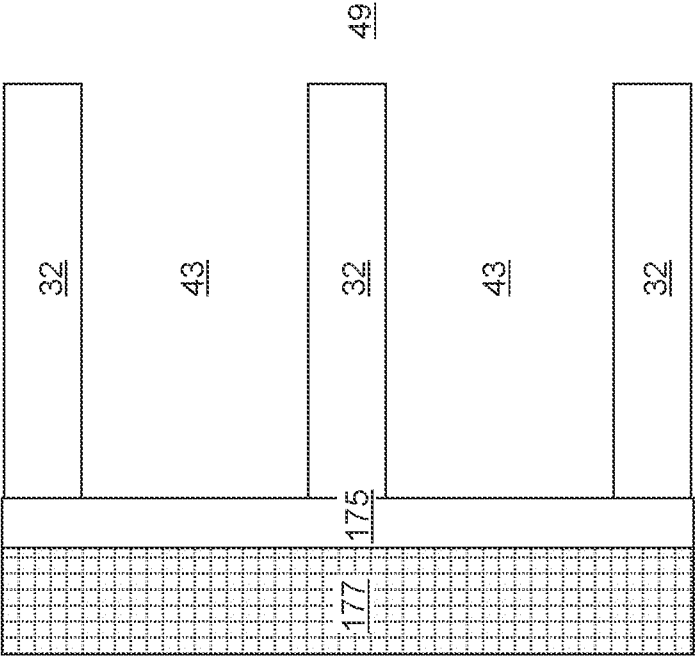


FIG. 23B

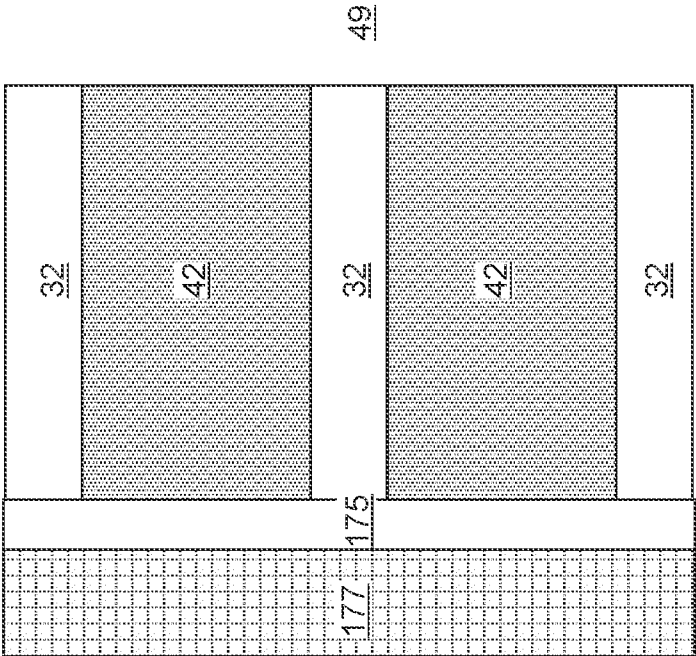


FIG. 23A

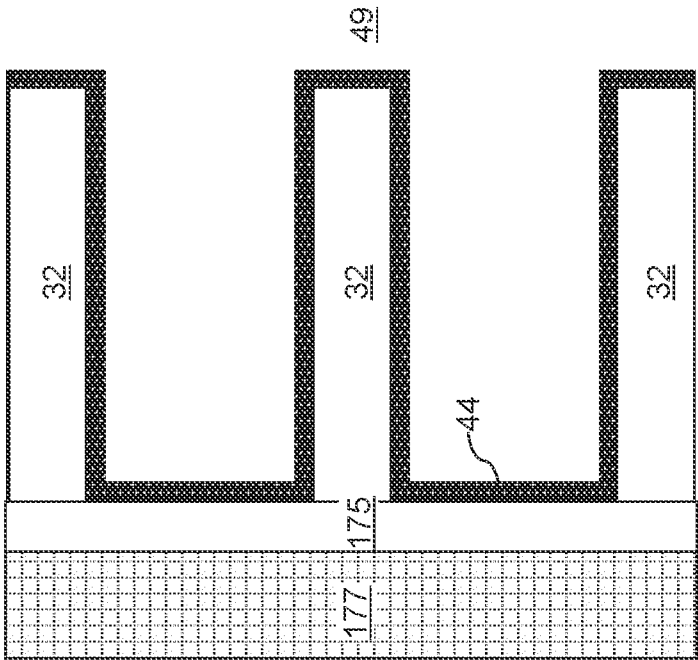


FIG. 24A

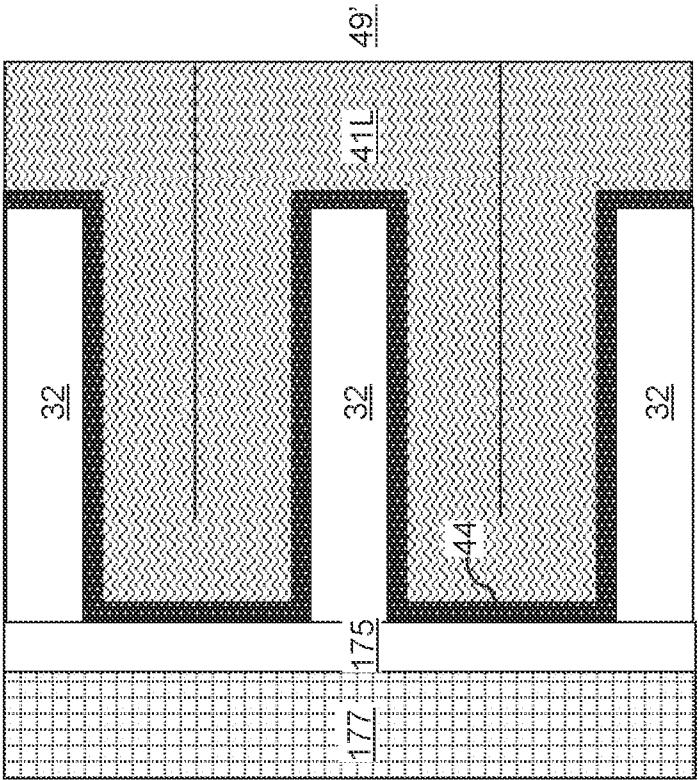


FIG. 24B

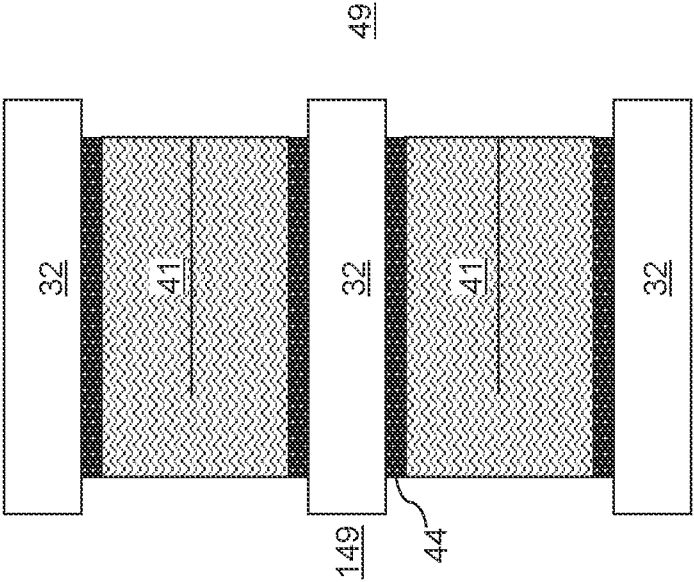


FIG. 25B

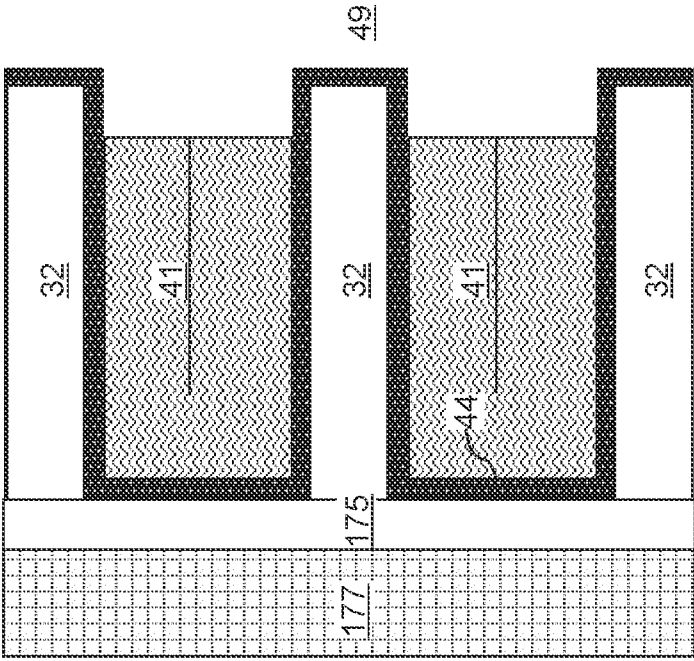


FIG. 25A

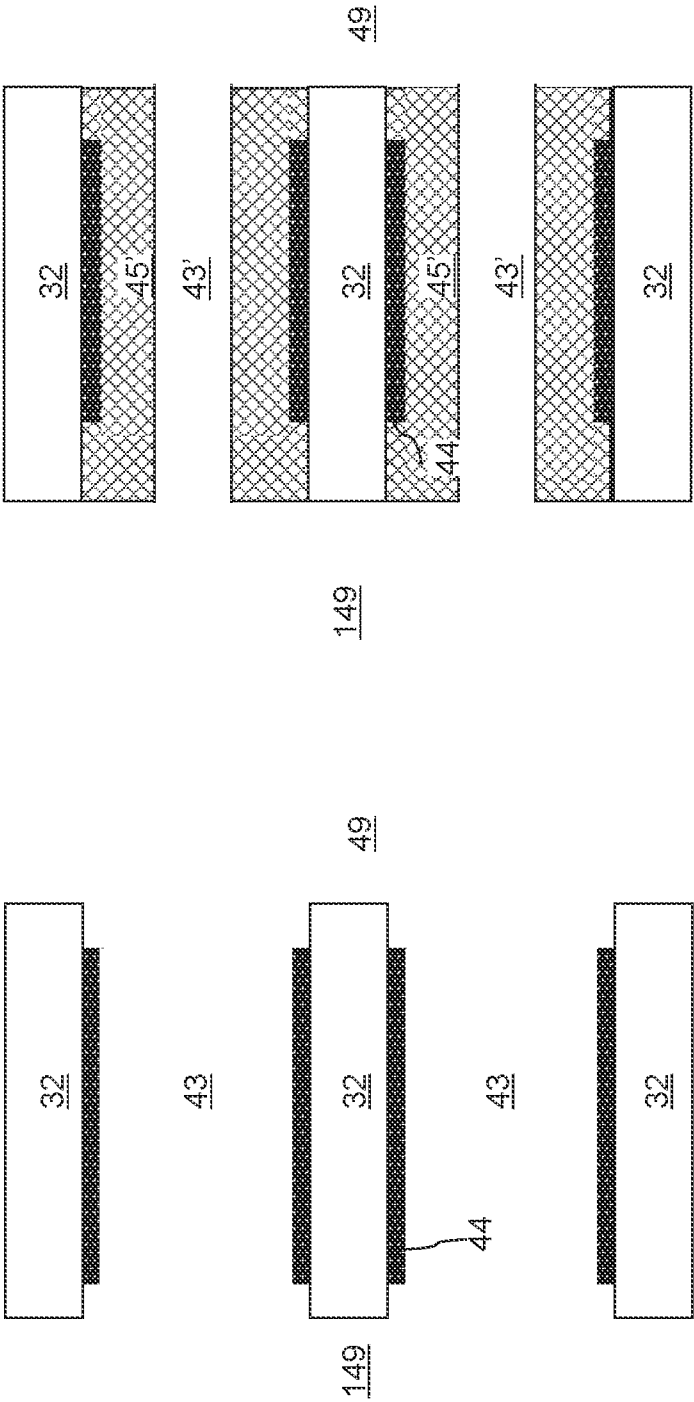


FIG. 26B

FIG. 26A

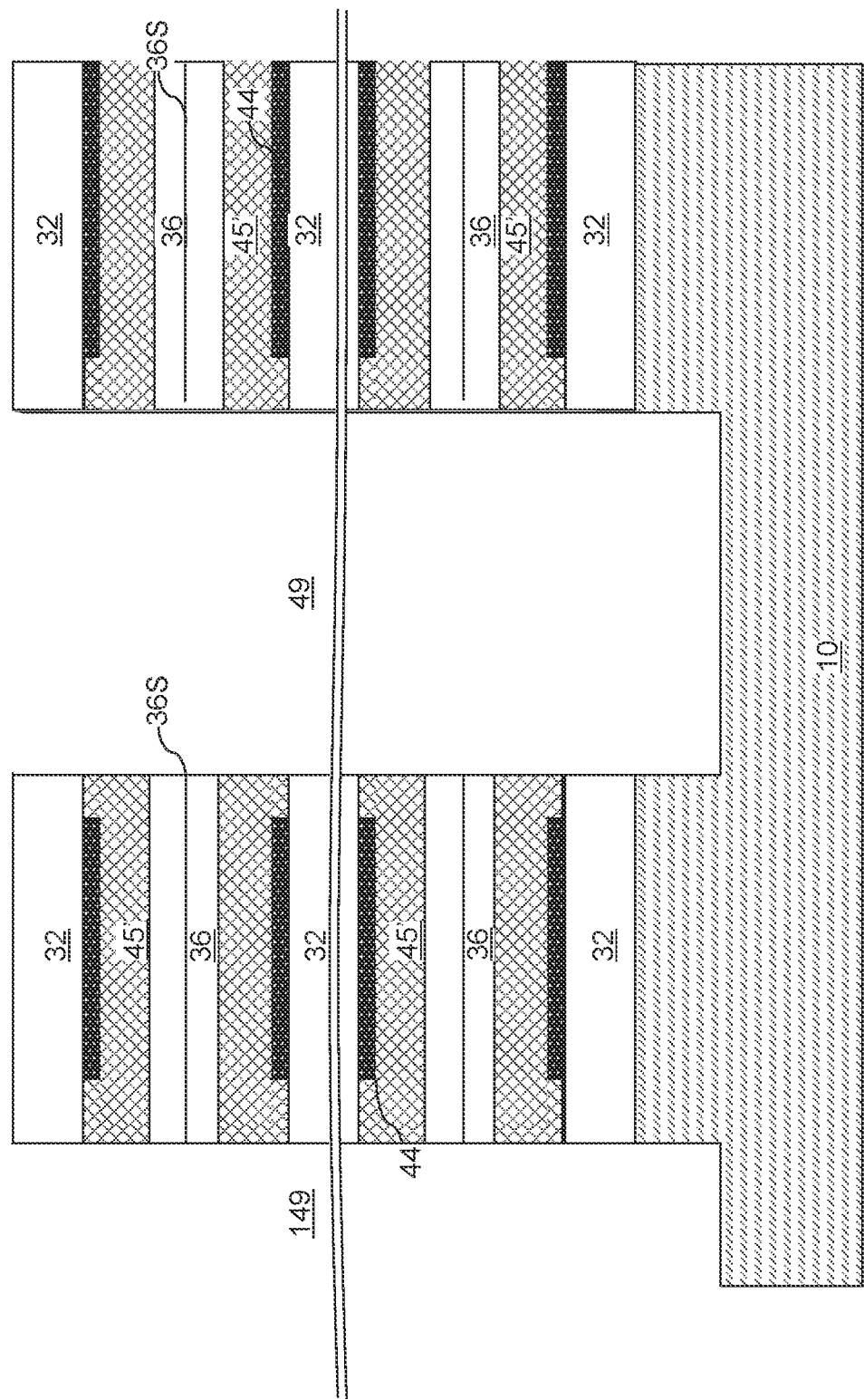


FIG. 27

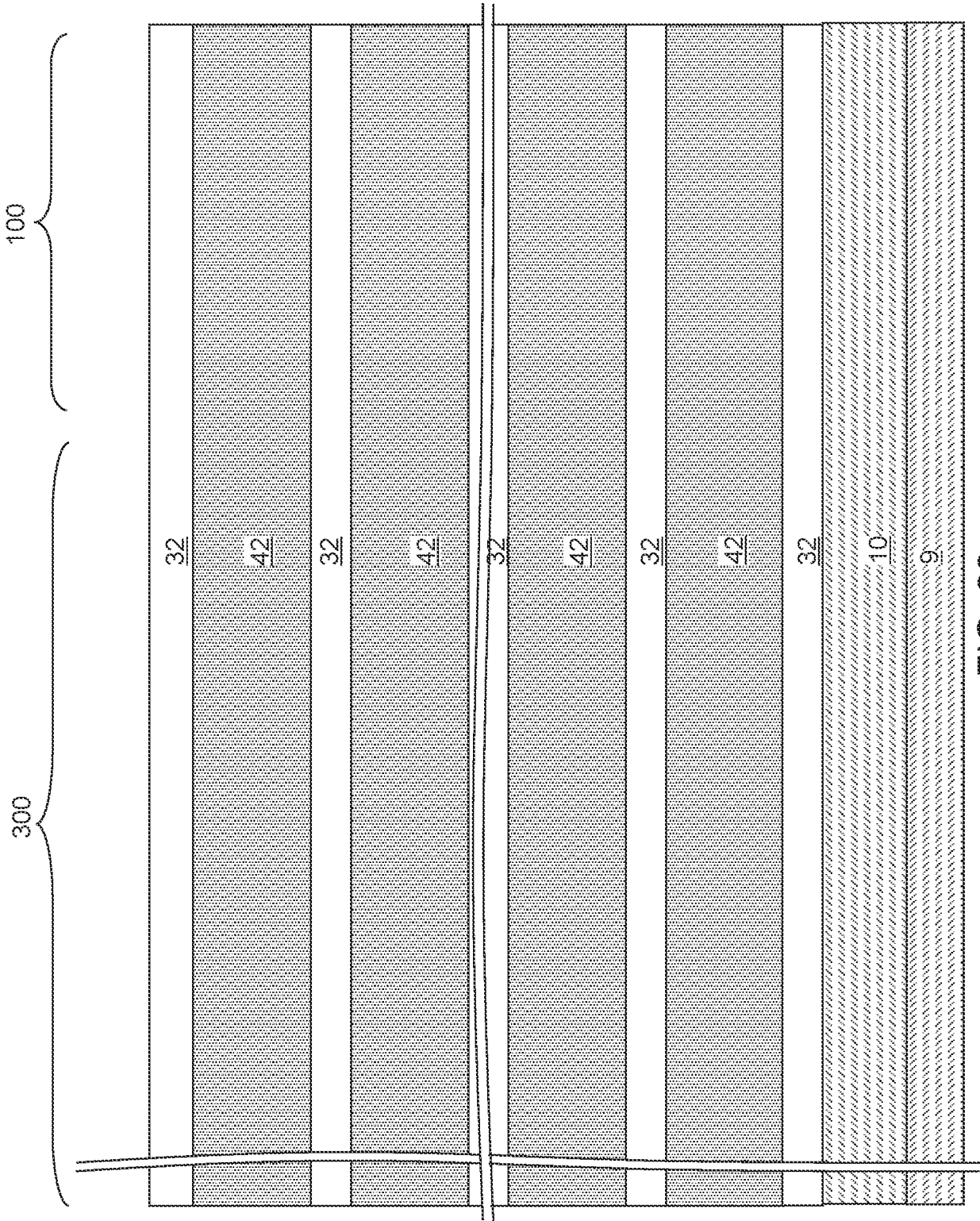


FIG. 28

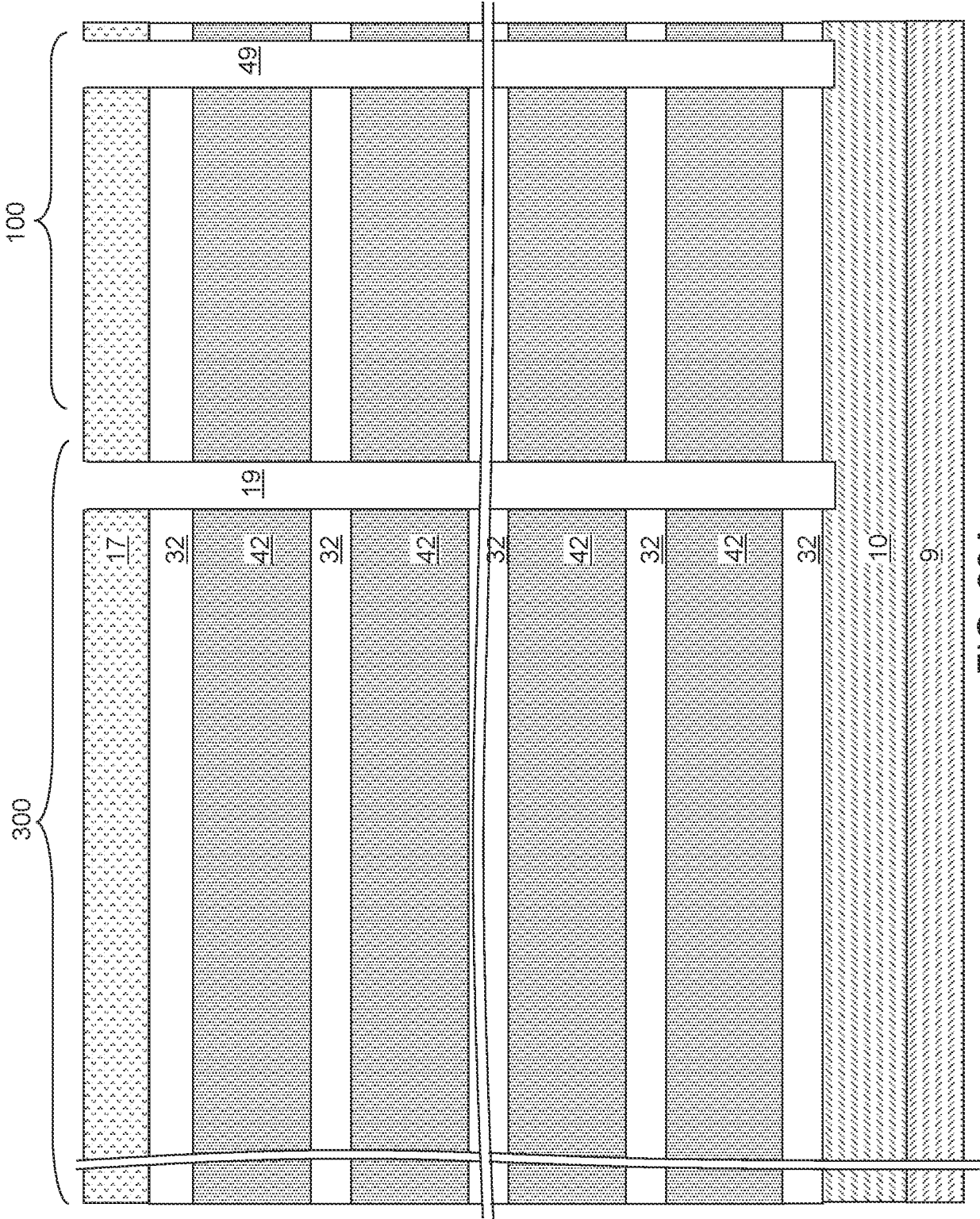


FIG. 29A

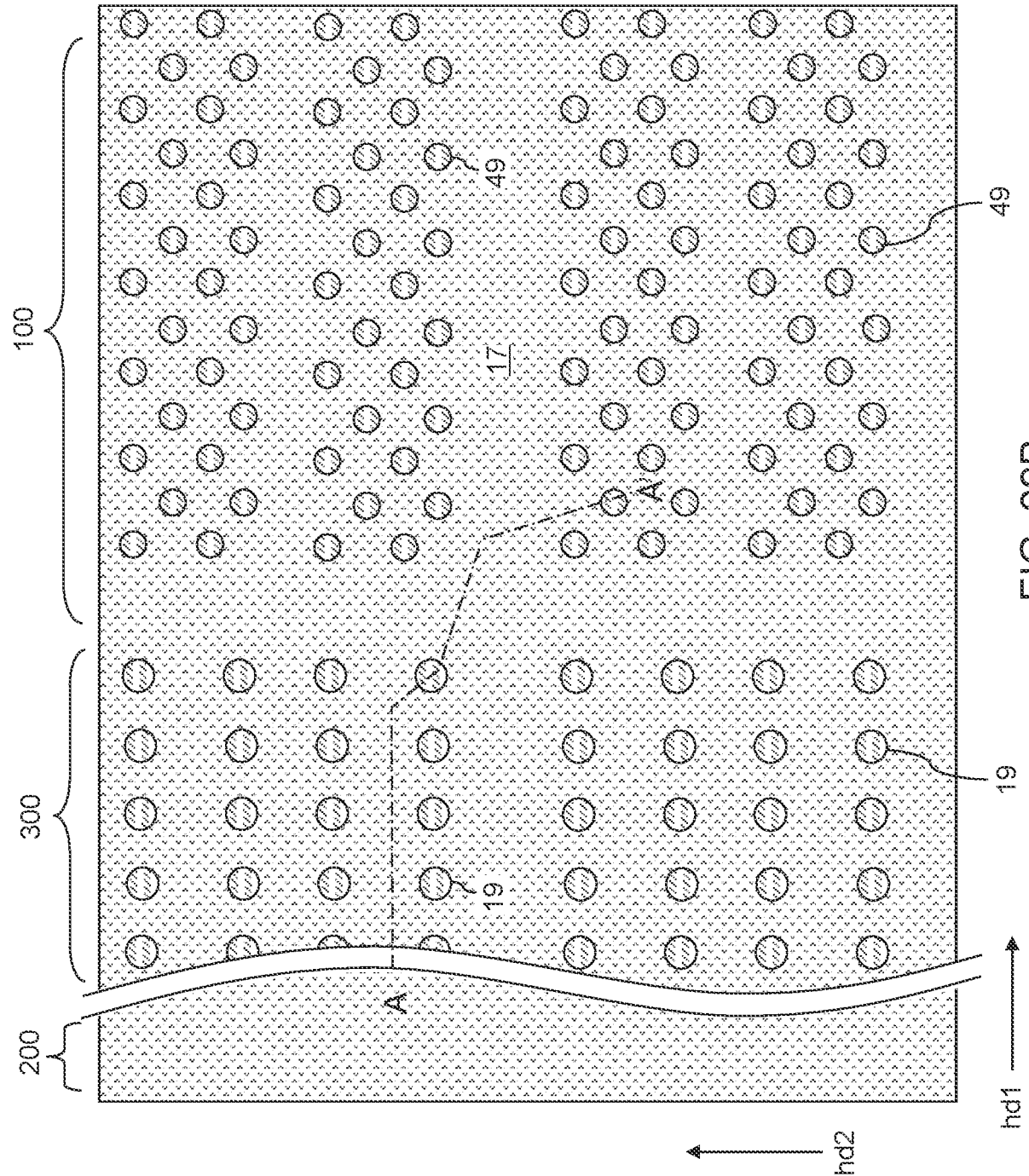


FIG. 29B

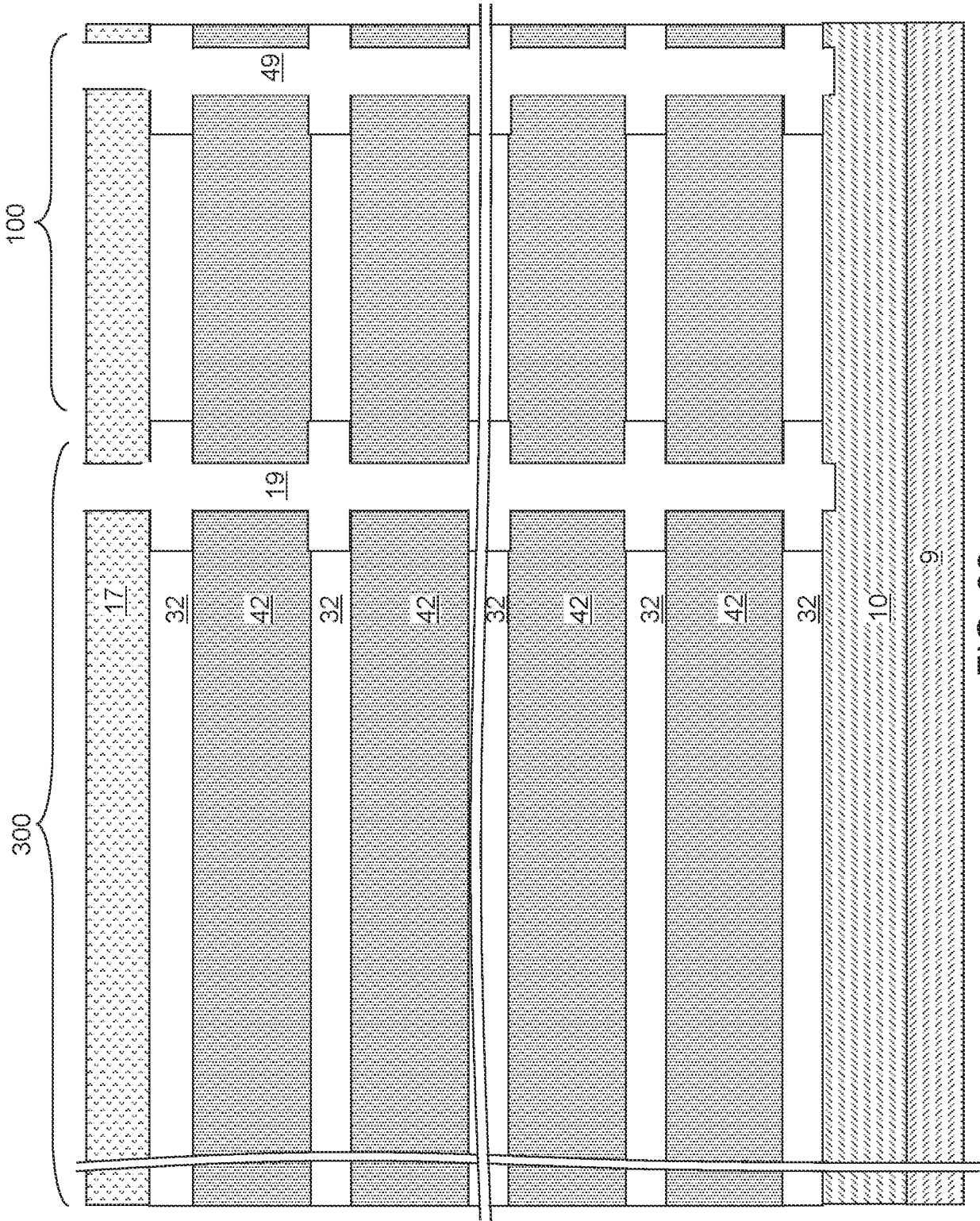


FIG. 30

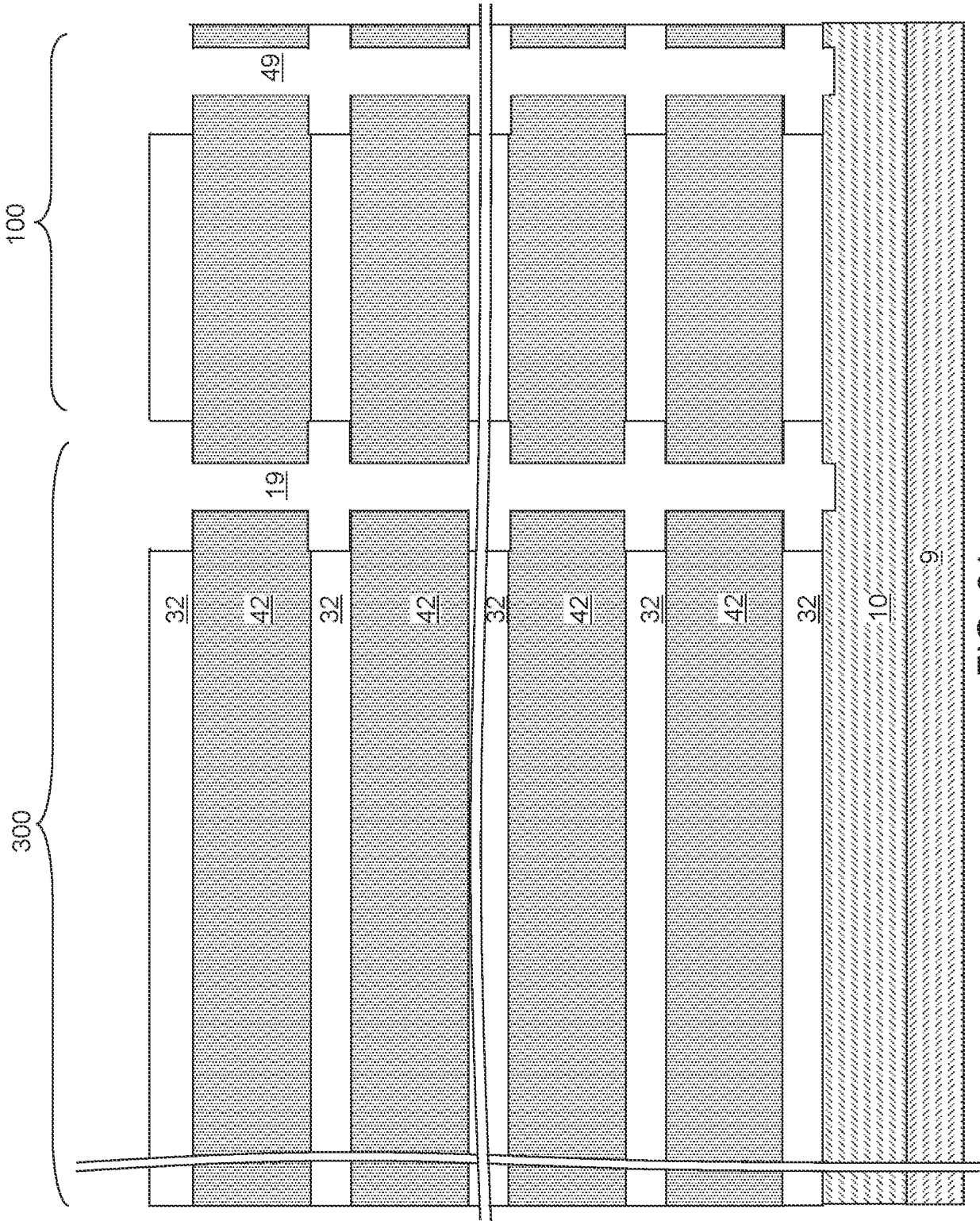


FIG. 31

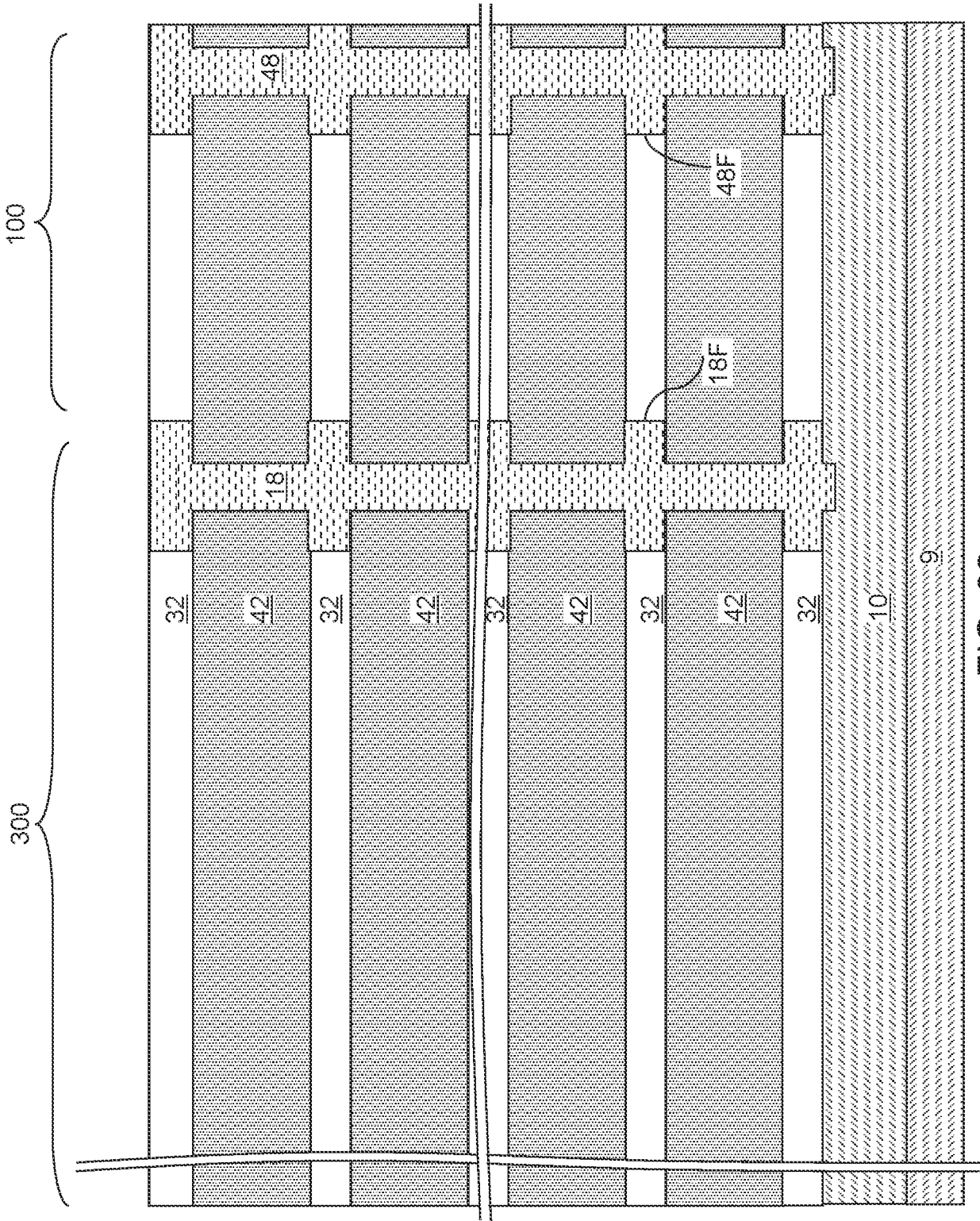
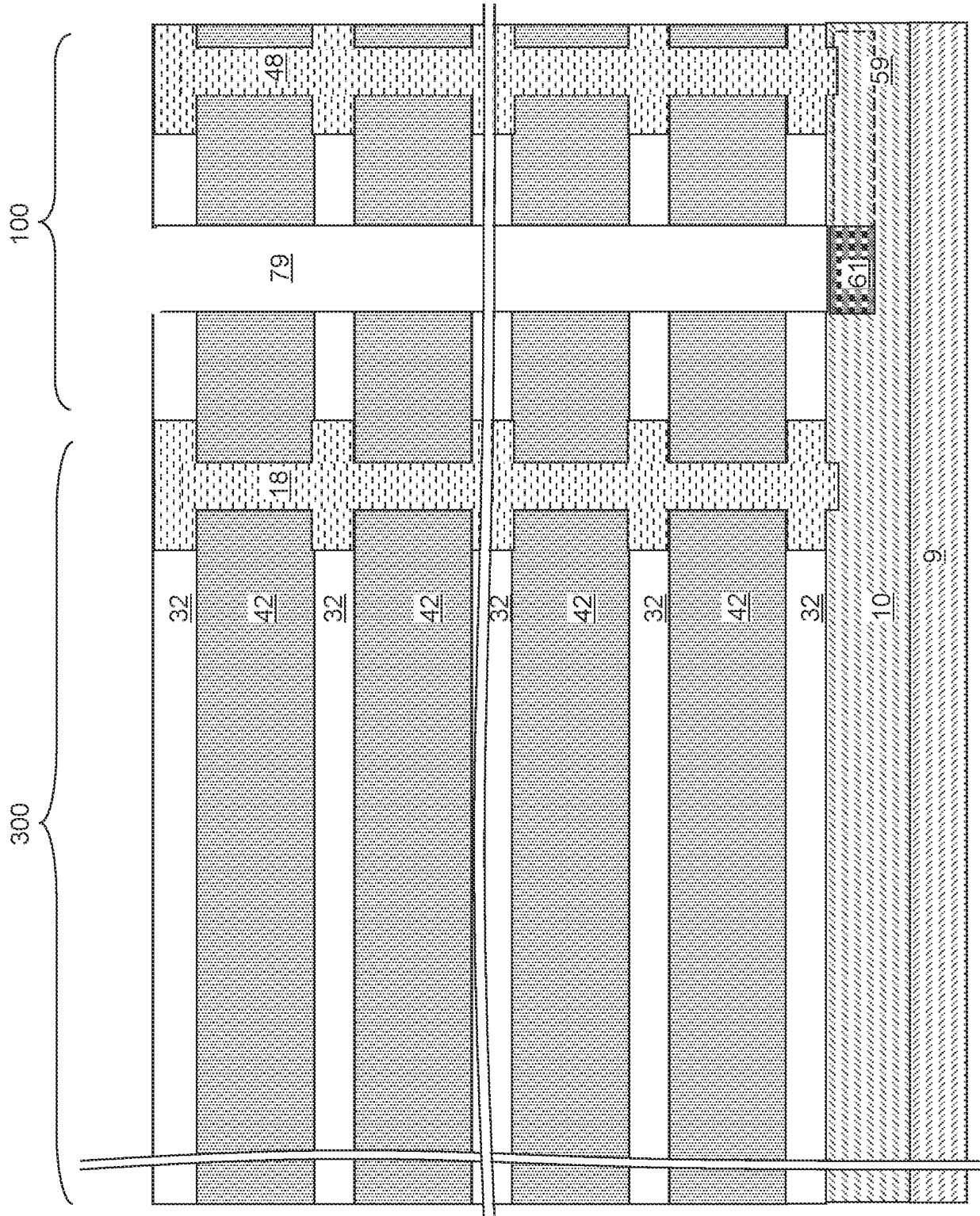


FIG. 32



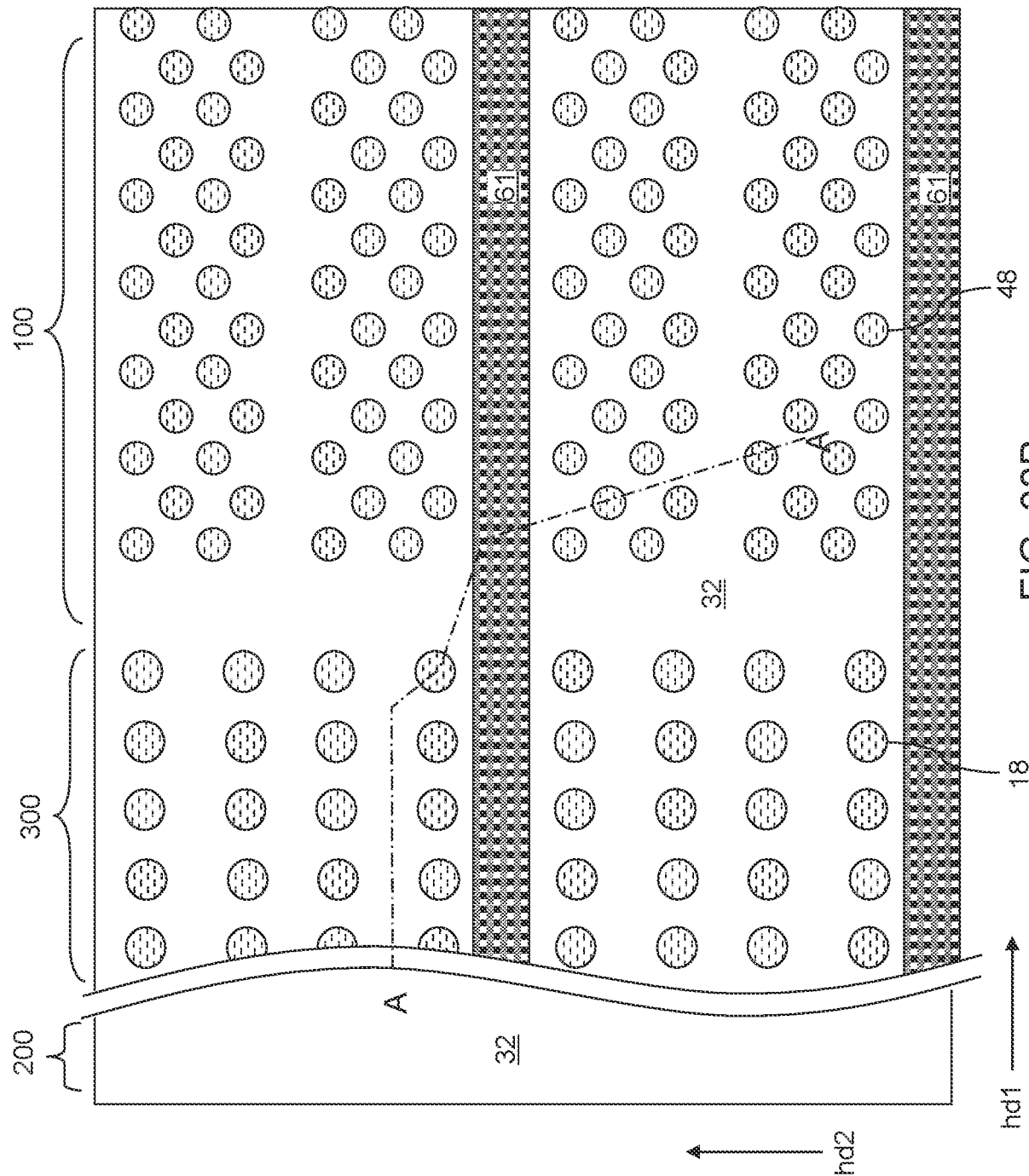


FIG. 33B

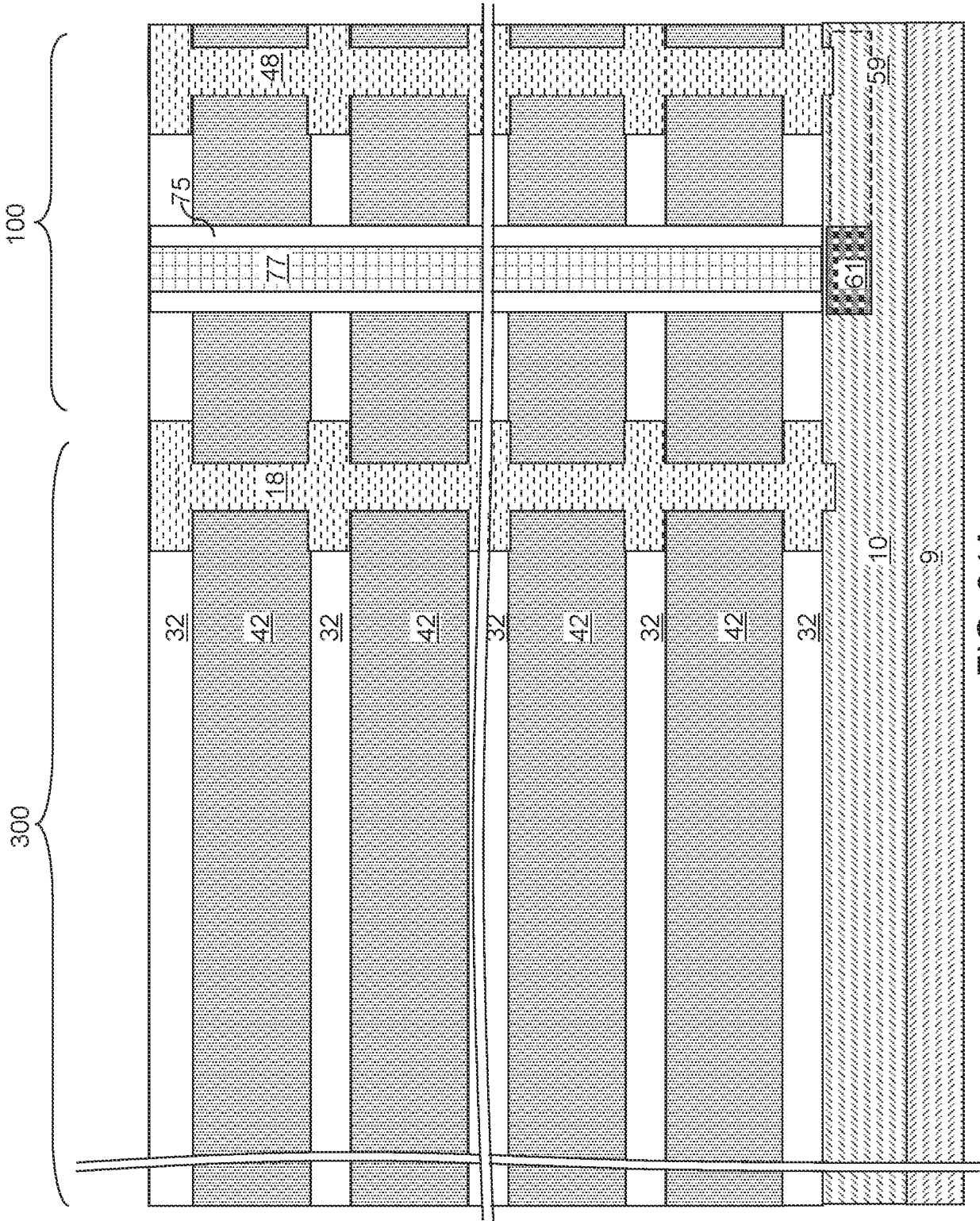
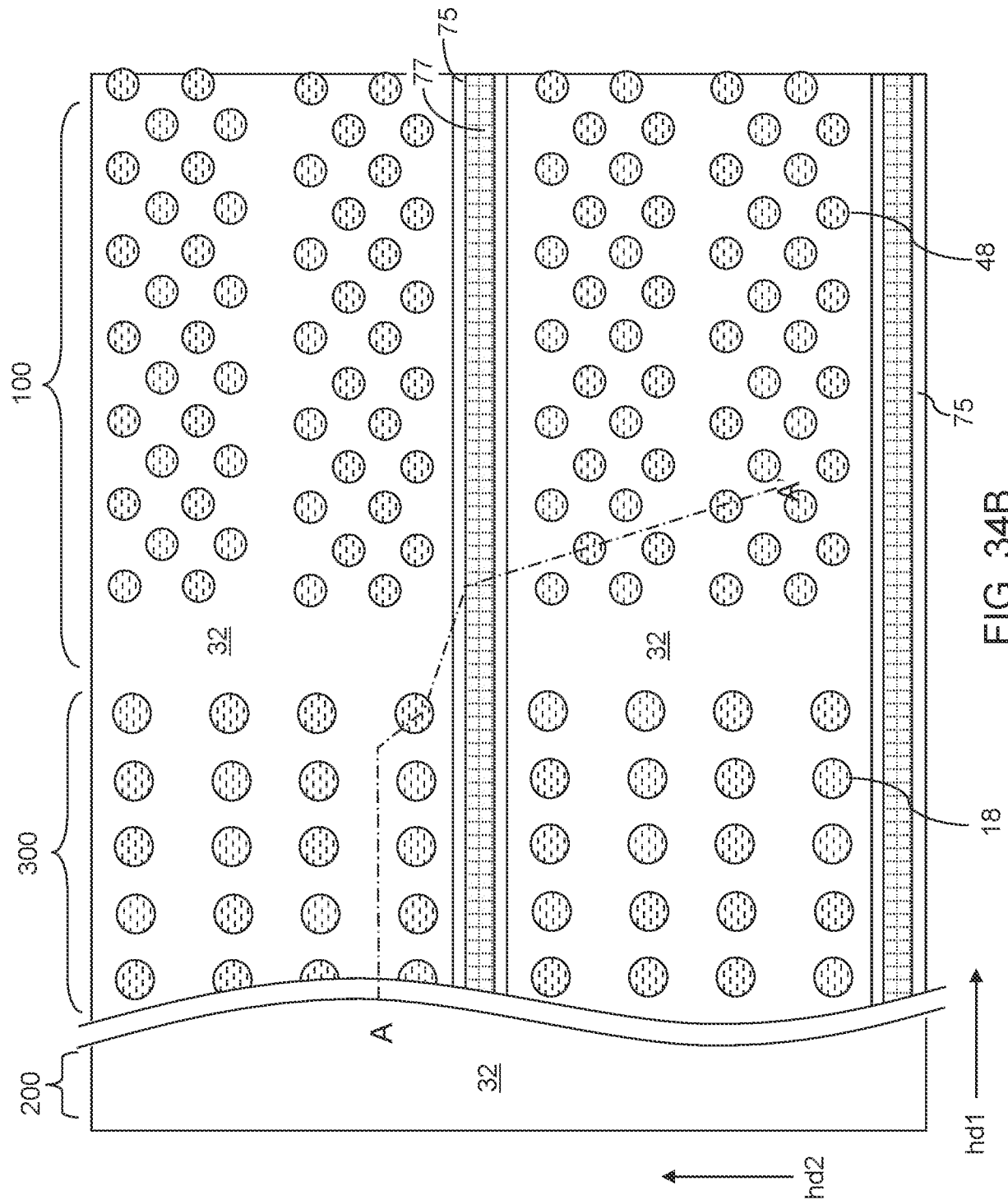
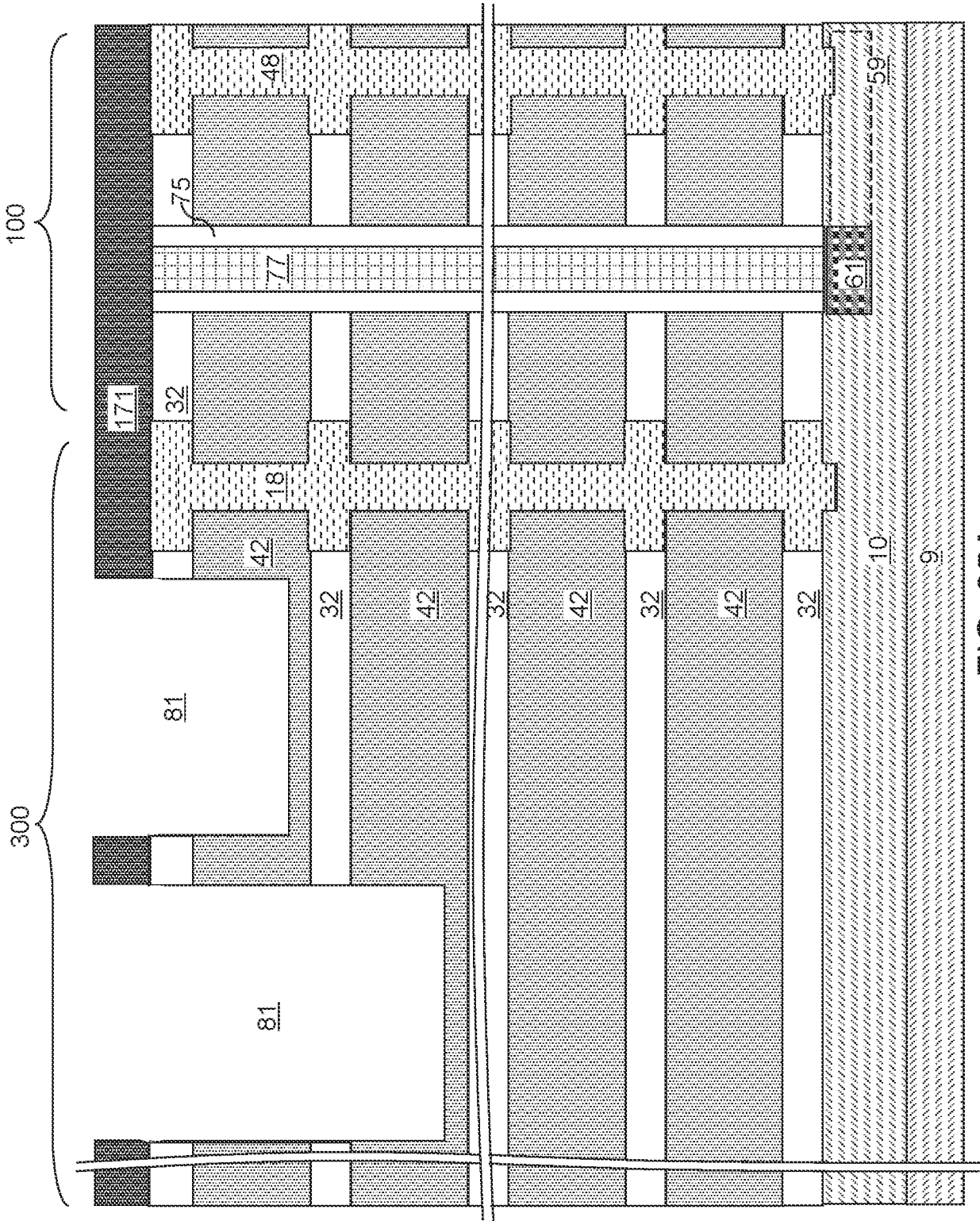


FIG. 34A





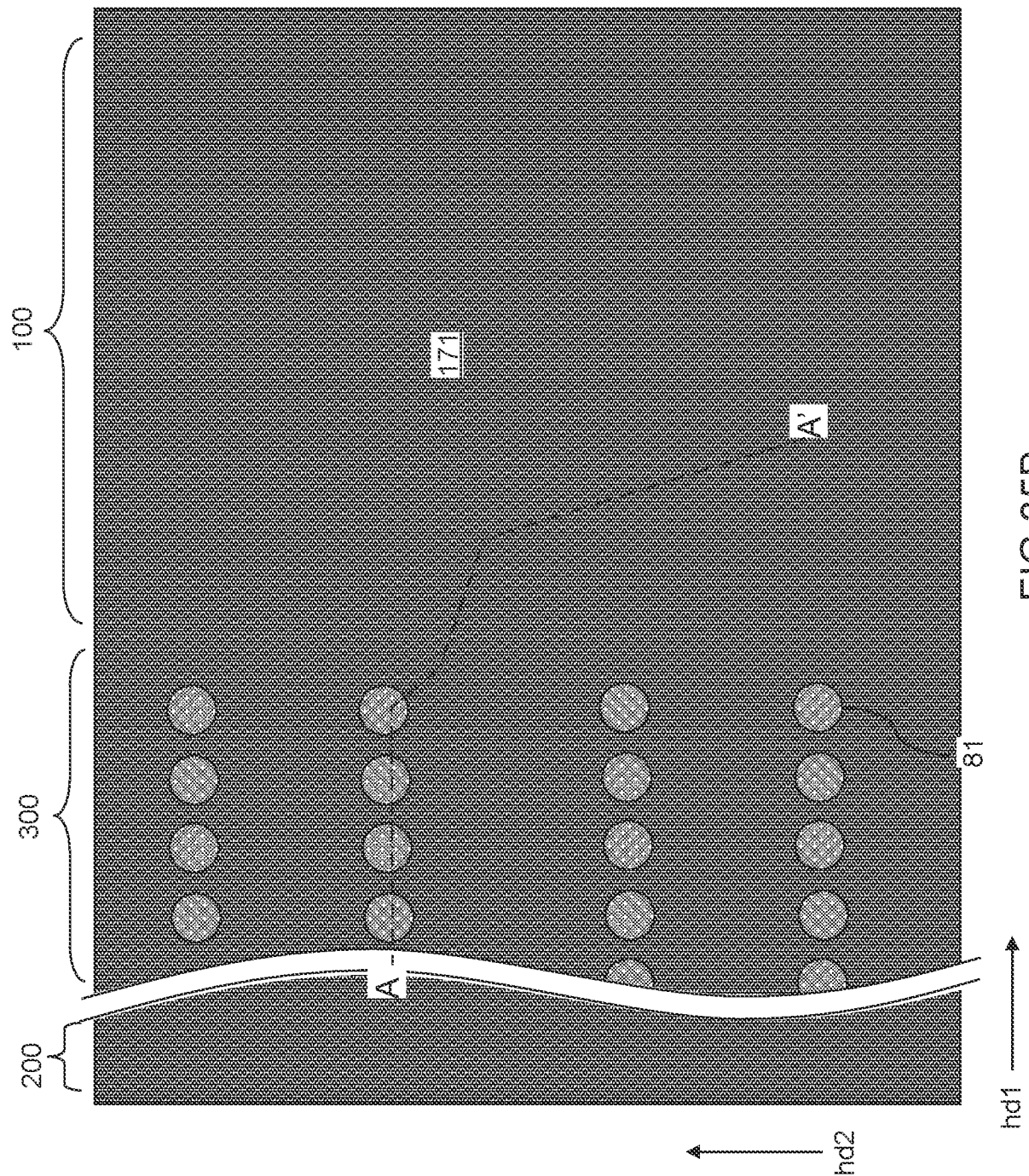


FIG. 35B

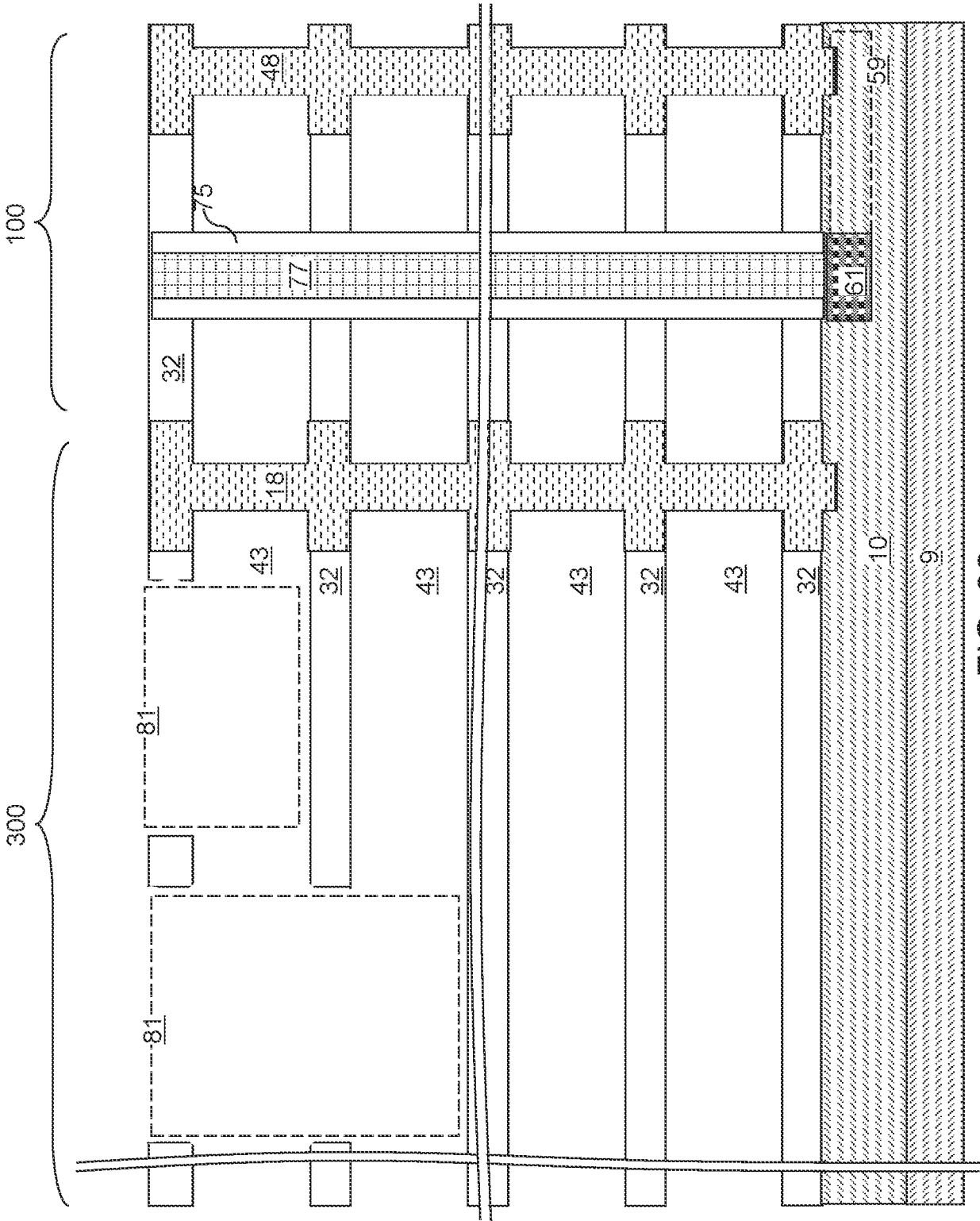


FIG. 36

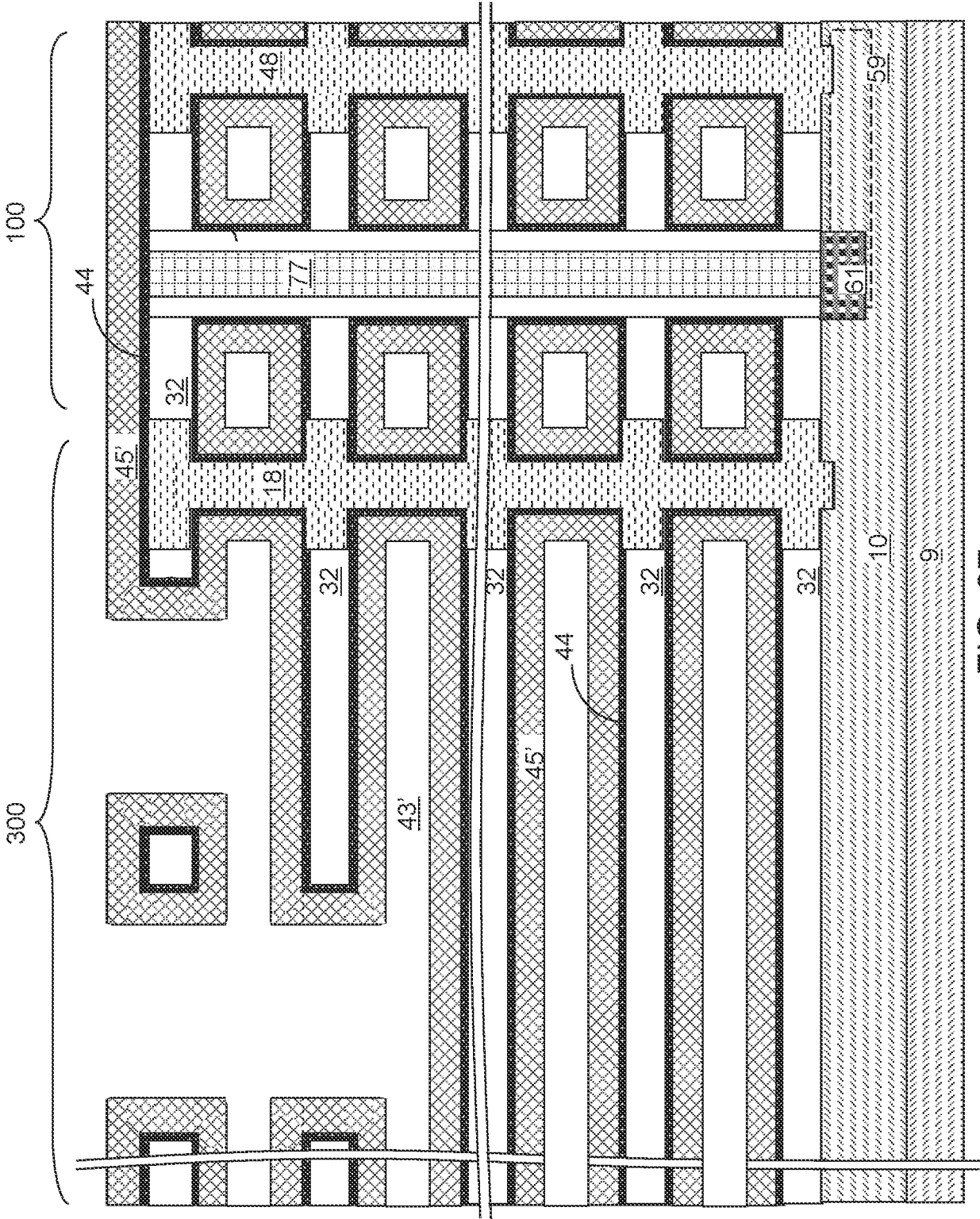
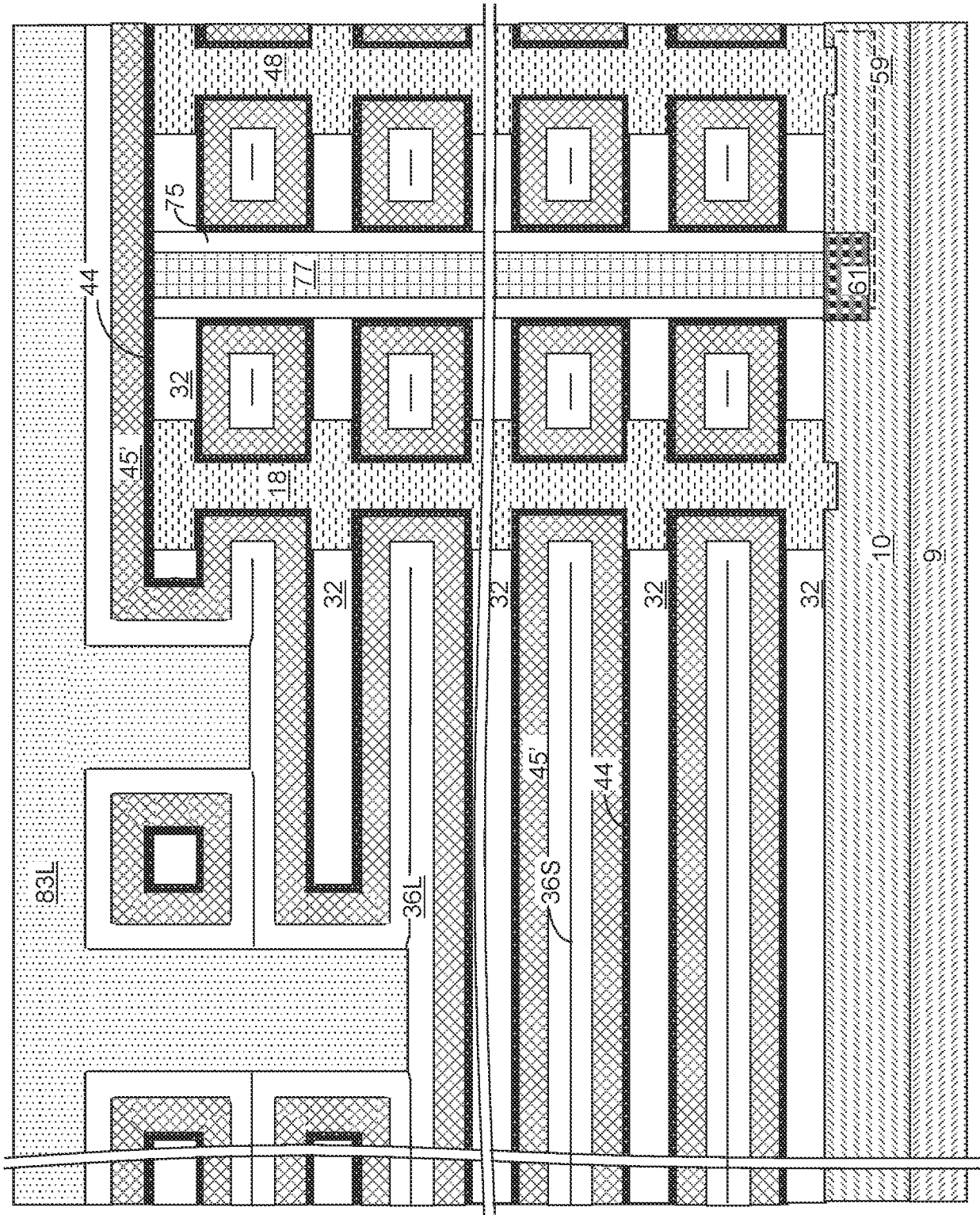


FIG. 37



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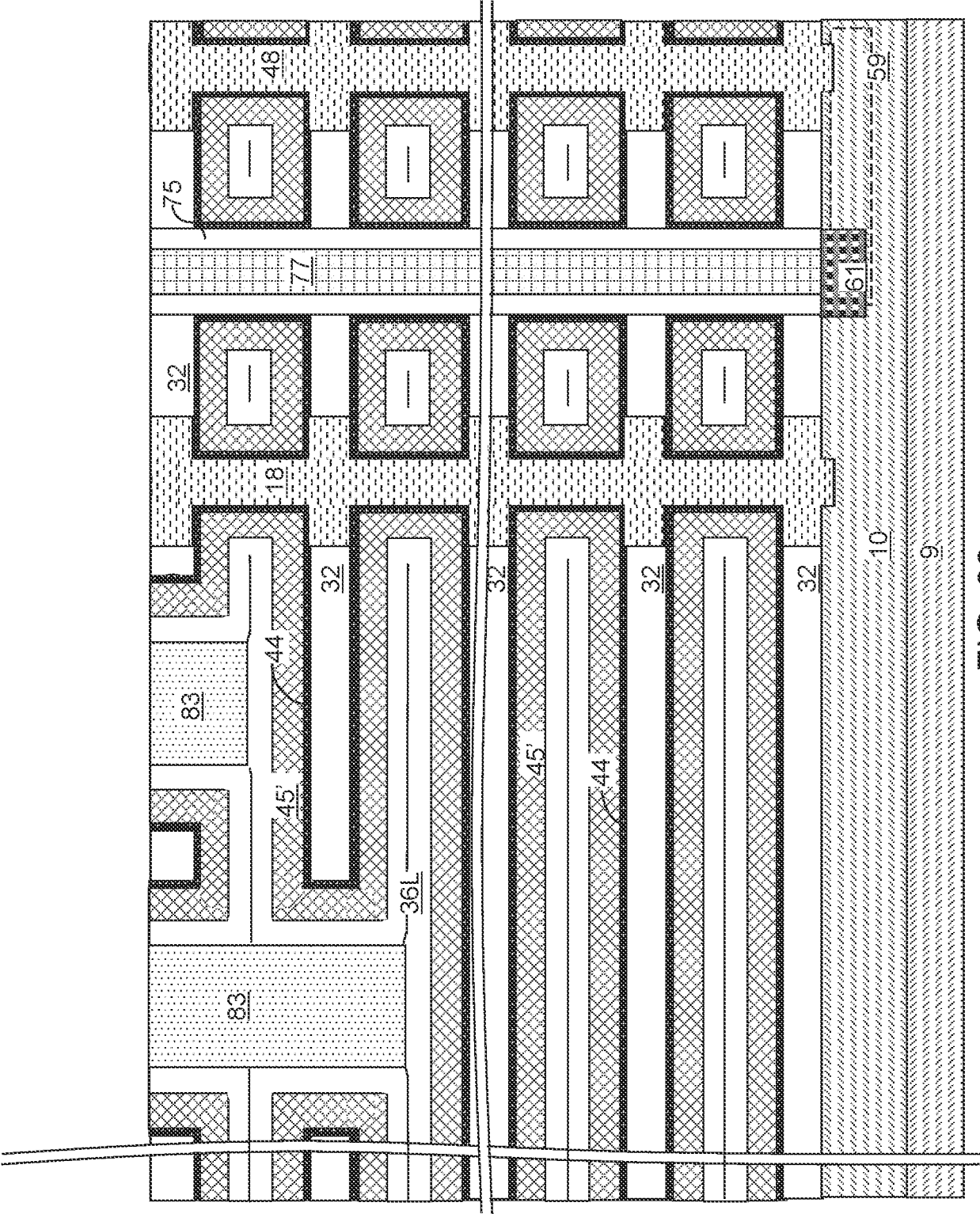


FIG. 39

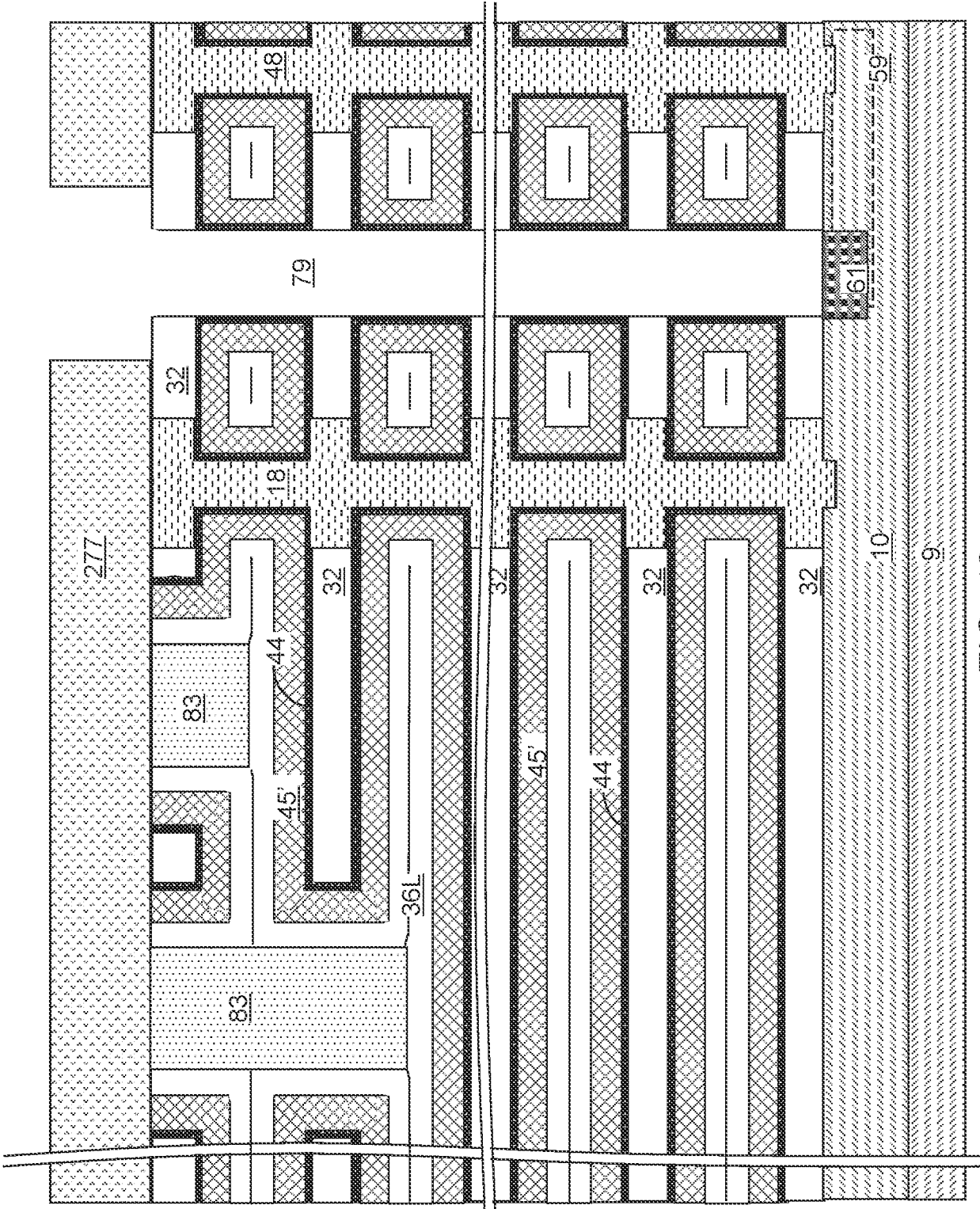


FIG. 40

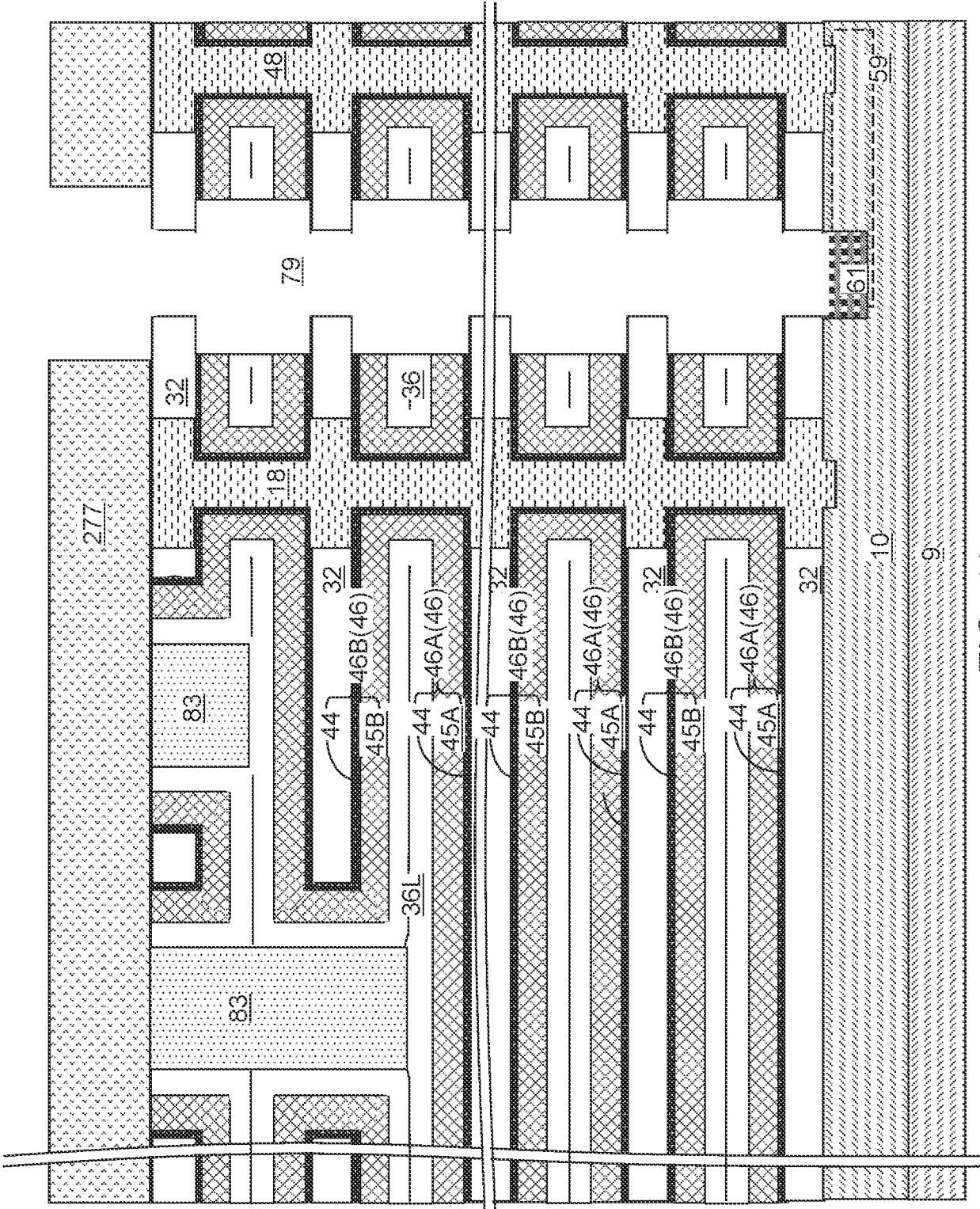


FIG. 41

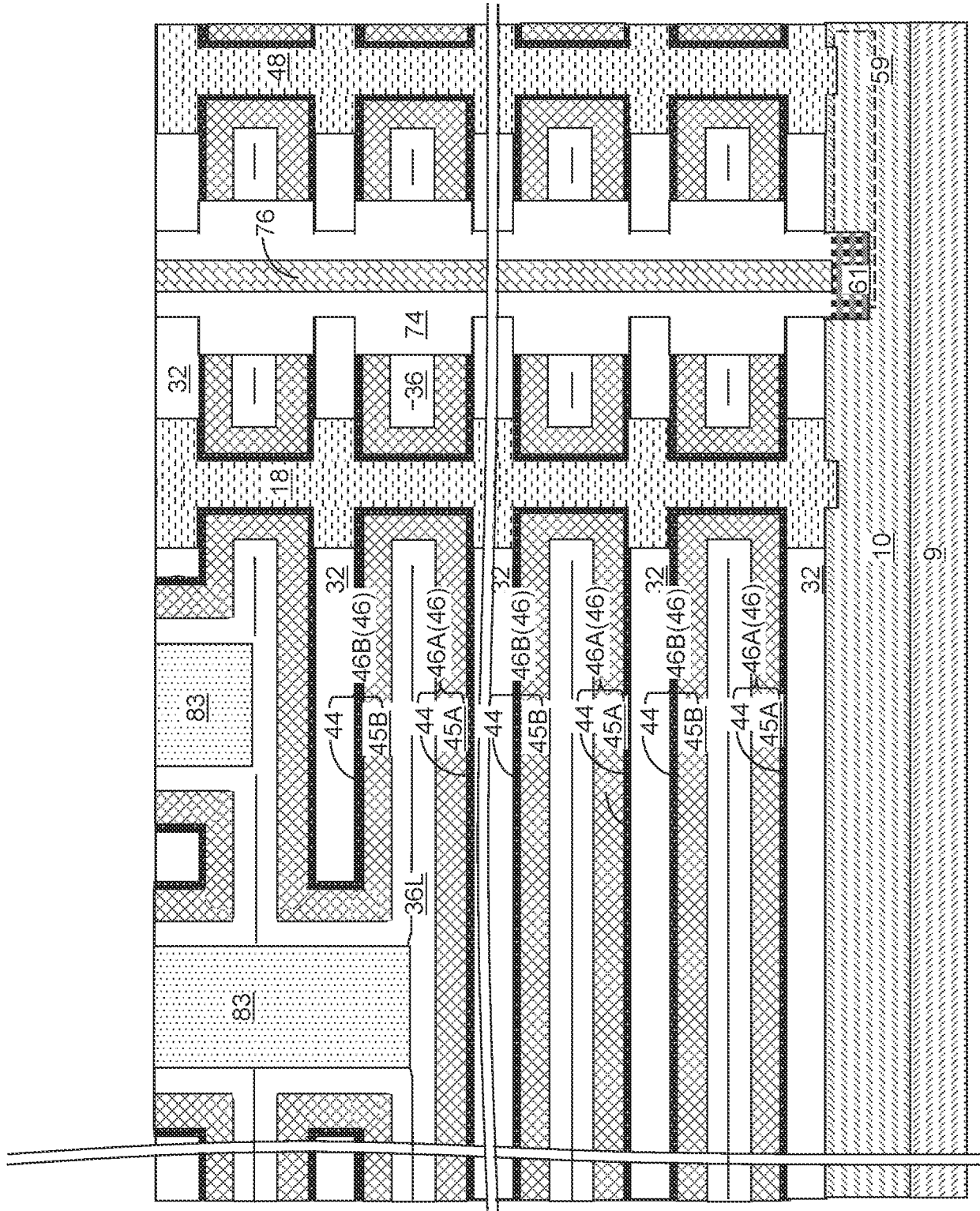
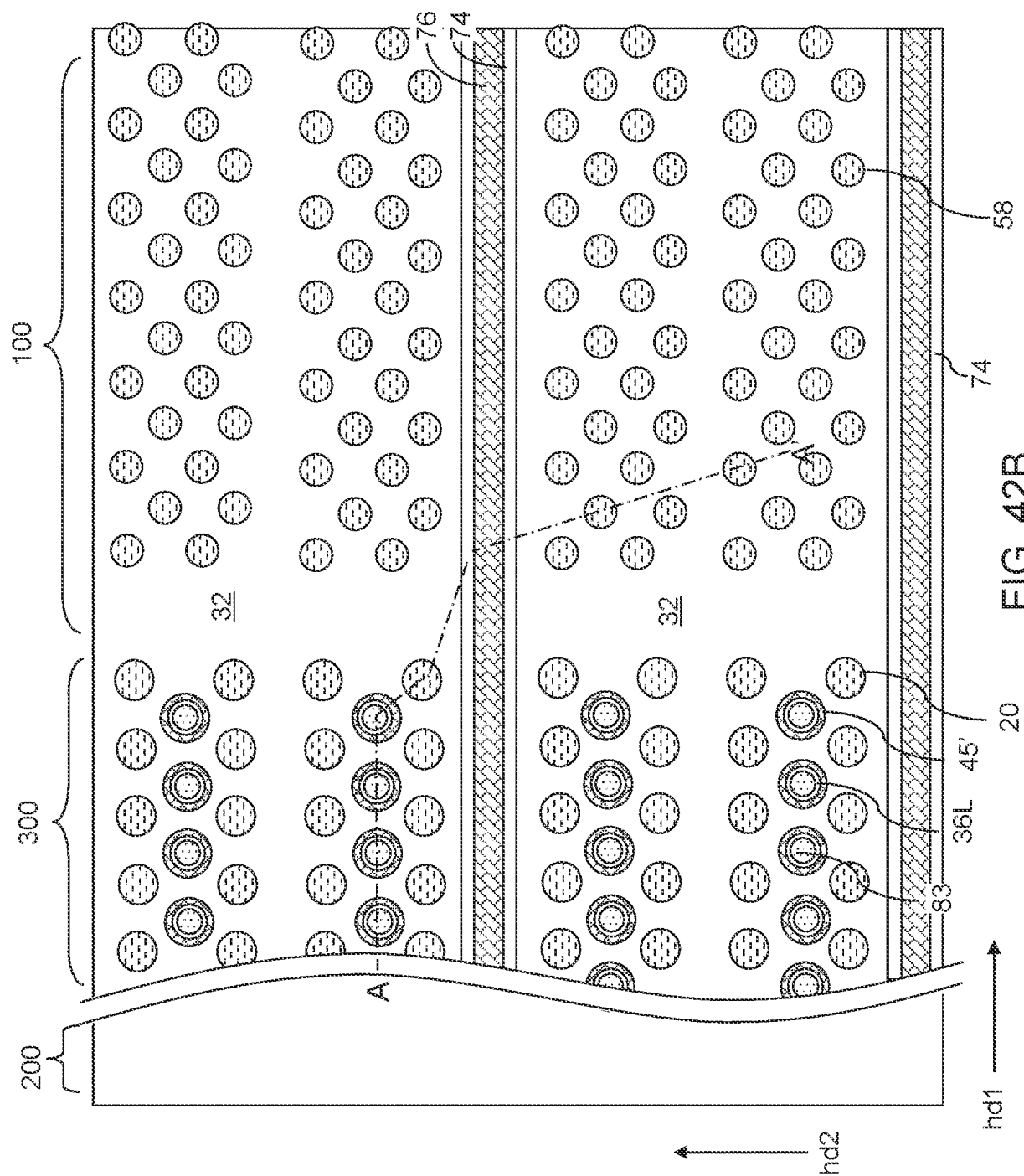


FIG. 42A



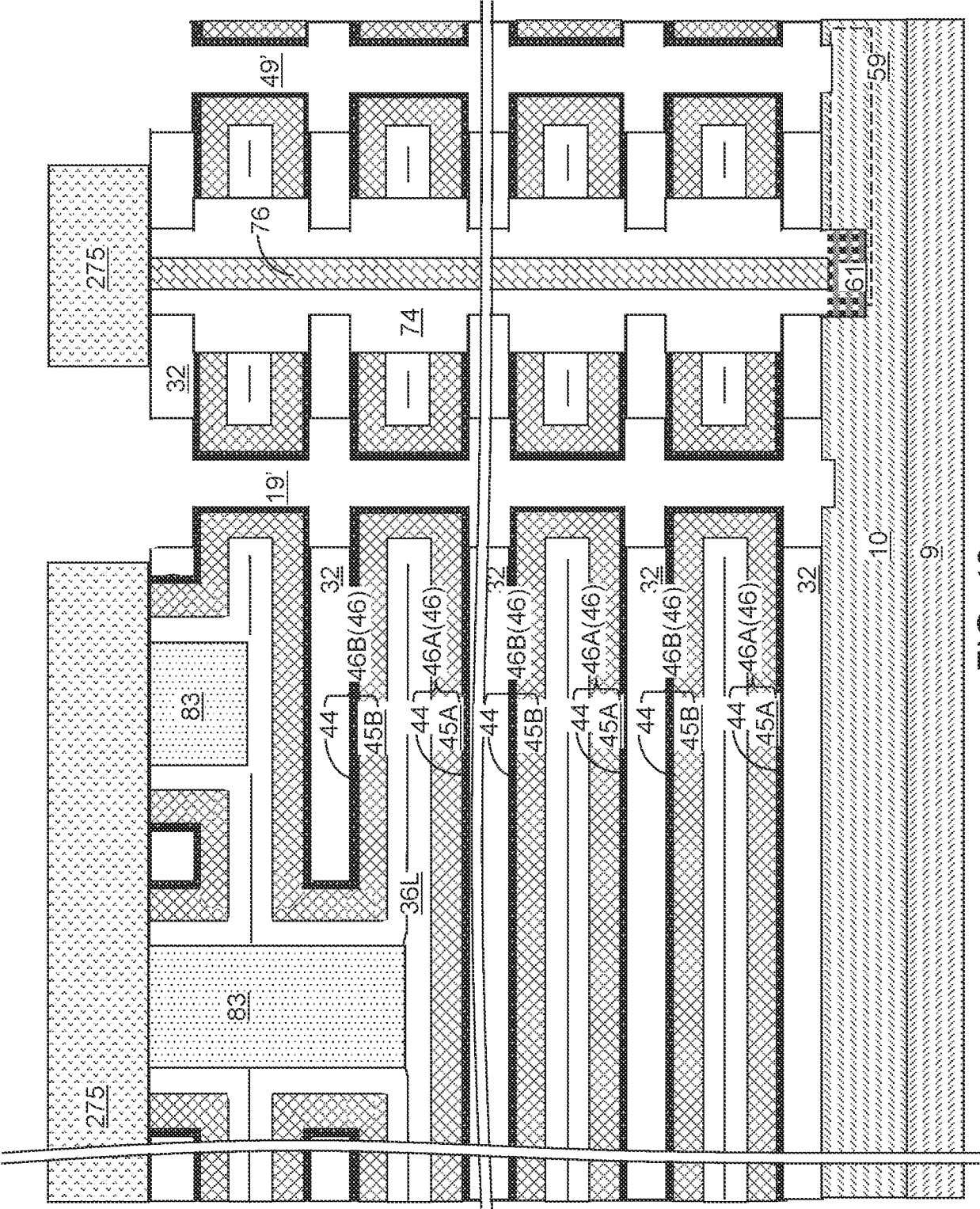


FIG. 43

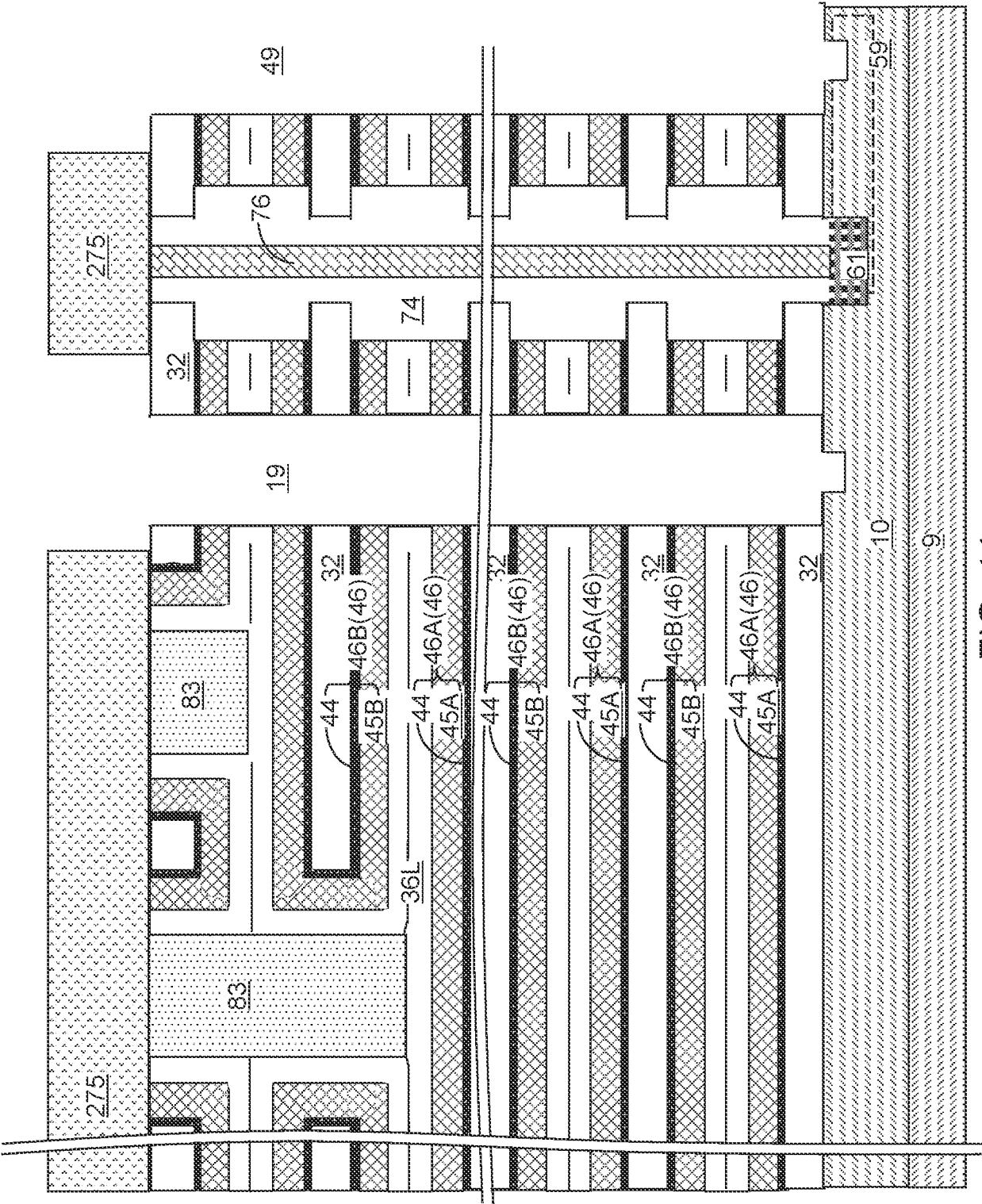
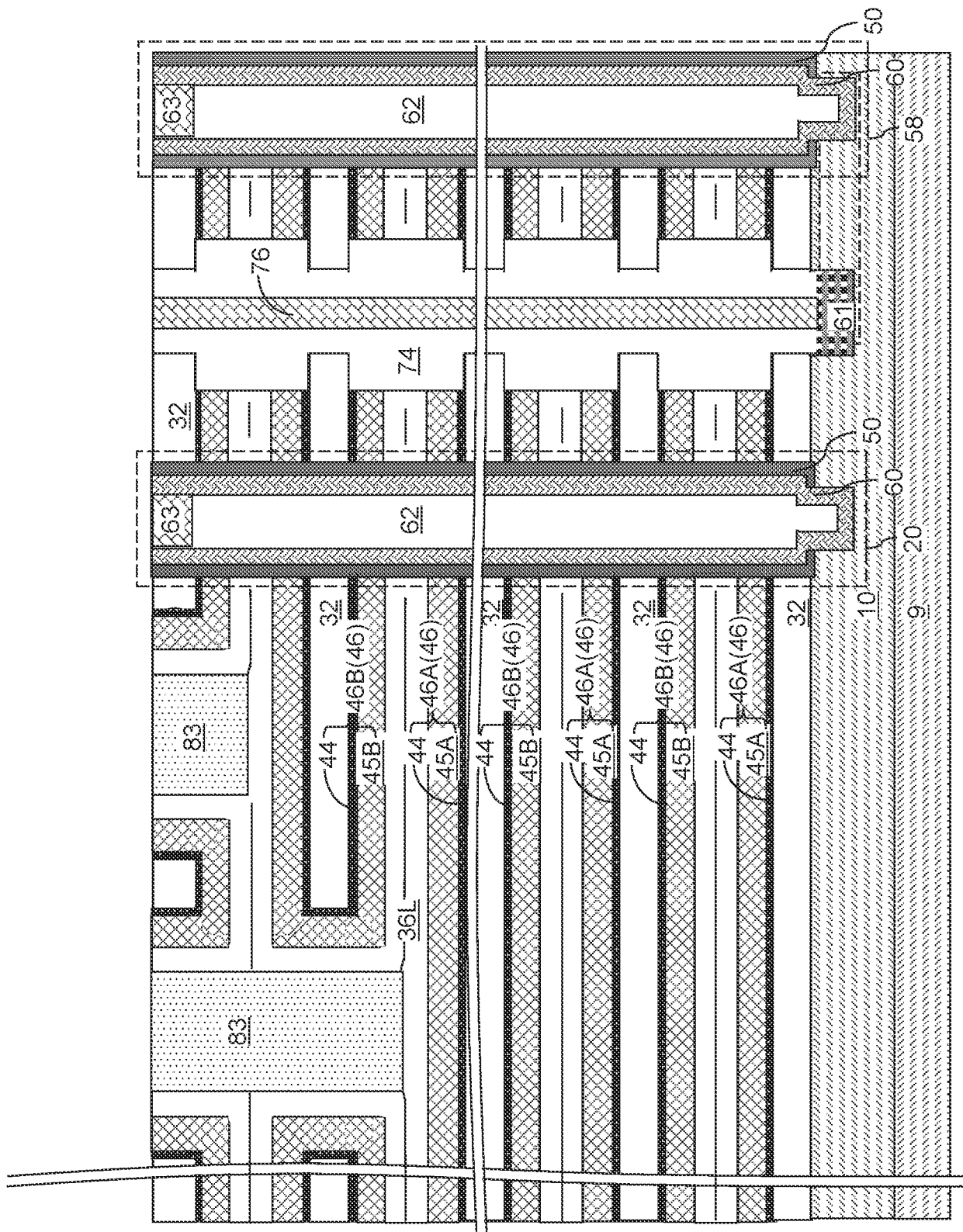


FIG. 44



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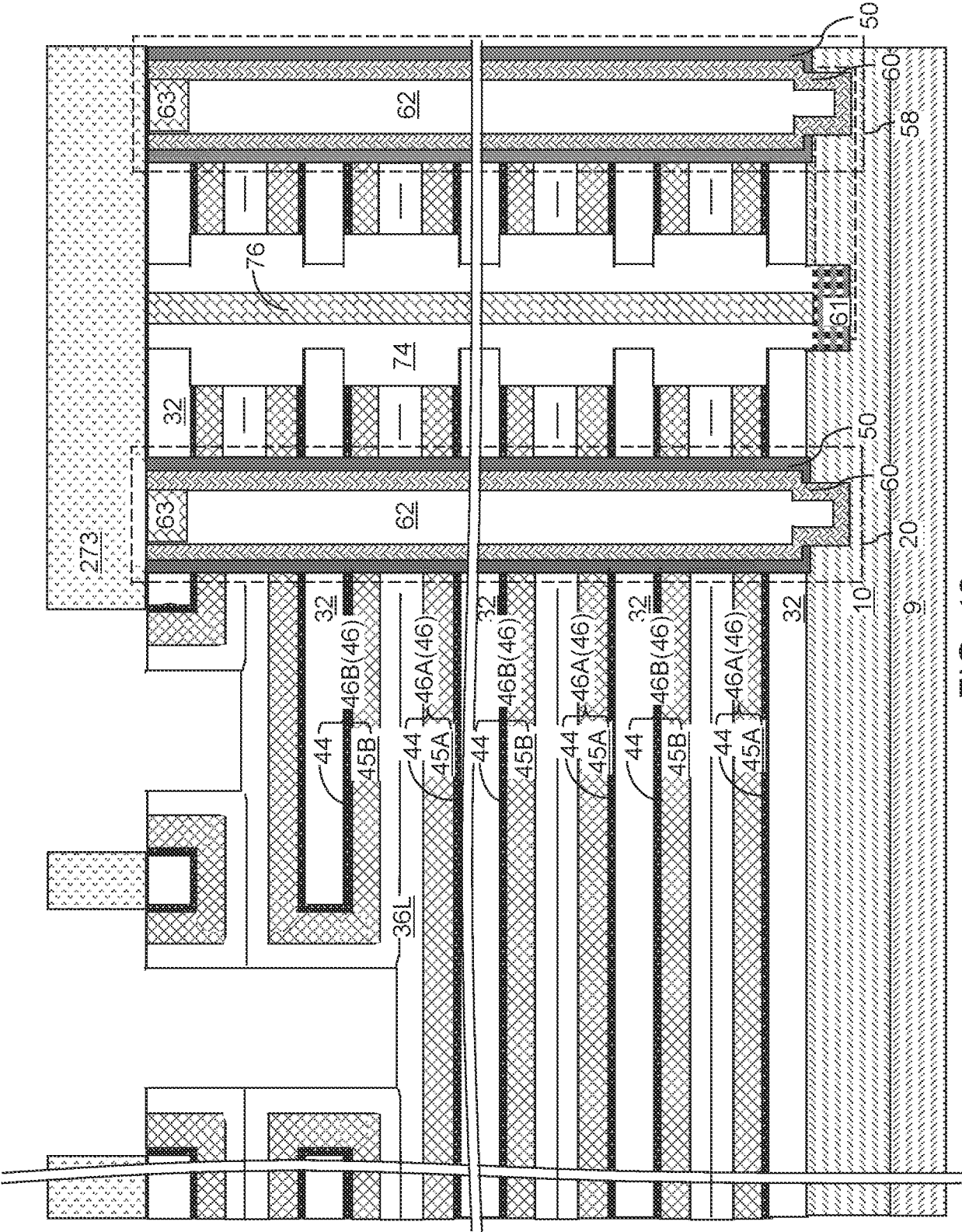


FIG. 46

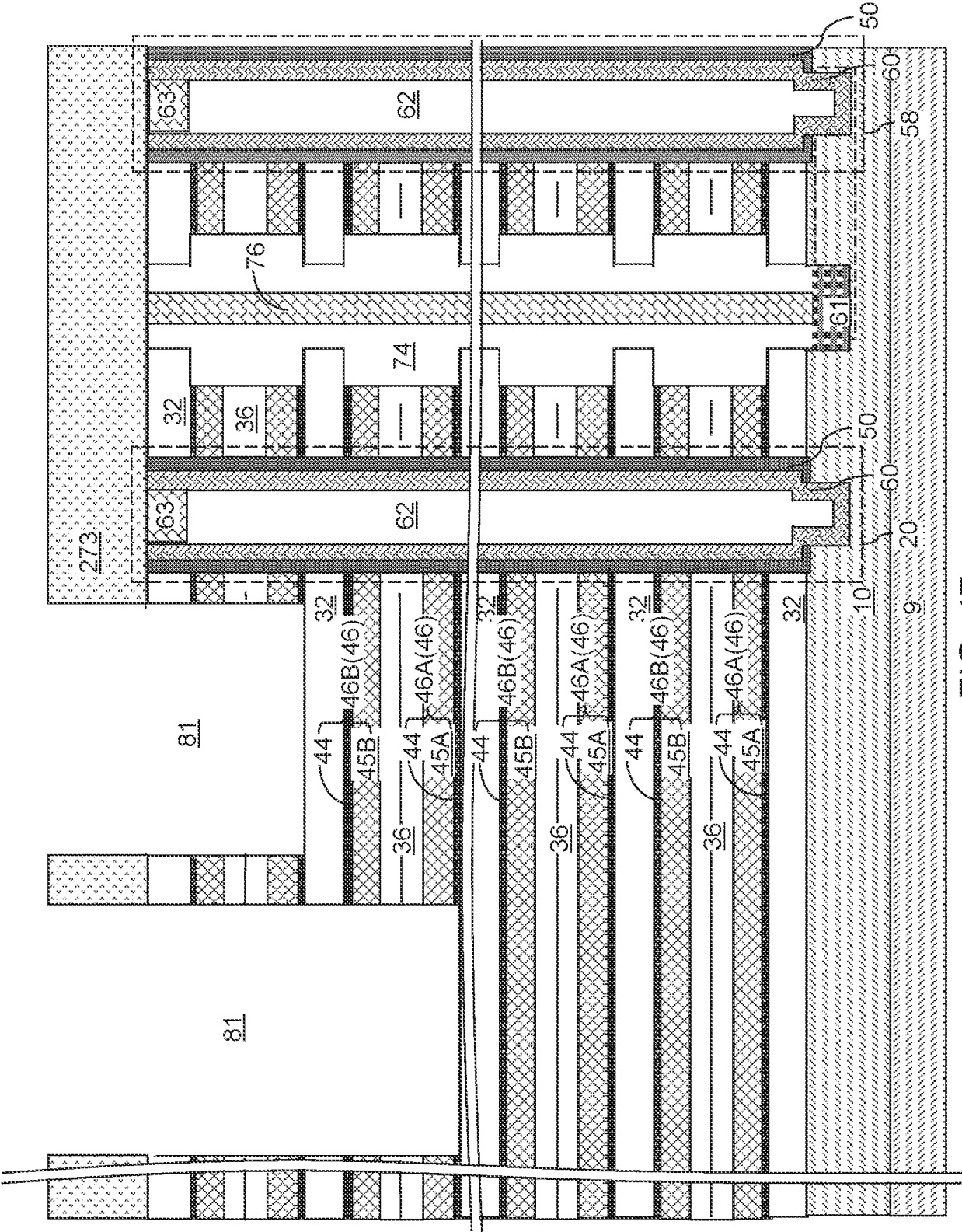


FIG. 47

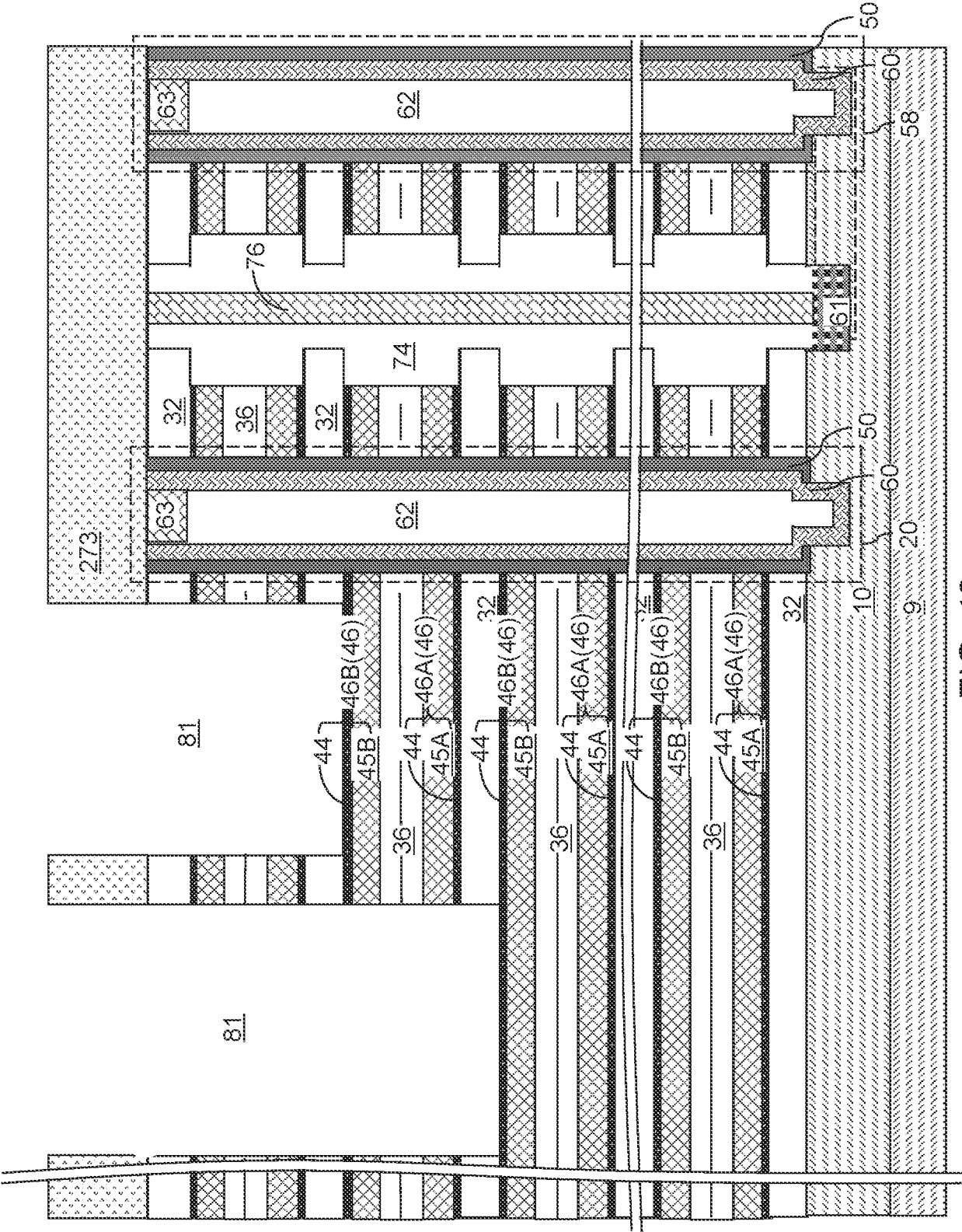


FIG. 48

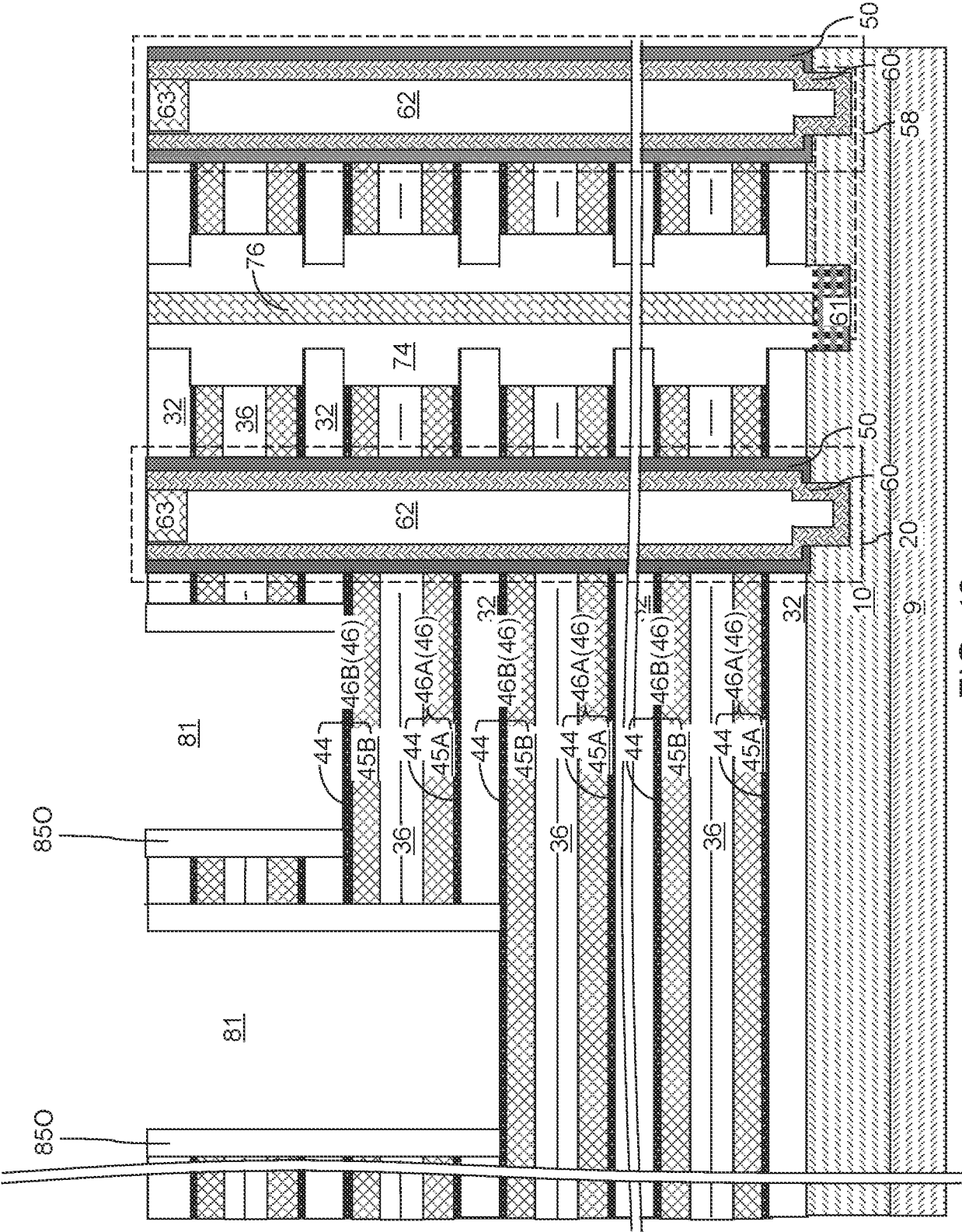


FIG. 49

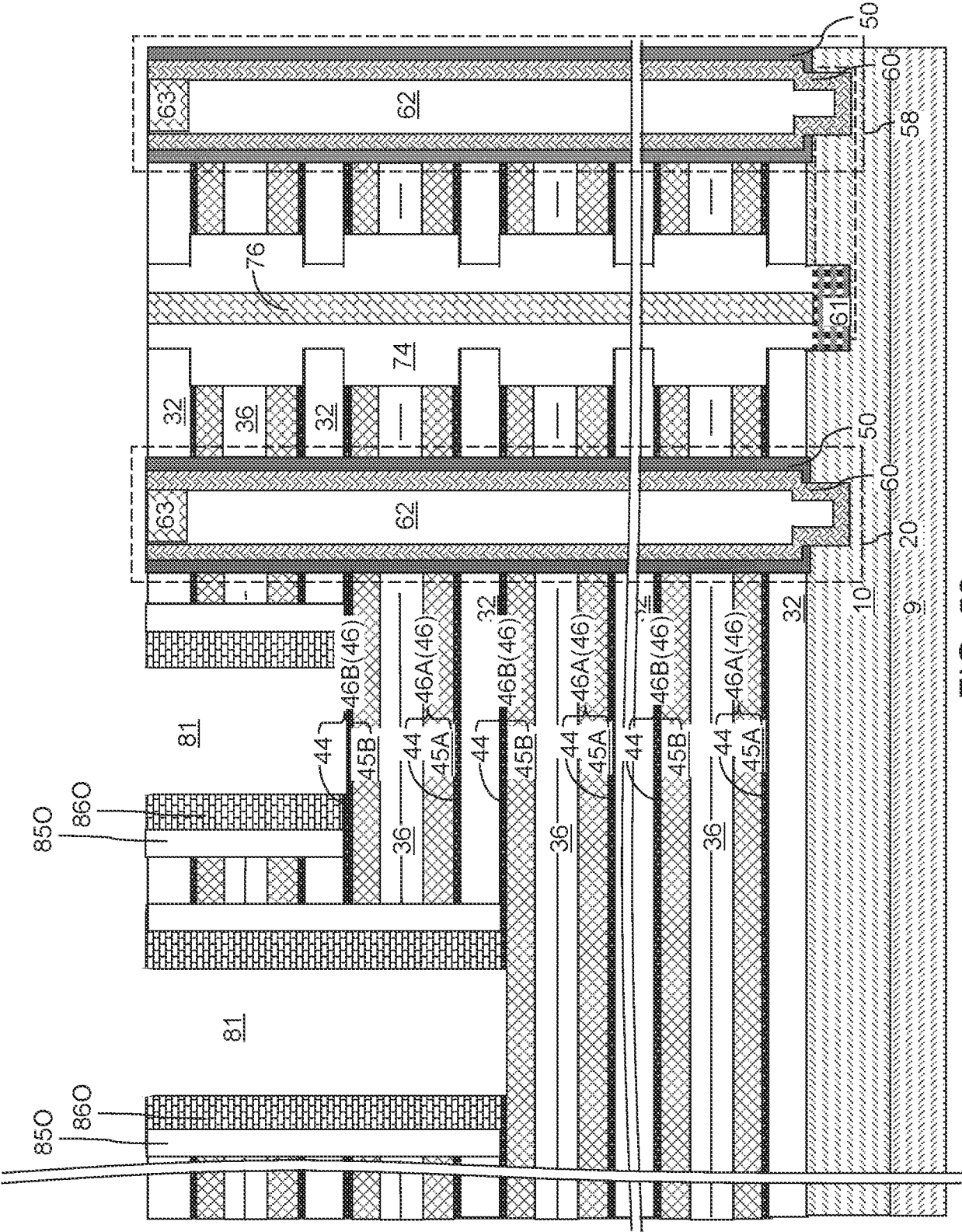
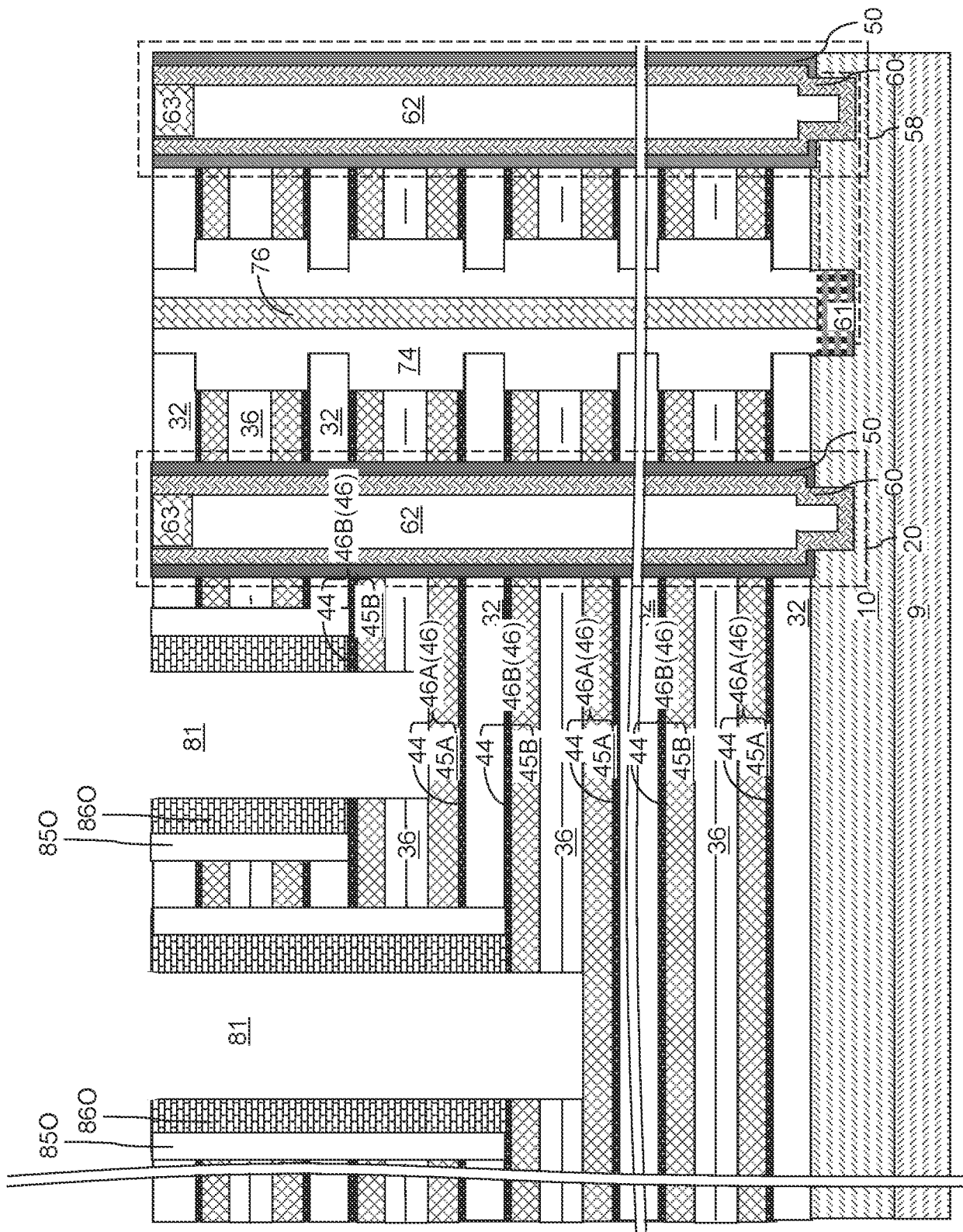


FIG. 50



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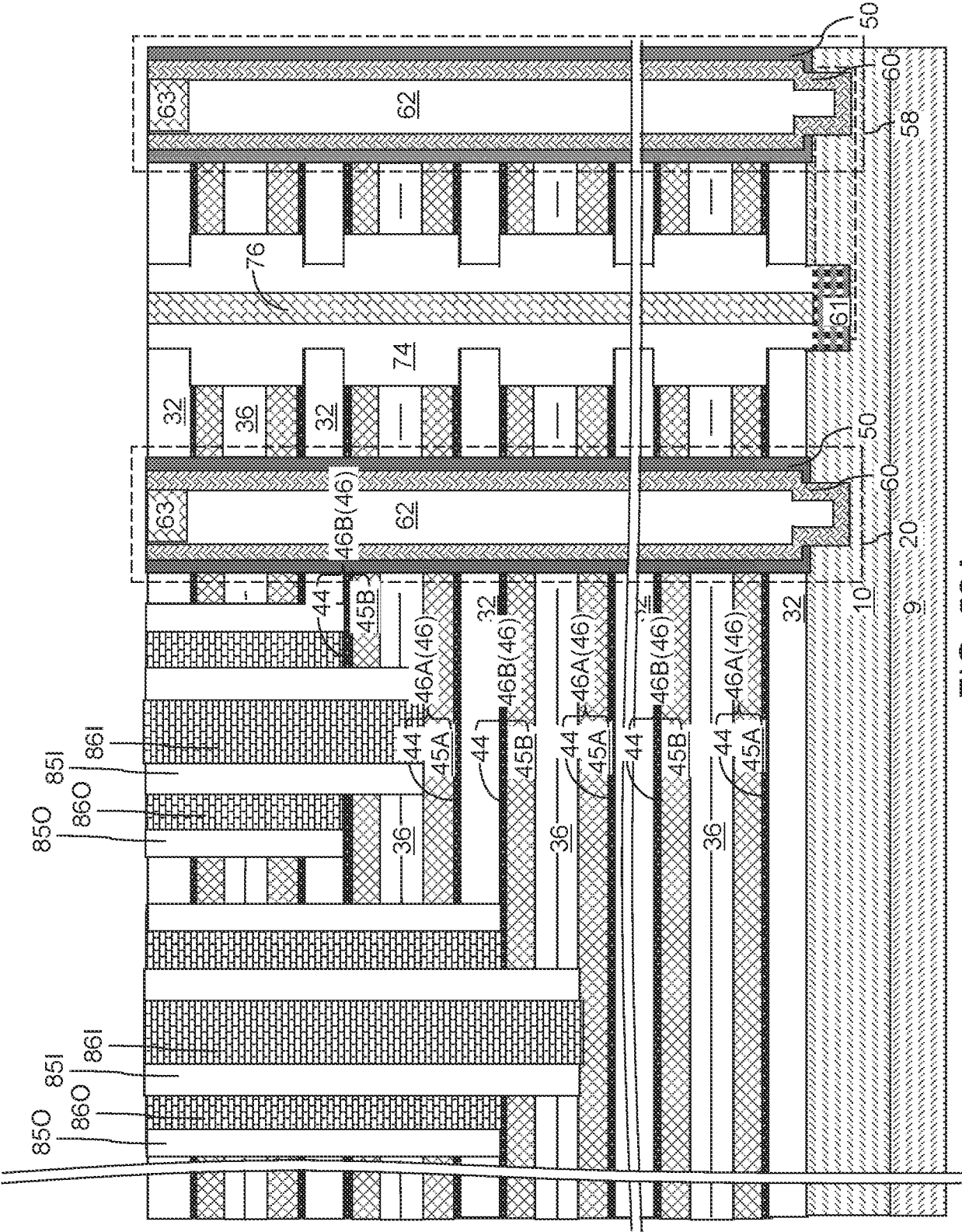
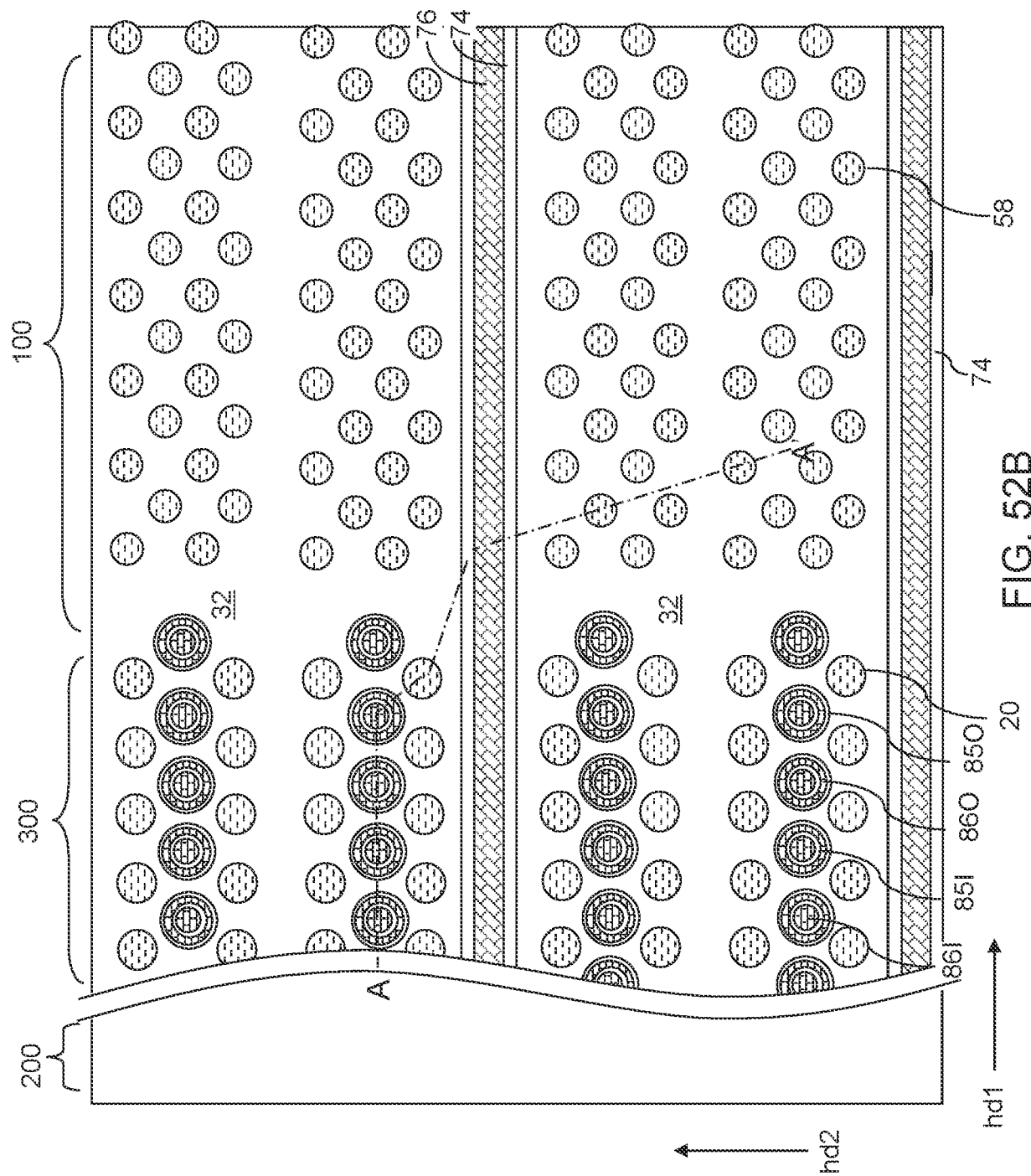
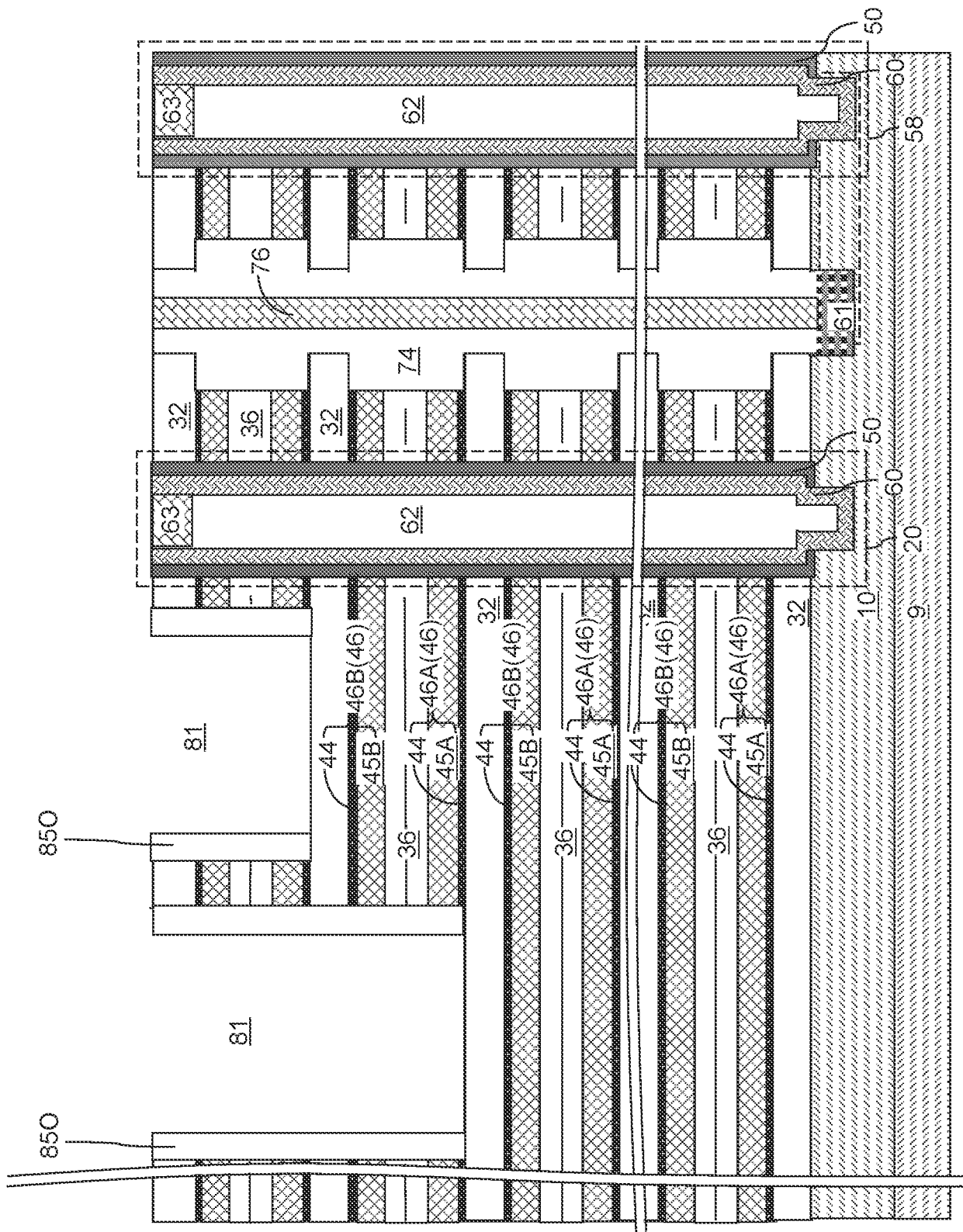
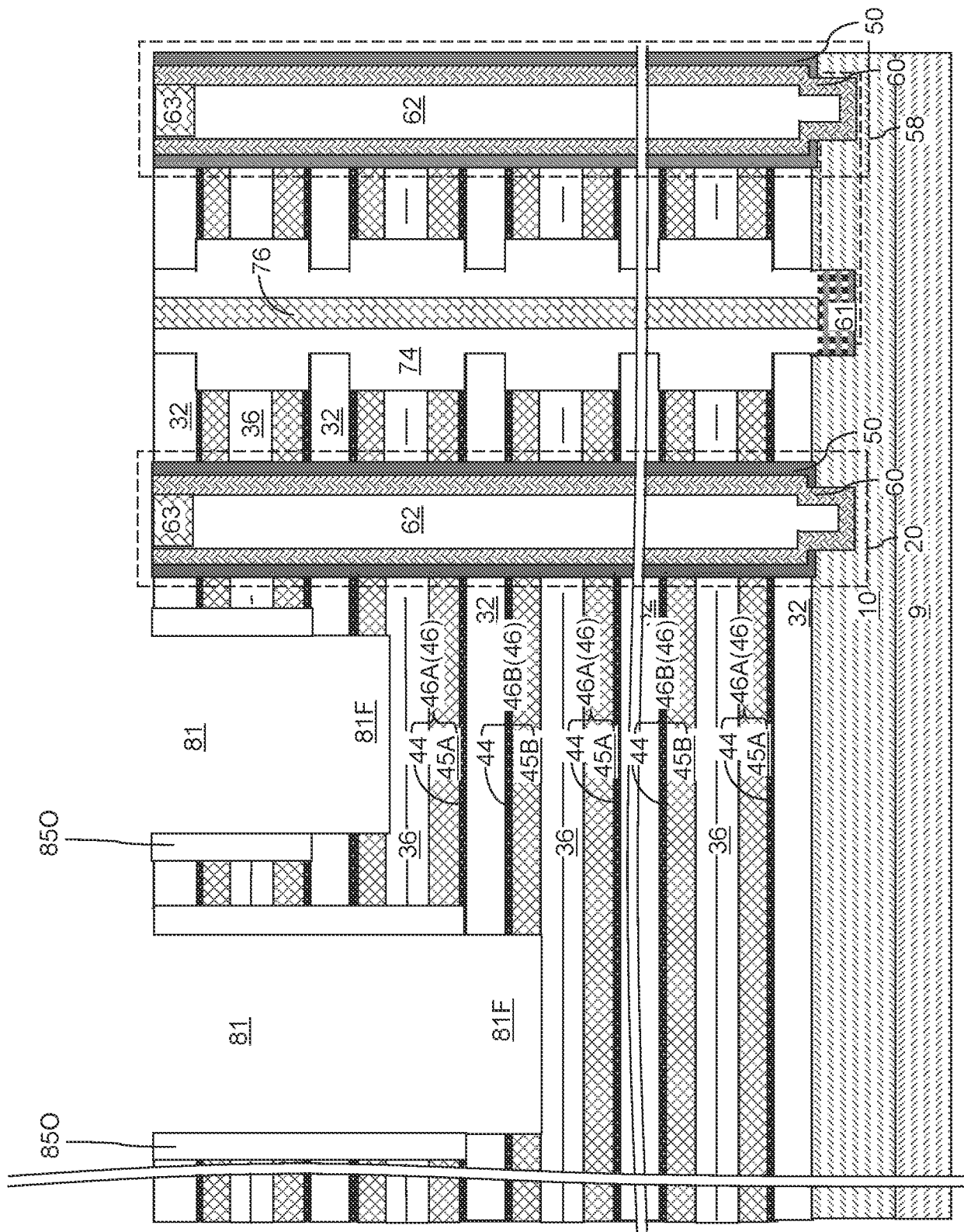
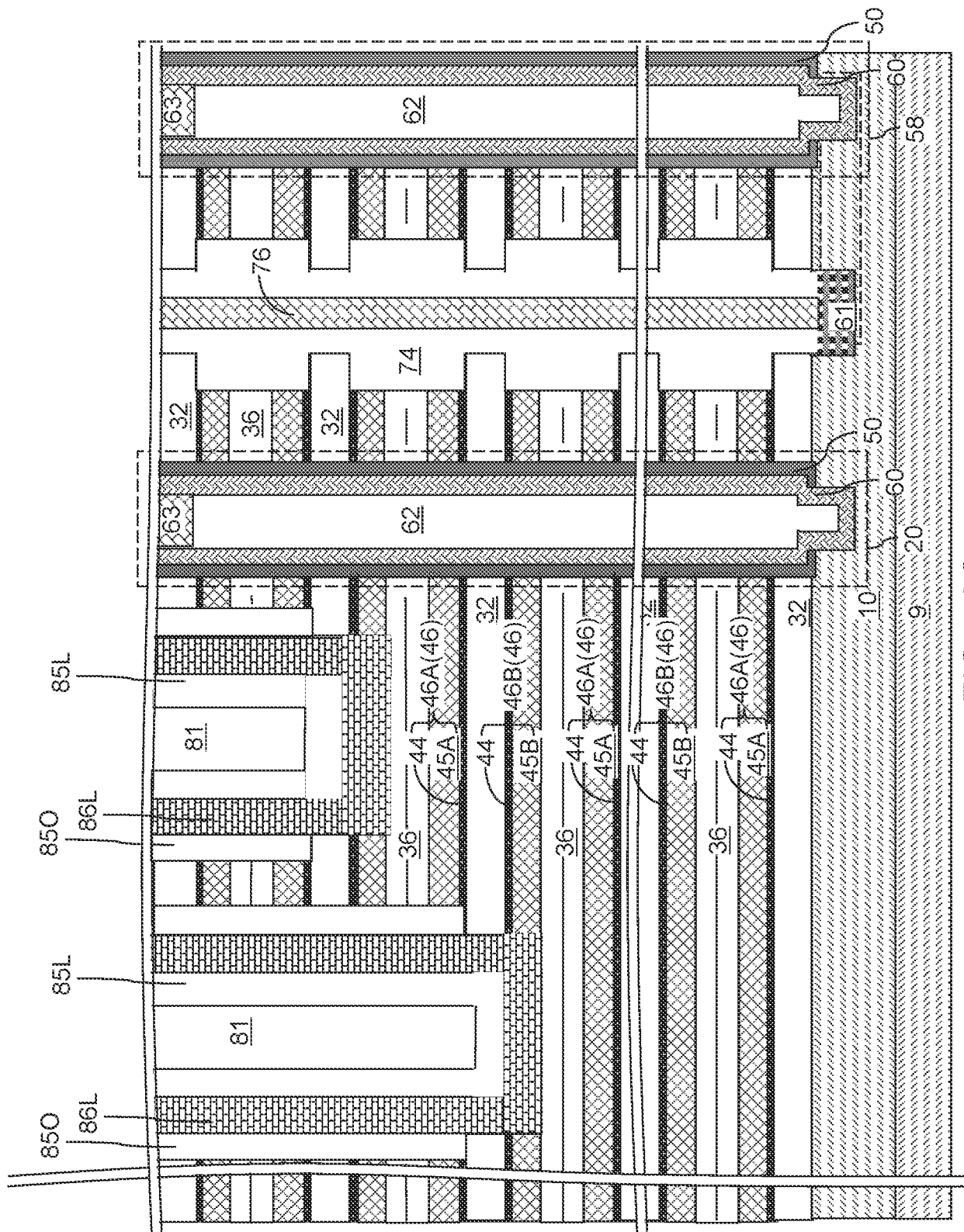


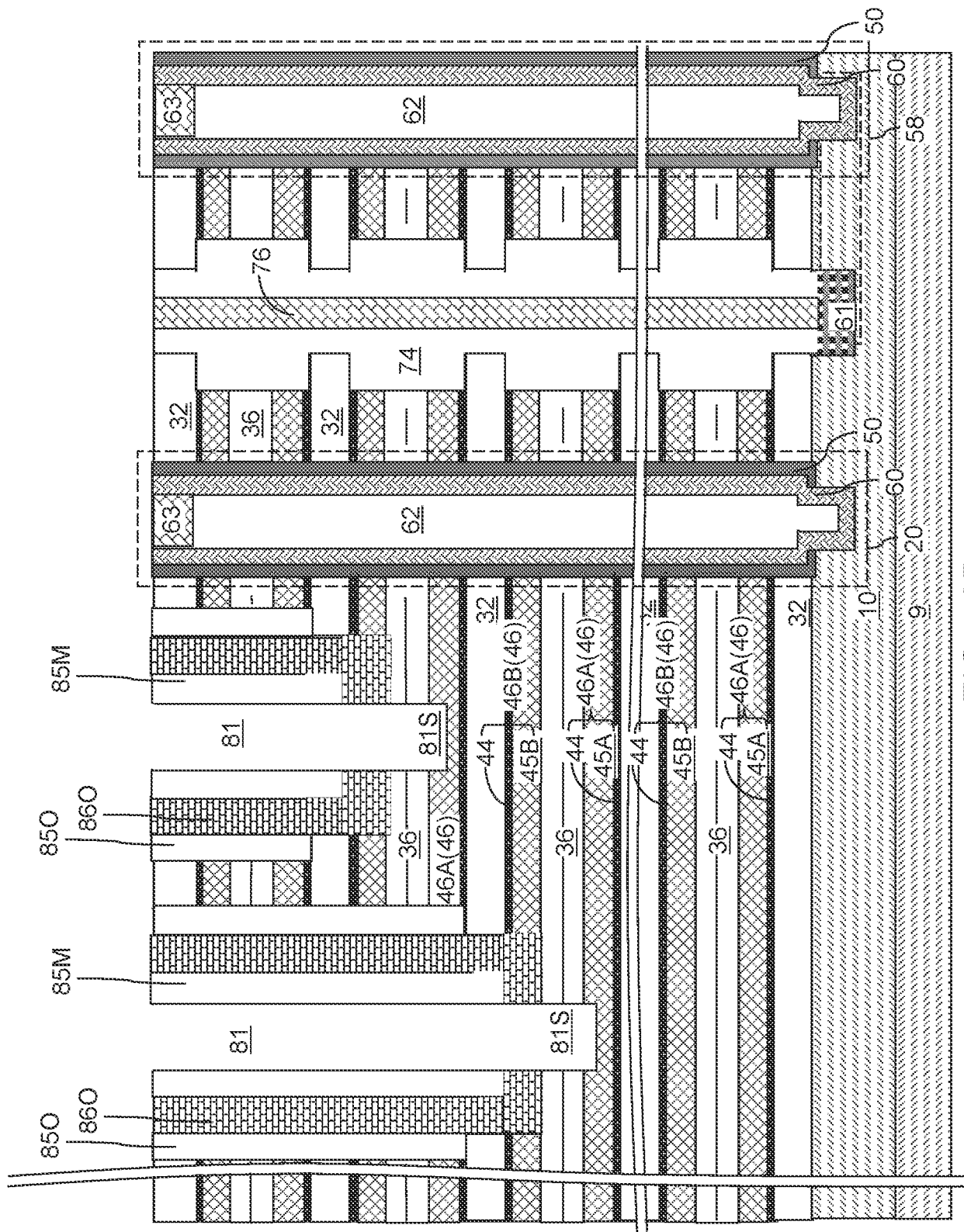
FIG. 52A



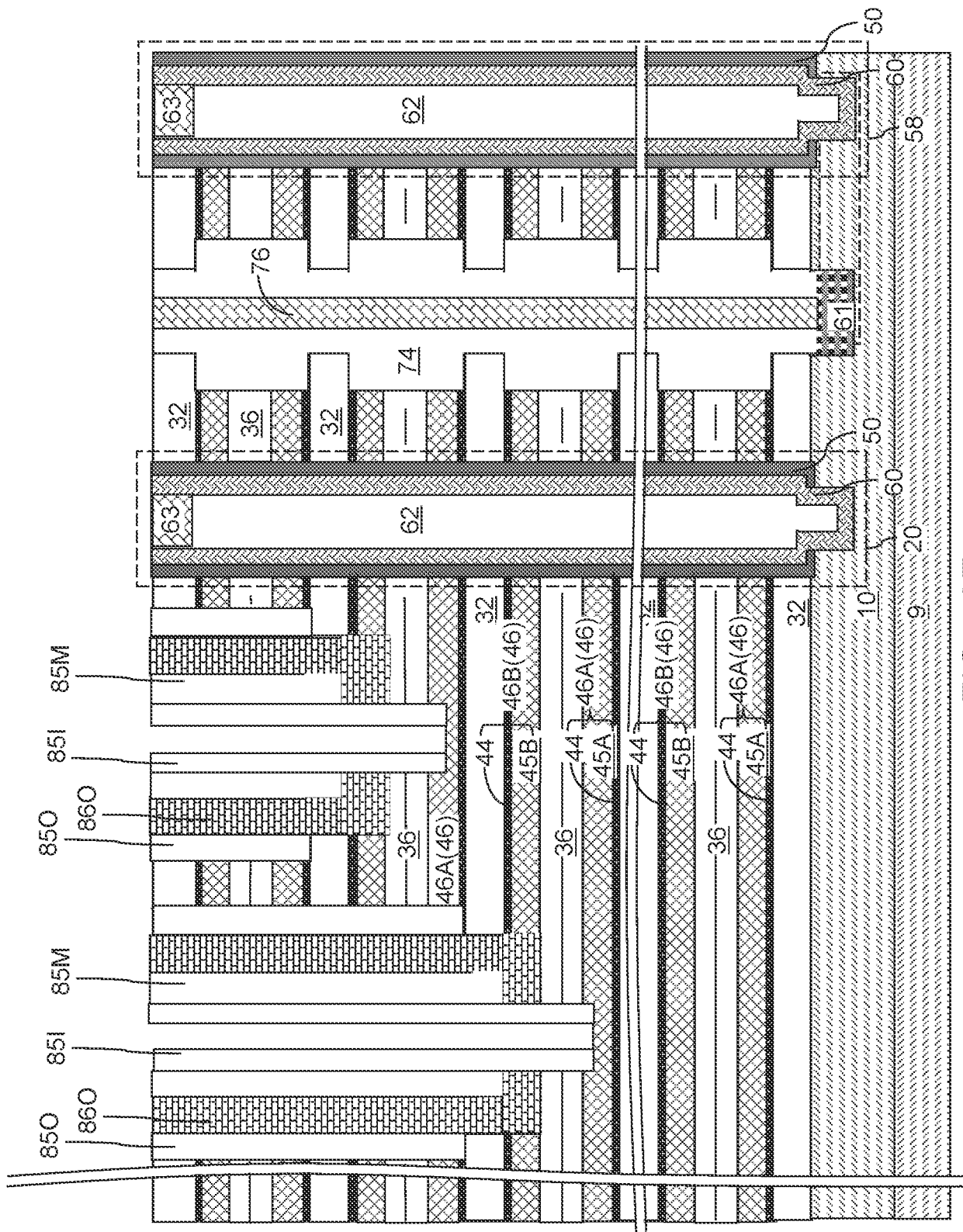








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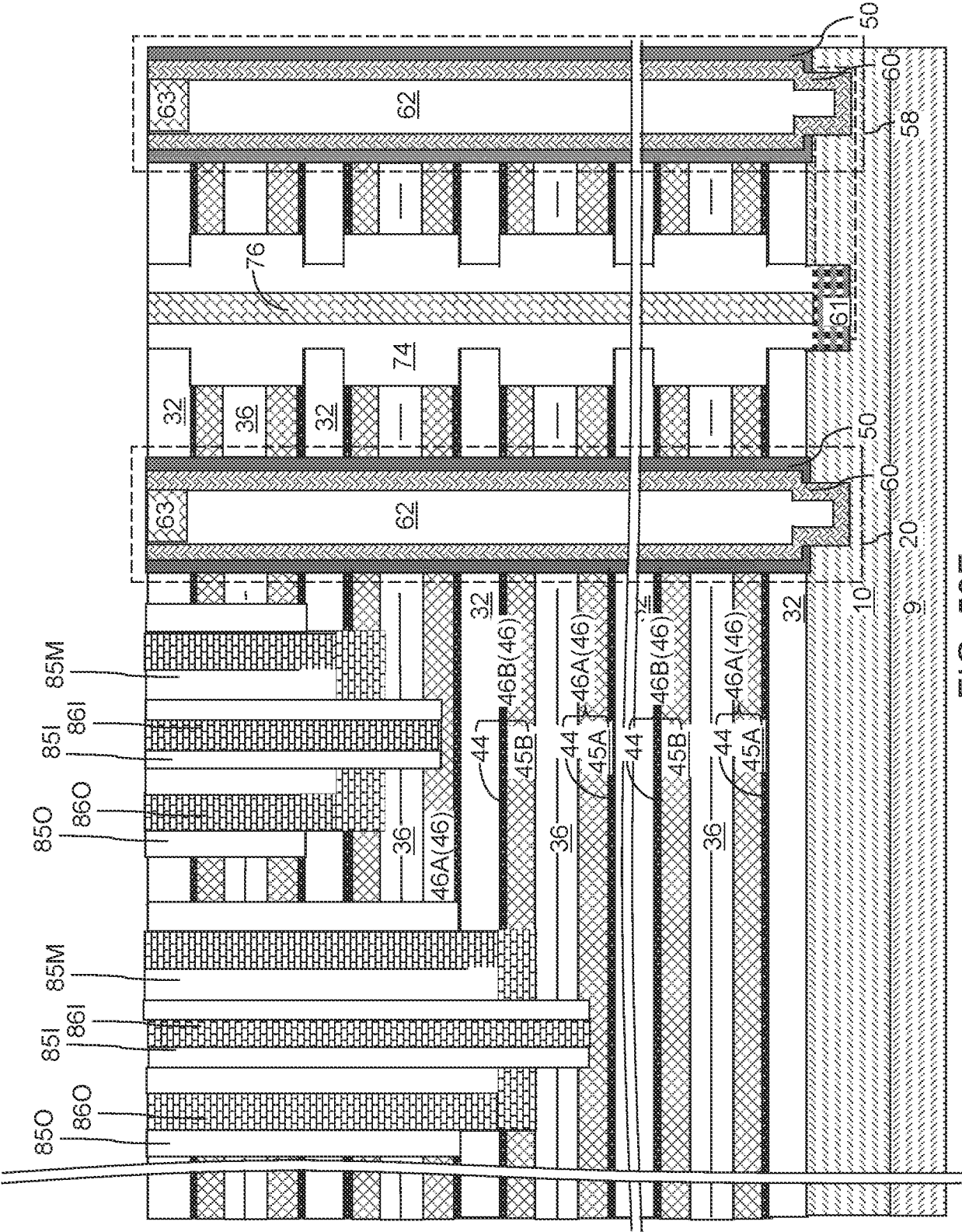


FIG. 53F

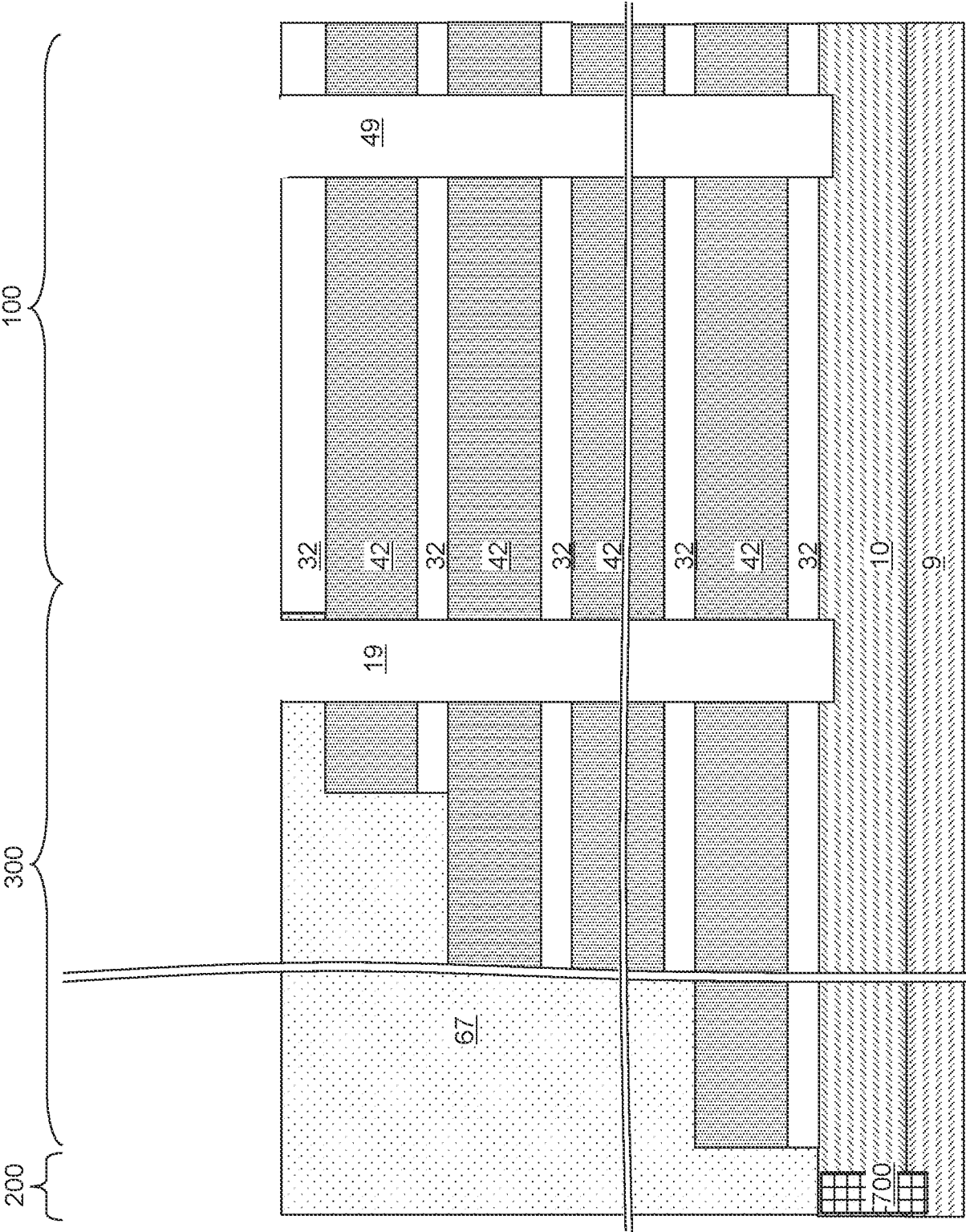
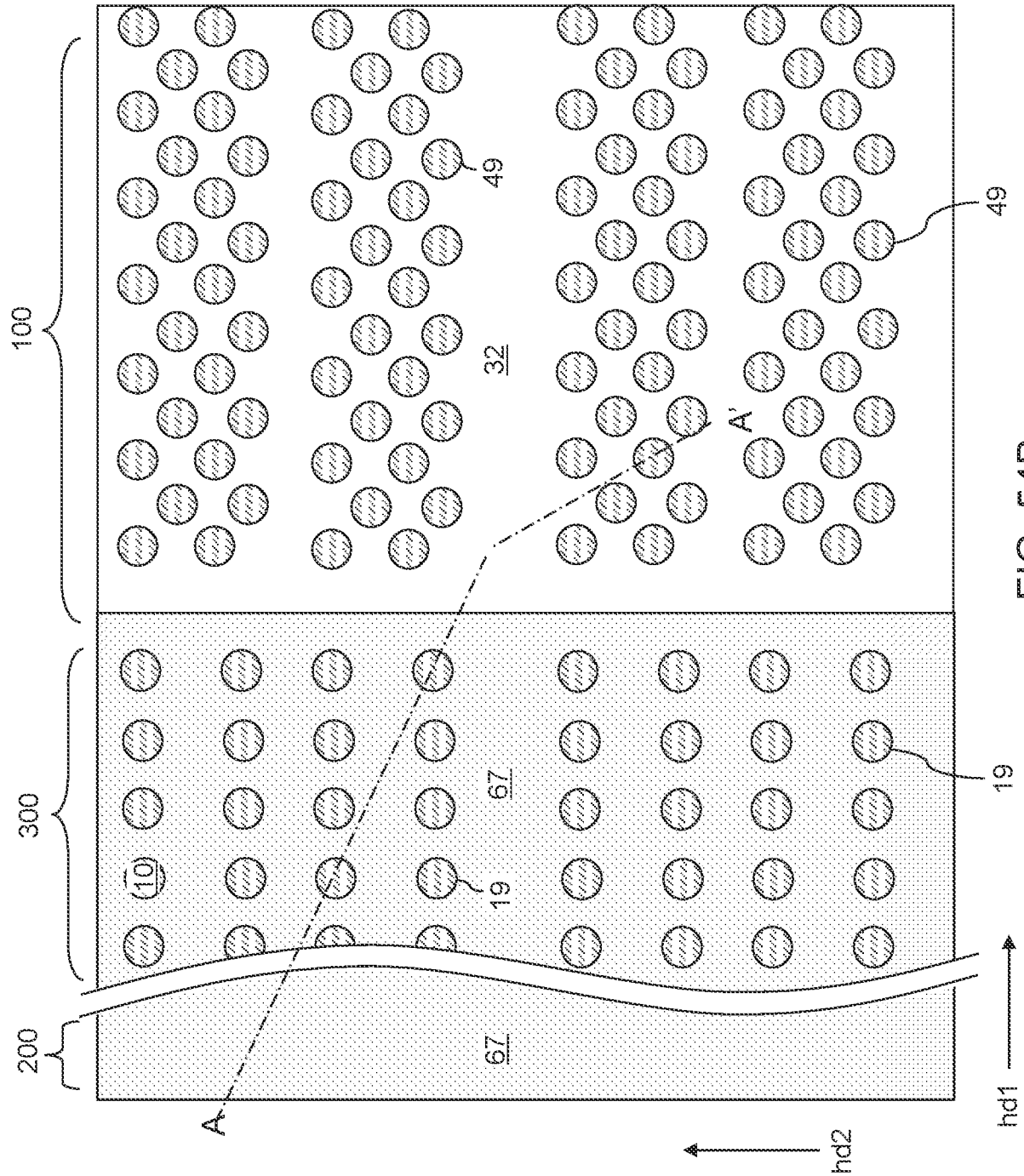


FIG. 54A



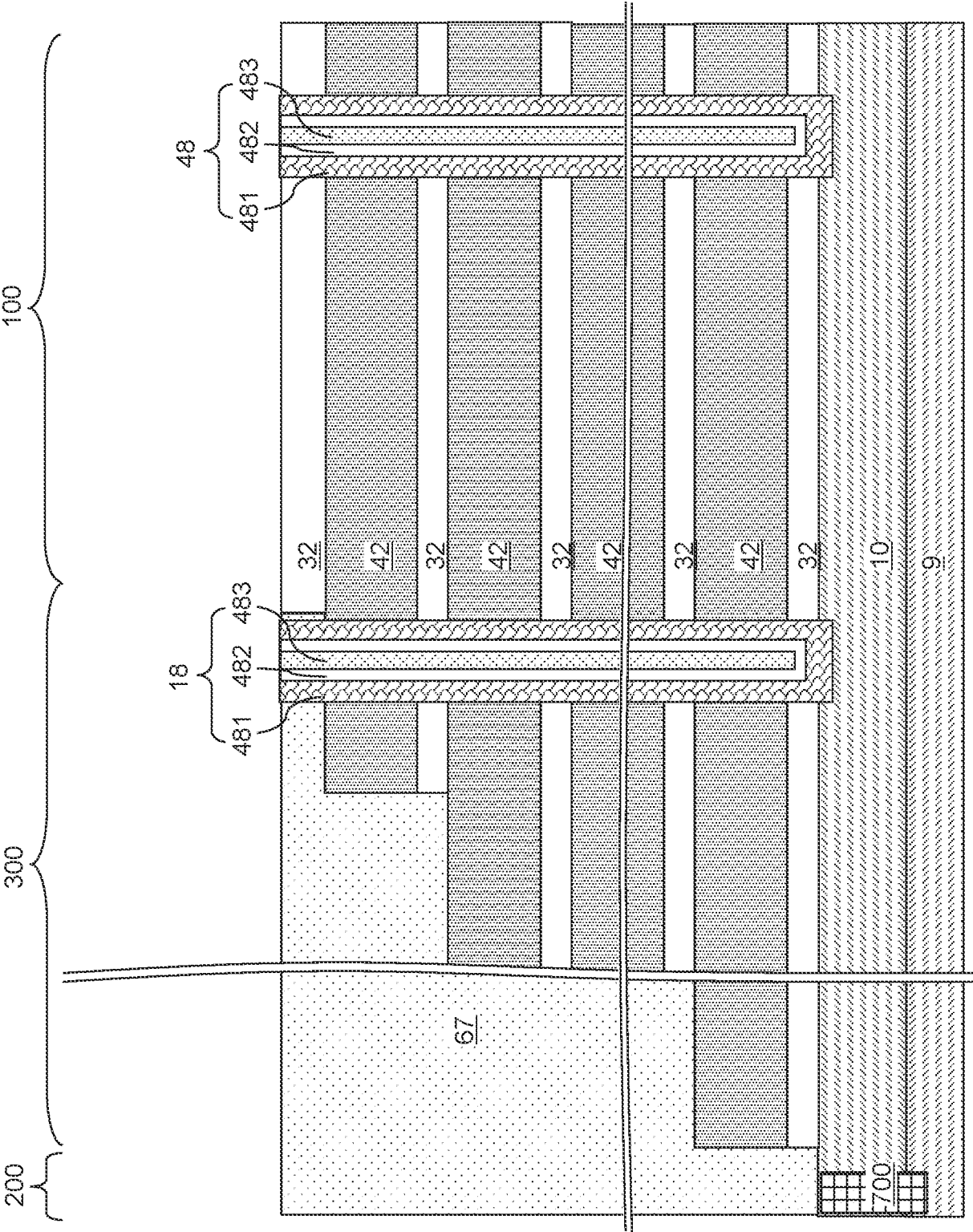


FIG. 55

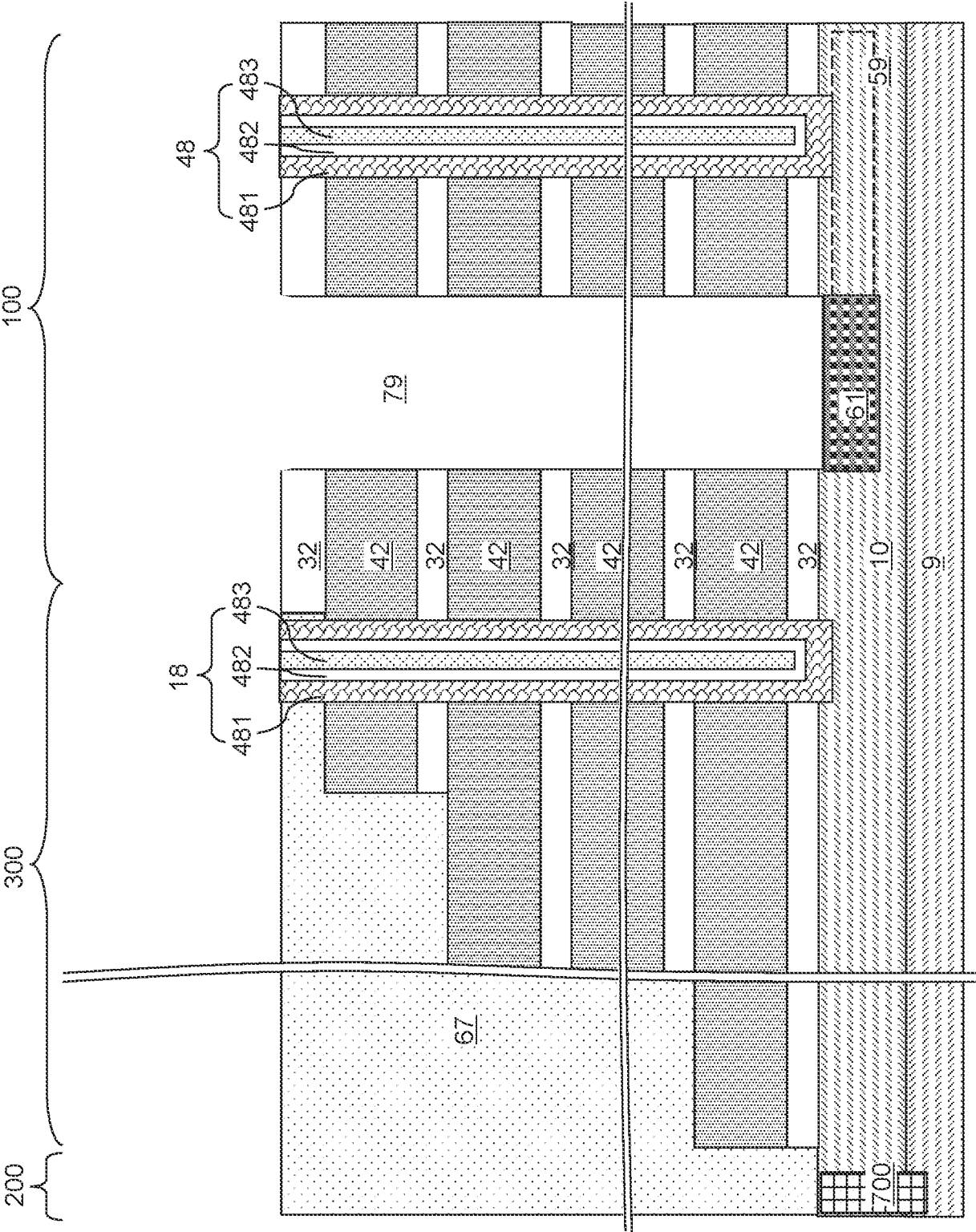
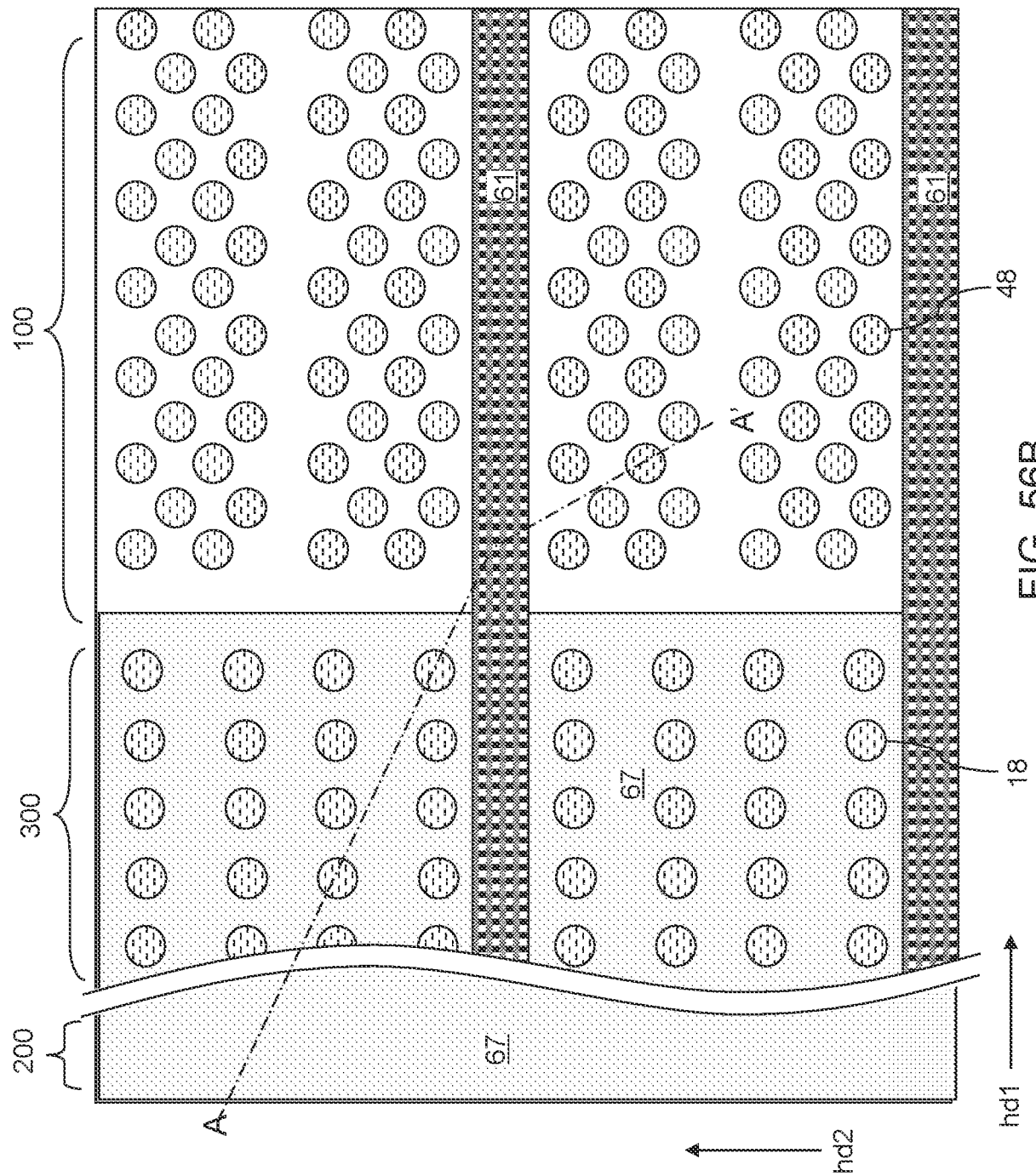
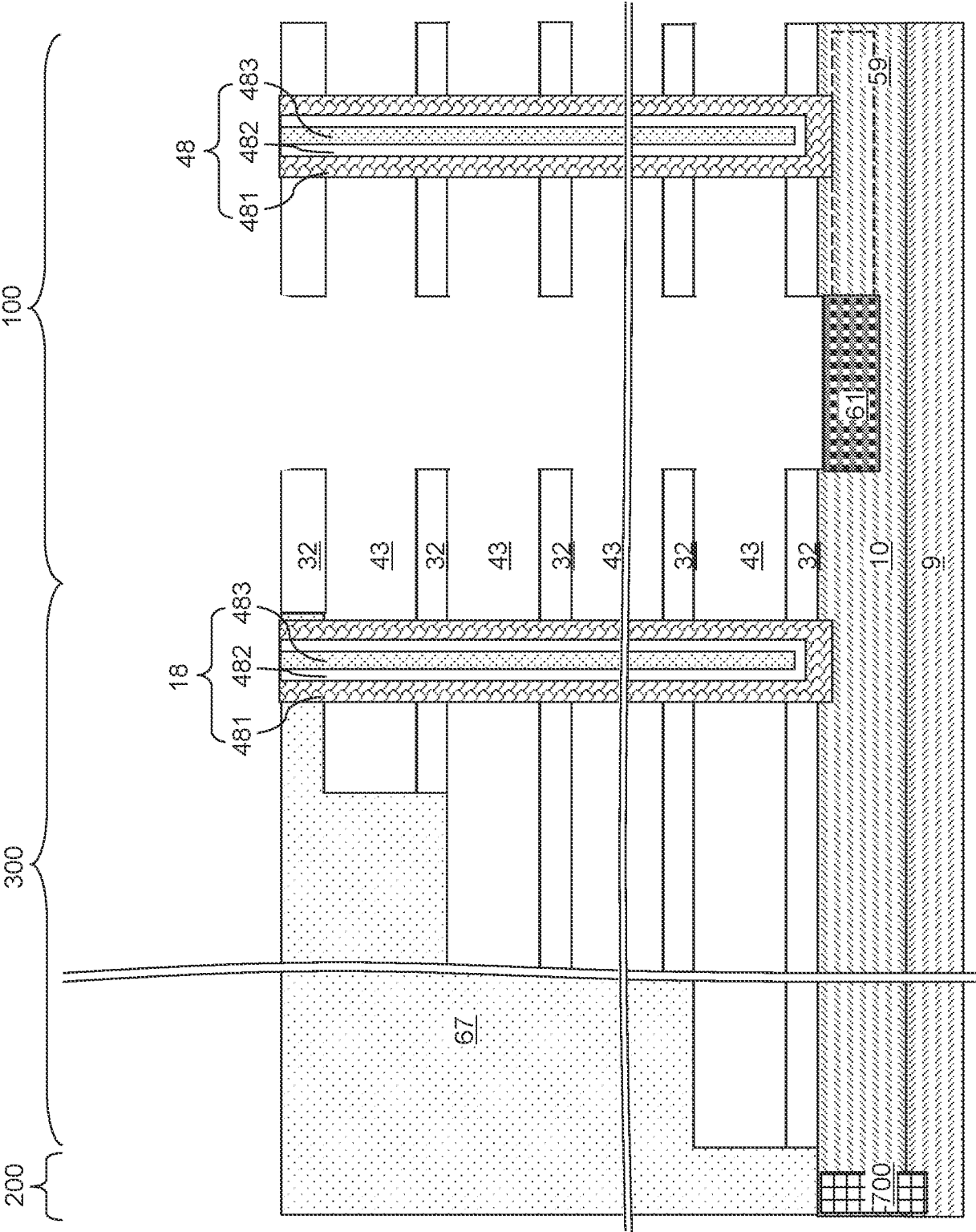
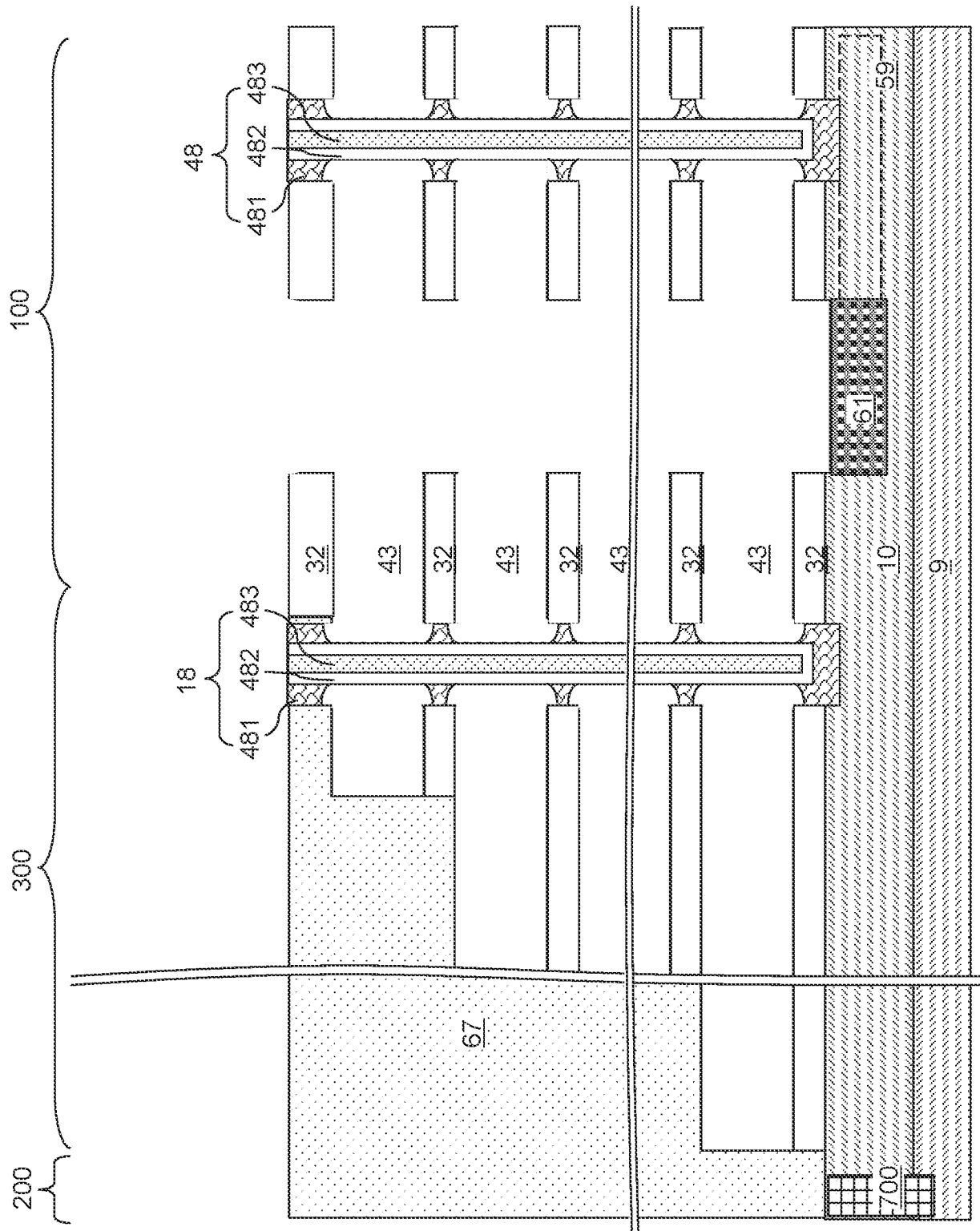


FIG. 56A







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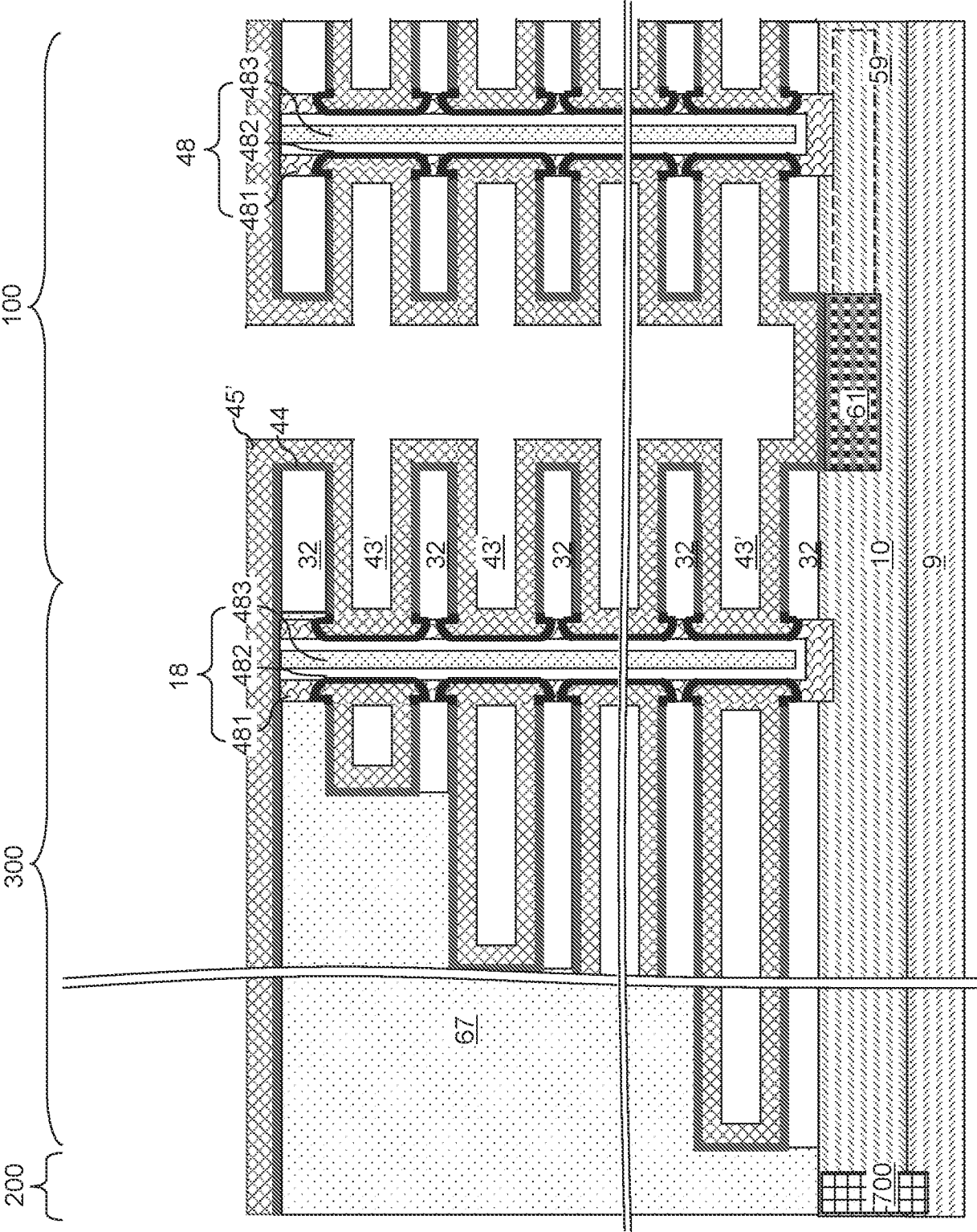
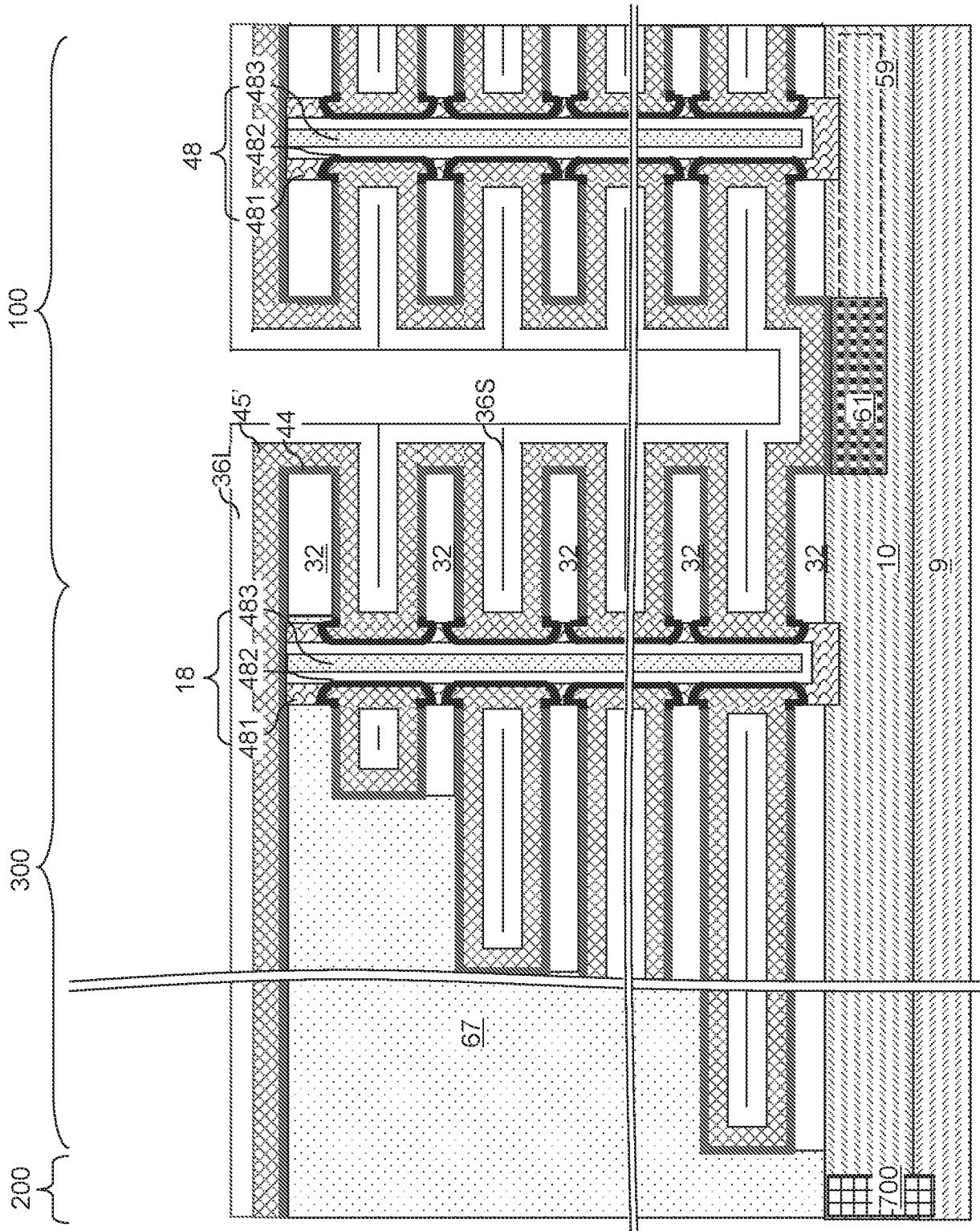


FIG. 59



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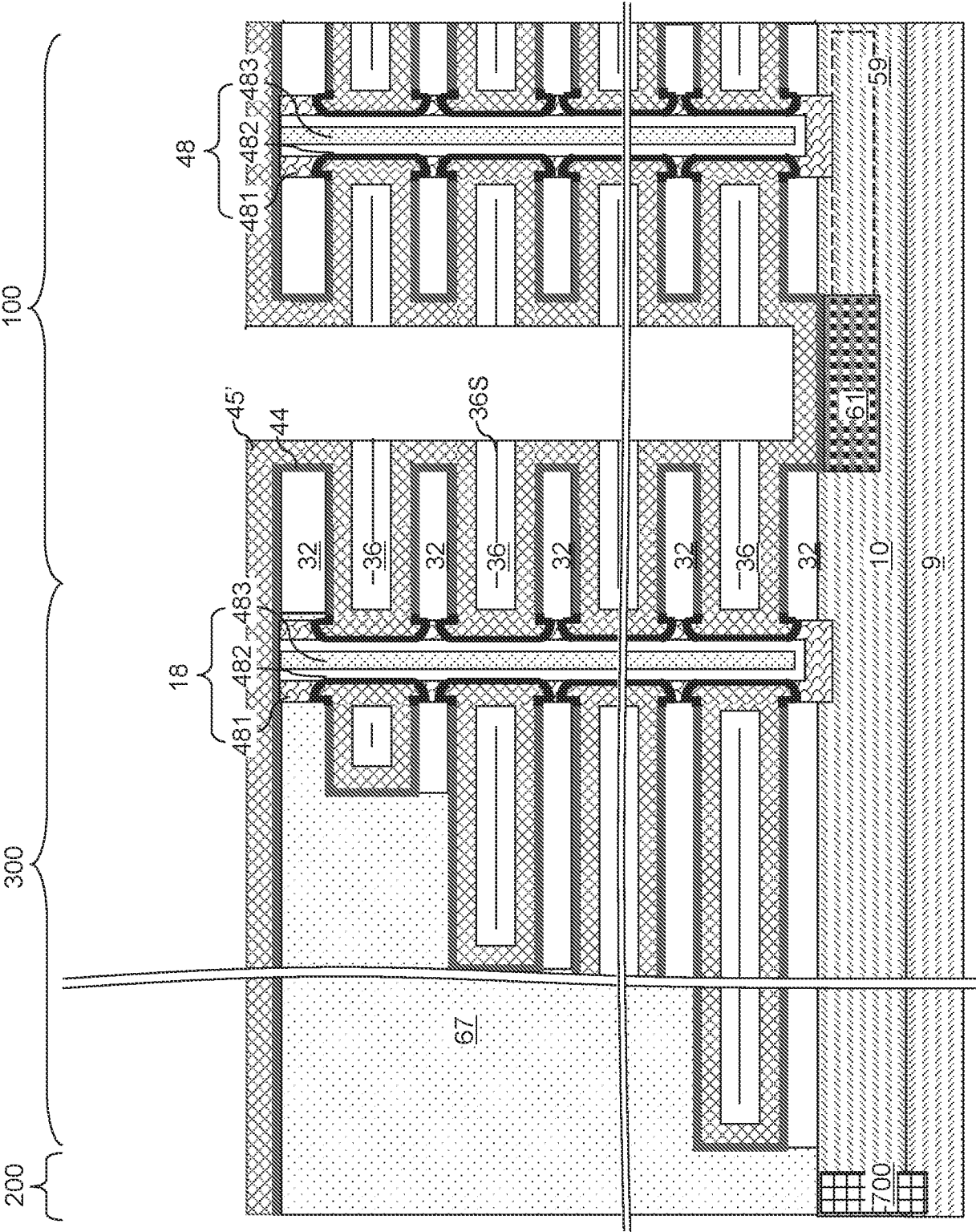


FIG. 61

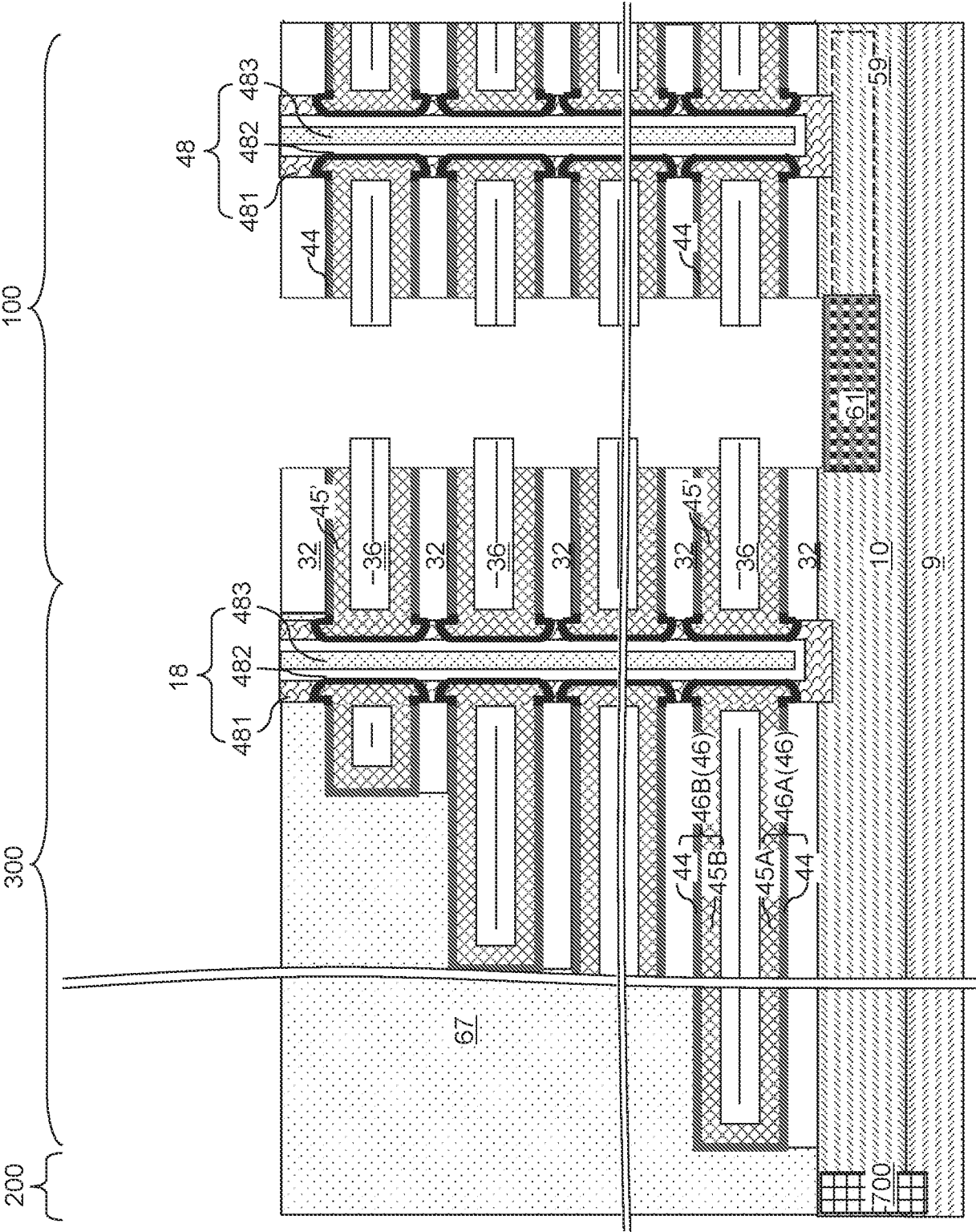


FIG. 62

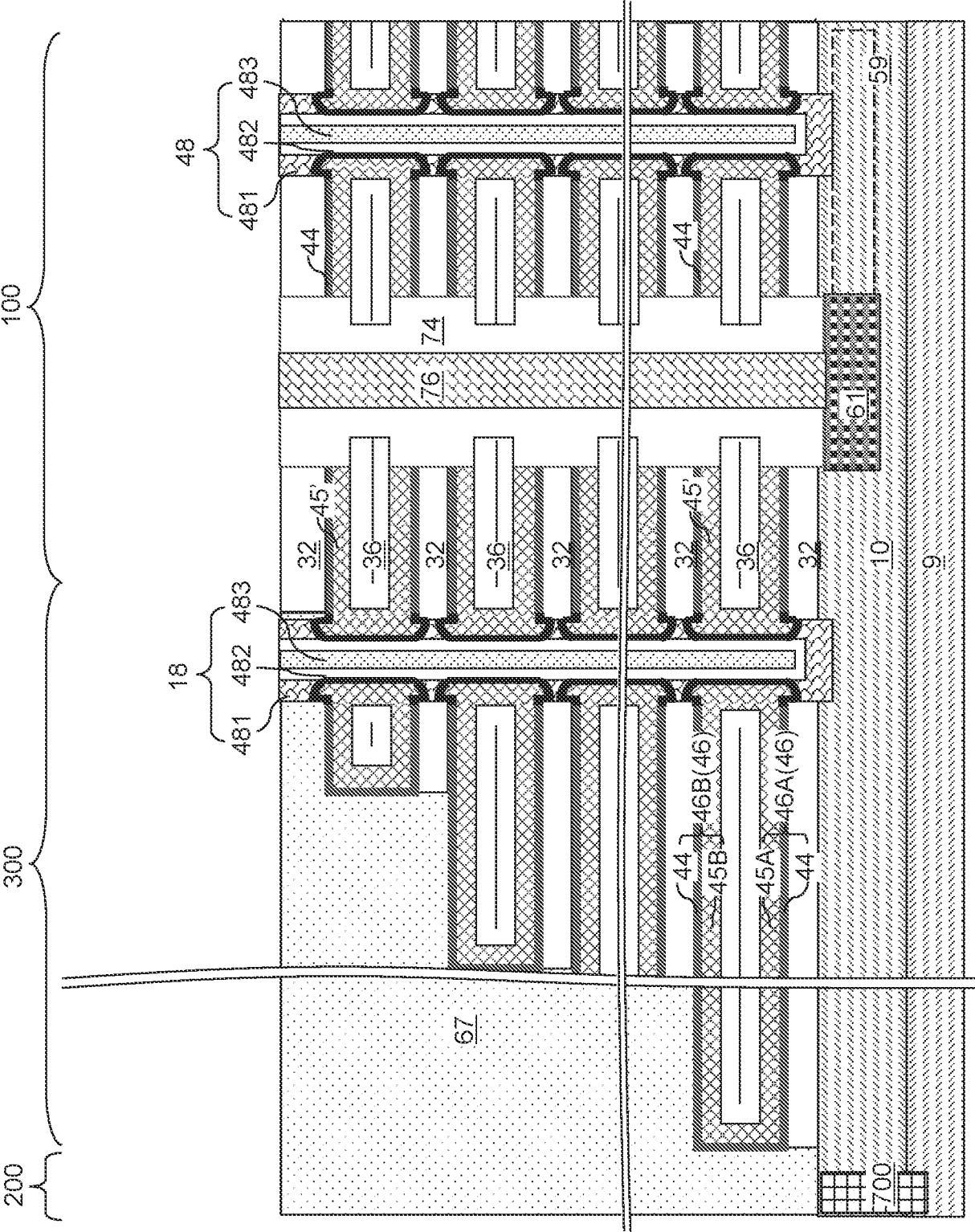


FIG. 63

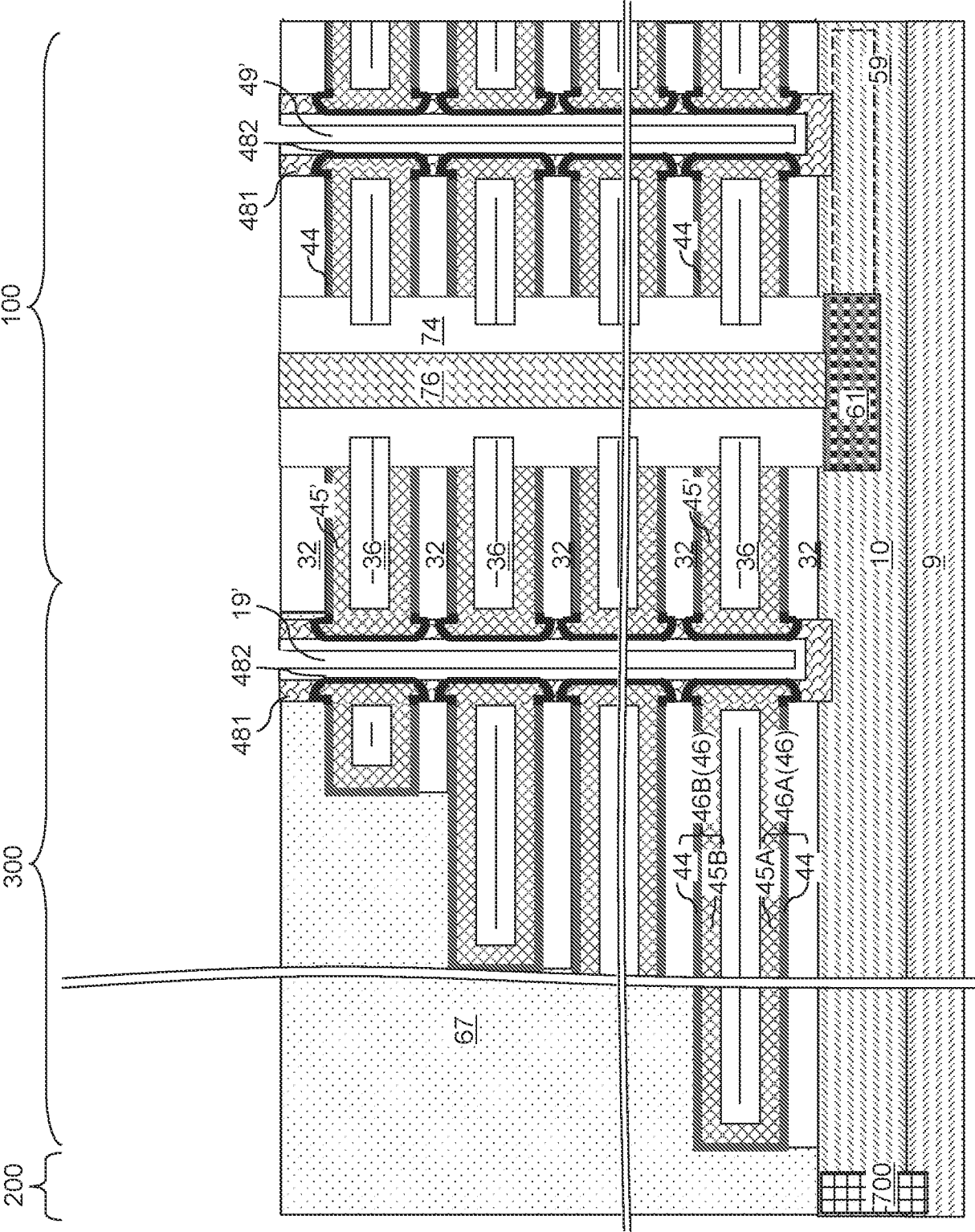
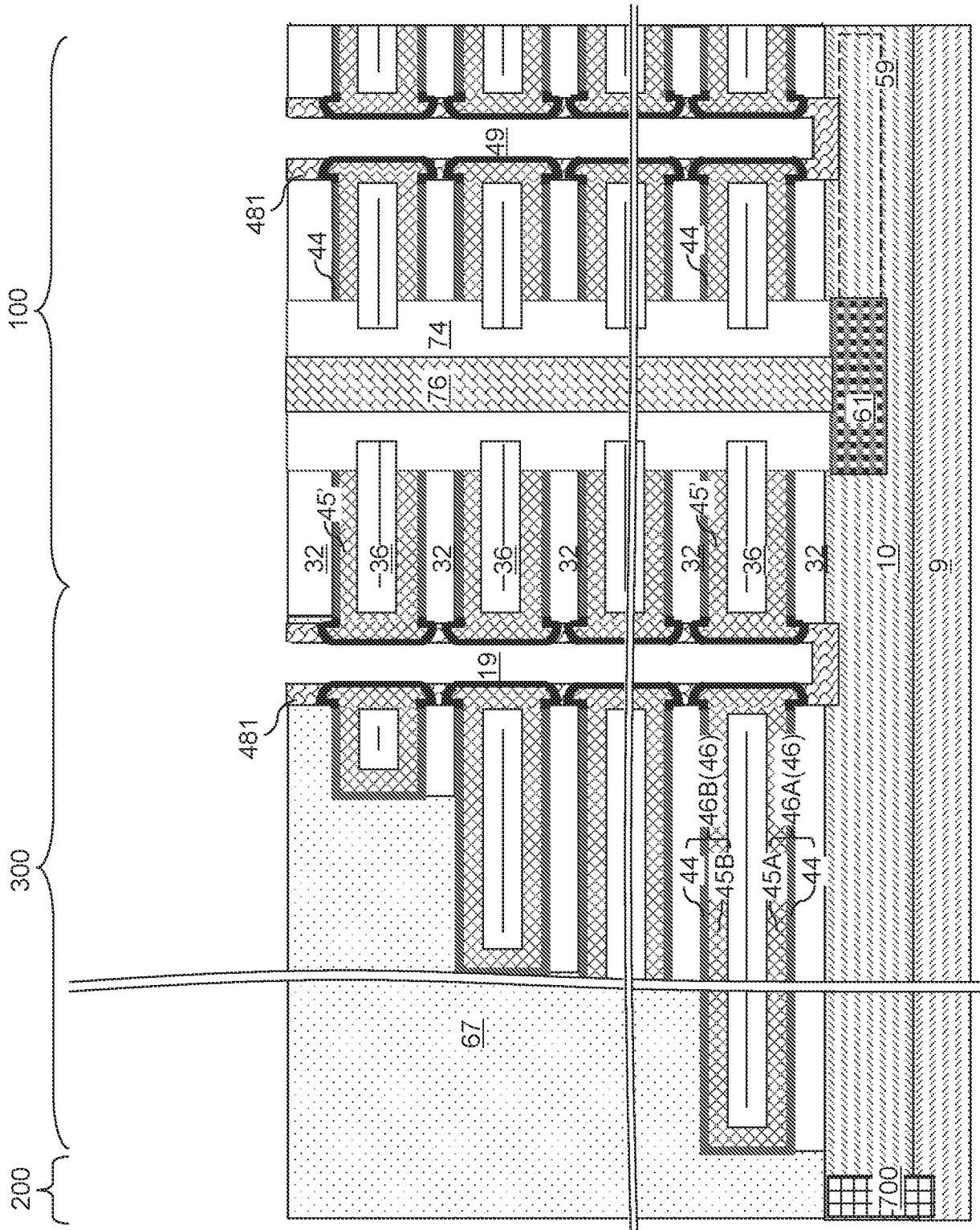
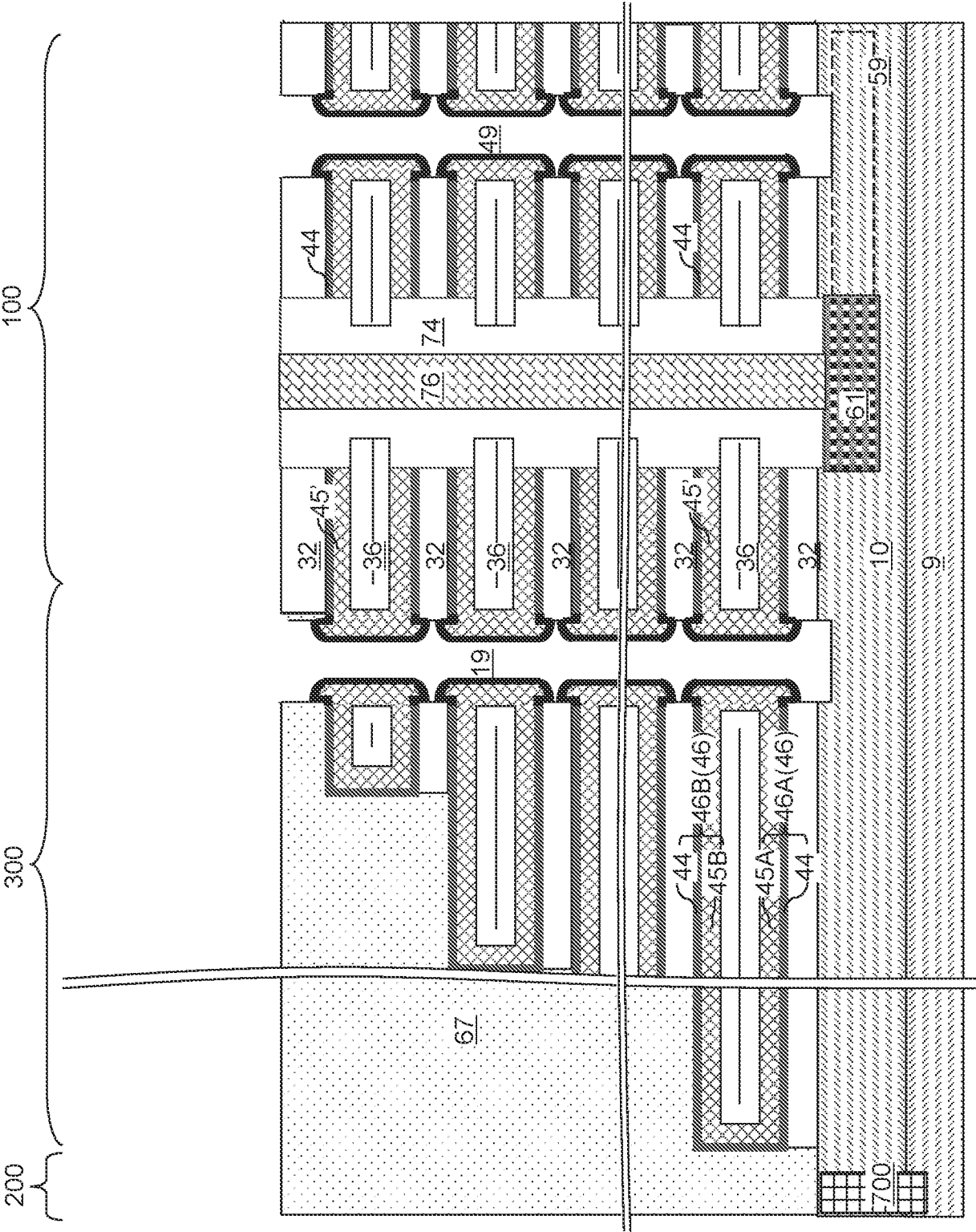


FIG. 64





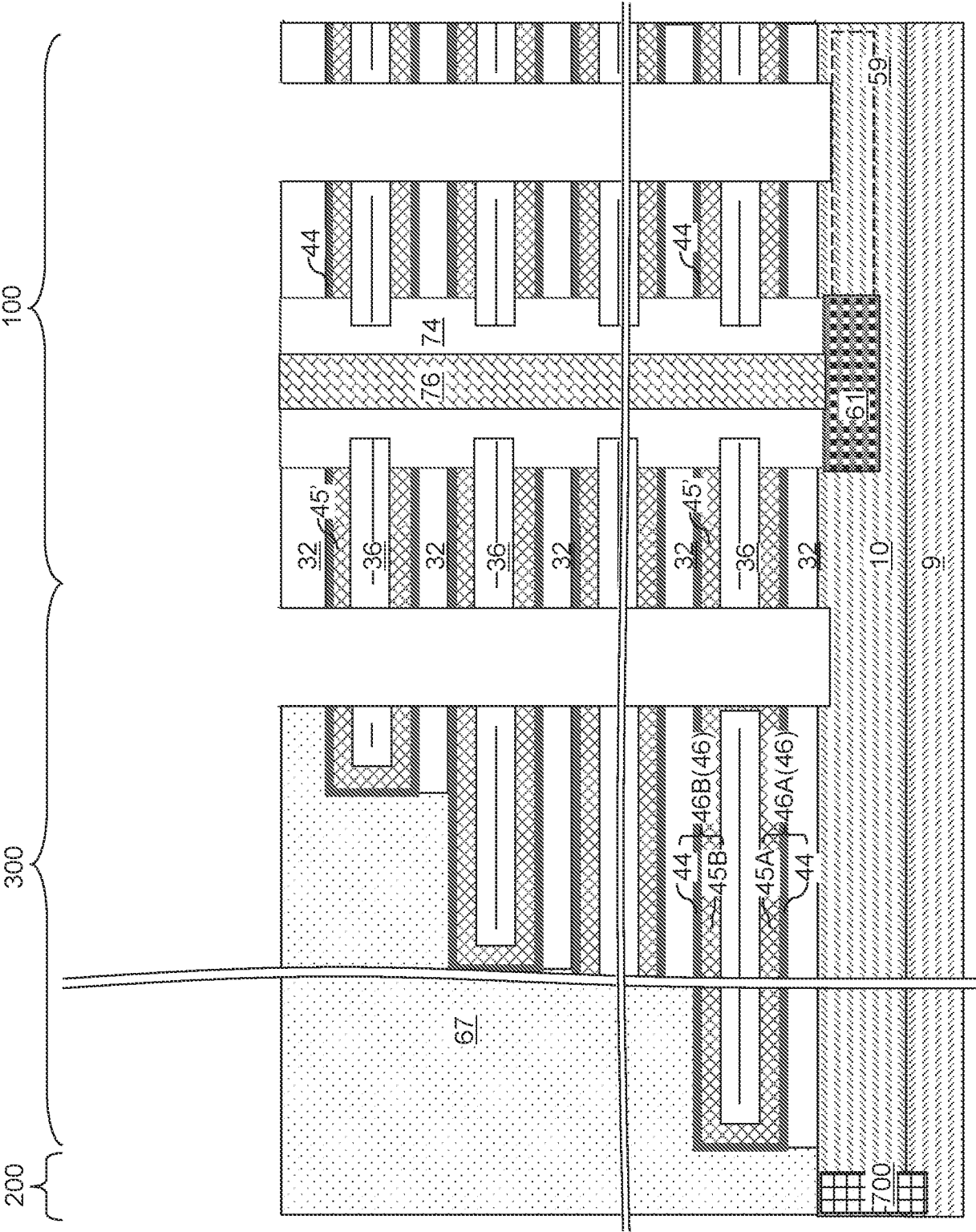
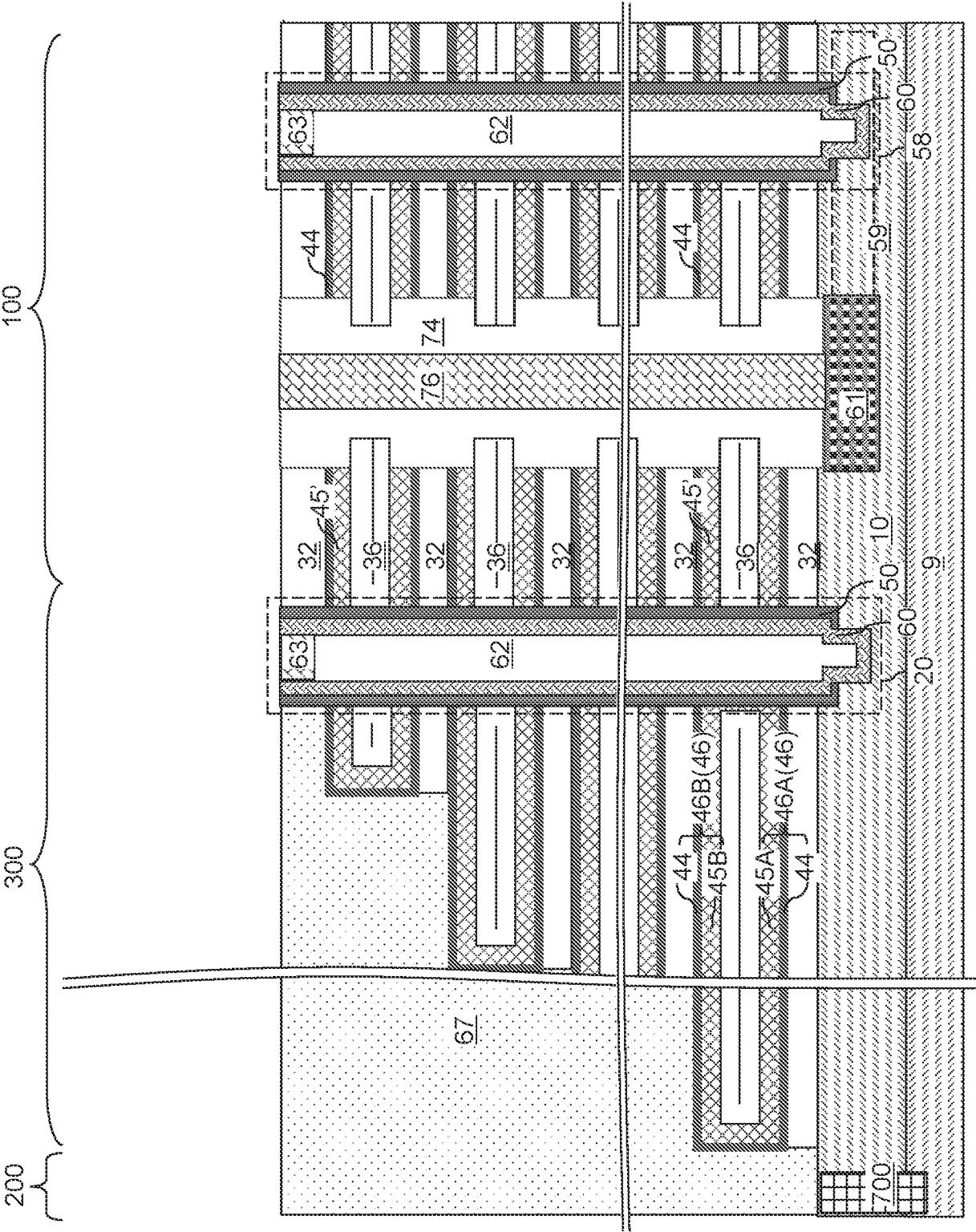
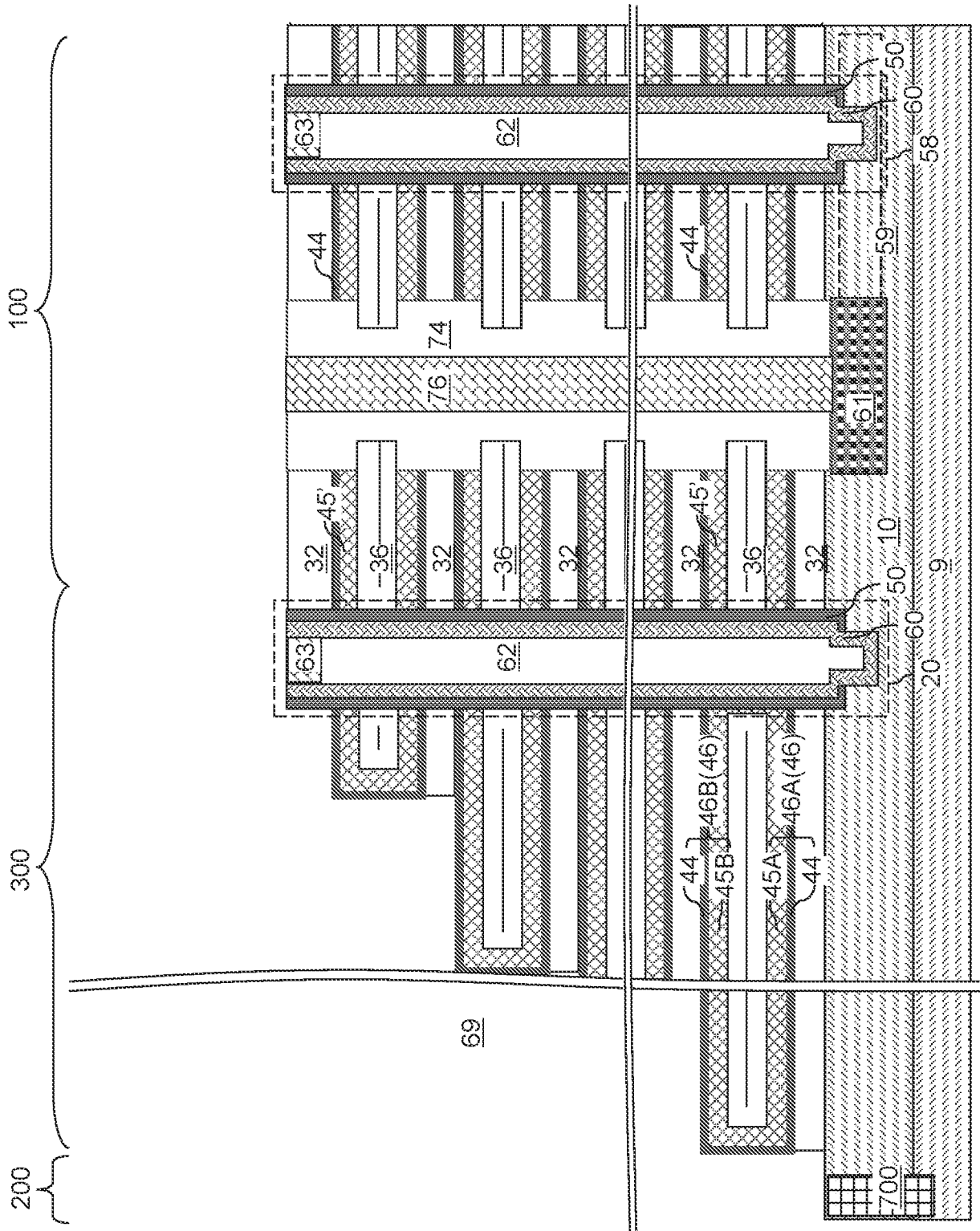
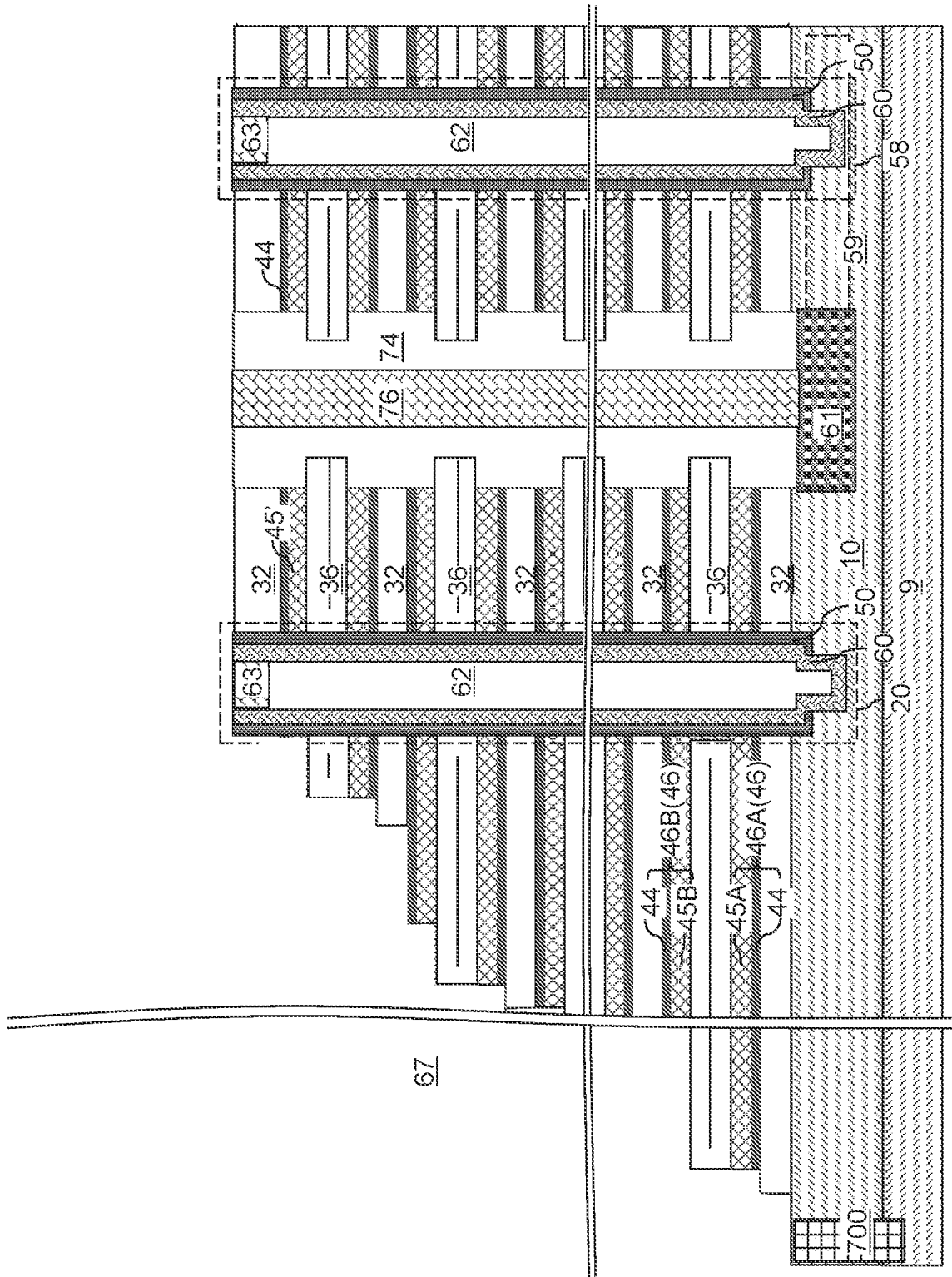
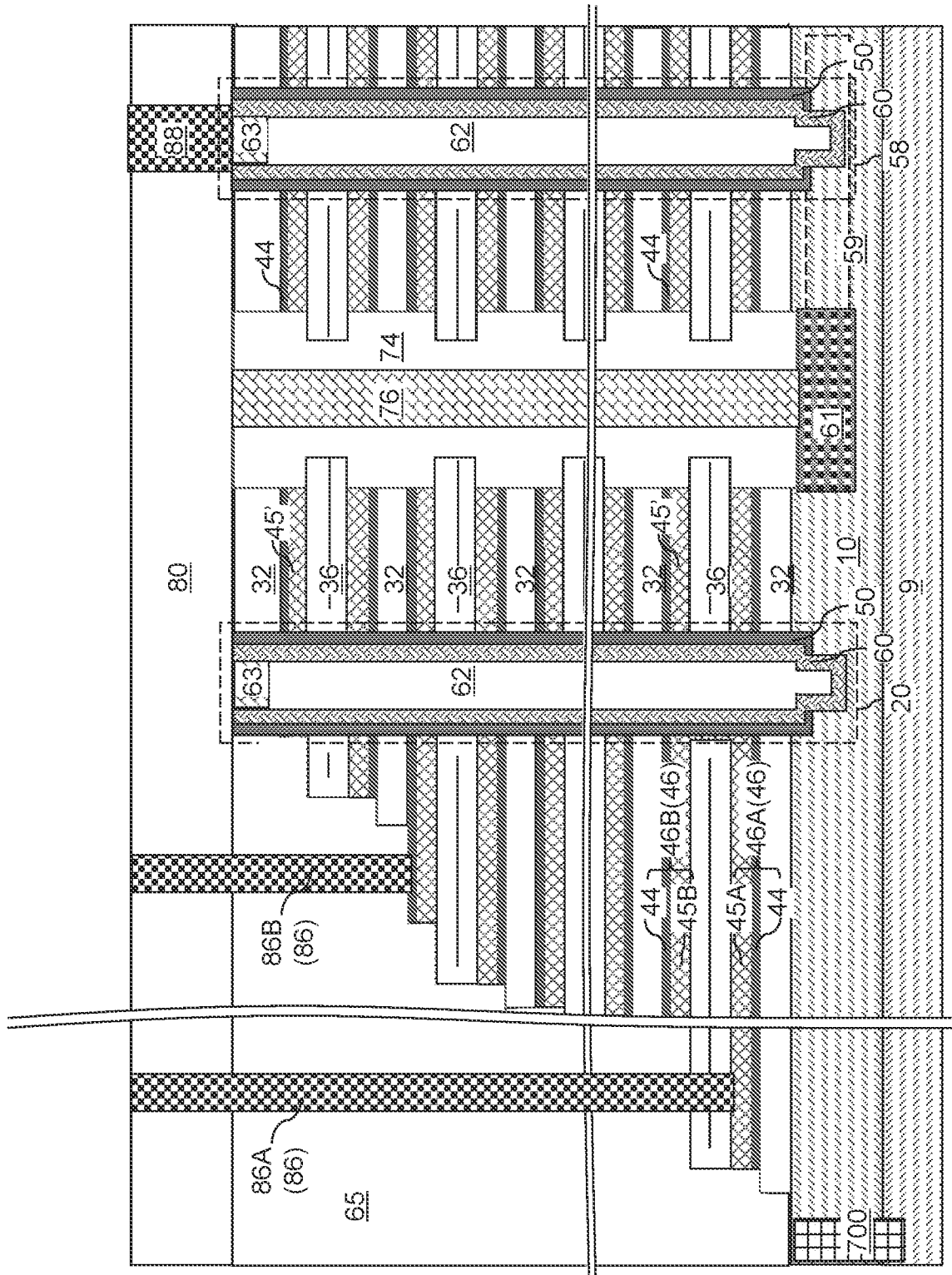


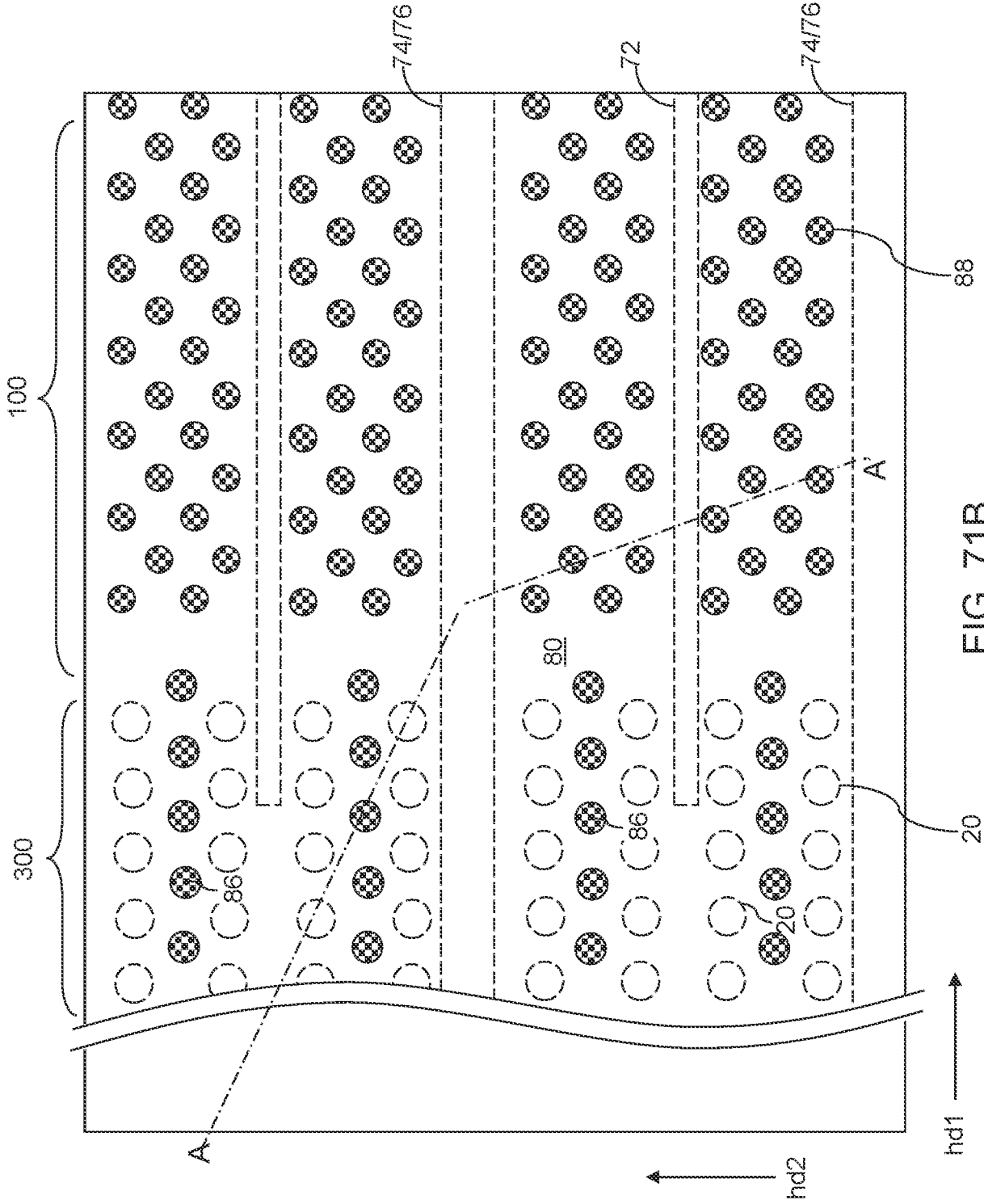
FIG. 67

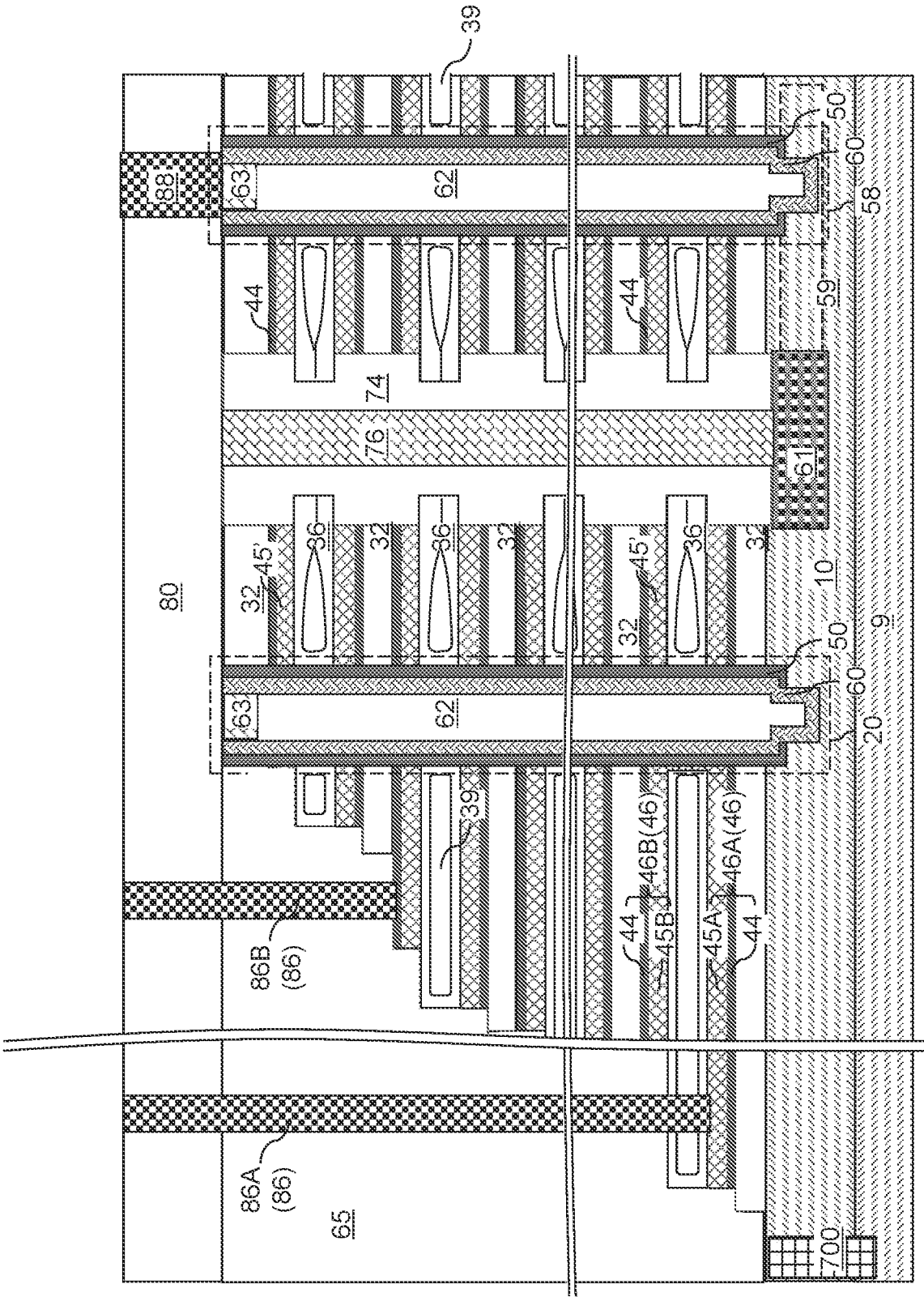












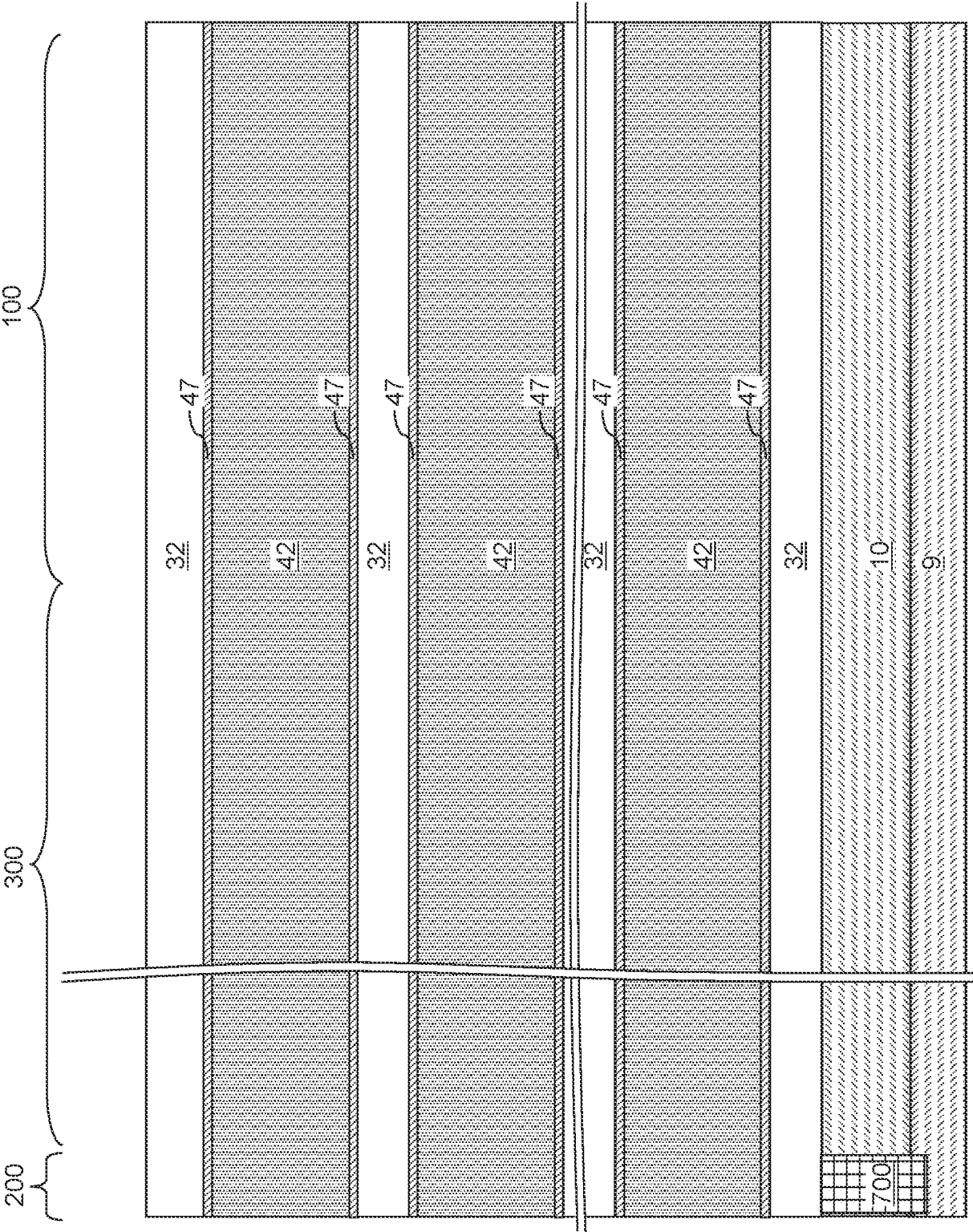


FIG. 73

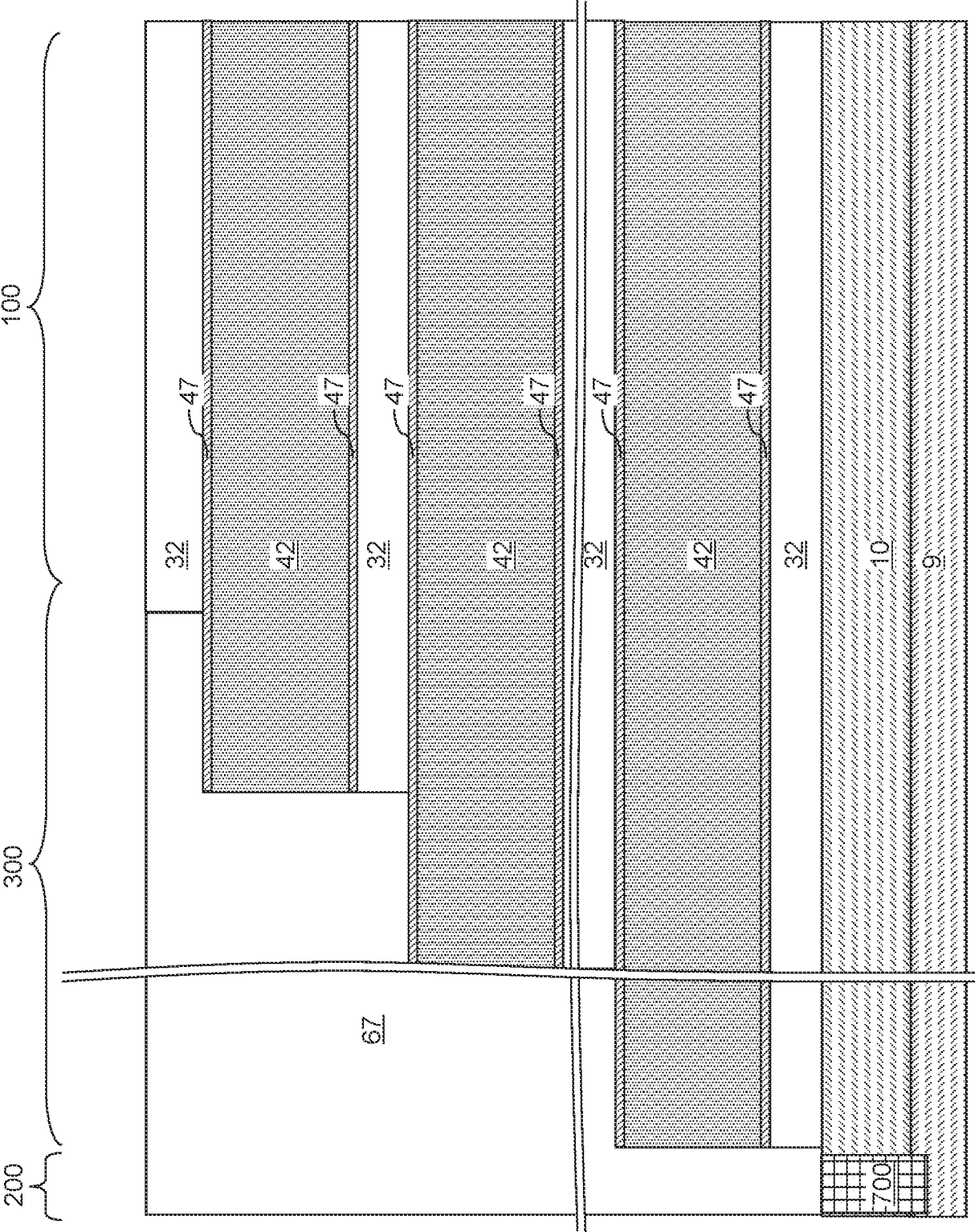


FIG. 74

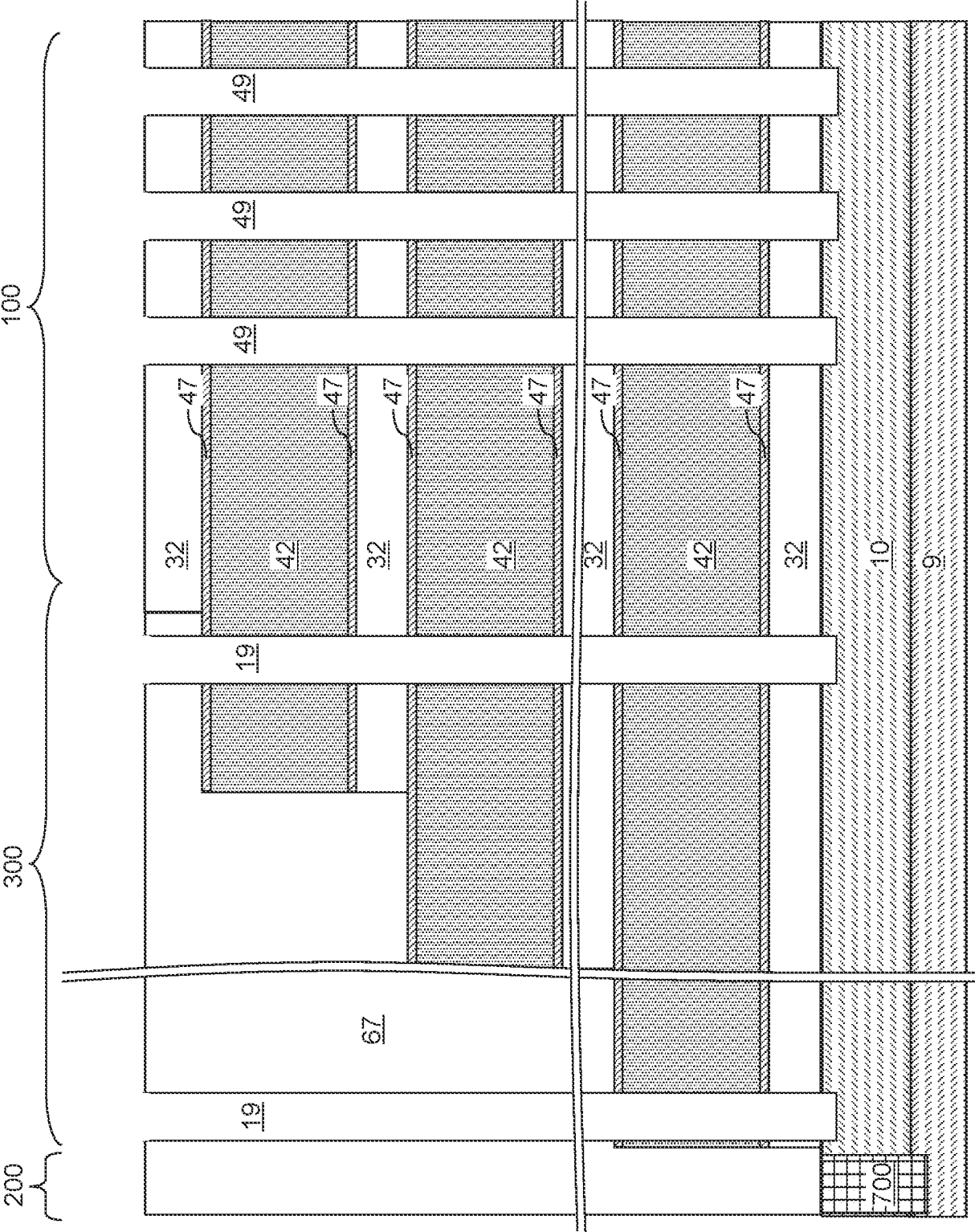
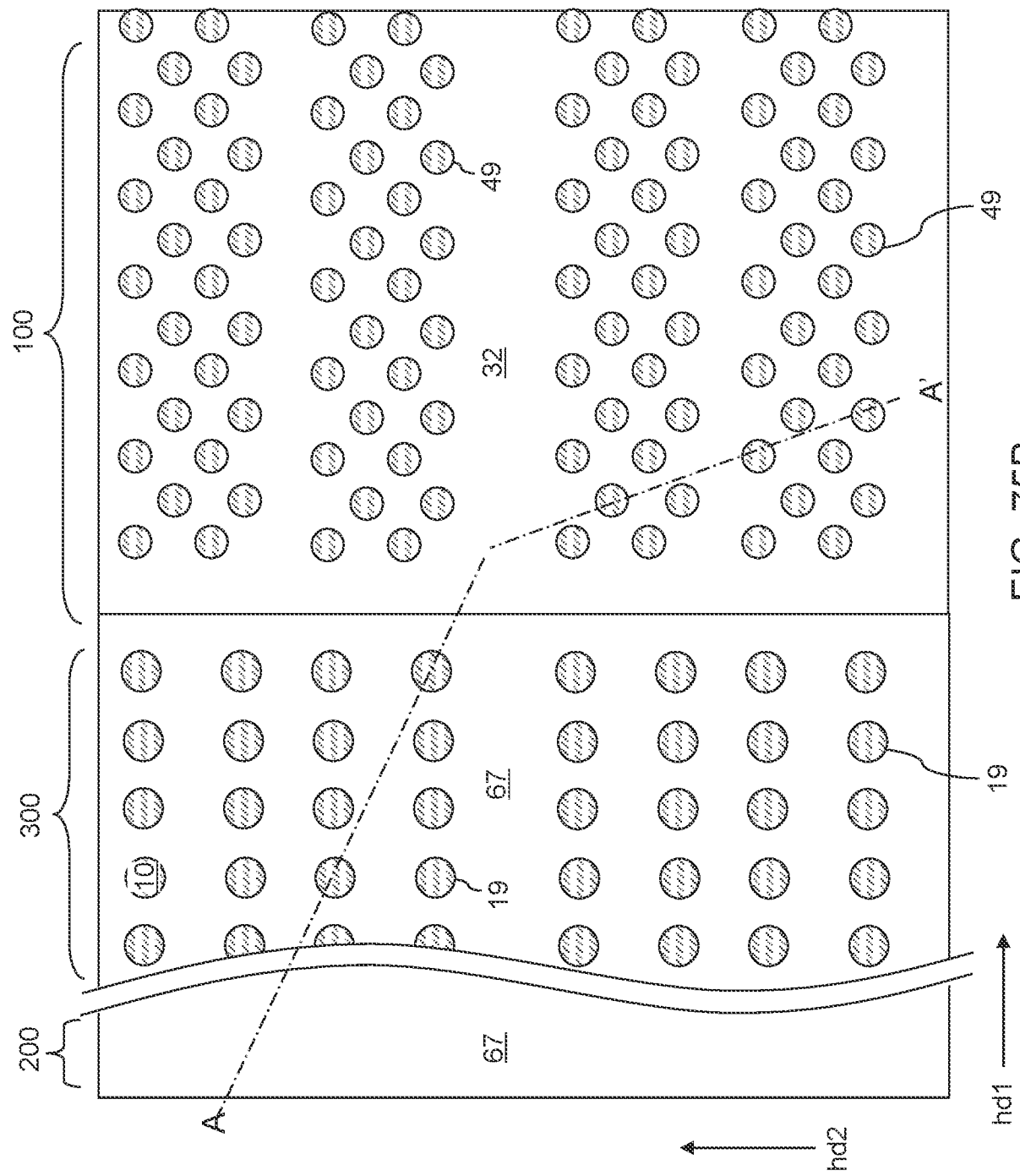


FIG. 75A



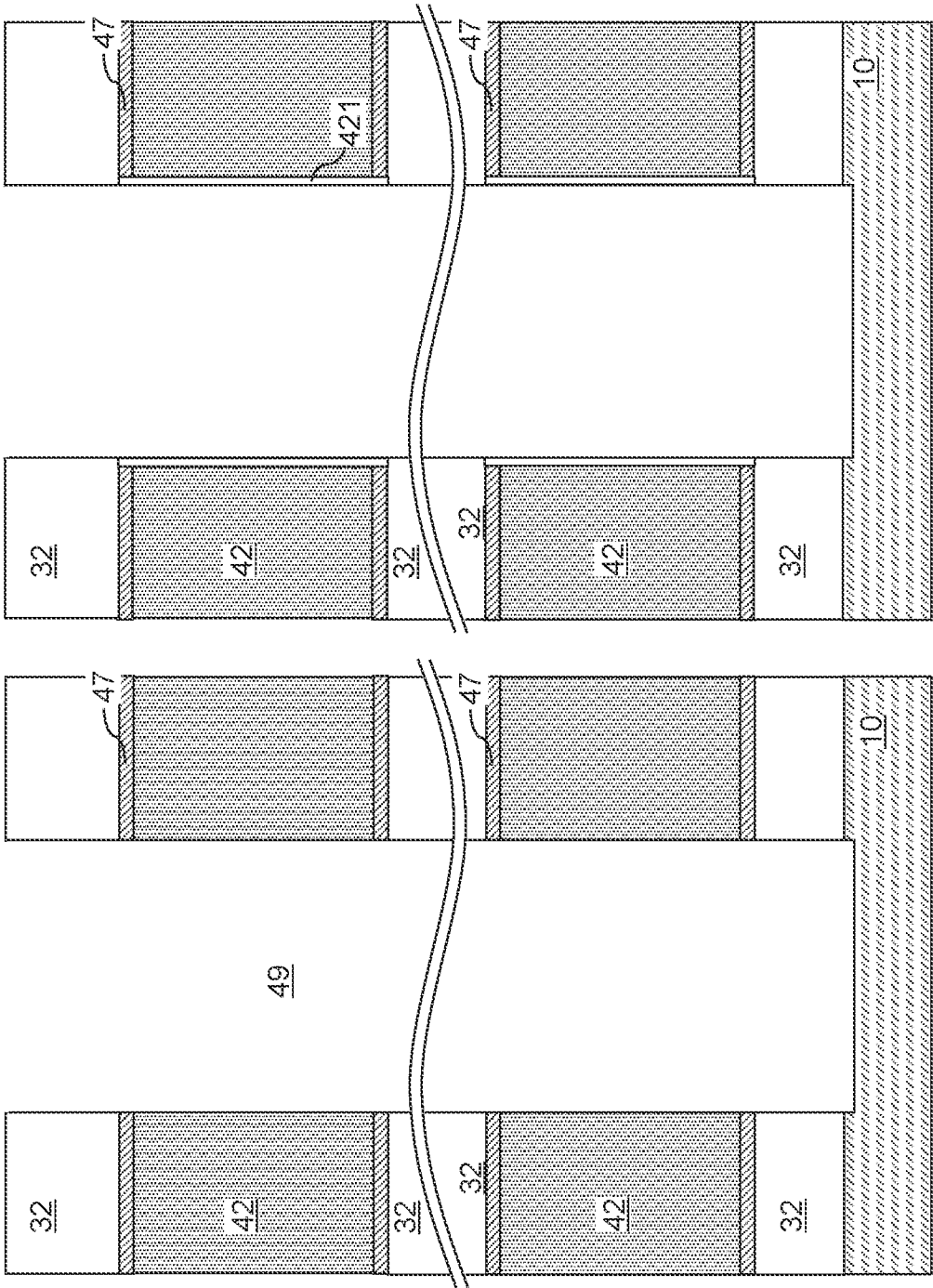


FIG. 76B

FIG. 76A

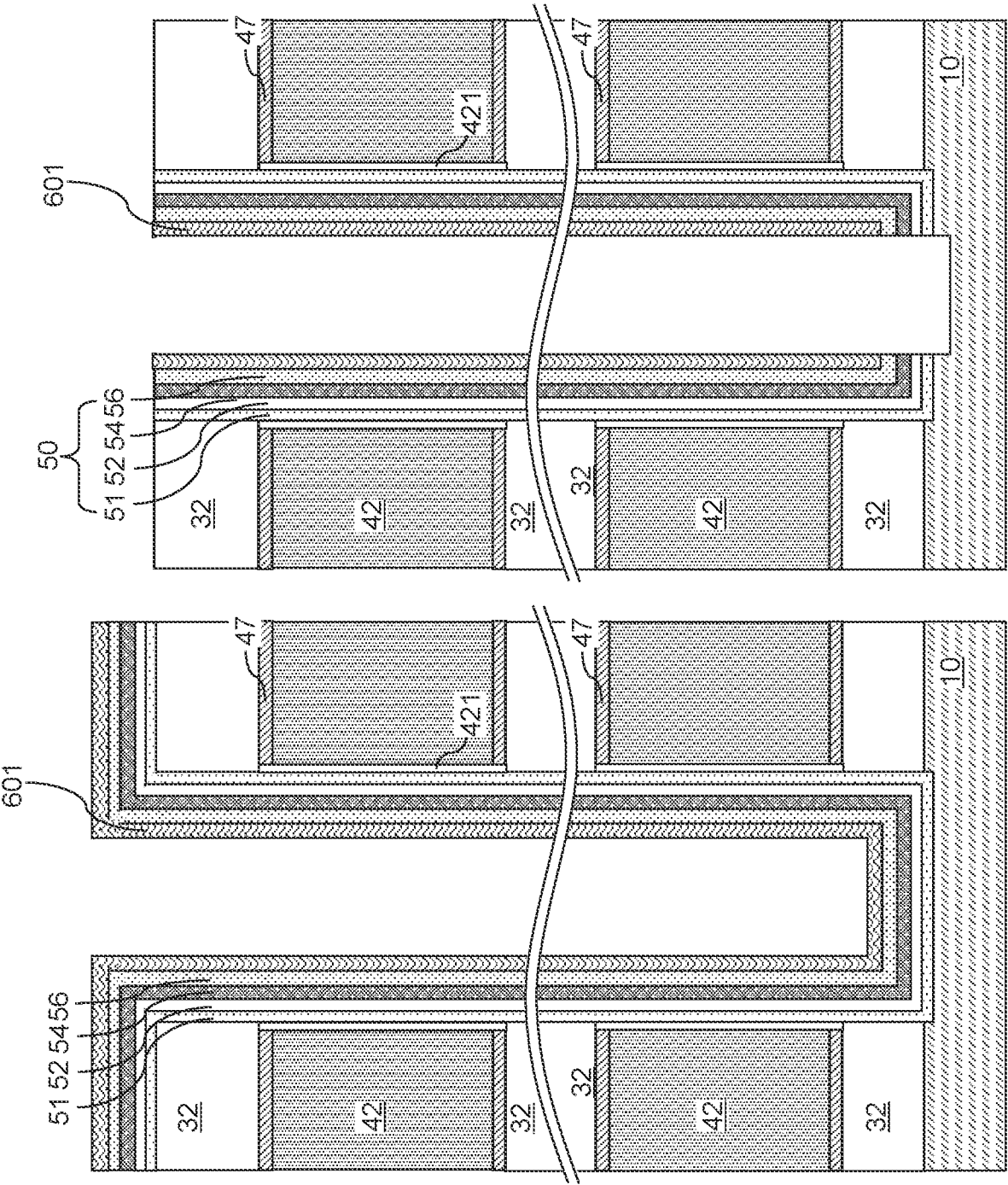


FIG. 76D

FIG. 76C

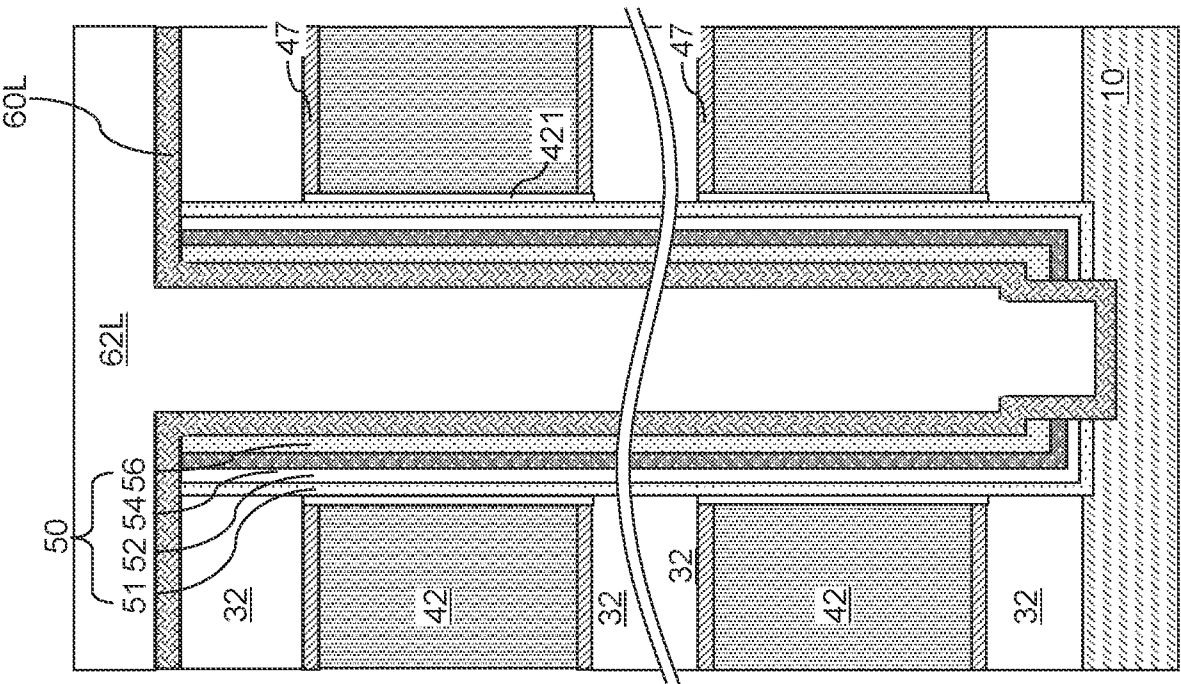


FIG. 76F

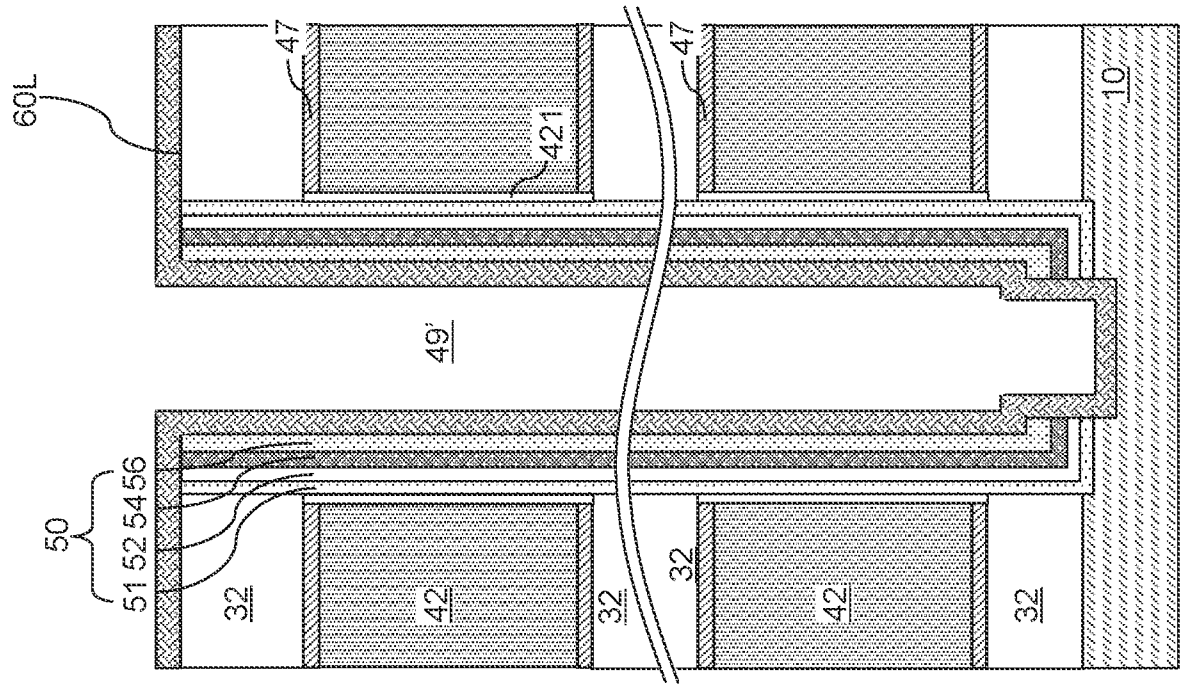


FIG. 76E

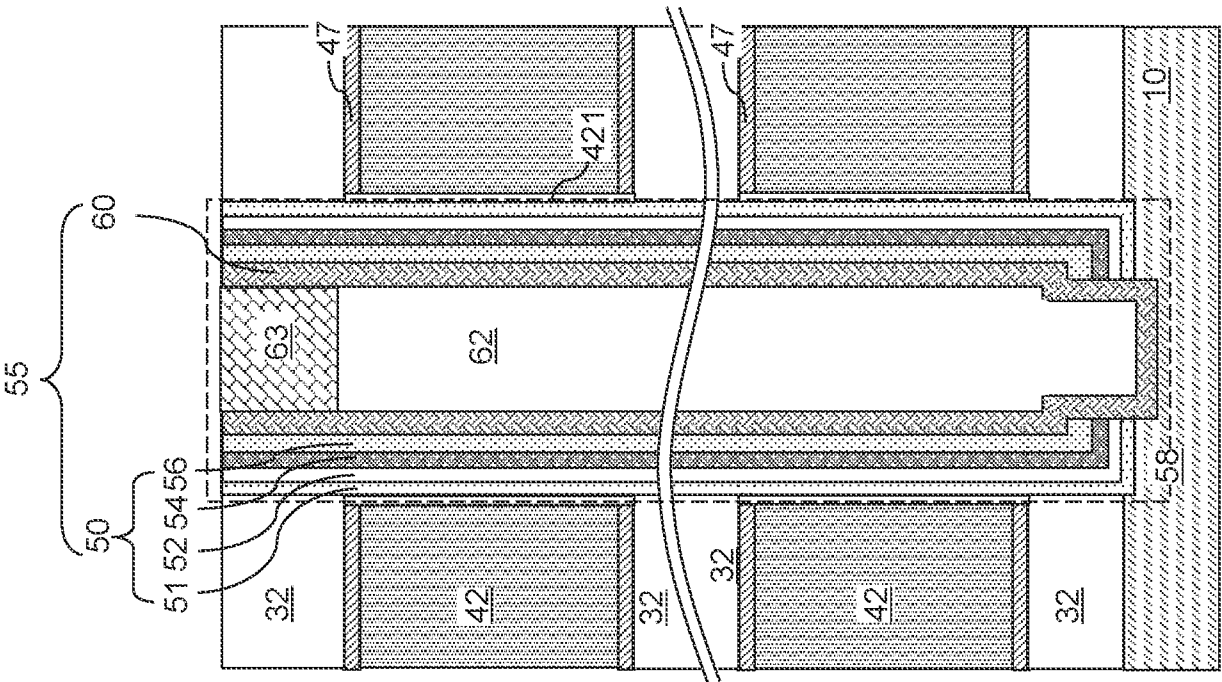


FIG. 76H

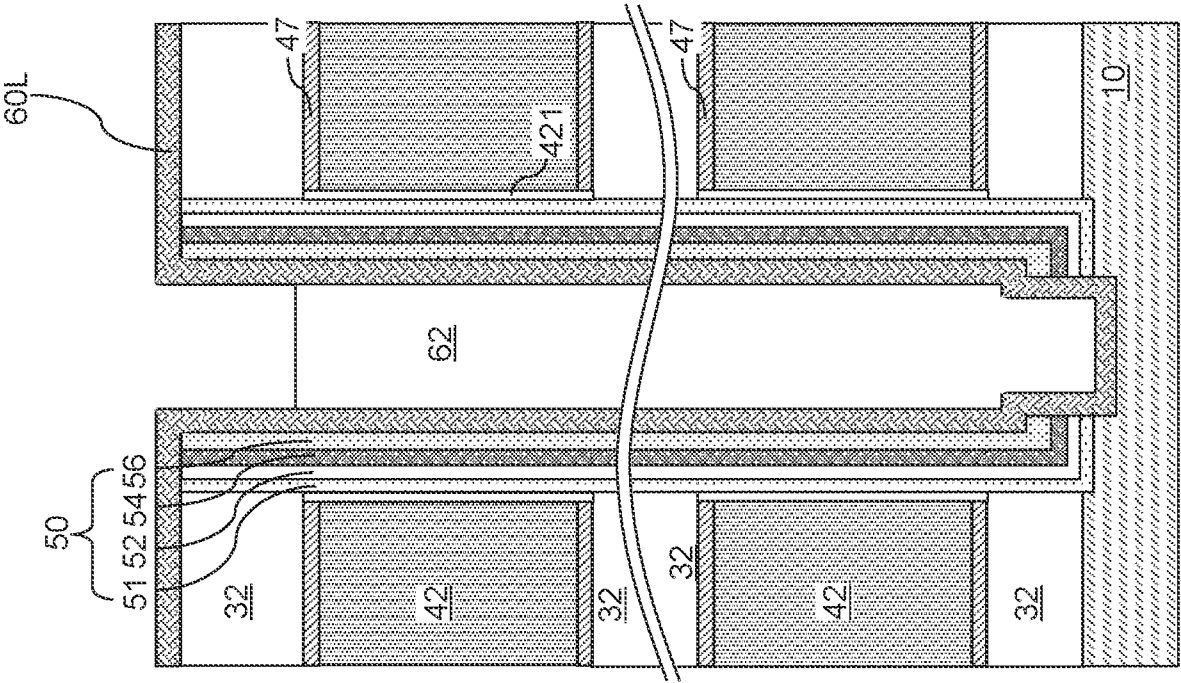


FIG. 76G

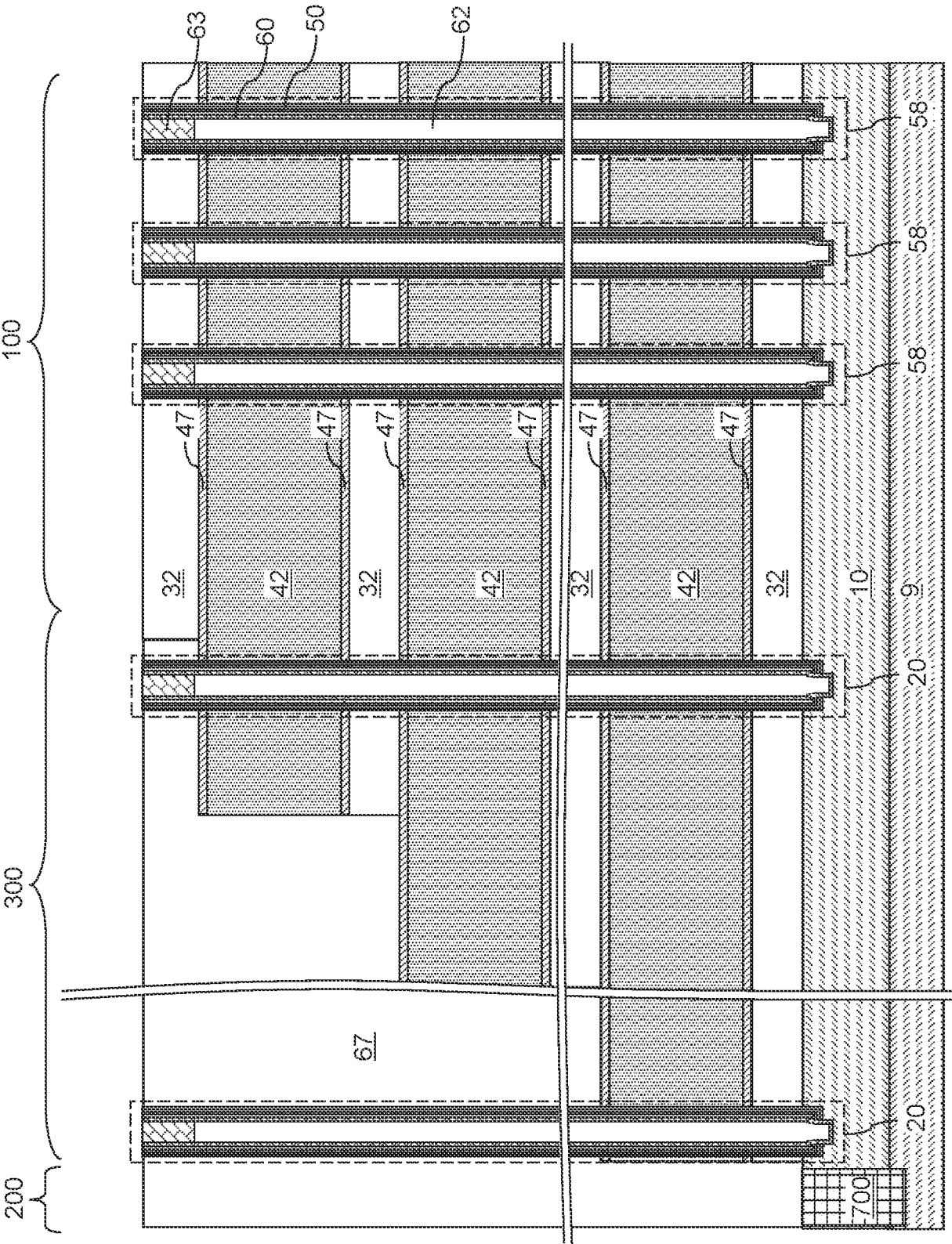


FIG. 77

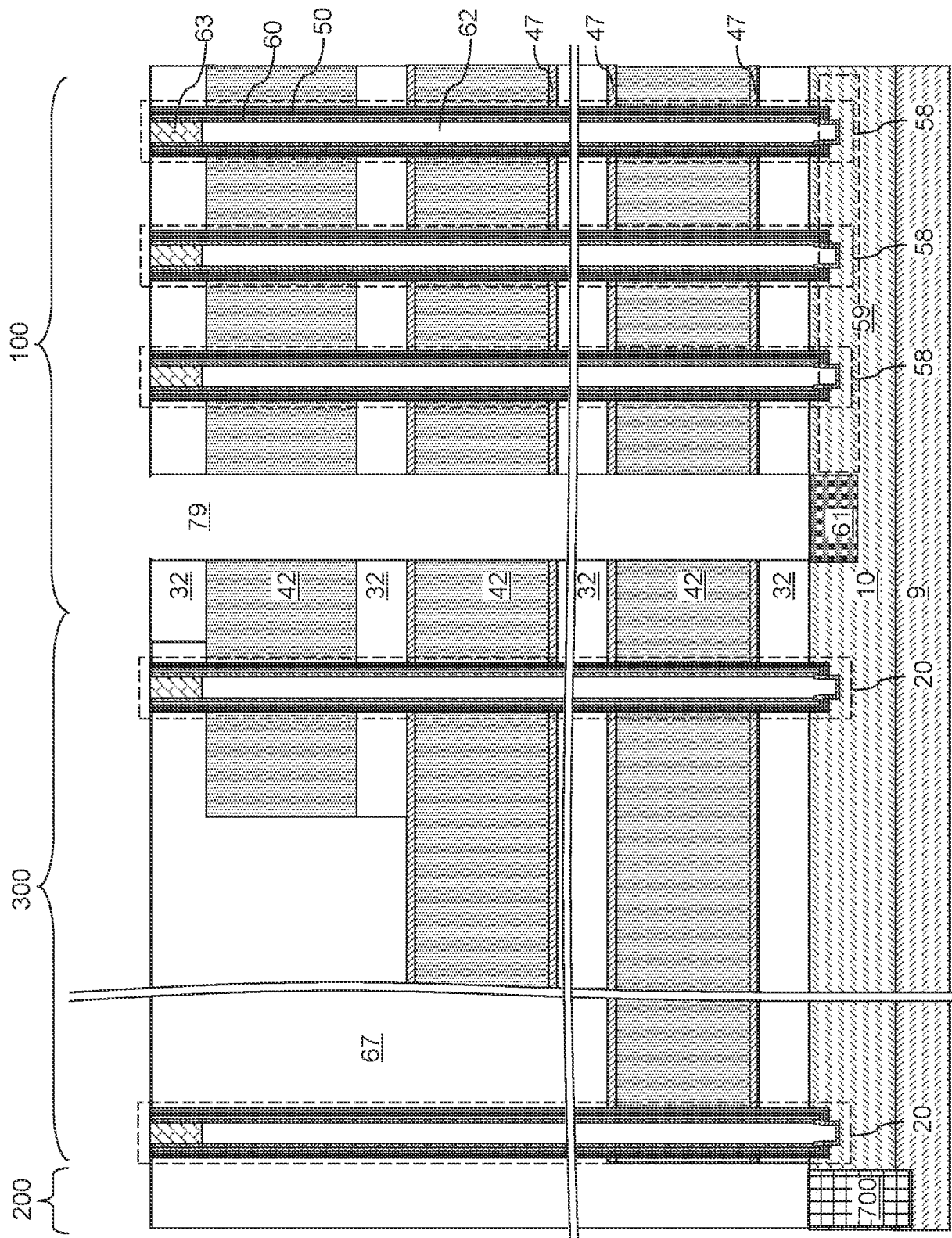


FIG. 78A

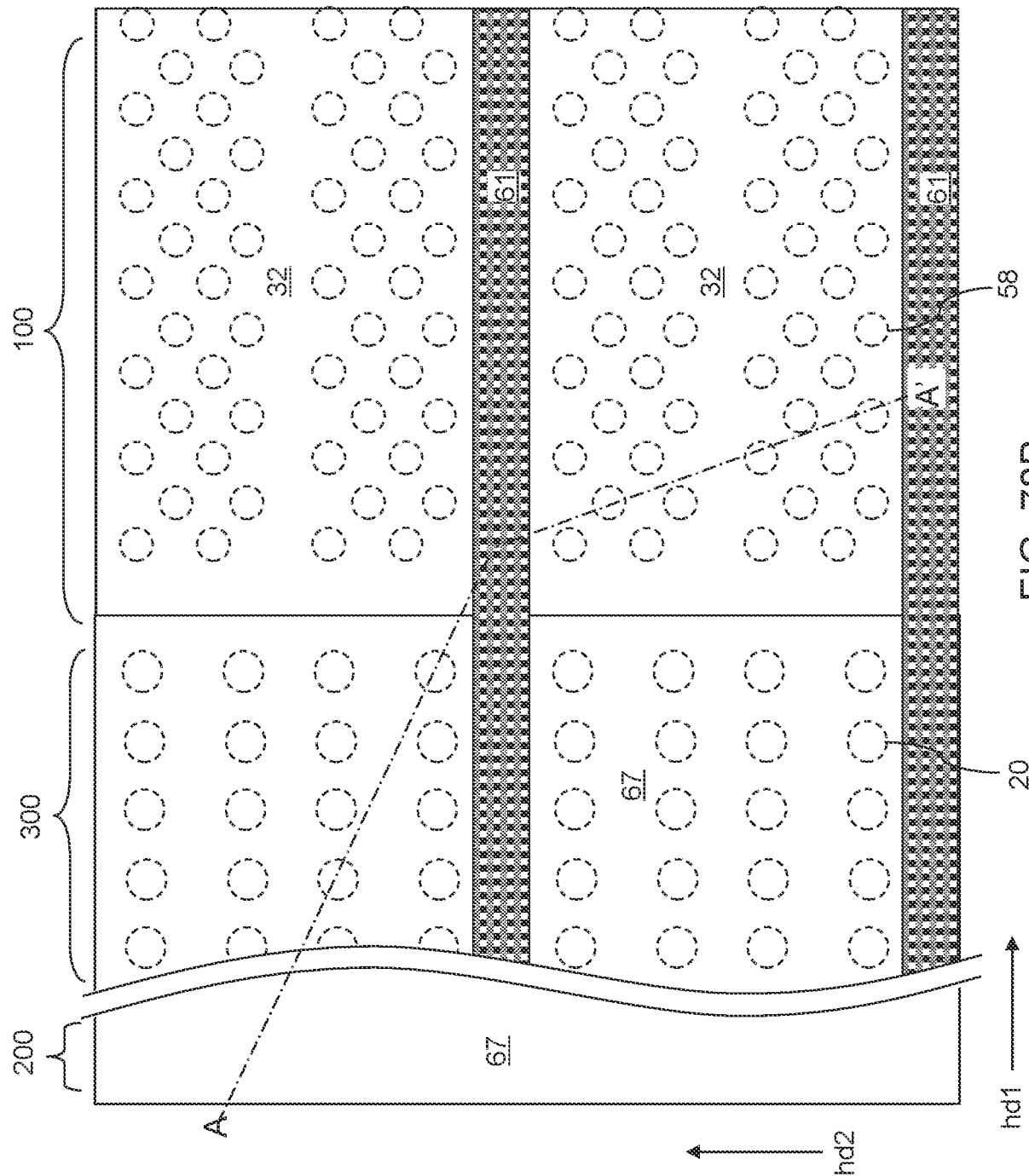


FIG. 78B

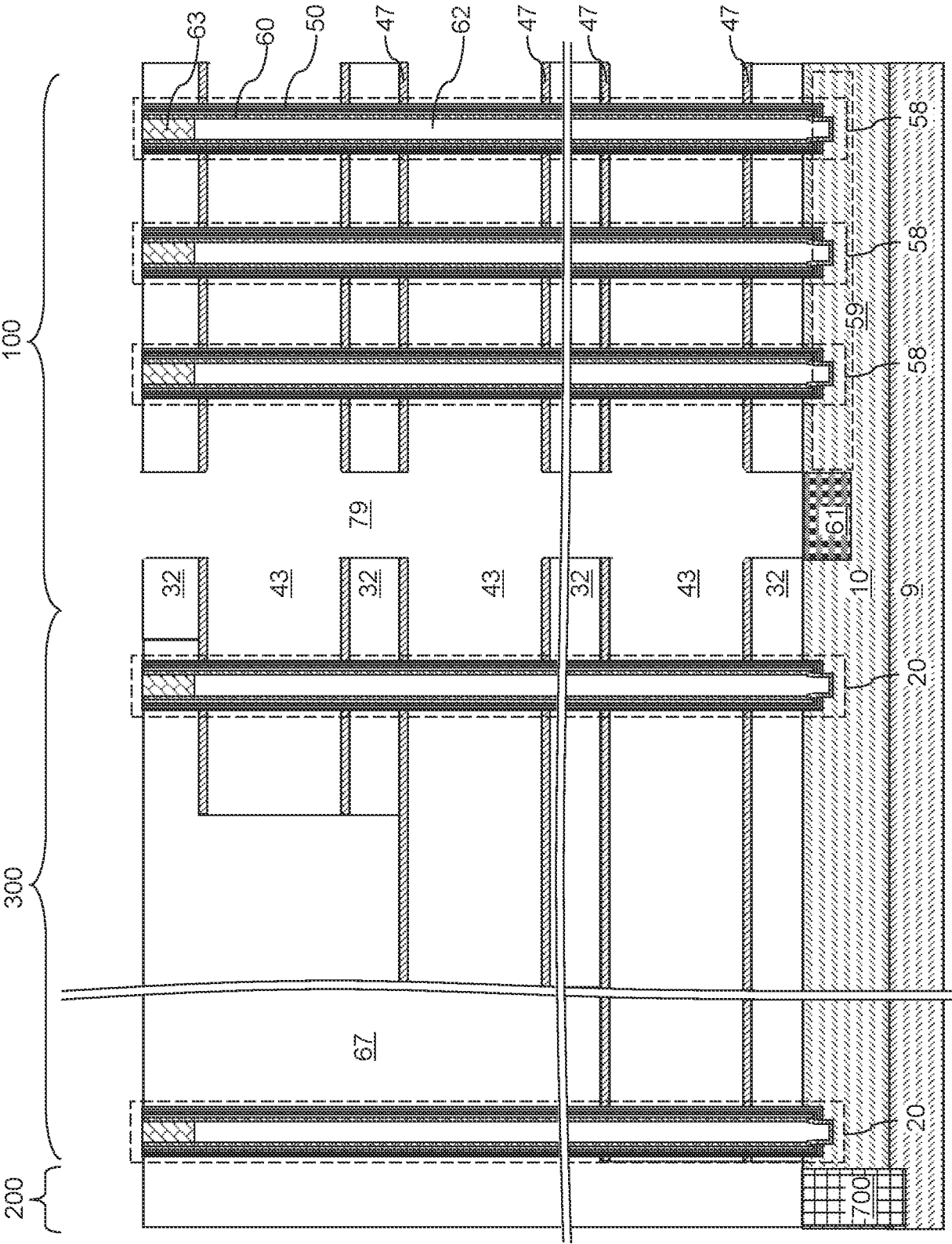


FIG. 79A

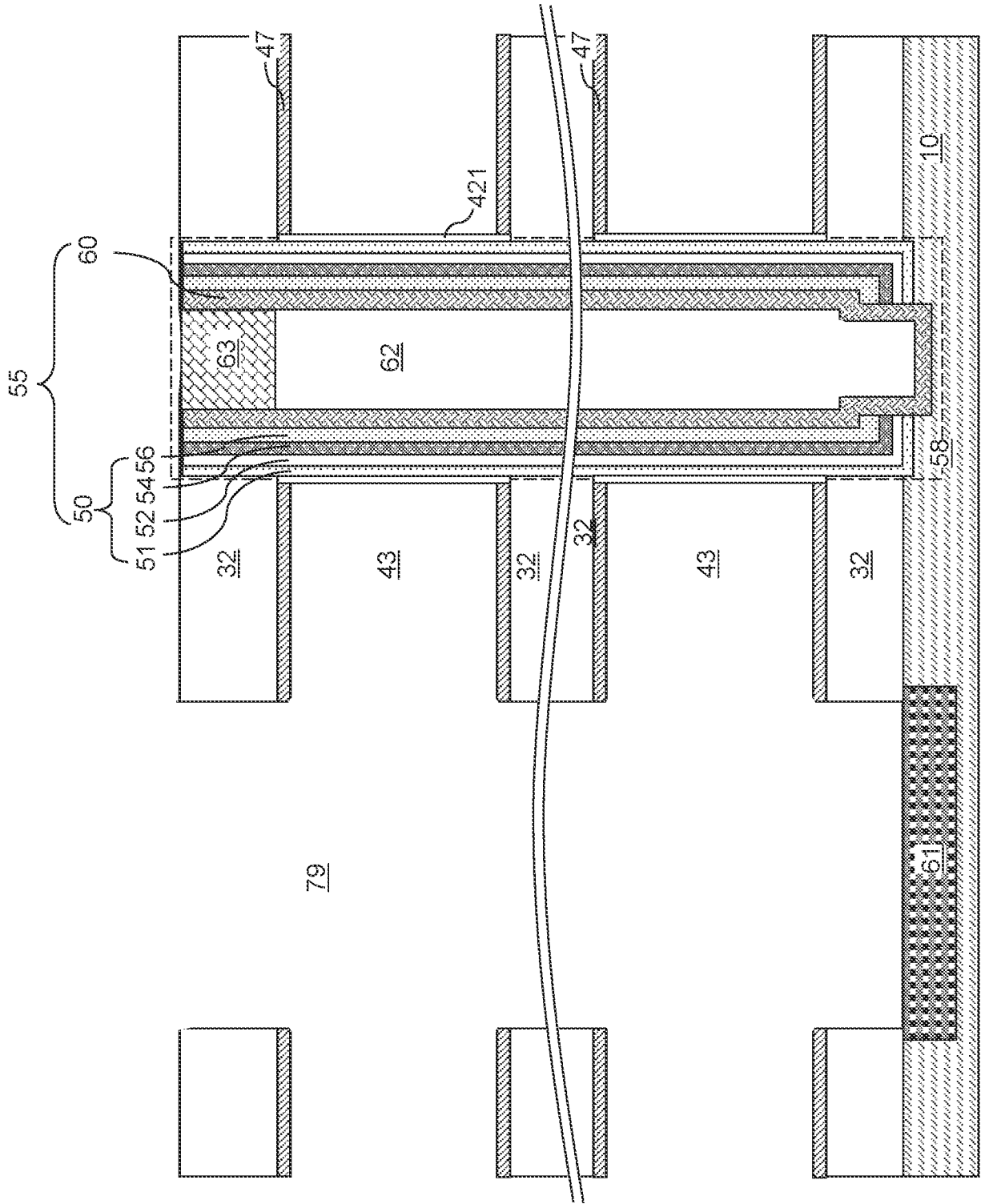


FIG. 79B

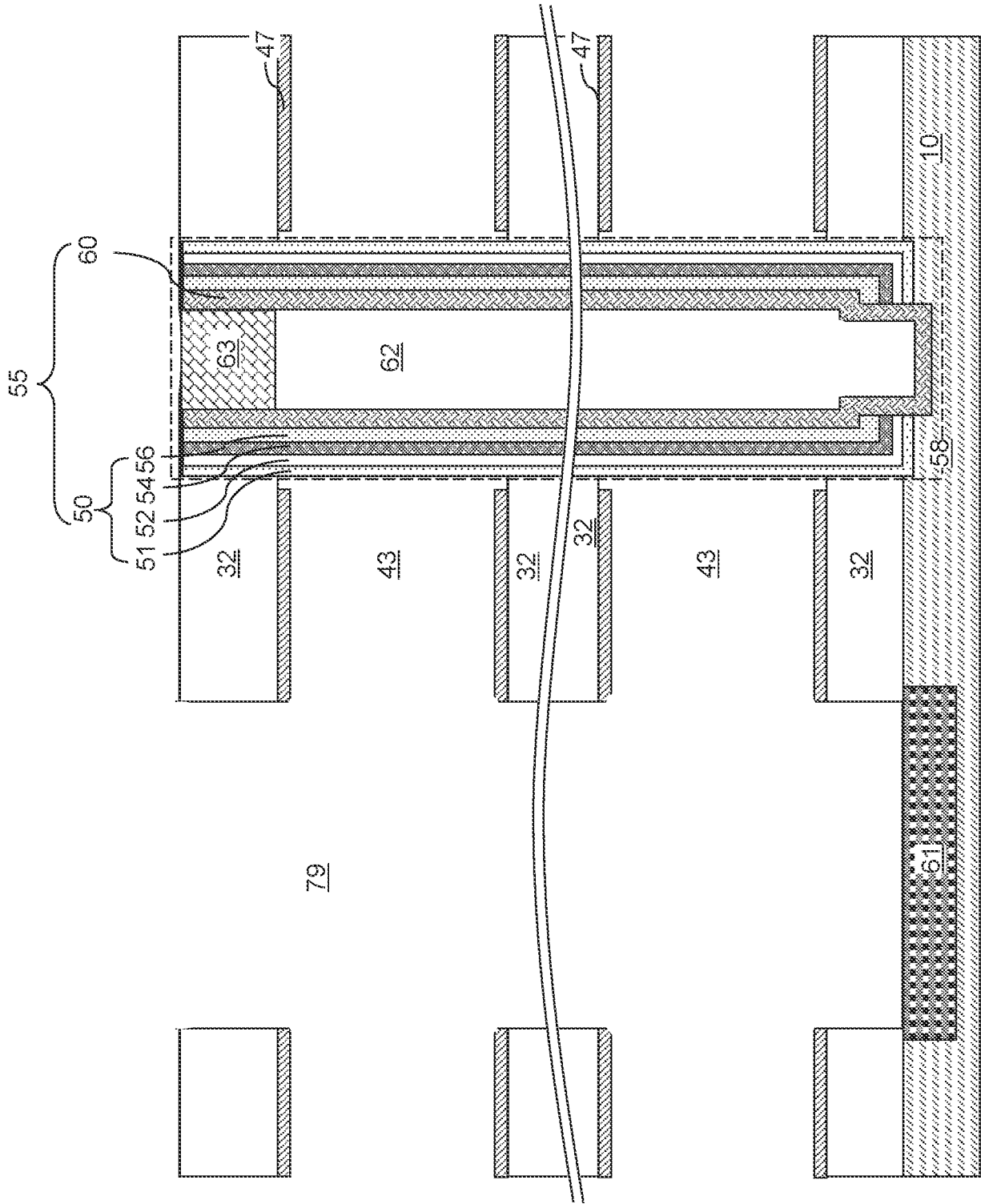


FIG. 80A

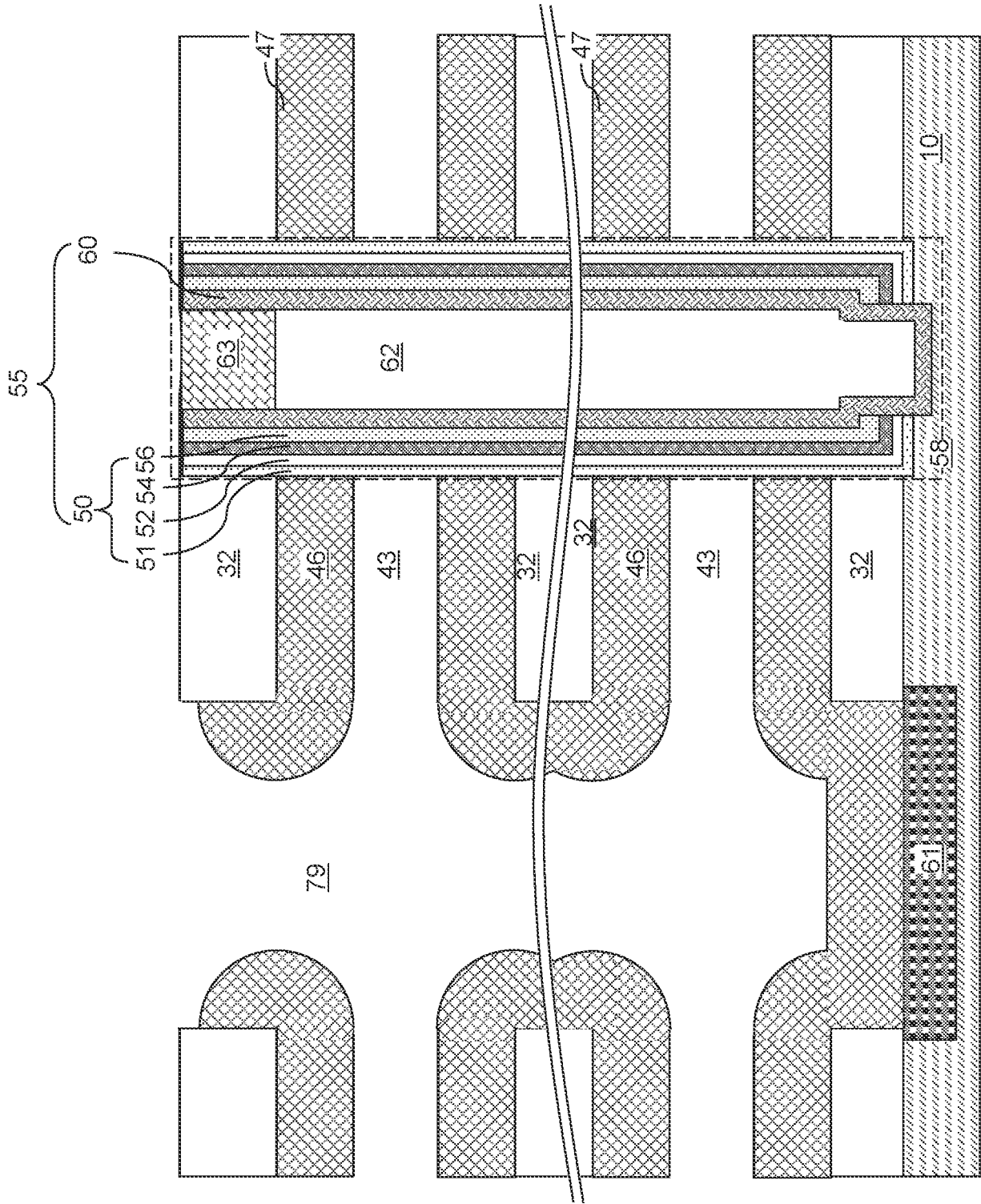


FIG. 80B

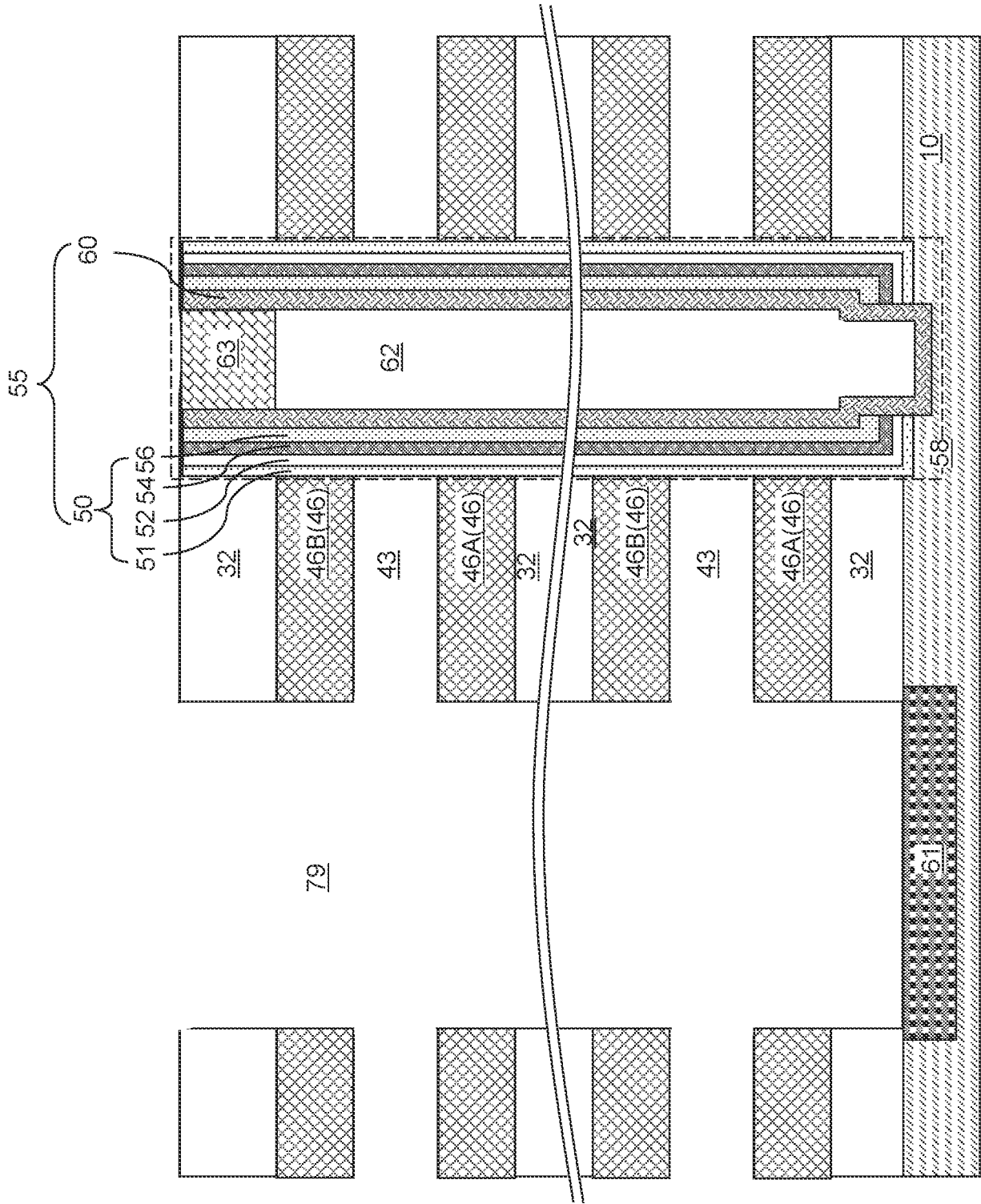
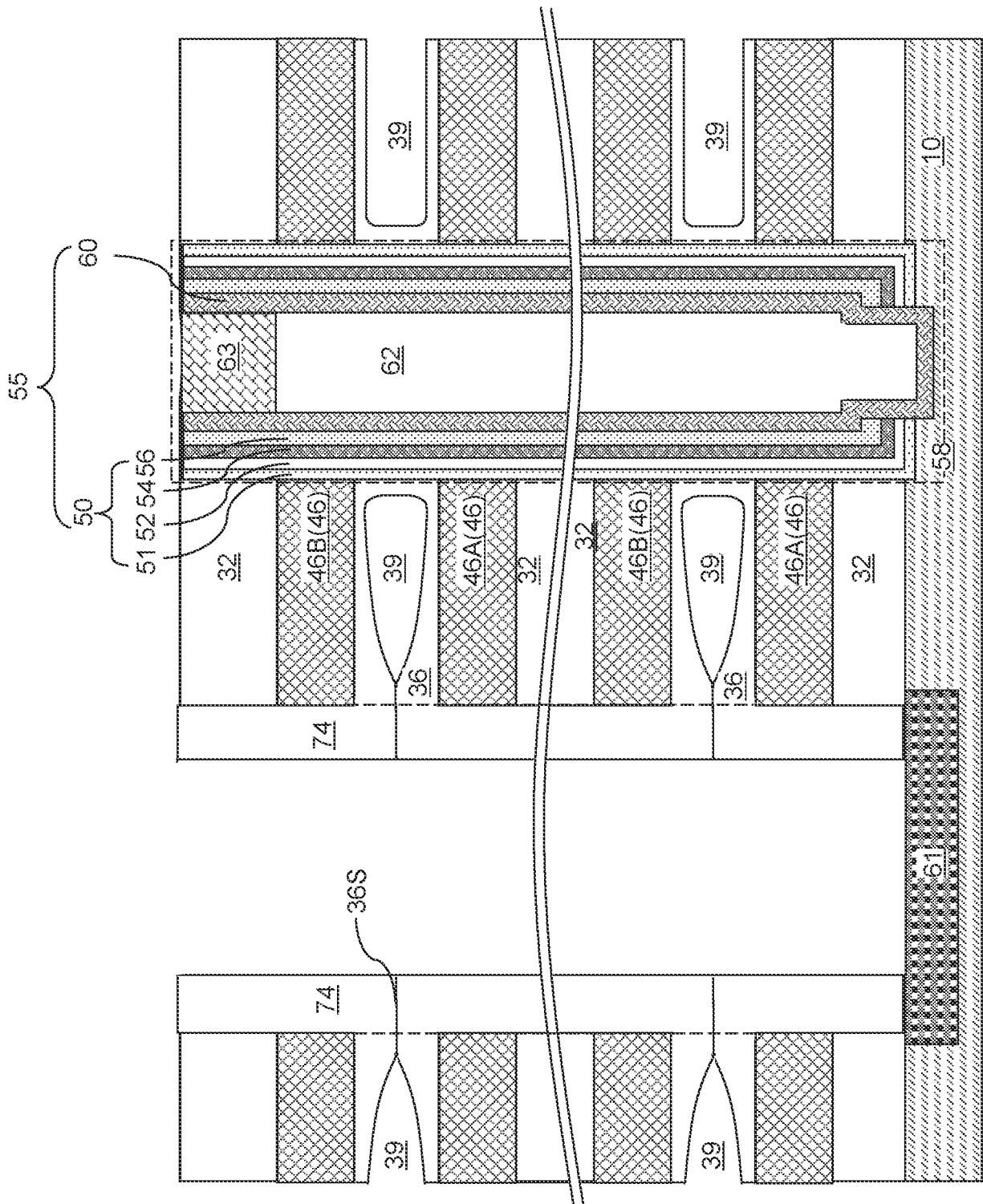


FIG. 80C



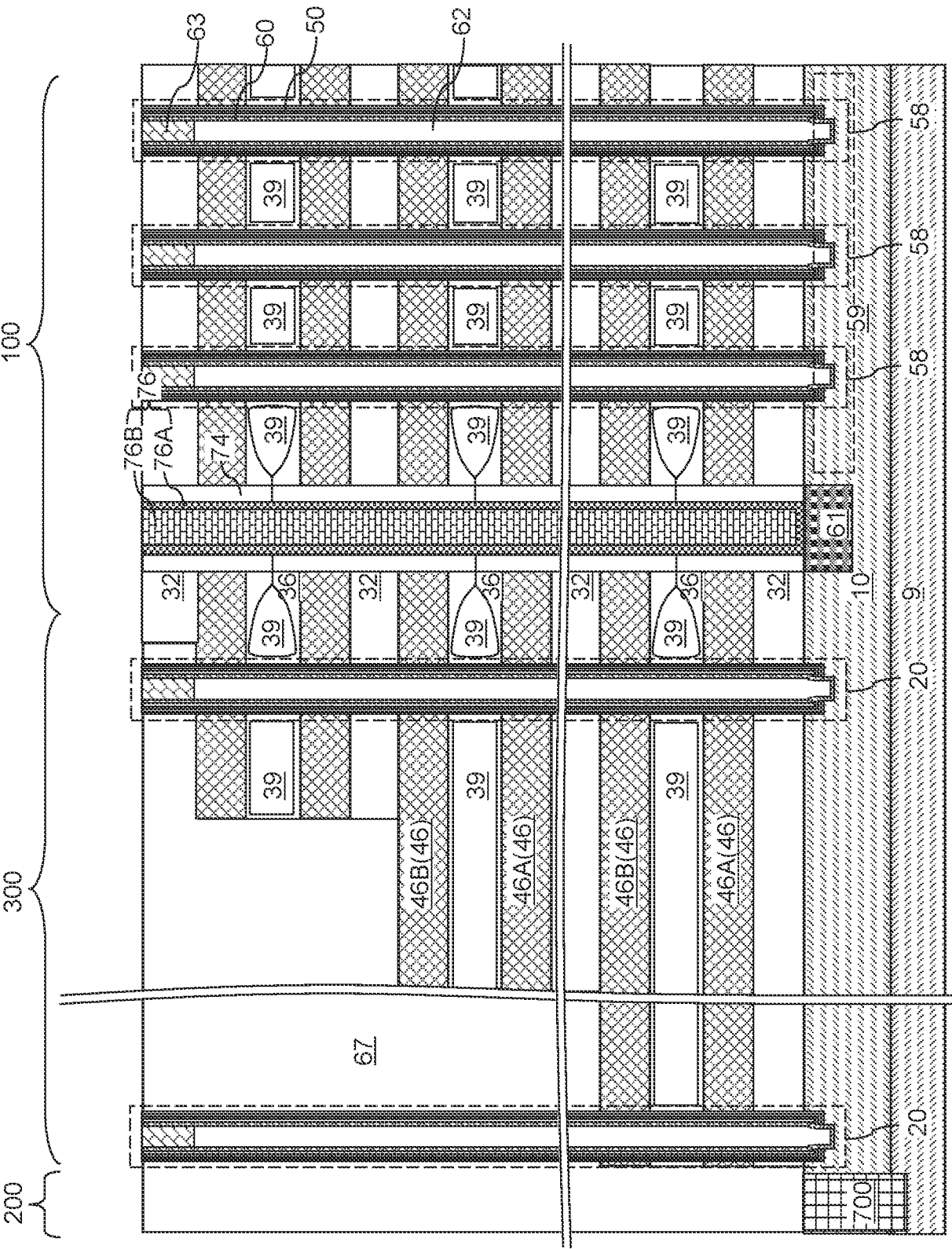


FIG. 81A

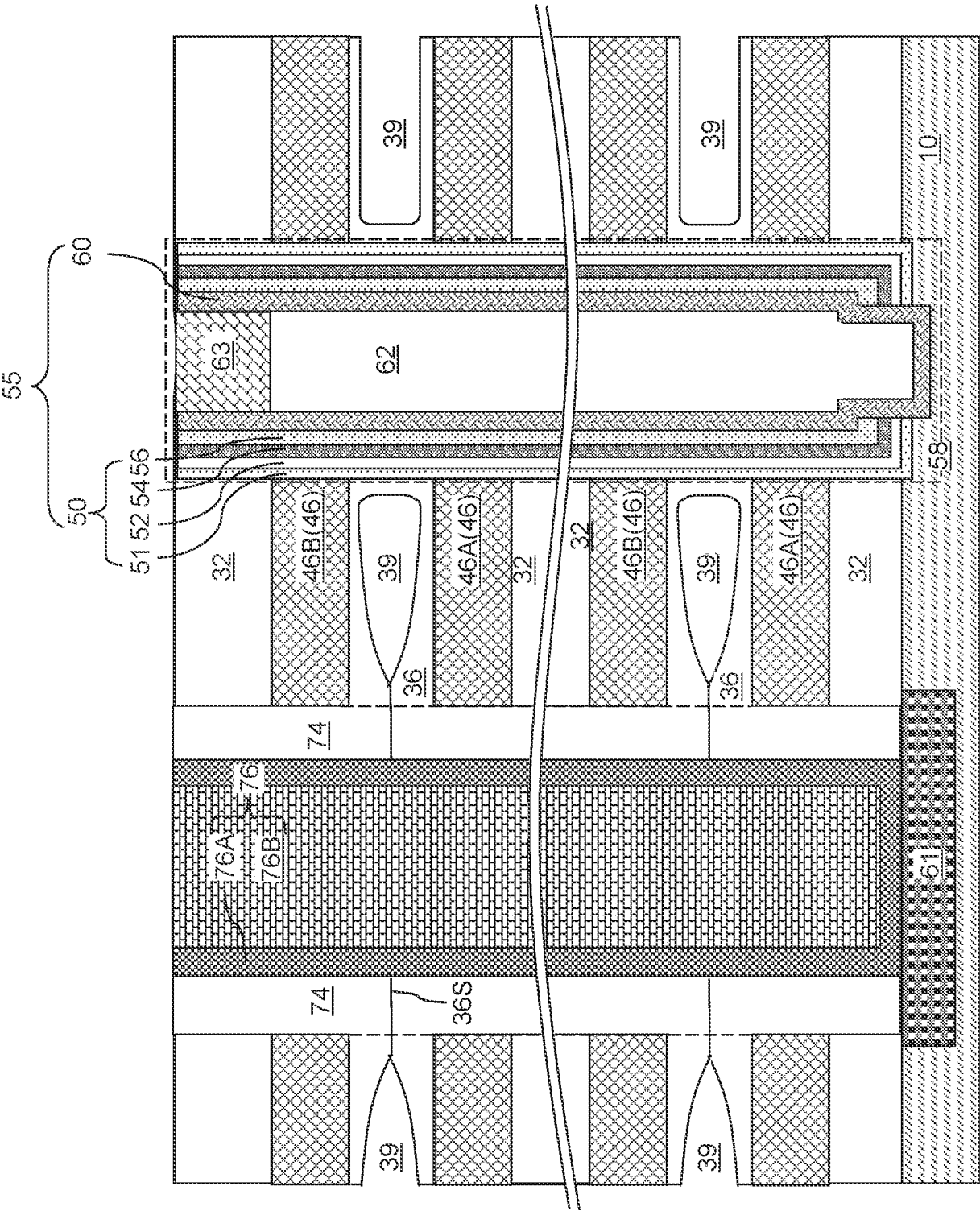


FIG. 81B

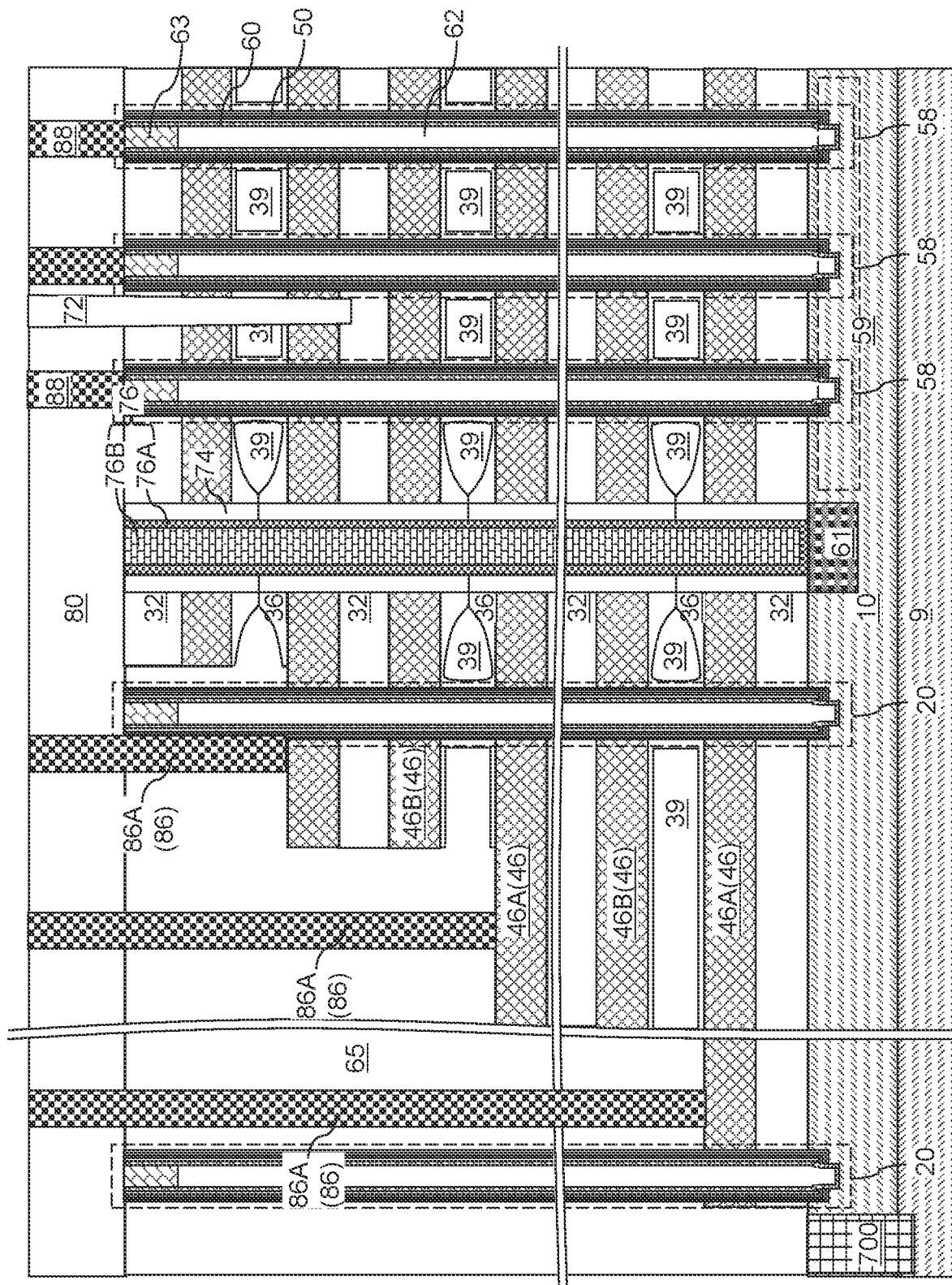
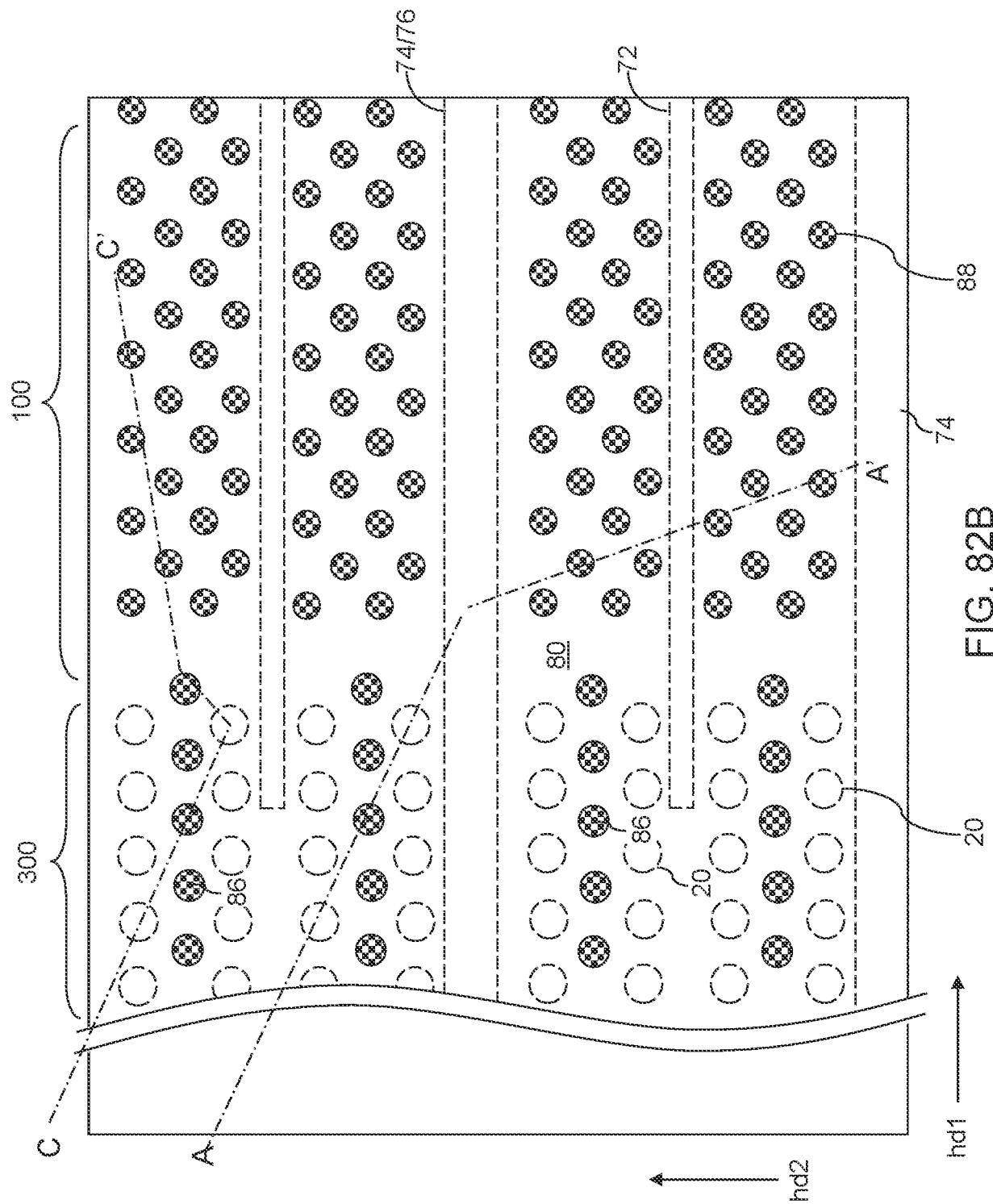


FIG. 82A



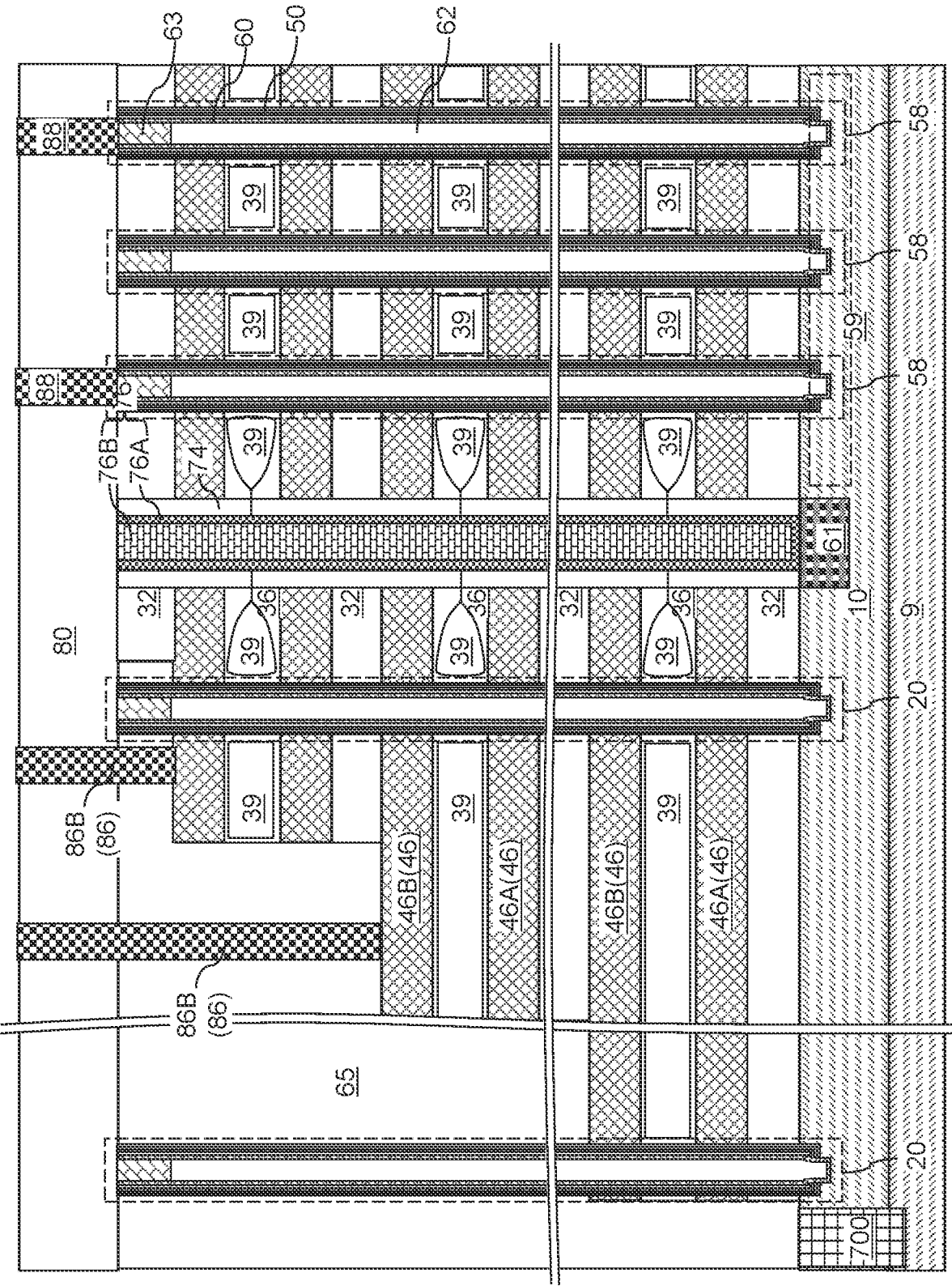


FIG. 82C

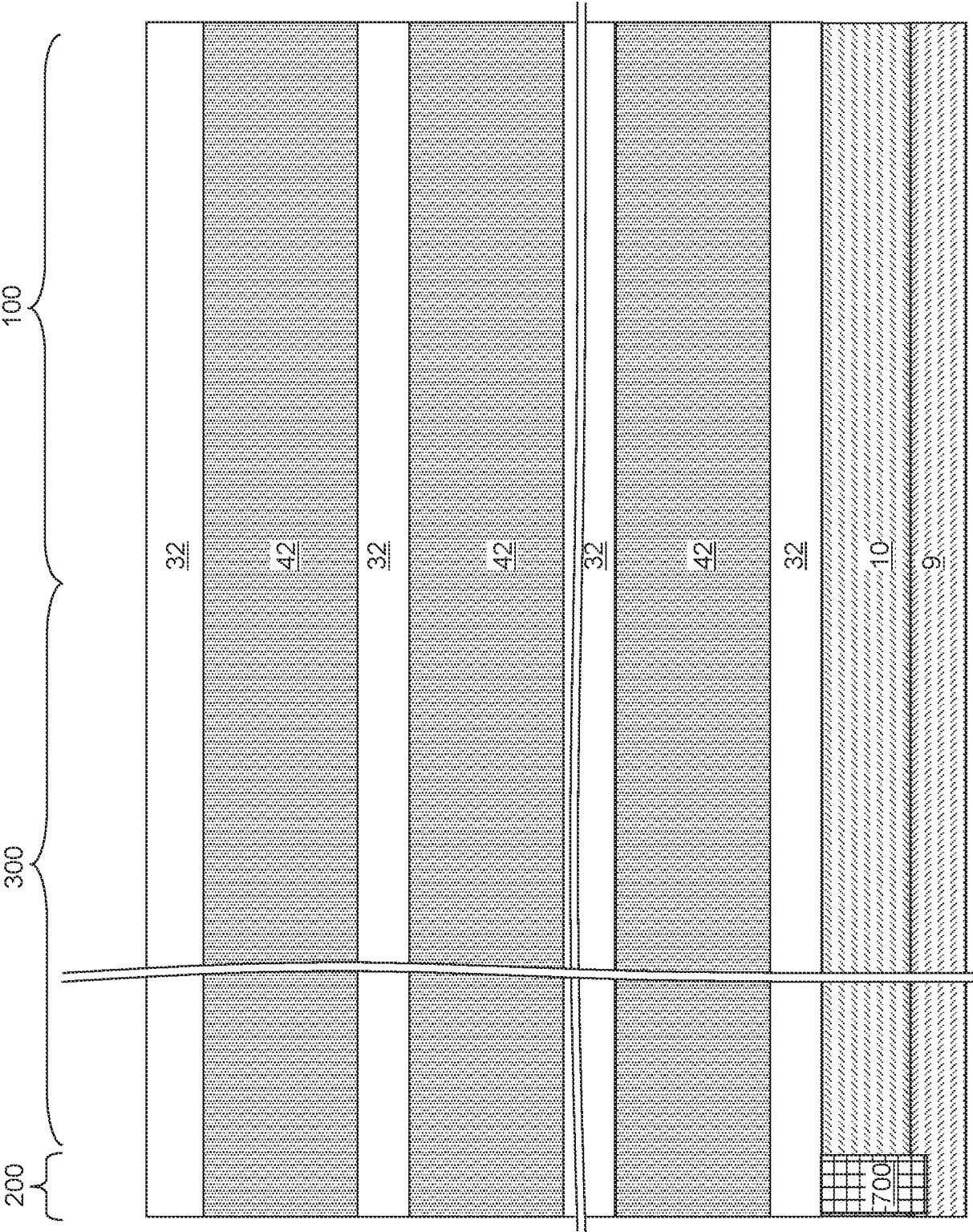


FIG. 83

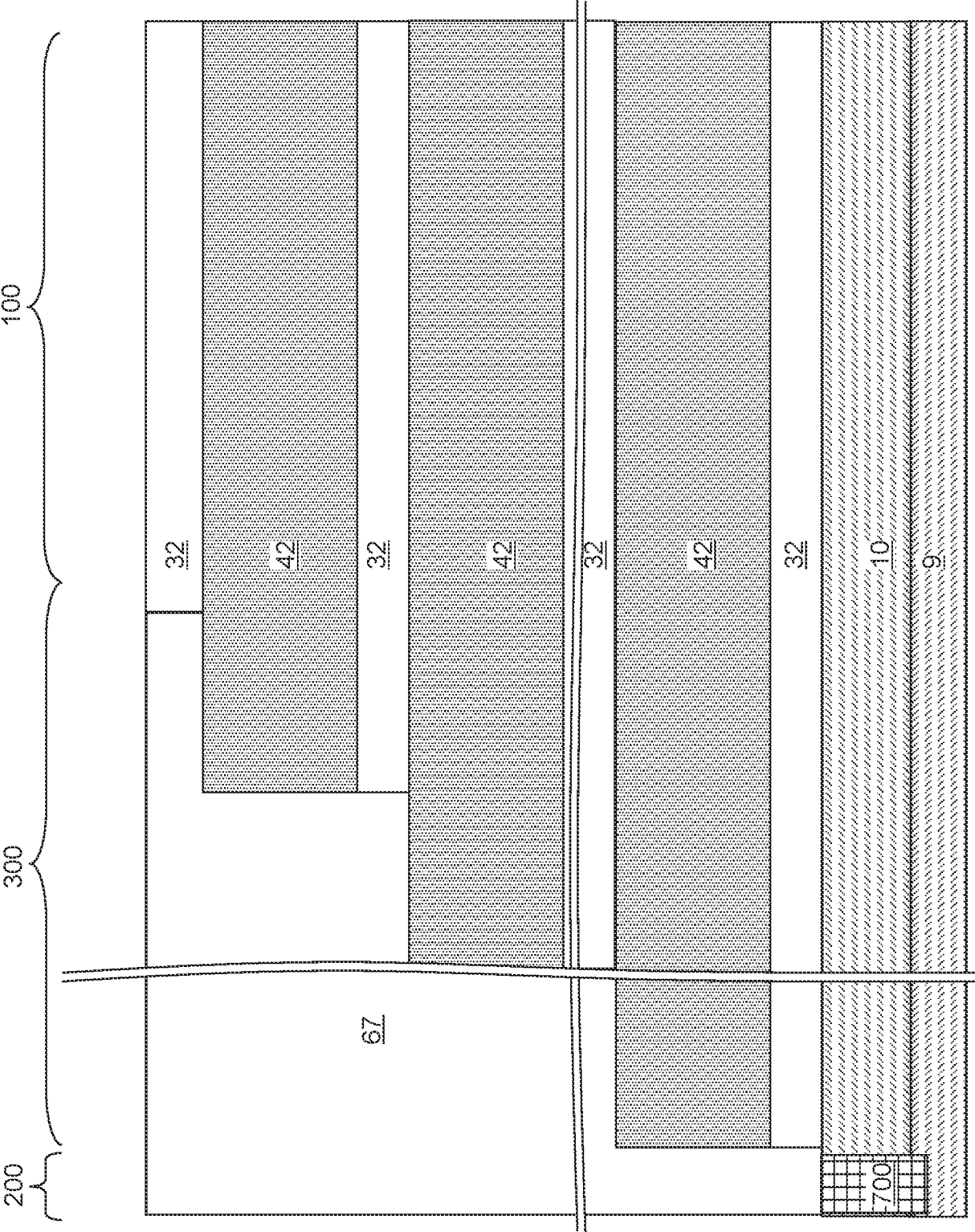


FIG. 84

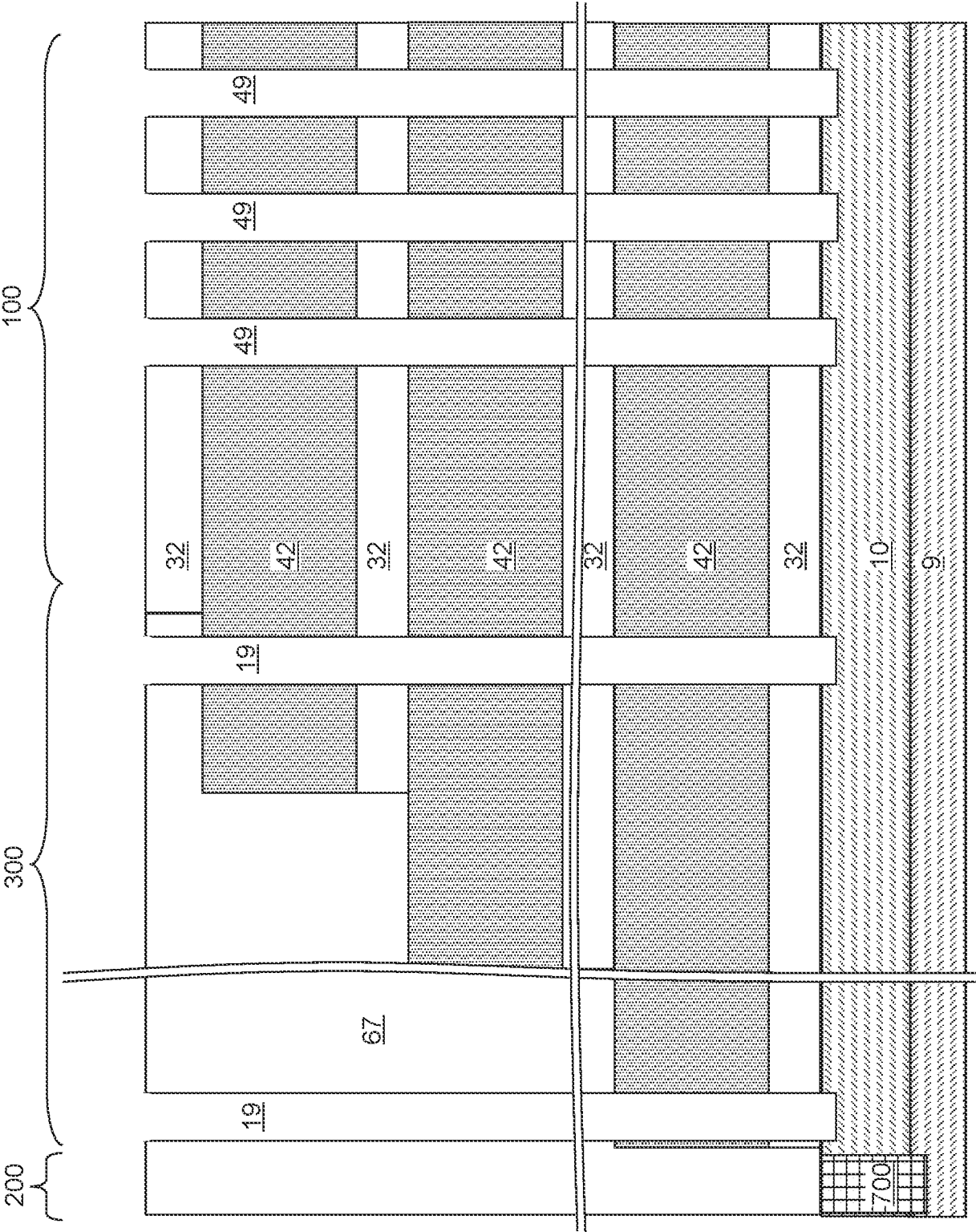
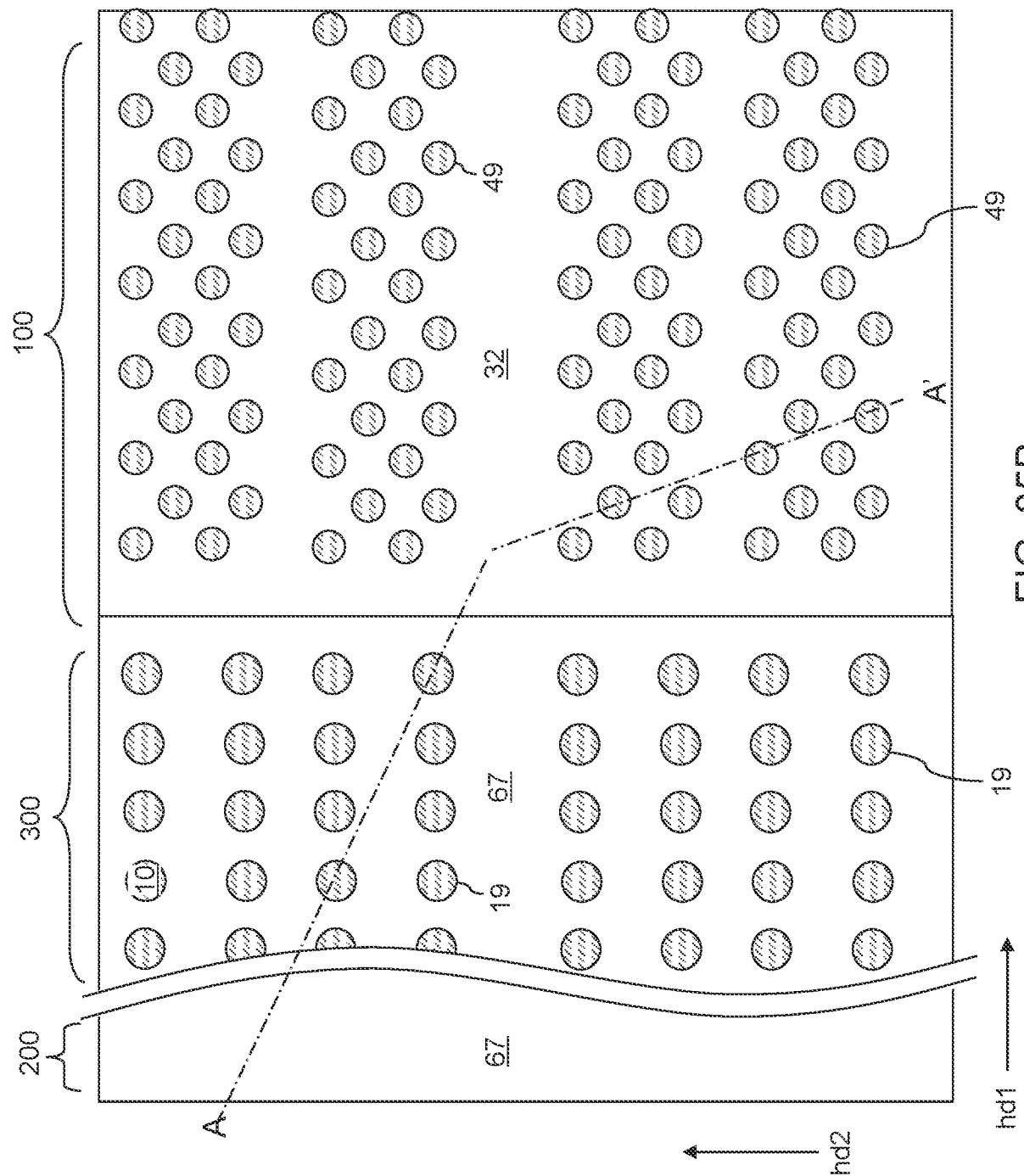


FIG. 85A



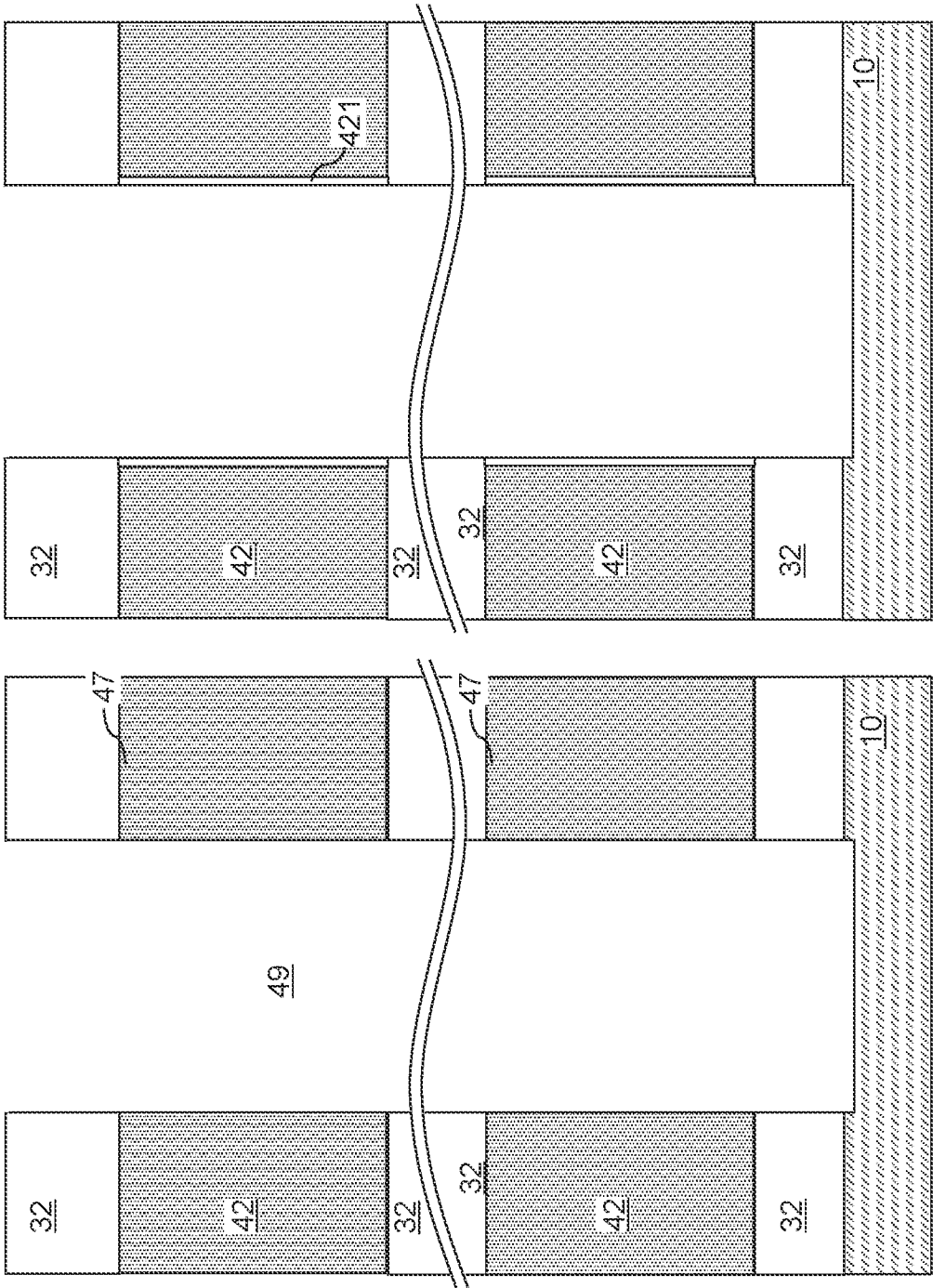


FIG. 86B

FIG. 86A

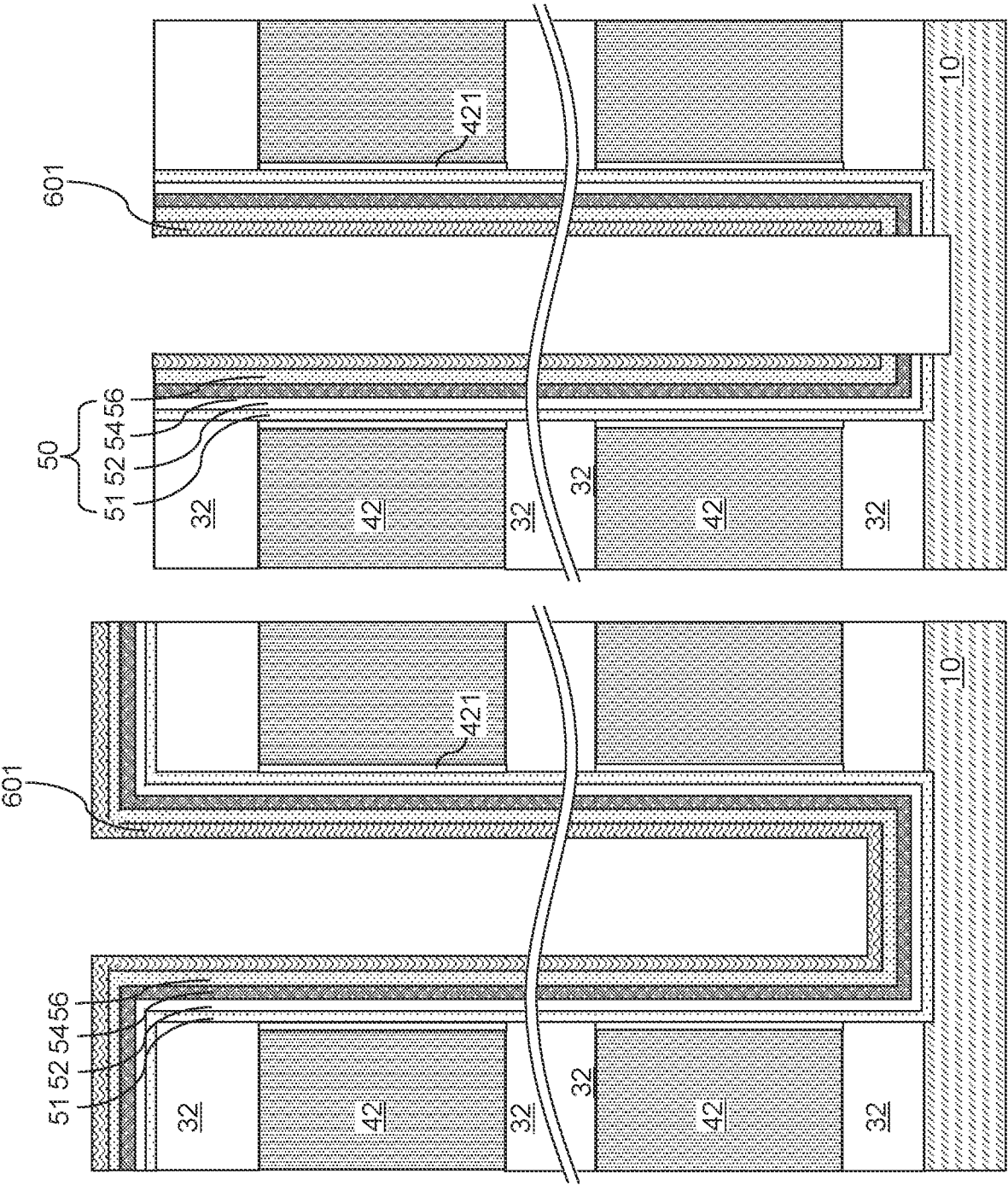


FIG. 86D

FIG. 86C

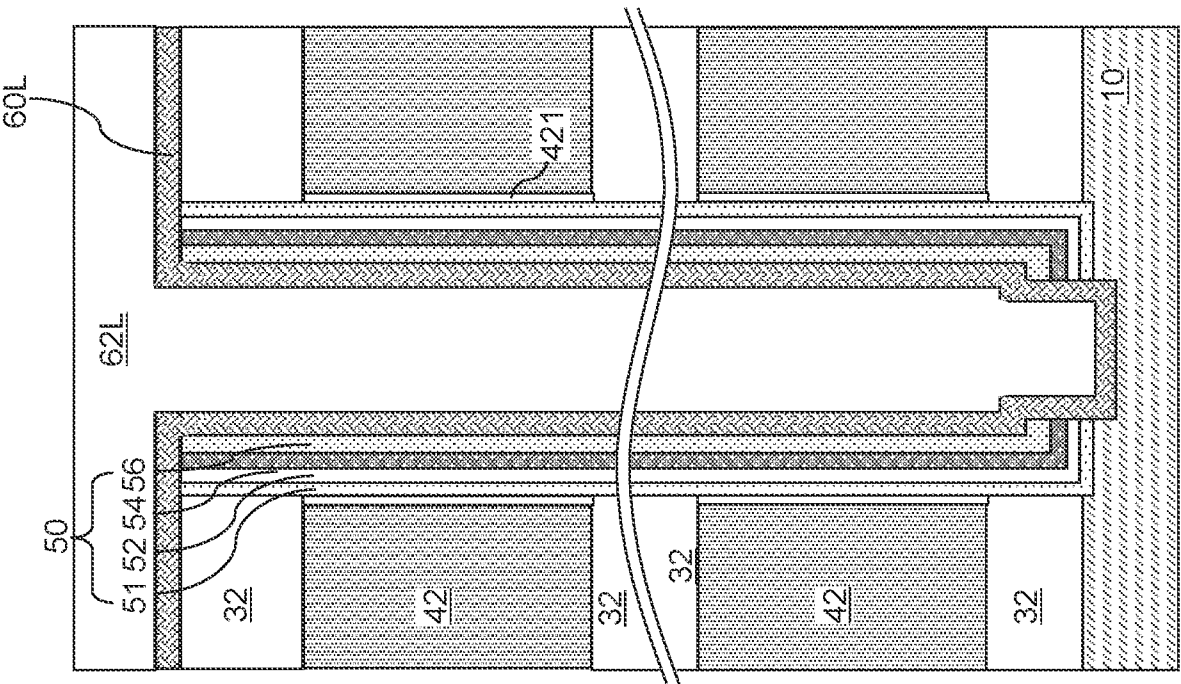


FIG. 86F

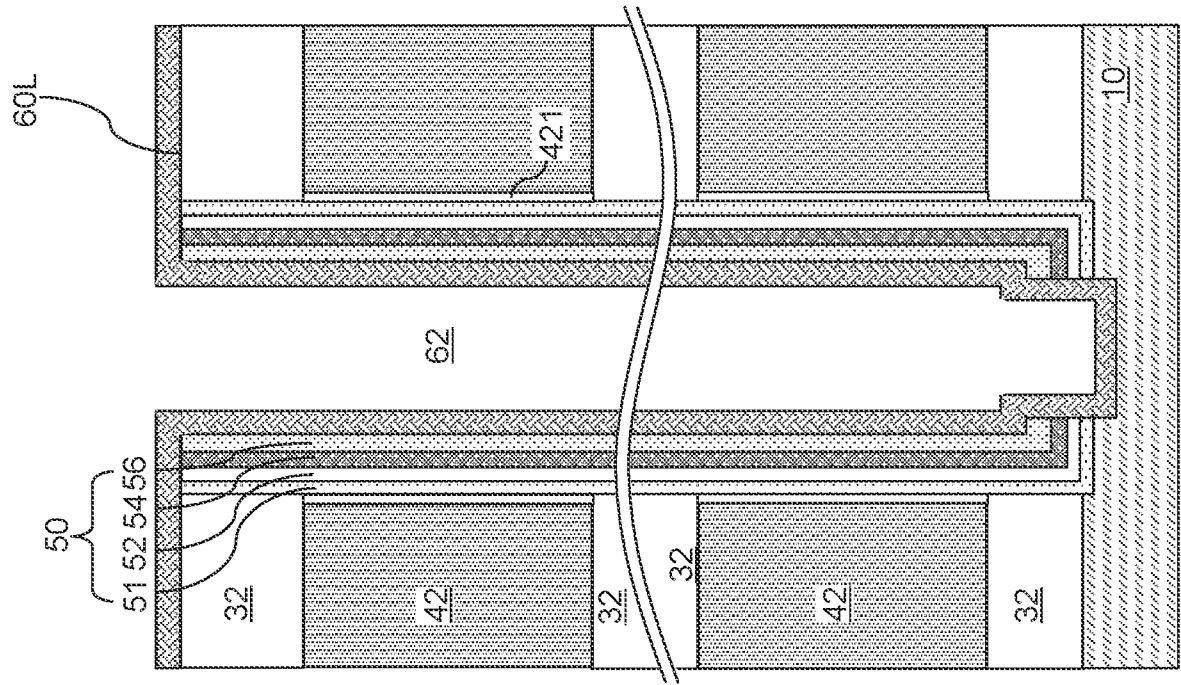


FIG. 86E

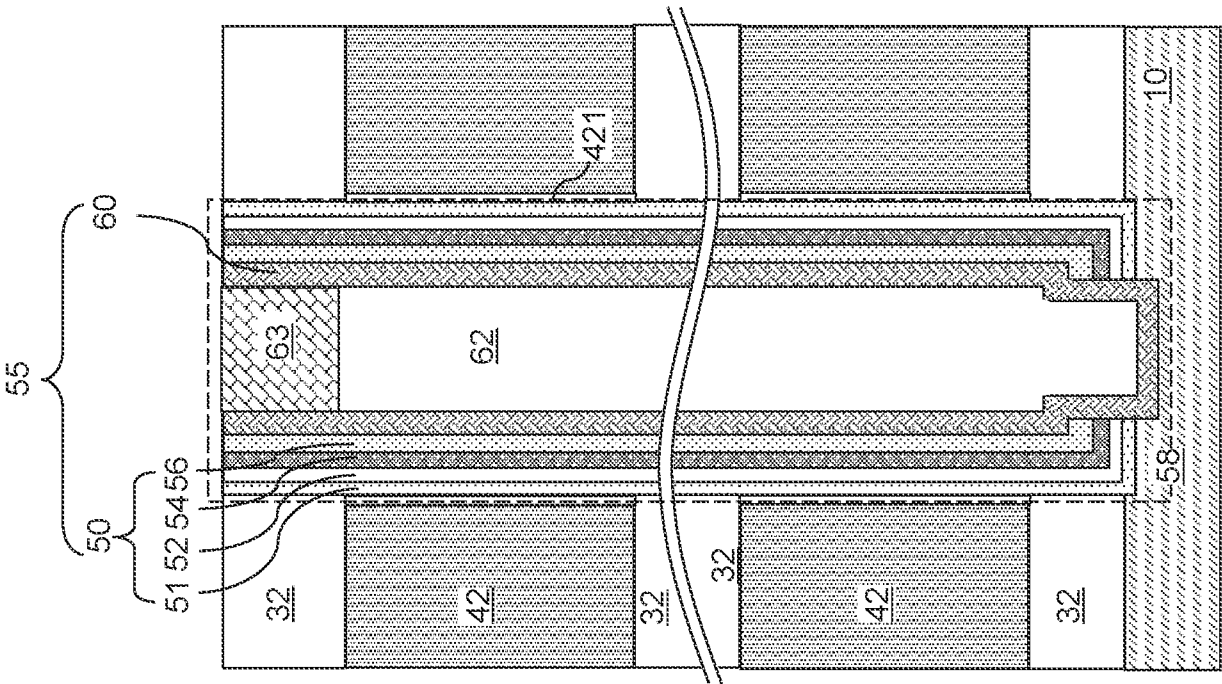


FIG. 86H

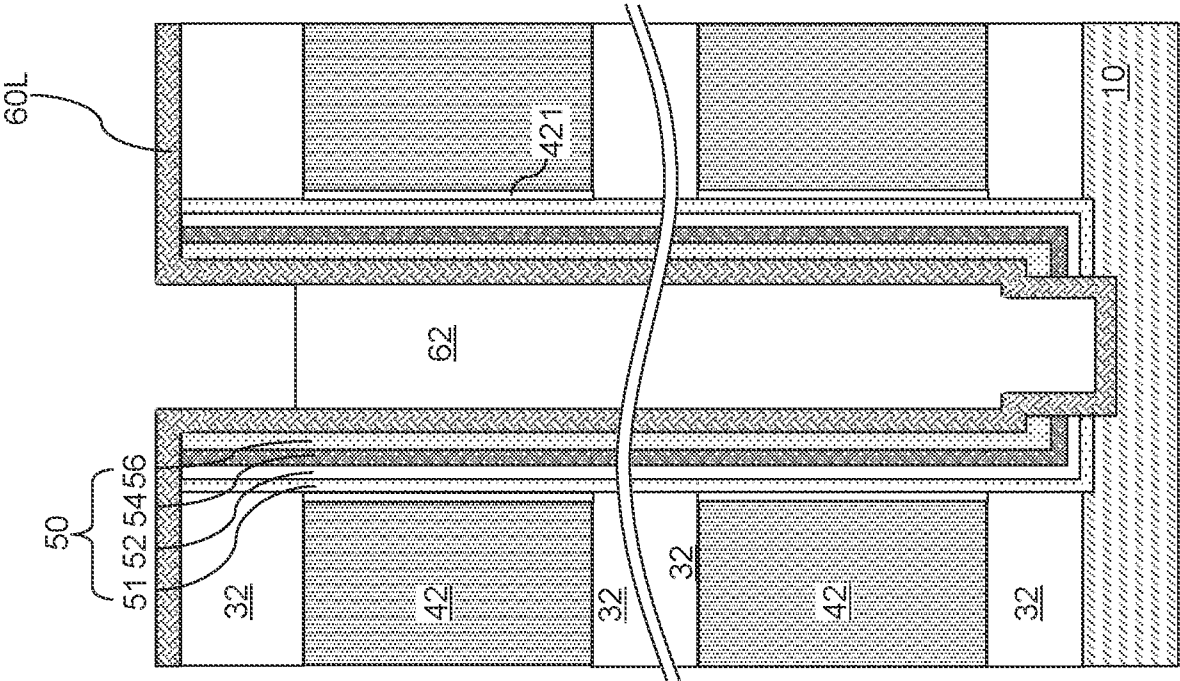


FIG. 86G

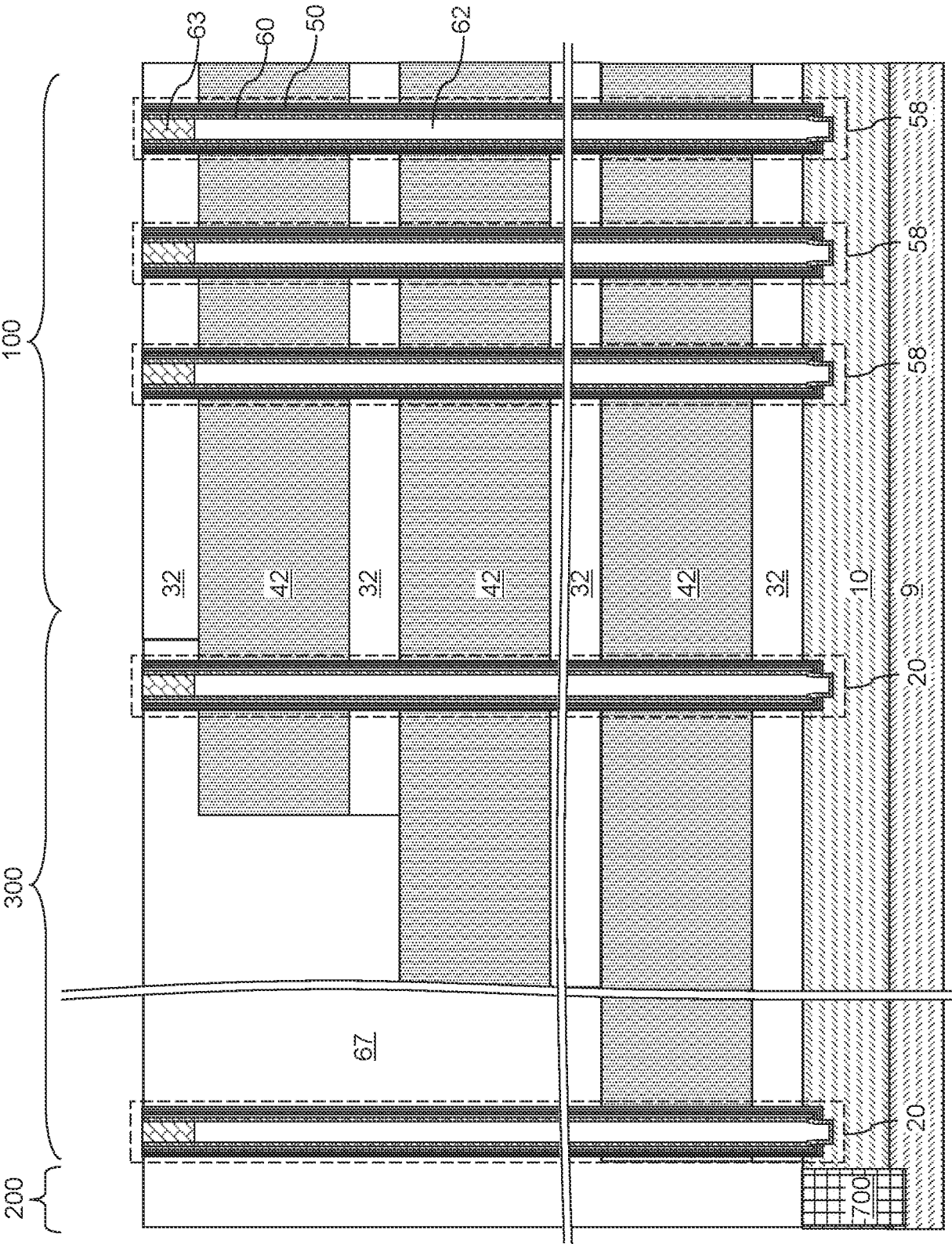


FIG. 87

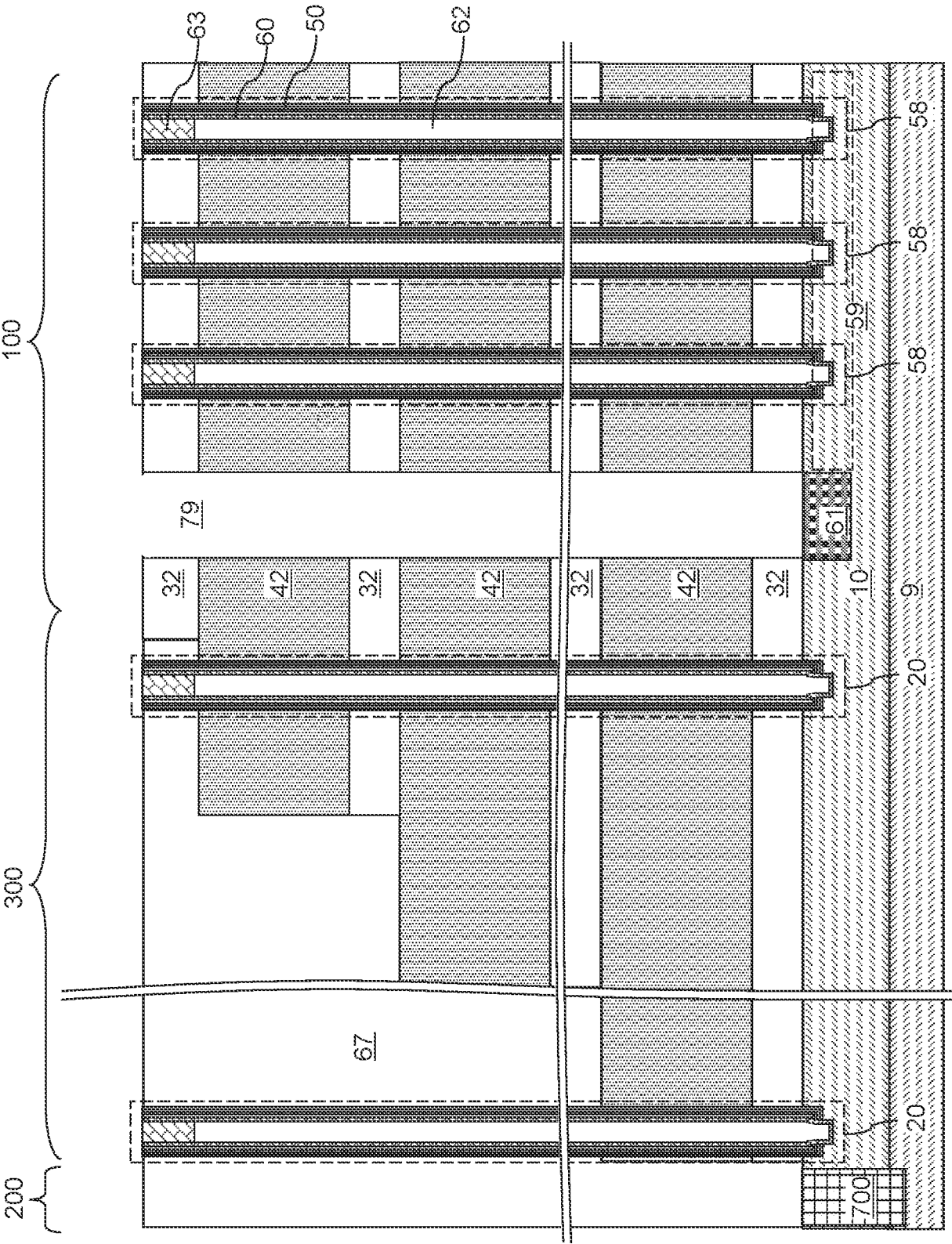


FIG. 88A

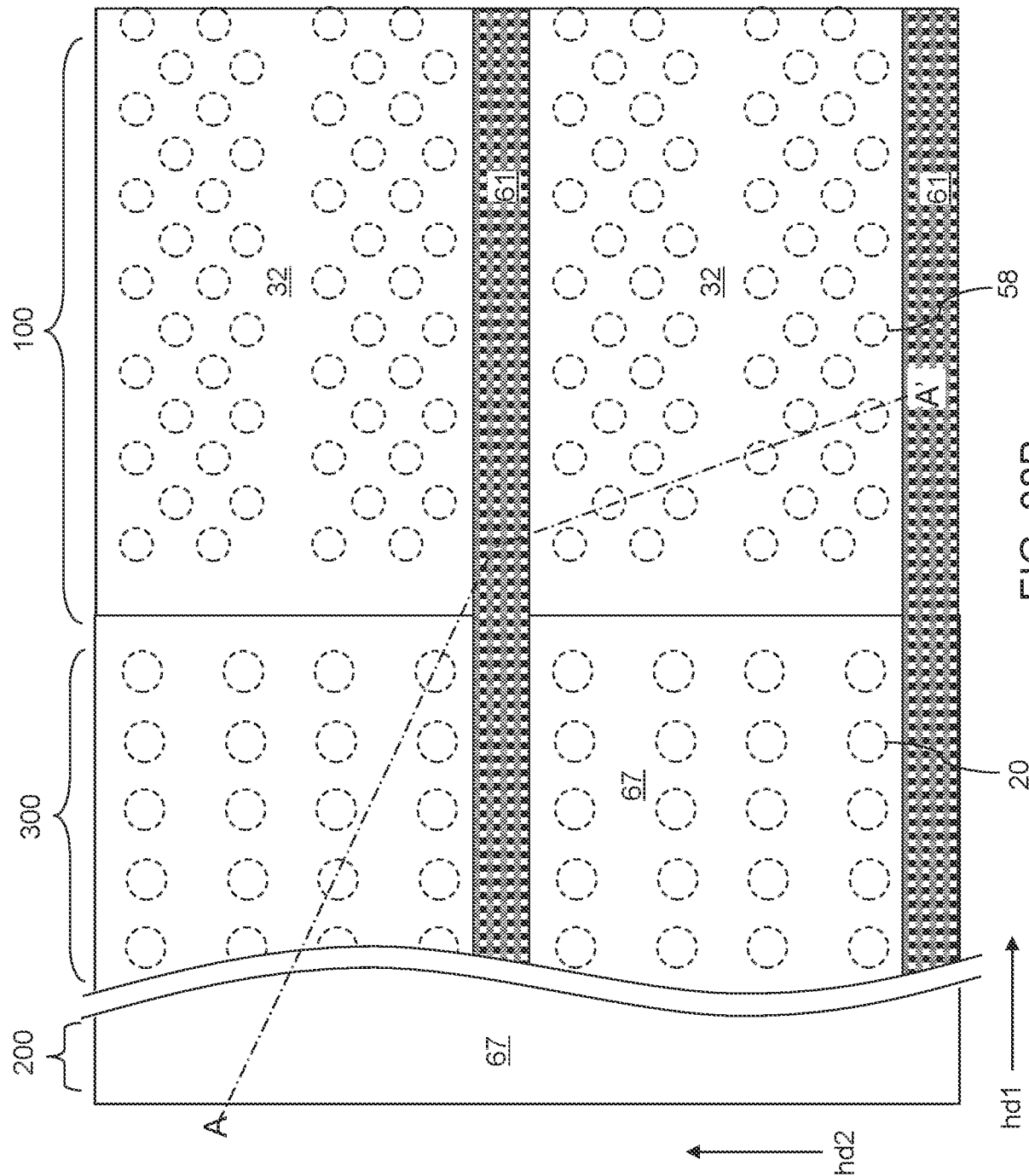
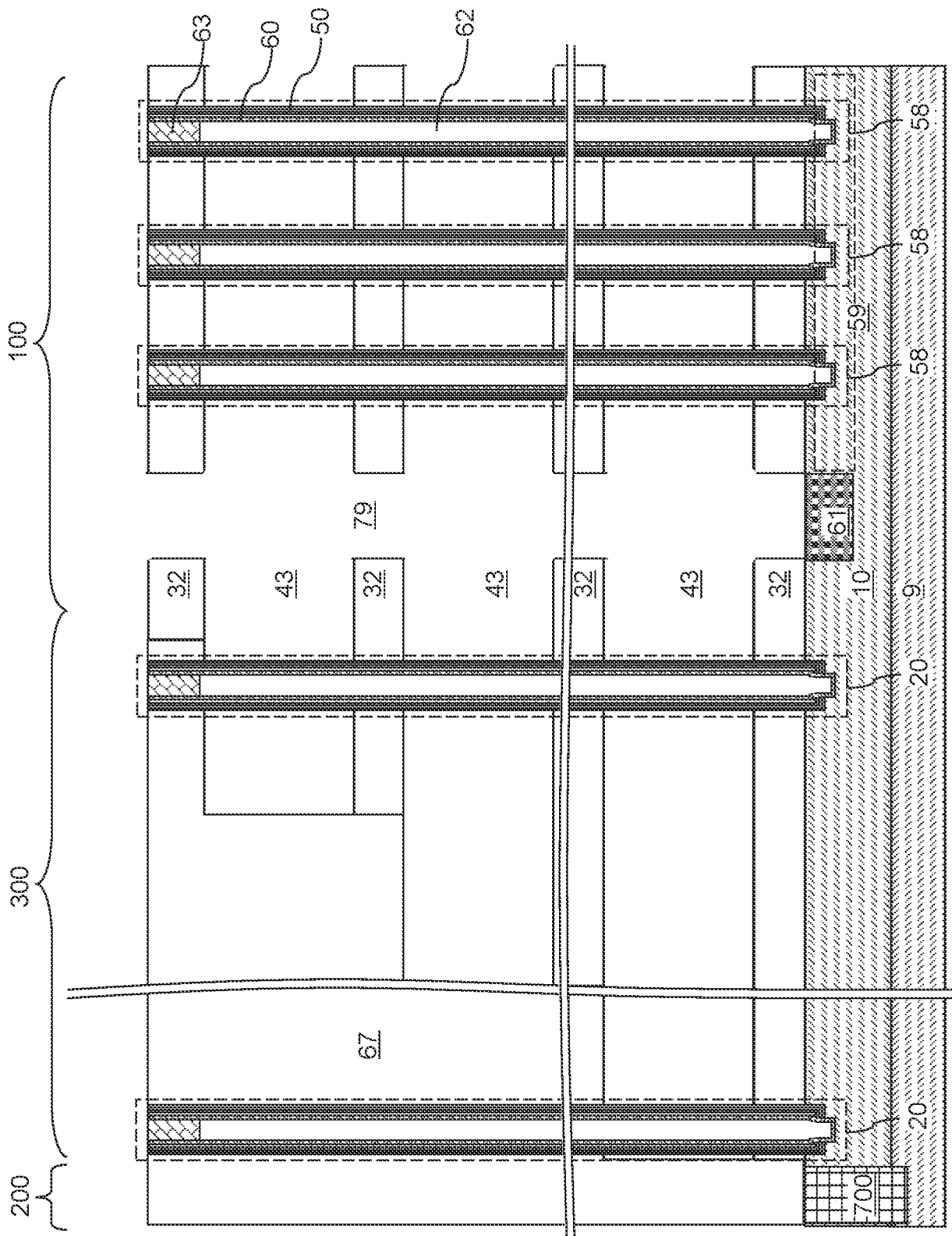


FIG. 88B



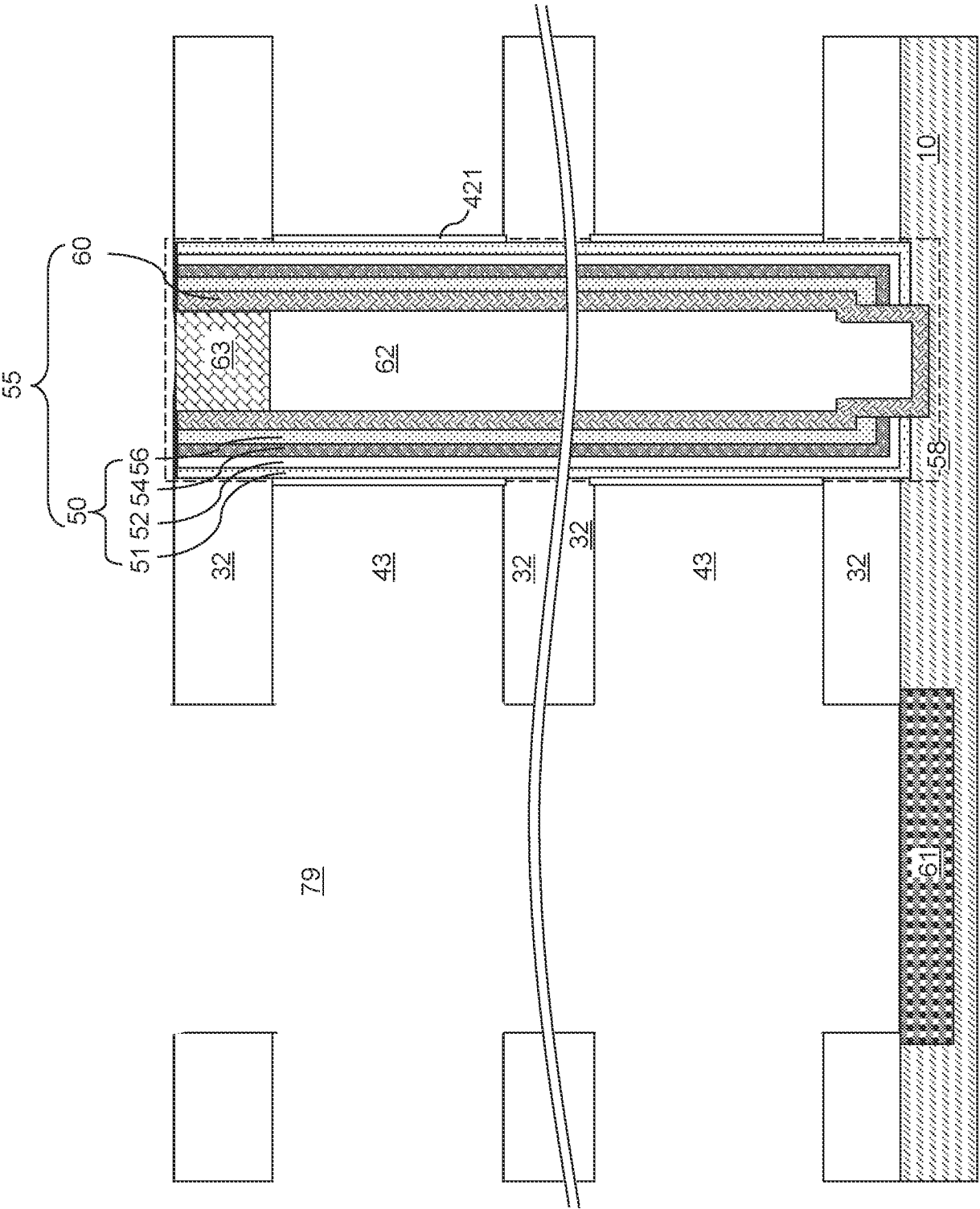


FIG. 89B

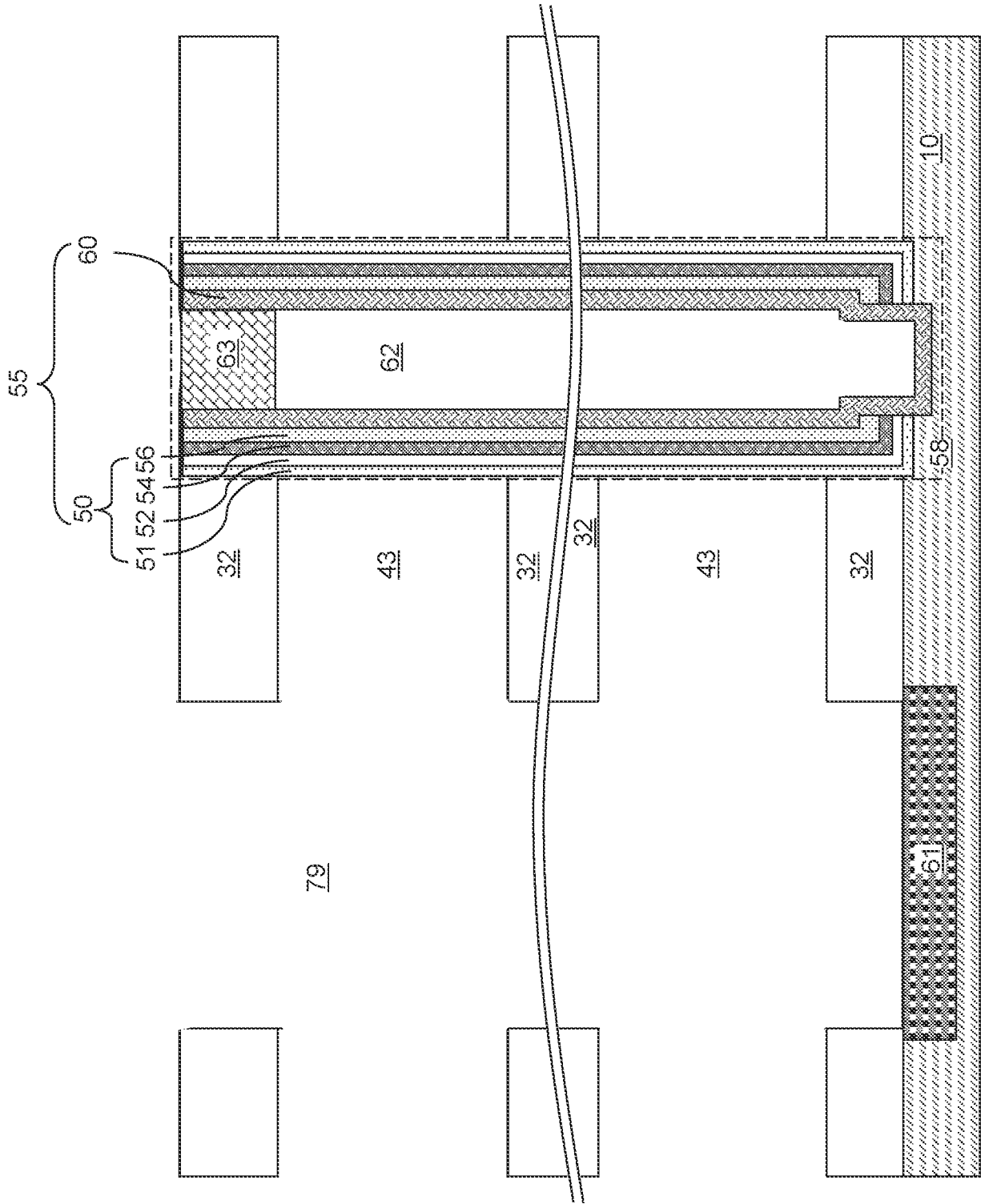


FIG. 90A

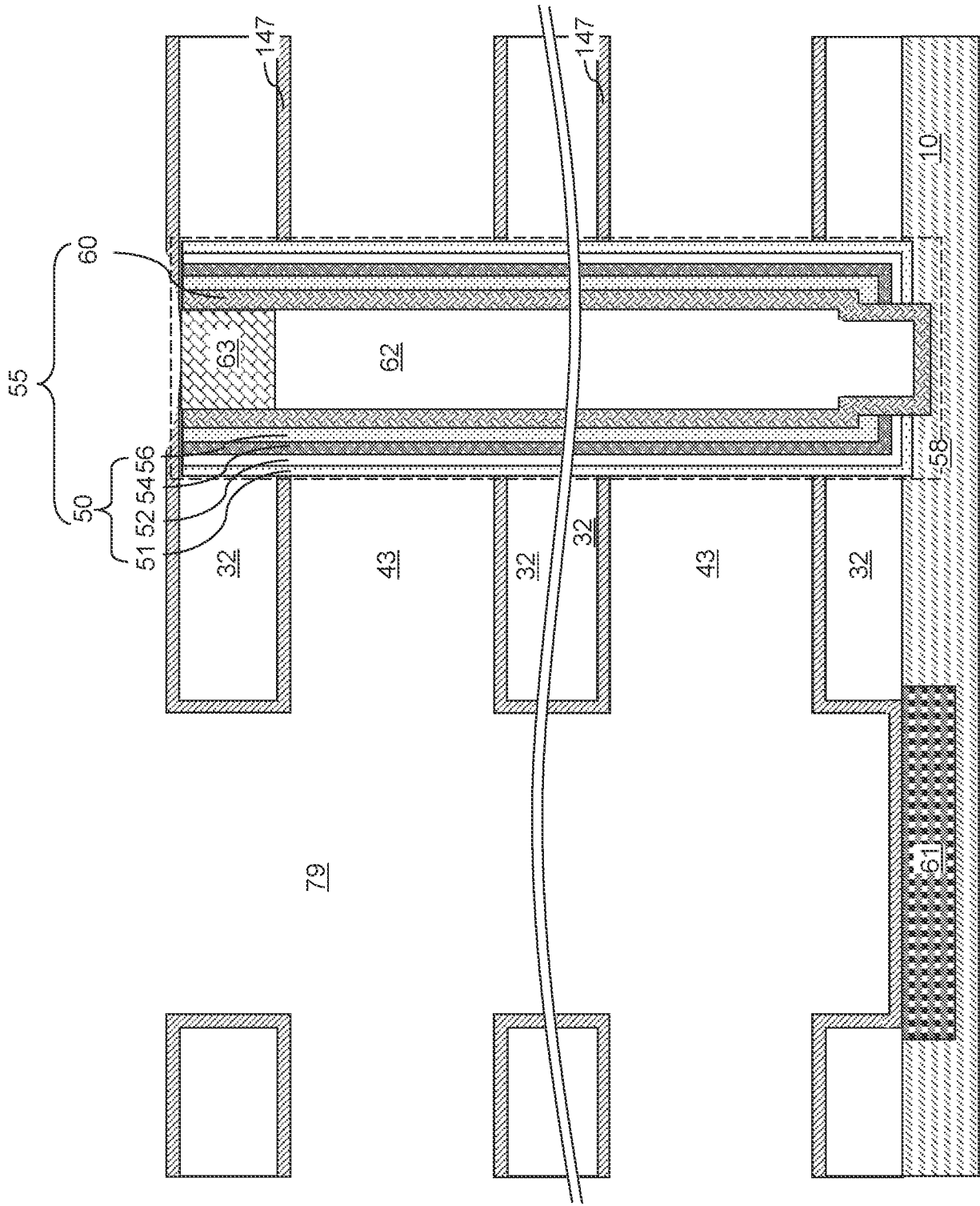
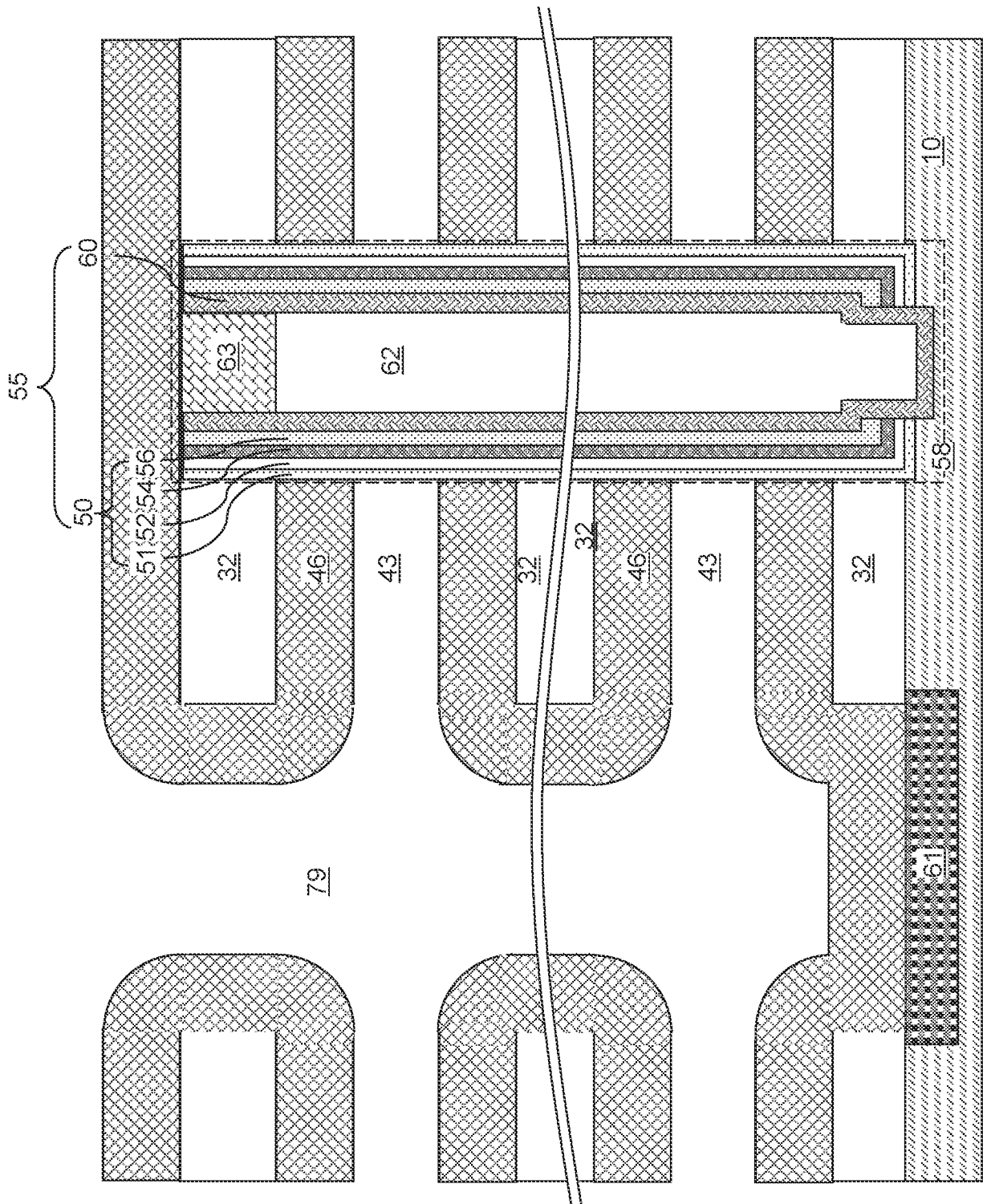
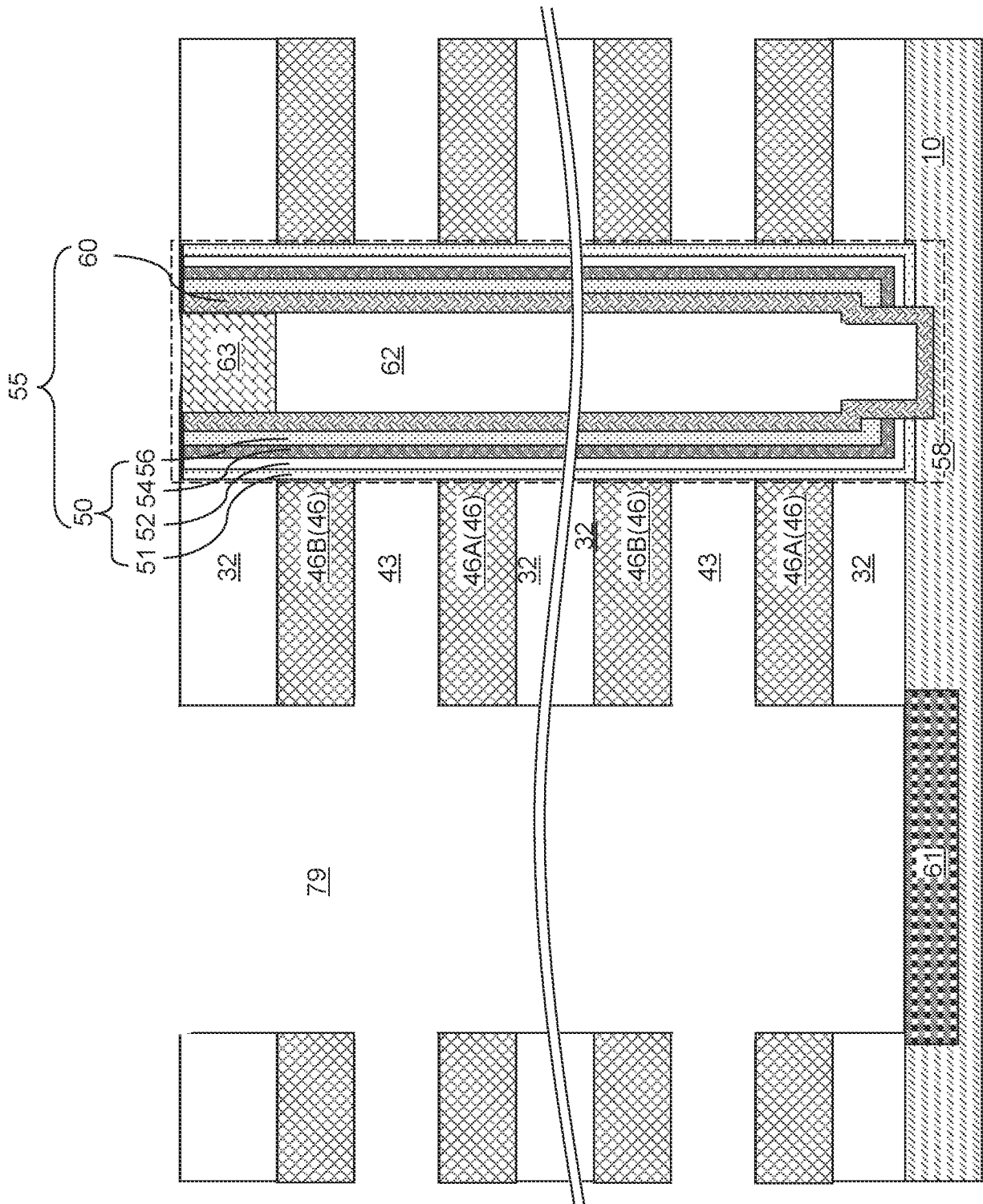
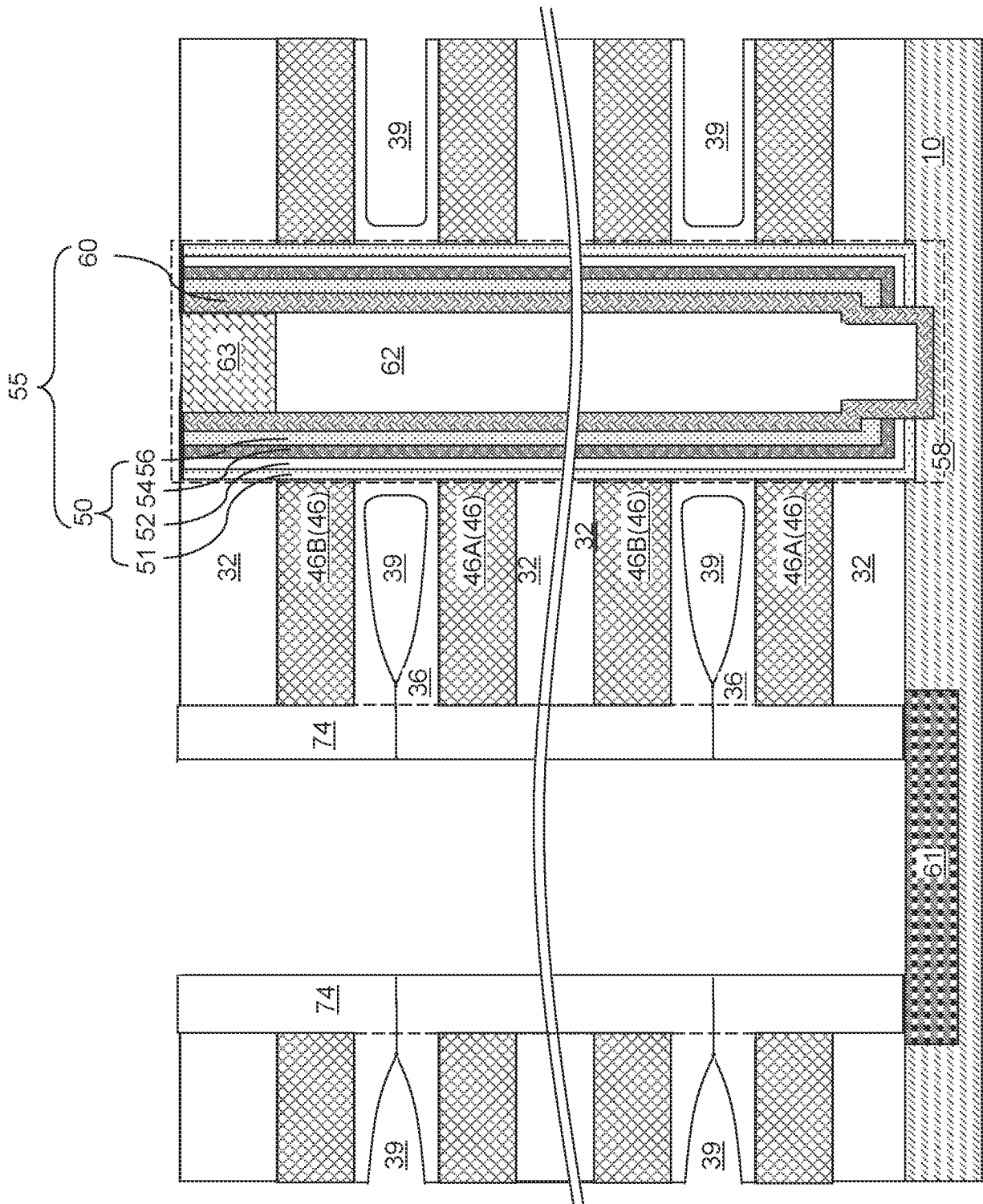
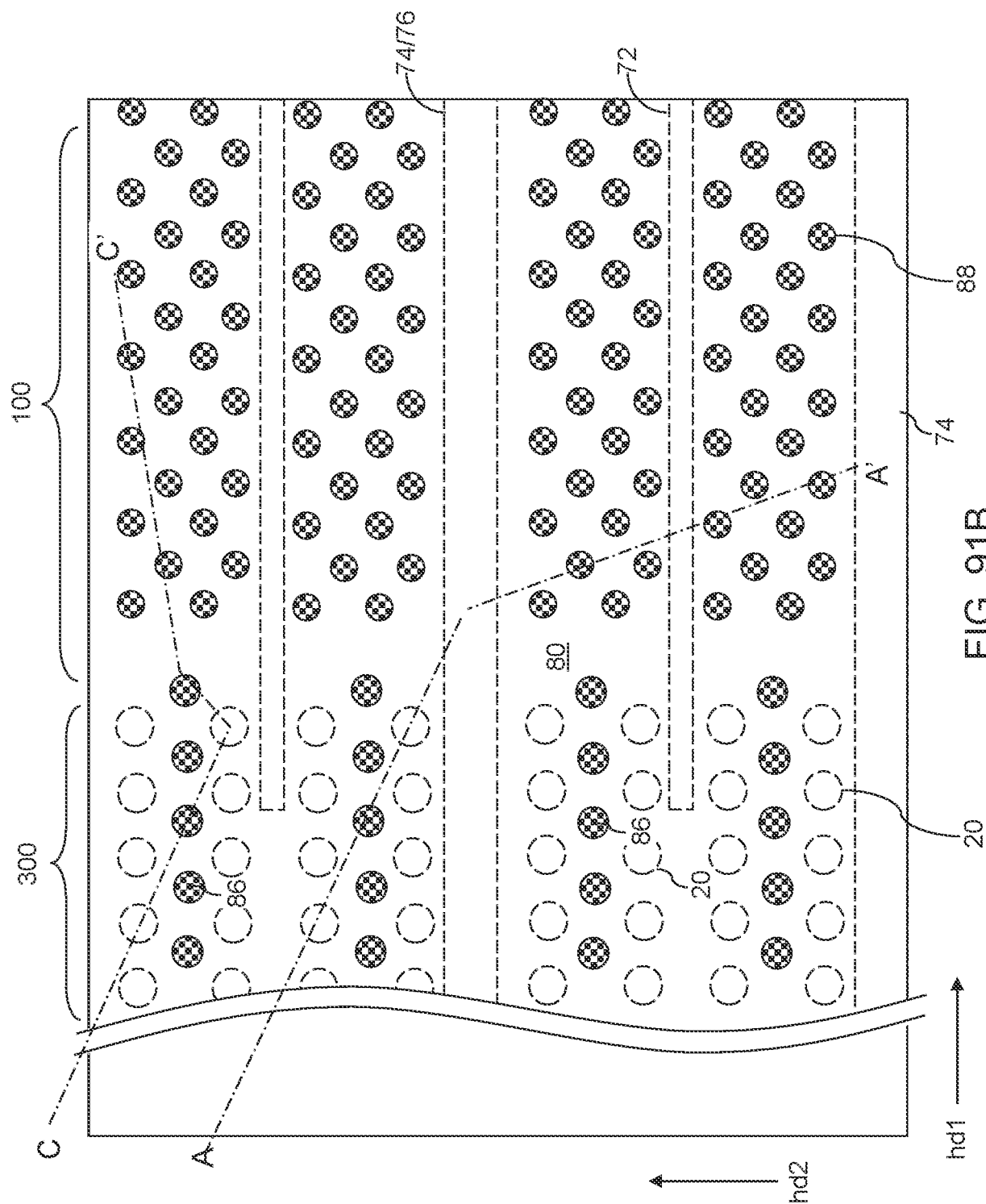


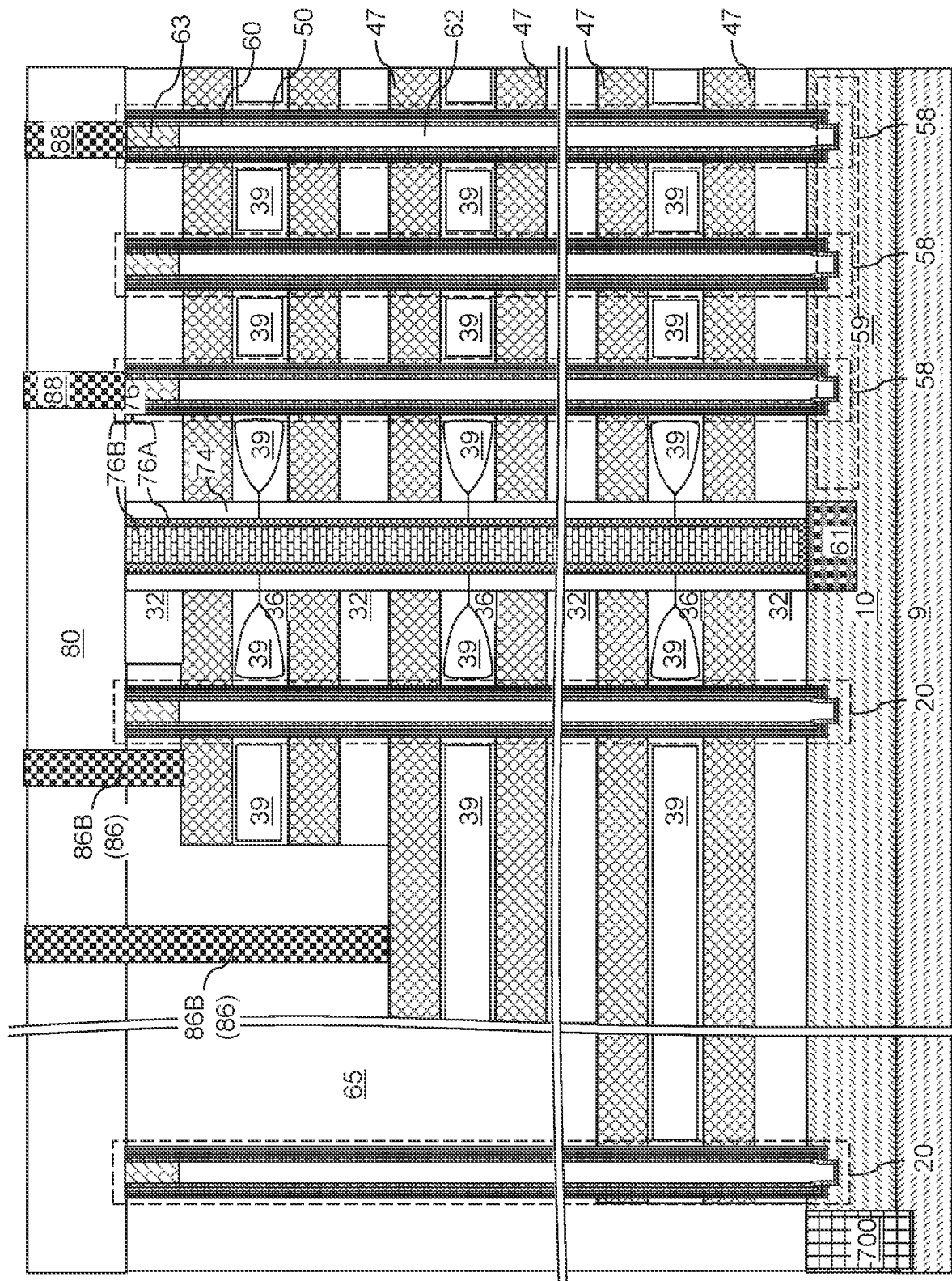
FIG. 90B











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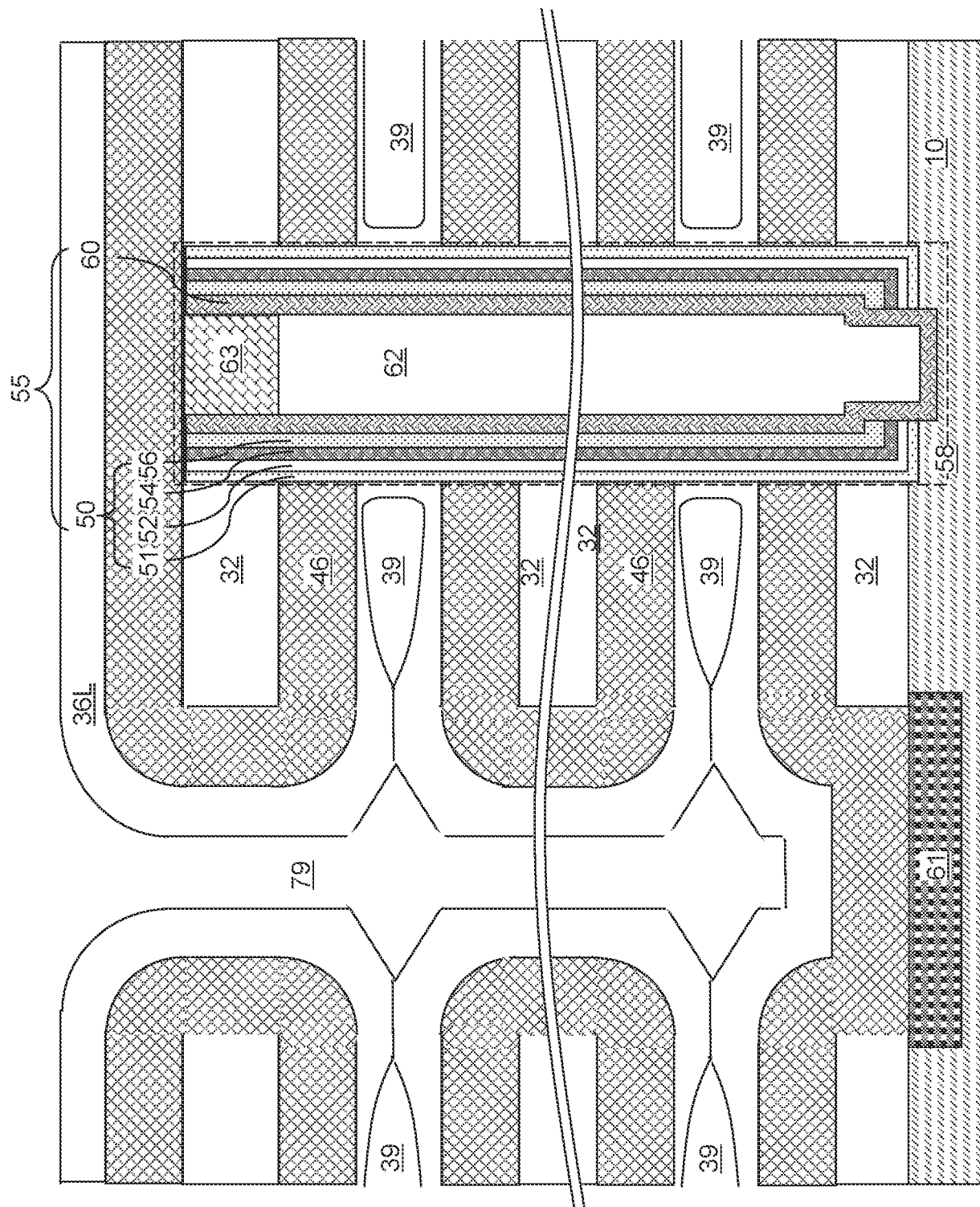
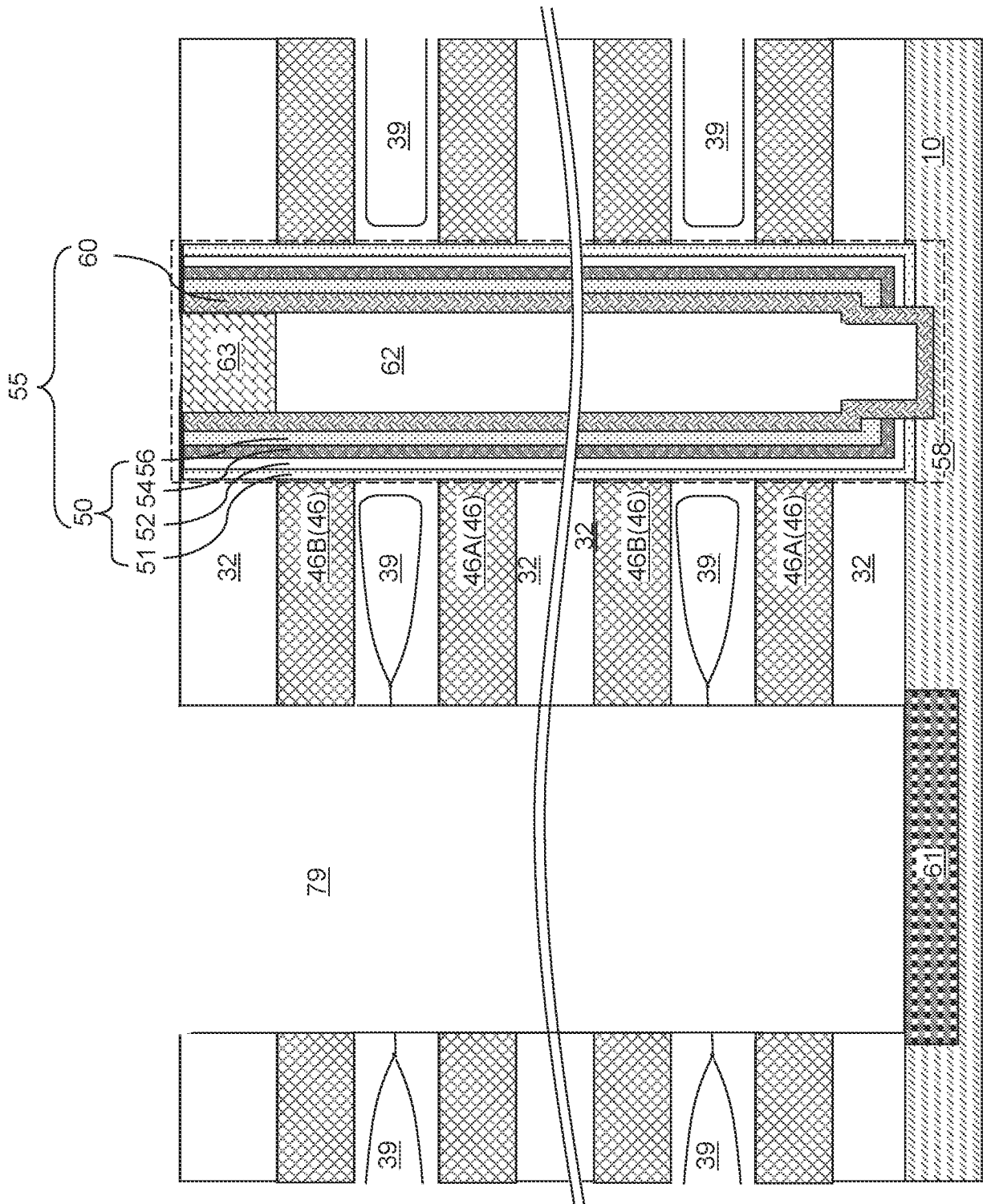


Fig. 92A



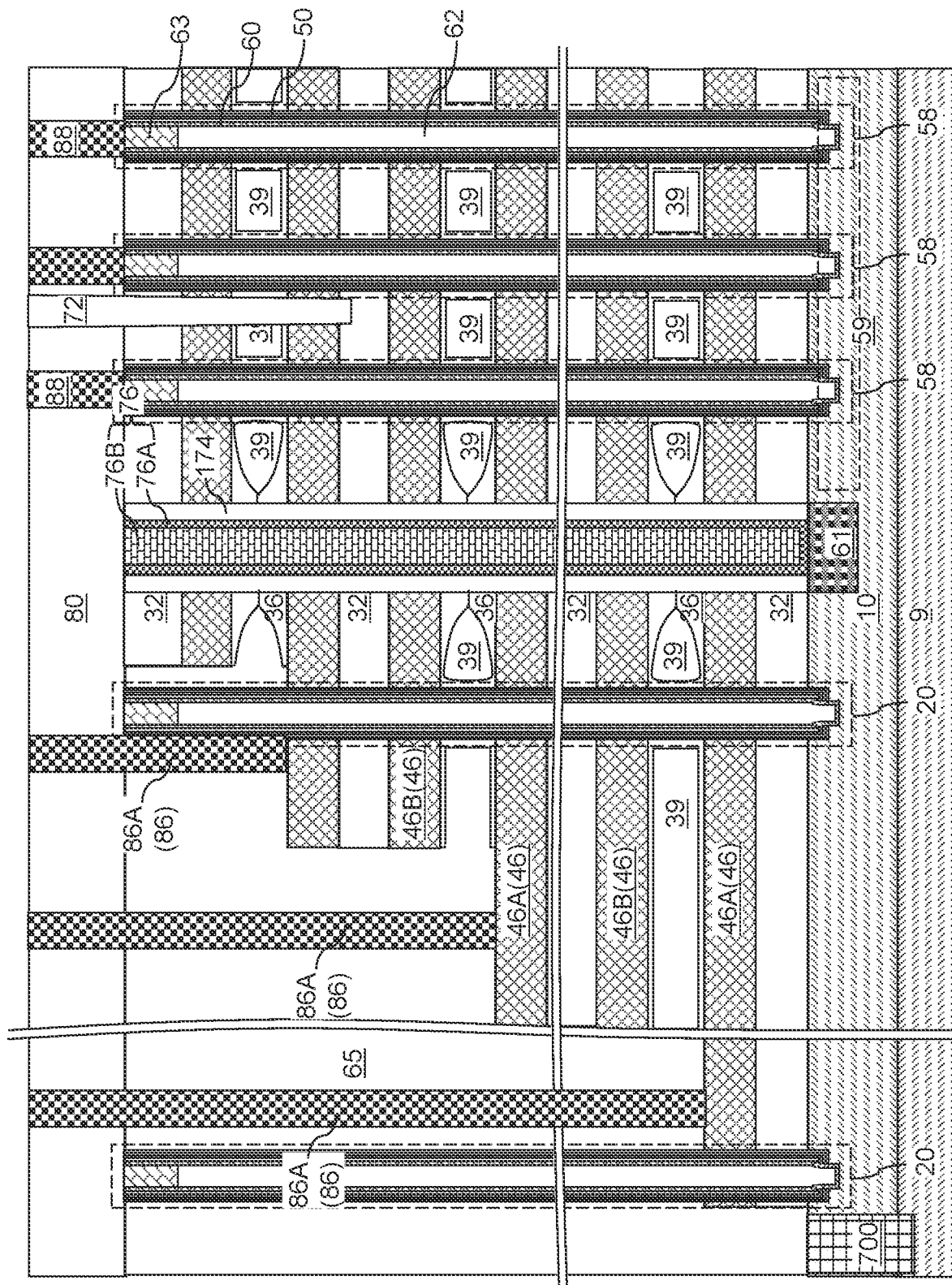
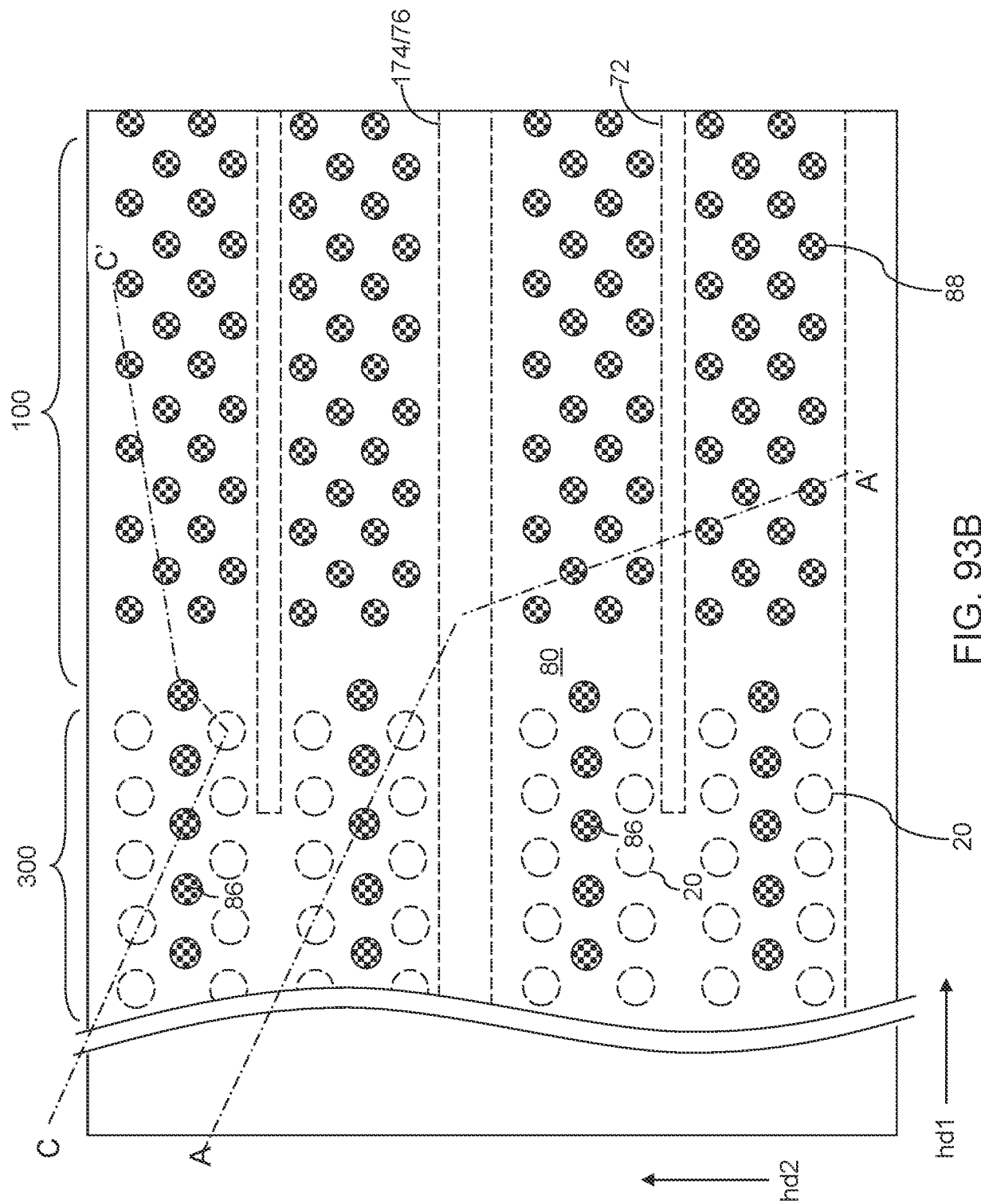
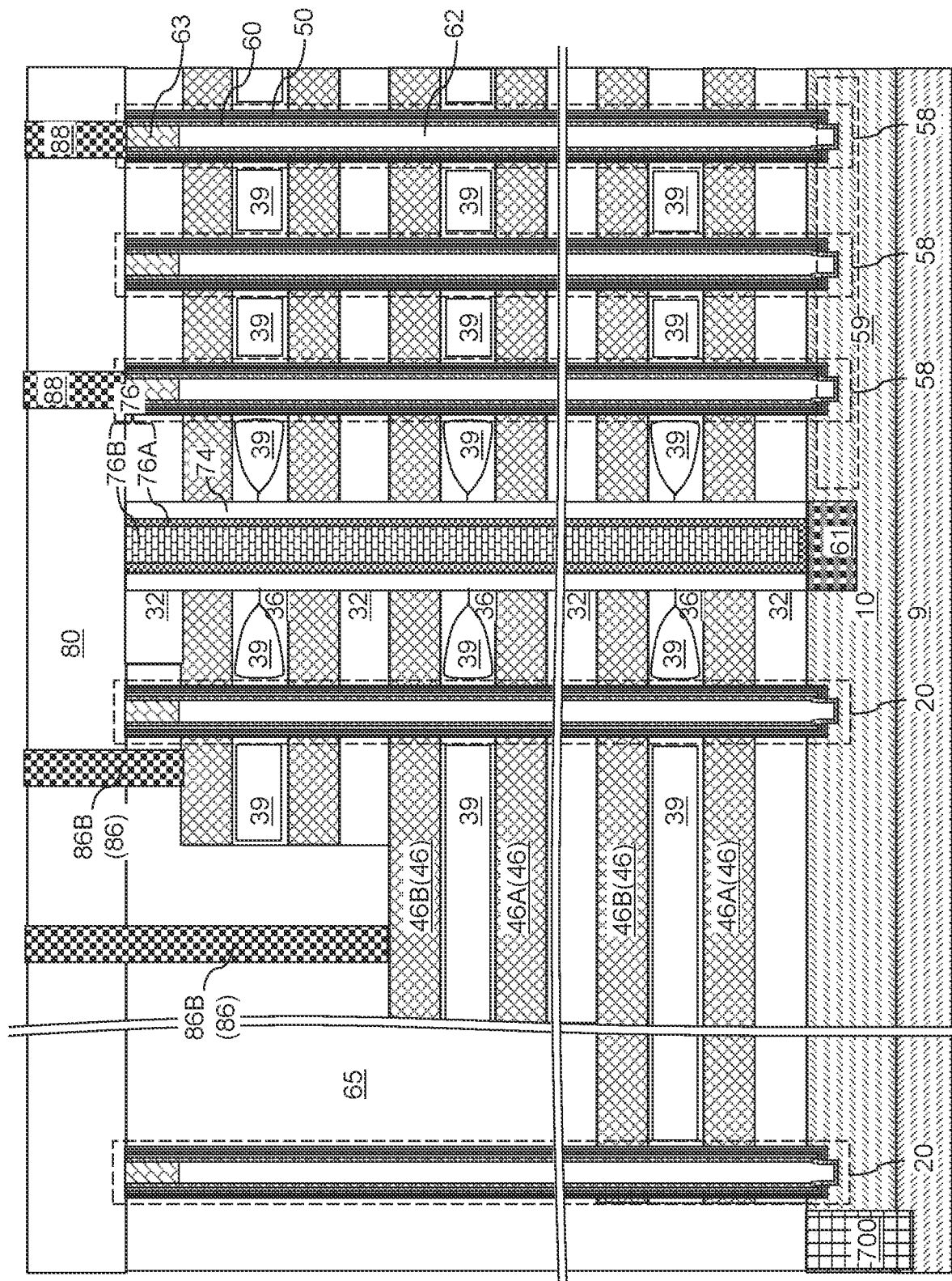


FIG. 3A





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INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2022/013971

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/115(2022.01)i; **H01L 21/3065**(2022.01)i; **H01L 21/311**(2022.01)i; **H01L 21/441**(2022.01)i;
H01L 21/443(2022.01)i; **H01L 21/768**(2022.01)i; **H01L 27/06**(2022.01)i; **H01L 27/108**(2022.01)i; **H01L 29/49**(2022.01)i
 CPC:H01L 27/115; H01L 21/3065; H01L 21/311; H01L 21/441; H01L 21/443; H01L 21/76871; H01L 27/0688; H01L
 27/108; H01L 27/10844; H01L 29/495

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 27/115; H01L 21/3065; H01L 21/311; H01L 21/441; H01L 21/443; H01L 21/768; H01L 27/06; H01L 27/108; H01L
 29/49

CPC:H01L 27/115; H01L 21/3065; H01L 21/311; H01L 21/441; H01L 21/443; H01L 21/76871; H01L 27/0688; H01L
 27/108; H01L 27/10844; H01L 29/495

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Databases consulted: Google Patents, Google Scholar, Orbit, Similari (AI-based) Search terms used: cavity, encapsulat+, porous
 +, three-dimensional, memory, repetition, first, second, type, kind+, layer, conductiv+, insulat+

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A X	US 2017125538 A1 (SanDisk Technologies LLC.) 04 May 2017 (2017-05-04) The whole document	1-16,20-33,35-38,41-74 17-19,34,39,40,75-80
A	US 10651196 B1 (SanDisk Technologies LLC.) 12 May 2020 (2020-05-12) The whole document	1-80
A	WO 2021029916 A1 (SANDISK TECHNOLOGIES LLC.) 18 February 2021 (2021-02-18) The whole document	1-80
A	US 10290648 B1 (SanDisk Technologies LLC.) 14 May 2019 (2019-05-14) The whole document	1-80
A	US 2021091106 A1 (YANGTZE MEMORY TECH. CO. LTD.) 25 March 2021 (2021-03-25) The whole document	1-80

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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 “P” document published prior to the international filing date but later than the priority date claimed

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 “Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
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Date of the actual completion of the international search

02 June 2022

Date of mailing of the international search report

02 June 2022

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CHANIEL Gilad

Telephone No.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2022/013971

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN 109326608 A (Macronix International Co. Ltd.) 12 February 2019 (2019-02-12) The whole document	1-80

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/US2022/013971

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				US	9793139	B2	17 October 2017
				CN	108028256	A	11 May 2018
				CN	108028256	B	28 January 2022
				US	2018033646	A1	01 February 2018
				US	10276583	B2	30 April 2019
				WO	2017074552	A1	04 May 2017
US	10651196	B1	12 May 2020	US	10651196	B1	12 May 2020
				US	2020152655	A1	14 May 2020
				CN	111566814	A	21 August 2020
				EP	3711094	A1	23 September 2020
				EP	3711094	A4	08 September 2021
				WO	2020096674	A1	14 May 2020
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				CN	113272958	A	17 August 2021
				KR	20210080583	A	30 June 2021
				US	2021050360	A1	18 February 2021
				US	10950626	B2	16 March 2021
				US	2021050359	A1	18 February 2021
				US	11018153	B2	25 May 2021
US	10290648	B1	14 May 2019	US	10290648	B1	14 May 2019
US	2021091106	A1	25 March 2021	US	2021091106	A1	25 March 2021
				CN	110785844	A	11 February 2020
				CN	110785844	B	29 January 2021
				CN	112768461	A	07 May 2021
				EP	3895214	A1	20 October 2021
				JP	2022519875	A	25 March 2022
				KR	20210102983	A	20 August 2021
				TW	1707461	B	11 October 2020
				TW	202114173	A	01 April 2021
				US	2022093641	A1	24 March 2022
				WO	2021051371	A1	25 March 2021
CN	109326608	A	12 February 2019	CN	109326608	A	12 February 2019
				CN	109326608	B	16 October 2020