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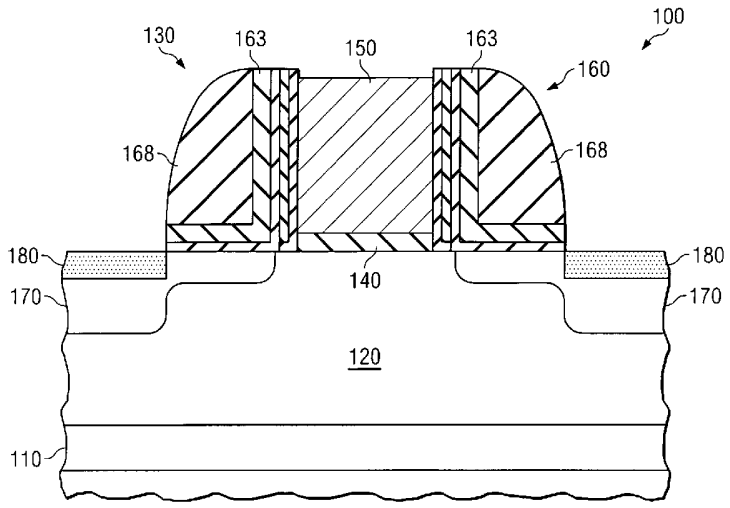
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[Continued on next page]

(54) Title: A METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE HAVING A SILICIDED GATE ELECTRODE AND A METHOD FOR MANUFACTURING AN INTEGRATED CIRCUIT INCLUDING THE SAME



(57) Abstract: The present invention provides a method for manufacturing a semiconductor device and a method for manufacturing an integrated circuit including the semiconductor device. The method for manufacturing the semiconductor device (100), among other possible steps, includes forming a polysilicon gate electrode over a substrate (110) and forming source/drain regions (170) in the substrate (110) proximate the polysilicon gate electrode. The method further includes forming a blocking layer (180) over the source/drain regions (170), the blocking layer (180) comprising a metal silicide, and siliciding the polysilicon gate electrode to form a silicided gate electrode (150).

WO 2005/096366 A1

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A METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE HAVING A SILICIDED GATE ELECTRODE AND A METHOD FOR MANUFACTURING AN INTEGRATED CIRCUIT INCLUDING THE SAME

TECHNICAL FIELD OF THE INVENTION

[0001] The present invention is directed, in general, to a method for manufacturing a semiconductor device and, more specifically, to a method for manufacturing a semiconductor device having a silicided gate electrode and a method for manufacturing an integrated circuit including the same.

BACKGROUND OF THE INVENTION

[0002] Metal gate electrodes are currently being investigated to replace polysilicon gate electrodes in today's ever shrinking and changing transistor devices. One of the principle reasons the industry is investigating replacing the polysilicon gate electrodes with metal gate electrodes is in order to solve problems of poly-depletion effects and boron penetration for future CMOS devices. Traditionally, a polysilicon gate electrode with an overlying silicide was used for the gate electrodes in CMOS devices. However, as device feature size continues to shrink, poly depletion becomes a serious issue when using polysilicon gate electrodes.

[0003] Accordingly, metal gates have been proposed. However, in order to optimize the threshold voltage (V_t) in CMOS devices, the metal gates need dual tunable work functions. For instance, the metal gates need tunable work functions for NMOS and PMOS

devices similar to present polysilicon gate technology, requiring the work functions of metal gates to range from 4.1~4.4eV for NMOS and 4.8~5.1eV for PMOS (*see*, B. Cheng, B. Maiti, S. Samayedam, J. Grant, B. Taylor, P. Tobin, J. Mogab, *IEEE Intl. SOI Conf. Proc.*, pp. 91-92, 2001).

[0004] Recently, silicided metal gates have been investigated based on the extension of existing self-aligned silicide (SALICIDE) technology. In this approach, polysilicon is deposited over the gate dielectric. A metal is deposited over the polysilicon and reacted to completely consume the polysilicon resulting in a fully silicided metal gate, rather than a deposited metal gate. The silicided metal gate provides a metal gate with the least perturbation to the conventional process and avoids contamination issues. Furthermore, poly doping has been shown to affect the work function of the silicided metal gates.

[0005] The silicided metal gates are not without their problems. One of the more significant problems associated with the silicided metal gates is attributed to the simultaneous formation of the silicided metal gate and the silicided source/drain regions. When formed simultaneously, the depth of the silicided source/drain regions is directly proportional to the thickness of the polysilicon gate electrode. As the polysilicon gate electrodes currently range in thickness from about 60 nm to about 120 nm, the silicided source/drain regions ultimately extend into the silicon substrate by up to about 60 nm to about 120 nm, respectively. Deep silicided source/drain

regions are nonetheless undesirable.

[0006] Various companies in the industry have attempted to separate the silicidation of the polysilicon gate and the silicidation of the source/drain regions. Those companies employ chemical mechanical polishing (CMP) technology to separate the steps. In such integration schemes, the gate electrode is masked by a silicon oxide layer and a silicide is then formed on the source/drain regions. Next, a blanket dielectric layer is deposited over the gate stack and silicided source/drain regions. The CMP process is then employed to expose the gate electrode for silicidation, while the source/drain regions are covered by the protective dielectric layer. The main drawback of this approach originates from the across-wafer non-uniformity inherently associated with polishing (such as dishing, etc.). In addition, the poly height on the active area may be different from the designed poly height. As a result, the height of the poly gate after polishing may suffer significant variation. Therefore, the silicidation may be inconsistent across-wafer, and/or wafer-to-wafer due to the thickness variation in poly-gate.

[0007] Accordingly, what is needed is a method for manufacturing silicided metal gate structures separate from the silicided source/drain regions that does not experience the drawbacks of the prior art methods.

SUMMARY OF THE INVENTION

[0008] To address the above-discussed deficiencies of the prior art, the present invention provides a method for manufacturing a semiconductor device and a method for manufacturing an integrated circuit including the semiconductor device. The method for manufacturing the semiconductor device, among other possible steps, includes forming a polysilicon gate electrode over a substrate and forming source/drain regions in the substrate proximate the polysilicon gate electrode. The method further includes forming a blocking layer over the source/drain regions, the blocking layer comprising a metal silicide, and siliciding the polysilicon gate electrode to form a silicided gate electrode.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIGURE 1 illustrates a cross-sectional view of one embodiment of a semiconductor device constructed according to the principles of the present invention;

[0010] FIGURE 2 illustrates a cross-sectional view of a partially completed semiconductor device manufactured in accordance with the principles of the present invention;

[0011] FIGURE 3 illustrates a cross-sectional view of the partially completed semiconductor device illustrated in FIGURE 2 after formation of a portion of gate sidewall spacers;

[0012] FIGURE 4 illustrates a cross-sectional view of the partially completed semiconductor device illustrated in FIGURE 3 after formation of lightly doped extension implants within the substrate;

[0013] FIGURE 5 illustrates a cross-sectional view of the partially completed semiconductor device illustrated in FIGURE 4 after forming the remaining portions of the gate sidewall spacers;

[0014] FIGURE 6 illustrates a cross-sectional view of the partially completed semiconductor device illustrated in FIGURE 5 after etching the cap oxide from the top of the substrate and top of the protective layer, as well as after formation of highly doped source/drain implants within the substrate;

[0015] FIGURE 7 illustrates a cross-sectional view of the partially completed semiconductor device illustrated in FIGURE 6 after subjecting the semiconductor device to a standard source/drain anneal, thereby activating source/drain regions, and after depositing a silicidation metal;

[0016] FIGURE 8 illustrates a cross-sectional view of the partially completed semiconductor device illustrated in FIGURE 7 after subjecting it to a rapid thermal anneal (RTA), and after a selective wet etch to remove un-reacted silicidation metal;

[0017] FIGURE 9 illustrates a cross-sectional view of the partially completed semiconductor device illustrated in FIGURE 8 after removing the protective layer from over the polysilicon gate electrode to form an opening;

[0018] FIGURE 10 illustrates a cross-sectional view of the partially completed semiconductor device illustrated in FIGURE 9 after depositing a second silicidation metal over the exposed portions of the polysilicon gate electrode, as well as over the remainder of the semiconductor device;

[0019] FIGURE 11 illustrates a cross-sectional view of the partially completed semiconductor device illustrated in FIGURE 10 after converting the polysilicon gate electrode to a silicided gate electrode;

[0020] FIGURE 12 illustrates an exemplary cross-sectional view of an integrated circuit (IC) incorporating devices constructed according to the principles of the present invention; and

[0021] FIGURE 13 illustrates another exemplary cross-sectional view of an integrated circuit (IC) incorporating devices constructed according to the principles of the present invention, where the top portion of the poly gate electrode is silicided to form a self-aligned silicide contact.

DETAILED DESCRIPTION

[0022] Referring initially to FIGURE 1, illustrated is a cross-sectional view of one embodiment of a semiconductor device 100 constructed according to the principles of the present invention. In the embodiment illustrated in FIGURE 1, the semiconductor device 100 includes a substrate 110. Located within the substrate 110 in the embodiment of FIGURE 1 is a well region 120. Additionally located over the substrate 110 and well region 120 is a gate structure 130.

[0023] The gate structure 130 illustrated in FIGURE 1 includes a gate oxide 140 located over the substrate 110, as well as a silicided gate electrode 150 located over the gate oxide 140. While the silicided gate electrode is illustrated in FIGURE 1 as a fully silicided gate electrode, those skilled in

the art understand that the silicided gate electrode 150 could also comprise a partially silicided gate electrode where only the top portion of the electrode is silicided. This embodiment might be used if there was a need to reduce the contact resistance of the silicided gate electrode 150.

[0024] The silicided gate electrode 150 may have a variety of thicknesses, nonetheless, a thickness ranging from about 50 nm to about 150 nm is exemplary. The silicided gate electrode 150, when constructed in accordance with the principles of the present invention, may comprise a number of different materials. For instance, in the illustrative embodiment shown in FIGURE 1 the silicided gate electrode 150 comprises nickel, however, it is envisioned that the silicided gate electrode 150 could comprise cobalt, platinum, titanium, tantalum, molybdenum, tungsten, etc., while staying within the scope of the present invention.

[0025] The silicided gate electrode 150 may also include a dopant or combination of several types of dopants therein. The dopant, such as boron, phosphorous, arsenic or another similar dopant based on whether the semiconductor device 100 is operating as a PMOS device or an NMOS device, is configured to tune the minimum energy required to bring an electron from the Fermi level to the vacuum level, or the so called work function.

[0026] The gate structure 130 further contains gate sidewall spacers 160 flanking both sides of the silicided gate electrode 150 and gate oxide 140. The gate sidewall spacers 160 in the embodiment of FIGURE 1 each include a number of different

layers. For instance the gate sidewall spacers 160, among other layers, each include L-shaped nitride spacers 163 and sidewall oxides 168. In this particular embodiment the L-shaped nitride spacers 163 comprise a unique nitride layer that includes carbon. The carbon content may be within a wide range, however, it is believed that a carbon content ranging from about 5% to about 10% is advantageous. The other layers, among other materials, could include a collection of oxides and nitrides. The gate sidewall spacers 160 may comprise many different types and numbers of layers while staying consistent with the principles of the present invention.

[0027] The semiconductor device 100 illustrated in FIGURE 1 additionally includes conventional source/drain regions 170 located within the substrate 110 and proximate the gate oxide 140. Located within the source/drain regions 170 are blocking layers 180. The blocking layers 180 in the embodiment of FIGURE 1 function both as a protectant from the silicidation material used to form the silicided gate electrode 150, as well as source/drain contact regions.

[0028] The blocking layers 180, when manufactured in accordance with the principles of the present invention, comprise a metal silicide. In one embodiment, the blocking layers 180 comprise a metal silicide different from the metal silicide of the silicided gate electrode 150, however, in another embodiment they comprise a metal silicide the same as the metal silicide of the silicided gate electrode 150. As the silicided gate electrode 150 in the embodiment of FIGURE 1

comprise nickel silicide, the blocking layers 180 comprise a different metal silicide. In this particular embodiment the blocking layers 180 comprise cobalt silicide. Nonetheless, other silicidation materials (e.g., nickel, platinum, titanium, tantalum, molybdenum, tungsten, etc.) could be used to form the blocking layers 180 and remain within the scope of the present invention. The blocking layers 180 may have a depth into the source/drain regions 170 ranging from about 10 nm to about 35 nm, among others. This depth needs to be sufficient to prevent the silicidation metal used to form the silicided gate electrode 150 from affecting the source/drain regions 170, however, small enough to be consistent with the design of the present invention.

[0029] Turning now to FIGURES 2-11, illustrated are cross-sectional views of detailed manufacturing steps instructing how one might, in an advantageous embodiment, manufacture a semiconductor device similar to the semiconductor device 100 depicted in FIGURE 1. FIGURE 2 illustrates a cross-sectional view of a partially completed semiconductor device 200 manufactured in accordance with the principles of the present invention. The partially completed semiconductor device 200 of FIGURE 2 includes a substrate 210. The substrate 210 may, in an exemplary embodiment, be any layer located in the partially completed semiconductor device 200, including a wafer itself or a layer located above the wafer (e.g., epitaxial layer). In the embodiment illustrated in FIGURE 2, the substrate 210 is a P-type substrate; however, one skilled in the art understands that

the substrate 210 could be an N-type substrate without departing from the scope of the present invention. In such a case, each of the dopant types described throughout the remainder of this document would be reversed. For clarity, no further reference to this opposite scheme will be discussed.

[0030] Located within the substrate 210 in the embodiment shown in FIGURE 2 is a well region 220. The well region 220, in light of the P-type semiconductor substrate 210, would more than likely contain an N-type dopant. For example, the well region 220 would likely be doped with an N-type dopant dose ranging from about 1E13 atoms/cm^2 to about 1E14 atoms/cm^2 and at an energy ranging from about 100 keV to about 500 keV. This results in the well region 220 having a peak dopant concentration ranging from about 5E17 atoms/cm^3 to about 1E19 atoms/cm^3.

[0031] Located over the substrate 210 in the embodiment of FIGURE 2 is a gate structure 230. The gate structure 230 includes a gate oxide 240 and a polysilicon gate electrode 250. The gate oxide 240 may comprise a number of different materials and stay within the scope of the present invention. For example, the gate oxide 240 may comprise silicon dioxide, or in an alternative embodiment comprise a high dielectric constant (K) material. In the illustrative embodiment of FIGURE 2, however, the gate oxide 240 is a silicon dioxide layer having a thickness ranging from about 0.5 nm to about 5 nm.

[0032] Any one of a plurality of manufacturing techniques could be used to form the gate oxide 240. For example, the gate

oxide 240 may be either grown or deposited. Additionally, the growth or deposition steps may require a significant number of different temperatures, pressures, gasses, flow rates, etc.

[0033] While the advantageous embodiment of FIGURE 2 dictates that the polysilicon gate electrode 250 comprise standard polysilicon, other embodiments exist where the polysilicon gate electrode, or at least a portion thereof, comprises amorphous polysilicon. The amorphous polysilicon embodiment may be particularly useful when a substantially planar upper surface of the polysilicon gate electrode 250 is desired.

[0034] The deposition conditions for the polysilicon gate electrode 250 may vary, however, if the polysilicon gate electrode 250 were to comprise standard polysilicon, such as the instance in FIGURE 2, the polysilicon gate electrode 250 could be deposited using a pressure ranging from about 100 torr to about 300 torr, a temperature ranging from about 620EC to about 700EC, and a SiH_4 or Si_2H_6 gas flow ranging from about 50 sccm to about 150 sccm. If, however, amorphous polysilicon were desired, the amorphous polysilicon gate electrode could be deposited using a pressure ranging from about 100 torr to about 300 torr, a temperature ranging from about 450EC to about 550EC, and a SiH_4 or Si_2H_6 gas flow ranging from about 100 sccm to about 300 sccm. In any instance, the polysilicon gate electrode 250 desirably has a thickness ranging from about 50 nm to about 150 nm.

[0035] The partially completed semiconductor device 200 illustrated in FIGURE 2 further includes a protective layer 260

located over the polysilicon gate electrode 250. The protective layer 260, which may comprise silicon nitride among other materials, may have a thickness ranging from about 5 nm to about 50 nm. It is desirable for the protective layer 260 to have a thickness small enough to allow a dopant to easily penetrate therethrough, however, large enough to provide the sufficient amount of protection to the polysilicon gate electrode 250.

[0036] Optionally located over the protective layer 260 is a silicon dioxide layer 270. The optional silicon dioxide layer 270 is designed to help pattern the gate oxide 240, polysilicon gate electrode 250 and protective layer 260. With that said, those skilled in the art understand that the gate oxide 240, polysilicon gate electrode 250, protective layer 260 and optional silicon dioxide layer 270 were originally blanket deposited. Those blanket layers were subsequently patterned resulting in the gate oxide 240, polysilicon gate electrode 250, protective layer 260 and optional silicon dioxide layer 270 illustrated in FIGURE 2. In one embodiment, the polysilicon gate electrode 250 and protective layer 260 are formed using a chemical vapor deposition (CVD) technique.

[0037] Turning briefly to FIGURE 3 illustrated is a cross-sectional view of the partially completed semiconductor device 200 illustrated in FIGURE 2 after formation of portions of gate sidewall spacers 310. The portions of the gate sidewall spacers 310 shown in FIGURE 3 include an oxide layer 320 and an offset nitride spacer 330. The oxide layer 320, as compared to similar layers used in the prior art, is formed at least partially using

a deposition process. In an exemplary process the oxide layer 320 is initially formed using a first deposition process, and then finished using a second oxidation process. The first deposition process allows the oxide layer 320 to form on the top and sidewalls of the protective layer 260. In an alternative embodiment the entire oxide layer 320 is deposited.

[0038] The offset nitride spacer 330 may comprise a standard silicon nitride spacer or a silicon nitride layer having carbon therein. If the offset nitride spacer 330 were to contain the carbon, the carbon might form from about 5% to about 10% of the layer. While the oxide layer 320 and the offset nitride spacer 330 are shown located only along the sides of the gate structure 230, those skilled in the art are aware that the layers were previously blanket formed and subsequently anisotropically etched to form the oxide layer 320 and the offset nitride spacer 330.

[0039] Turning now to FIGURE 4, illustrated is a cross-sectional view of the partially completed semiconductor device 200 illustrated in FIGURE 3 after formation of lightly doped extension implants 410 within the substrate 210. The lightly doped extension implants 410 are conventionally formed and generally have a peak dopant concentration ranging from about 1E19 atoms/cm^3 to about 2E20 atoms/cm^3. As is standard in the industry, the lightly doped extension implants 410 have a dopant type opposite to that of the well region 220 they are located within. Accordingly, the lightly doped extension implants 410 are doped with a P-type dopant in the illustrative embodiment

shown in FIGURE 4.

[0040] Turning now to FIGURE 5, illustrated is a cross-sectional view of the partially completed semiconductor device 200 illustrated in FIGURE 4 after forming the remaining portions of the gate sidewall spacers 310. Particularly, a cap oxide 510, L-shaped nitride spacers 520 and sidewall oxides 530 complete the gate sidewall spacers 310. The cap oxide 510, among other purposes, has the job of preventing the L-shaped nitride spacers 520 from directly contacting the substrate 210. Most likely, the cap oxide 510 will be deposited over the partially completed semiconductor device 200 using a process similar to that used to form the oxide layer 320.

[0041] The L-shaped nitride spacers 520 may comprise any type of nitride, however, in an exemplary embodiment the L-shaped nitride spacers 520 comprise a nitride material that includes carbon. The carbon content, which may range from about 5% to about 10% of the L-shaped nitride spacers 520, is included within the L-shaped nitride spacers 520 to change the rate at which they etch. In the embodiment where the L-shaped nitride spacers 520 include carbon, the L-shaped nitride spacers 520 may be deposited using bis t-butylaminosilane (BTBAS) and ammonia (NH_3) precursors in a CVD reactor. Advantageously, the carbon causes the L-shaped nitride spacers 520 to etch at a slower rate than a traditional nitride layer. In an exemplary situation, after having been annealed using a temperature ranging from about 1000EC to about 1100EC, the carbon causes the L-shaped nitride spacers 520 to have an etch selectivity of about 50:1

when compared to the traditional nitride layer.

[0042] The sidewall oxides 530 that are located over the L-shaped nitride spacers 520 are conventional. In the given embodiment of FIGURE 5, the sidewall oxides 530 were blanket deposited and then subjected to an anisotropic etch. The resulting sidewall oxides 530 complete the gate sidewall spacers 310 illustrated in the embodiment of FIGURE 5.

[0043] Turning now to FIGURE 6, illustrated is a cross-sectional view of the partially completed semiconductor device 200 illustrated in FIGURE 5 after etching the cap oxide 510 from the top of the substrate 210 and top of the protective layer 260, as well as after formation of highly doped source/drain implants 610 within the substrate 210. Those skilled in the art understand the conventional processes that could be used to etch the cap oxide 510.

[0044] The formation of the highly doped source/drain implants 610 is also conventional. Generally the highly doped source/drain implants 610 have a peak dopant concentration ranging from about 1E18 atoms/cm^3 to about 1E21 atoms/cm^3. Also, the highly doped source/drain implants 610 should typically have a dopant type opposite to that of the well region 220 they are located within. Accordingly, in the illustrative embodiment shown in FIGURE 6, the highly doped source/drain implants 610 are doped with a P-type dopant.

[0045] Turning now to FIGURE 7, illustrated is a cross-sectional view of the partially completed semiconductor device 200 illustrated in FIGURE 6 after subjecting the semiconductor

device 200 to a standard source/drain anneal, thereby activating source/drain regions 710. It is believed that a source/drain anneal conducted at a temperature ranging from about 1000EC to about 1100EC and a time period ranging from about 1 second to about 5 seconds would be sufficient. It should be noted that other temperatures, times, and processes could be used to activate the source/drain regions 710.

[0046] Additionally illustrated in FIGURE 7 is the formation of a silicidation metal 720 over the exposed portions of the source/drain regions 710 as well as over the gate structure 230. The silicidation metal 720 in the embodiment shown in FIGURE 7 happens to be a thin cobalt layer, however, other materials that react with silicon to form a silicide could easily be used. For instance it is known that the silicidation metal 720 may also comprise nickel, platinum, titanium, tantalum, molybdenum, tungsten, another similar metal, or any combination thereof while staying within the scope of the present invention. In the embodiment of FIGURE 7, the silicidation metal 720 comprises a different metal than the silicidation metal 1010 (FIGURE 10). Nonetheless, this is not required to remain within the scope of the present invention.

[0047] The silicidation metal 720 may be formed using a number of different processes, and may be formed to a number of different thicknesses. In one embodiment of the invention the silicidation metal 720 is deposited to a thickness ranging from about 3 nm to about 10 nm. Such thicknesses, however, might be used when the silicidation metal 720 comprises cobalt. Various

other thicknesses could be used if the silicidation metal 720 were to comprise one of the different metals disclosed above.

[0048] Turning now to FIGURE 8, illustrated is a cross-sectional view of the partially completed semiconductor device 200 illustrated in FIGURE 7 after subjecting it to a rapid thermal anneal (RTA). This RTA attempts to cause the silicidation metal 720 to react with the silicon of the source/drain regions 710 to form blocking layers 810. In the instance where the silicidation metal 720 comprises cobalt, the RTA causes the cobalt to react with the silicon to form a cobalt silicide.

[0049] The RTA may be conducted using a variety of different temperatures and times. Nonetheless, it is believed that the RTA, in an exemplary embodiment, should be conducted in a rapid thermal processing tool at a temperature ranging from about 400EC to about 600EC for a time period ranging from about 5 seconds to about 60 seconds. The specific temperature and time period are typically based, however, on the ability to form the blocking layers 810 to a desired depth, as well as the silicide materials selected.

[0050] A selective wet etch, using for example a mixture of sulfuric acid (H_2SO_4), hydrogen peroxide (H_2O_2) and water (H_2O), may then be used to remove un-reacted silicidation metal 720 on regions other than exposed silicon, such as on sidewall and gate. Additionally, another optional RTA step may be used to form a low resistivity phase of the silicide. In the case of using cobalt silicidation metal, the first RTA forms CoSi, while

the optional RTA forms $CoSi_2$, which has lower resistivity and is more stable. This optional RTA step is typically performed using a temperature ranging from about 650EC to about 800EC for a time period ranging from about 5 to about 60 seconds.

[0051] Turning now to FIGURE 9, illustrated is a cross-sectional view of the partially completed semiconductor device 200 illustrated in FIGURE 8 after removing the protective layer 260 from over the polysilicon gate electrode 250 to form an opening 910. Unique to the present invention, the etchant used to remove the protective layer 260 does not substantially affect other structures or films. More specifically, the hot phosphoric acid etchant used to remove the protective layer 260 does not affect the L-shaped nitride spacer 520 and blocking layers 810. Even though the protective layer 260 and the L-shaped nitride spacer 520 both comprise silicon nitride, the carbon content of the L-shaped nitride spacer 520 provides substantial protection from the etchant.

[0052] Turning now to FIGURE 10, illustrated is a cross-sectional view of the partially completed semiconductor device 200 illustrated in FIGURE 9 after depositing a second silicidation metal 1010 over the exposed portions of the polysilicon gate electrode 250, as well as over the remainder of the semiconductor device 200. In a preferred embodiment, the silicidation metal 1010 is designed to fully silicidize the polysilicon gate electrode 250. As it takes approximately 1 nm of nickel to fully silicidize approximately 1.8 nm of polysilicon, the thickness of the silicidation metal 1010 should

be at least 56% of the thickness of the polysilicon gate electrode 250. To be comfortable, however, it is suggested that the thickness of the silicidation metal 1010 should be at least 60% of the thickness of the polysilicon gate electrode 250. Thus, where the thickness of the polysilicon gate electrode 250 ranges from about 50 nm to about 150 nm, as described above, the thickness of the silicidation metal 1010 should range from approximately 30 nm to about 90 nm. It should also be noted that the silicidation metal 1010 may comprise a number of different metals or combinations of metals while staying within the scope of the present invention. For example, the silicidation metal 1010 may comprise any metal known to react with polysilicon to form a metal silicide.

[0053] In an alternative embodiment of the invention, a thinner layer of silicidation metal 1010 may be formed over the exposed portions of the polysilicon gate electrode 250, as well as over the remainder of the semiconductor device 200. In this instance, the thinner layer of silicidation metal 1010 will only react with the top portion of the polysilicon gate electrode 250, to form a partially silicided gate electrode. The thickness of the thinner layer of silicidation metal 1010 could range from about 3 nm to about 15 nm to only partially silicide the silicided gate electrode. This embodiment is particularly useful for applications where a poly-gate oxide interface is used, rather than a silicide-gate oxide interface, as is the case in the fully silicided gate electrode discussed directly above.

[0054] Turning now to FIGURE 11, illustrated is the partially completed semiconductor device 200 illustrated in FIGURE 10 after converting the polysilicon gate electrode 250 to a silicided gate electrode 1110. Those skilled in the art understand the steps that might be required to form the silicided gate electrode 1110, including subjecting the polysilicon gate electrode 250 and metal silicide layer 1010 to another RTA. This RTA is designed to convert the polysilicon gate electrode 250 to the silicided gate electrode 1110. The annealing temperature depends on the silicide metal being used. For example, it is believed that the RTA may be conducted at a temperature ranging from about 350EC to about 550EC and a time period ranging from about 10 second to about 100 seconds to accomplish the silicidation when nickel is used. It should be noted that other temperatures, times, and processes could be used if another metal were used. In a preferred embodiment, the silicidation metal 1010 fully silicidizes the polysilicon gate electrode 250. The silicide, however, does not form on the source/drain region 710 at this time because of the blocking layers 810.

[0054] After completing the silicided gate electrode 1110, the partially completed semiconductor device 200 may be subjected to a selective removal process. For instance, in one embodiment of the invention the device could be subjected to an etch recipe consisting of sulfuric acid (H_2SO_4), hydrogen peroxide (H_2O_2) and water (H_2O). This specific etch recipe has a high degree of selectivity and could easily remove any remaining

portions of the silicidation metal 1010. Thereafter the manufacture of the partially completed semiconductor device 200 would continue in a conventional manner, optimally resulting in a device similar to the semiconductor device 100 illustrated in FIGURE 1. It should be noted that the exact order of the steps illustrated with respect to FIGUREs 2-11 may change depending on the process flow. Additionally, various other steps could be added to the description of FIGUREs 2-11.

[0055] The method of manufacturing the semiconductor device as discussed with respect to FIGUREs 2-11 provides many benefits over the prior art methods. First, and possibly most important, it separates the formation of the silicided gate electrode and blocking layers (e.g., silicided source/drain contact regions) into different steps. Advantageously, this allows the depth of the blocking layers (e.g., silicided source/drain contact regions) to be independent of the thickness of the silicided gate electrode. The decoupling of the two steps is achieved by taking advantage of the chemical selectivity of thin films to certain etch chemistries. Accordingly, CMP is not needed as it is in the prior art methods capable of decoupling the steps. As such, the method of the present invention is applicable to devices having different step heights, whether by design or process variation. The CMP technique of the prior art is not capable of accepting such variations in step heights.

[0056] Additionally, the method of the present invention allows the blocking layers to also function as the silicided source/drain regions. Accordingly, the present invention

requires less processing steps than the prior art options. Further, the method of the present invention allows the semiconductor device to easily choose different silicidation metals for the silicide gate electrode and blocking layers (e.g., silicided source/drain regions). In the embodiment discussed above, the silicided gate electrode benefits from using nickel as the silicidation material. The nickel, at least as compared to cobalt, allows the sheet resistance of the silicided gate electrode to remain small as the gate length continues to increase. Similarly, the blocking layers benefit from using cobalt as the silicidation material. The cobalt, at least as compared to nickel, reduces piping defect issues in the source/drain regions. Thus the embodiment of the method discussed with respect to FIGURE 2-11 makes the best use of both nickel and cobalt. It is believed that the other metals would have similar advantages.

[0057] Referring now to FIGURE 12, illustrated is an exemplary cross-sectional view of an integrated circuit (IC) 1200 incorporating devices 1210 constructed according to the principles of the present invention. The IC 1200 may include devices, such as transistors used to form CMOS devices, BiCMOS devices, Bipolar devices, as well as capacitors or other types of devices. The IC 1200 may further include passive devices, such as inductors or resistors, or it may also include optical devices or optoelectronic devices. Those skilled in the art are familiar with these various types of devices and their manufacture. In the particular embodiment illustrated in FIGURE

12, the IC 1200 includes the devices 1210 having dielectric layers 1220 located thereover. Additionally, interconnect structures 1230 are located within the dielectric layers 1220 to interconnect various devices, thus, forming the operational integrated circuit 1200.

[0058] Referring finally to FIGURE 13, illustrated is another exemplary cross-sectional view of an integrated circuit (IC) 1300 incorporating devices 1310 constructed according to the principles of the present invention. In the particular embodiment illustrated in FIGURE 13, the IC 1300 includes devices 1310 having a gate electrode that is only partially silicided. The partially silicided gate electrode is desirable to reduce contact resistance of the poly electrode while keeping the poly-gate oxide interface without a silicide forming at the interface. Located over the devices 1310 are dielectric layers 1320. Additionally, interconnect structures 1330 are located within the dielectric layers 1320 to interconnect various devices, thus, forming the operational integrated circuit 1300.

CLAIMS:

1. A method for manufacturing a semiconductor device, comprising:

forming a polysilicon gate electrode over a substrate;

forming source/drain regions in said substrate proximate said polysilicon gate electrode;

forming a blocking layer over said source/drain regions, said blocking layer comprising a metal silicide;

siliciding said polysilicon gate electrode to form a silicided gate electrode.

2. The method as recited in Claim 1 wherein said forming a blocking layer occurs prior to said siliciding said polysilicon gate electrode.

3. The method as recited in Claim 1 wherein said blocking layer is a silicided source/drain contact region.

4. The method as recited in Claim 1 wherein said silicided gate electrode comprises a different metal silicide than said blocking layer.

5. The method as recited in Claim 4 wherein said blocking layer comprises a cobalt silicide and said silicided gate electrode comprises a nickel silicide.

6. The method as recited in Claim 1 wherein said blocking layer has a thickness ranging from about 10 nm to about 35 nm.

7. The method as recited in Claim 1 further including forming a protective layer over said polysilicon gate electrode prior to said forming a blocking layer over said source/drain regions.

8. The method as recited in Claim 7 wherein said protective layer is a silicon nitride protective layer.

9. The method as recited in Claim 1 wherein siliciding said polysilicon gate electrode to form a silicided gate electrode includes fully siliciding said polysilicon gate electrode to form a fully silicided gate electrode.

10. A method for manufacturing an integrated circuit, comprising:

forming semiconductor devices over a substrate, including;

forming a polysilicon gate electrode over a substrate;

forming source/drain regions in said substrate proximate said polysilicon gate electrode;

forming a blocking layer over said source/drain regions, said blocking layer comprising a metal silicide;

siliciding said polysilicon gate electrode to form a silicided gate electrode; and

forming interconnects within dielectric layers located over

said substrate for electrically contacting said semiconductor devices.

11. The method as recited in Claim 10 wherein said forming a blocking layer occurs prior to said siliciding said polysilicon gate electrode.

12. The method as recited in Claim 10 wherein said blocking layer is a silicided source/drain contact region.

13. The method as recited in Claim 10 wherein said silicided gate electrode comprises a different metal silicide than said blocking layer.

14. The method as recited in Claim 13 wherein said blocking layer comprises a cobalt silicide and said silicided gate electrode comprises a nickel silicide.

15. The method as recited in Claim 10 wherein said blocking layer has a thickness ranging from about 10 nm to about 35 nm.

16. The method as recited in Claim 10 further including forming a protective layer over said polysilicon gate electrode prior to said forming a blocking layer over said source/drain regions.

17. The method as recited in Claim 16 wherein said protective layer is a silicon nitride protective layer.

18. The method as recited in Claim 10 wherein siliciding said polysilicon gate electrode to form a silicided gate electrode includes fully siliciding said polysilicon gate electrode to form a fully silicided gate electrode.

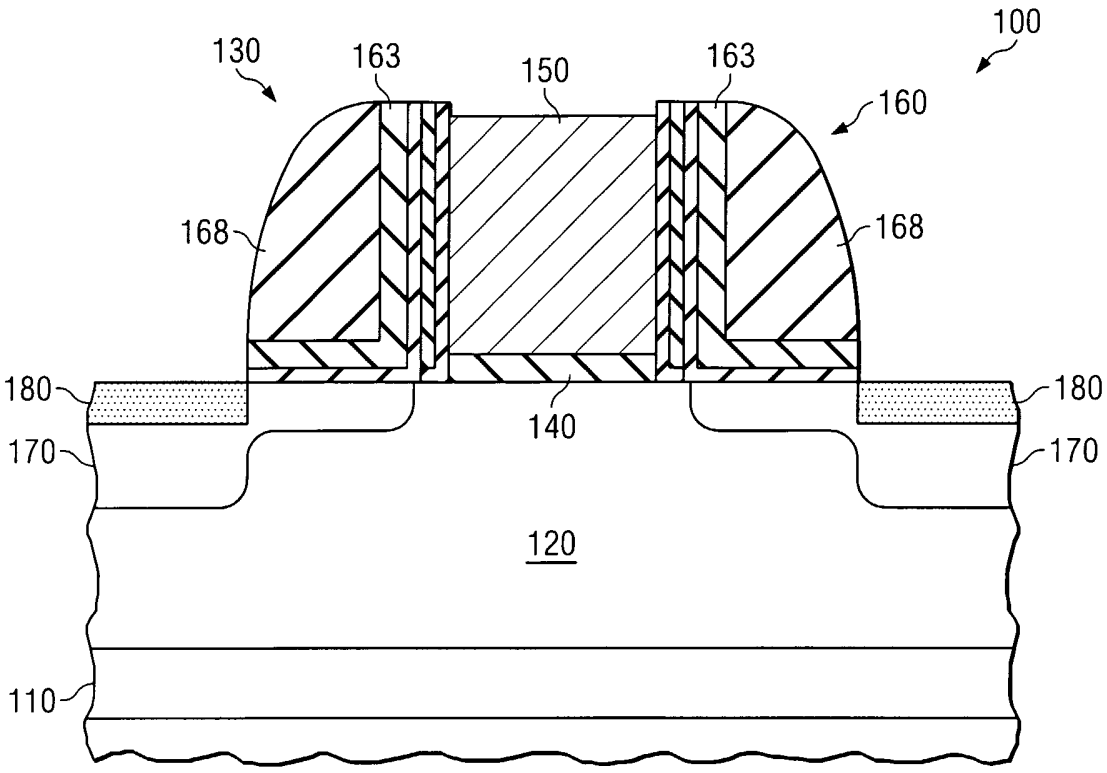

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FIG. 1

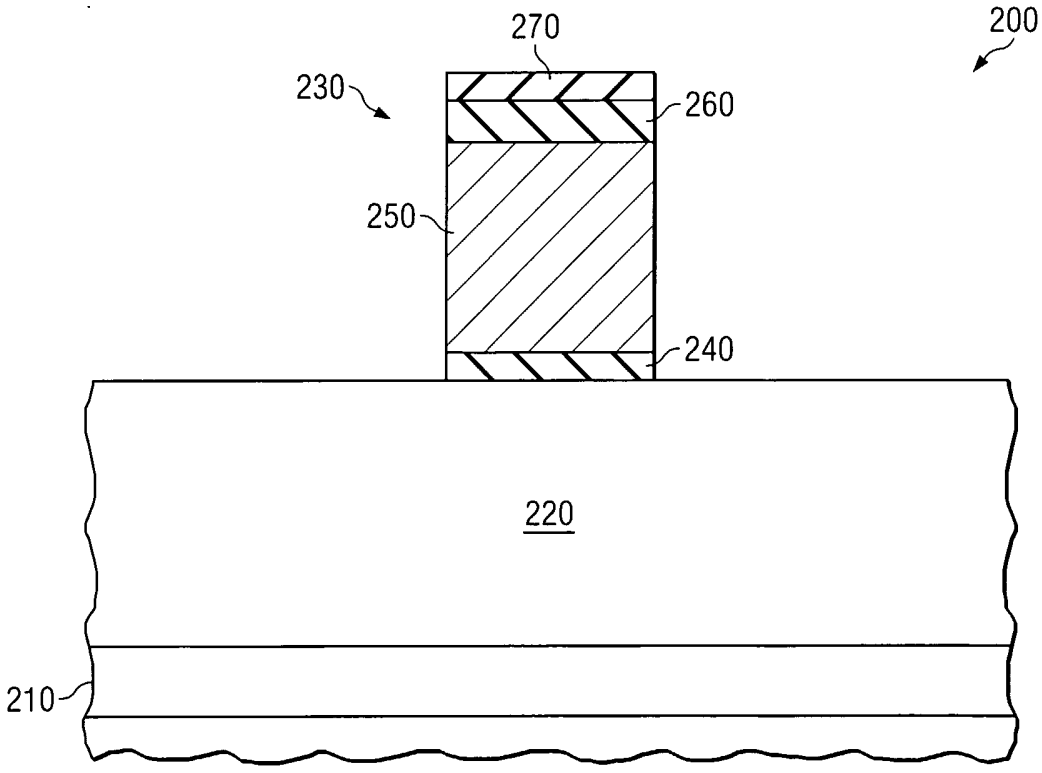

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FIG. 2

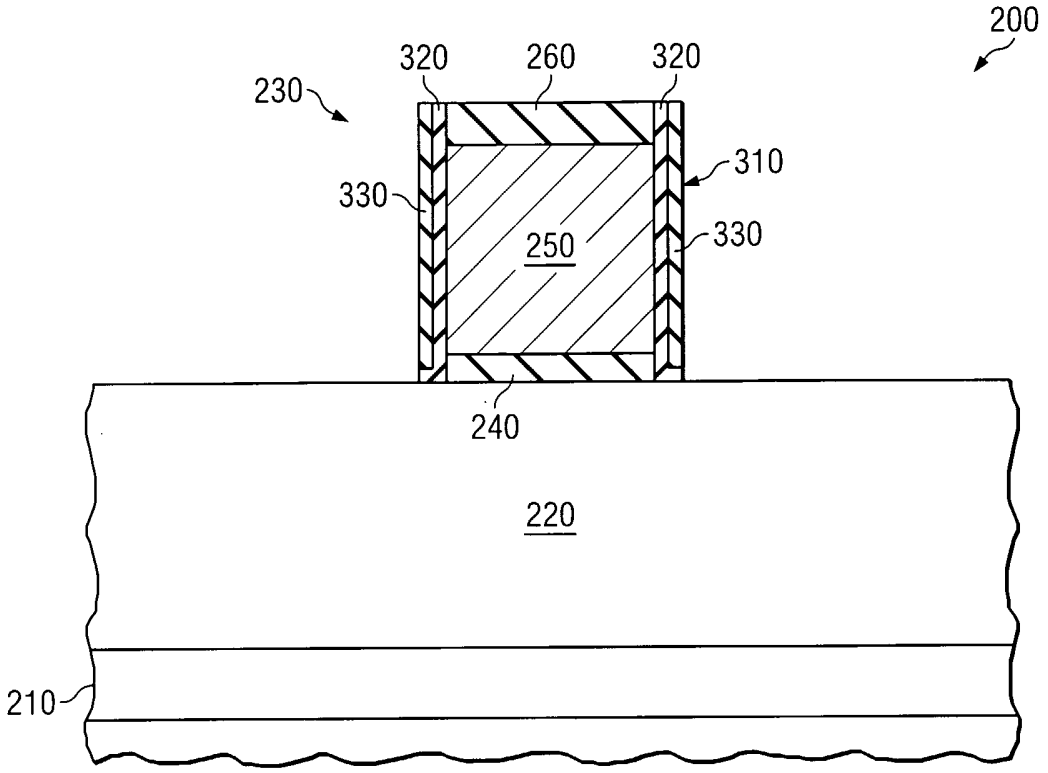

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FIG. 3

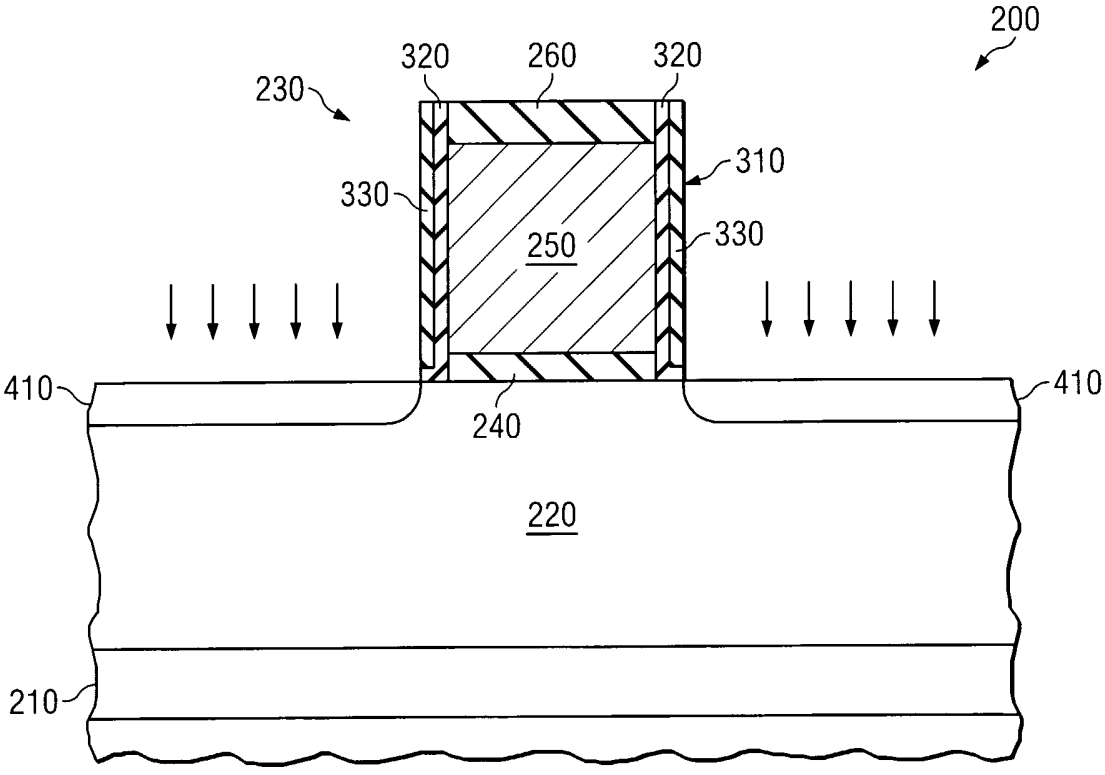

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FIG. 4

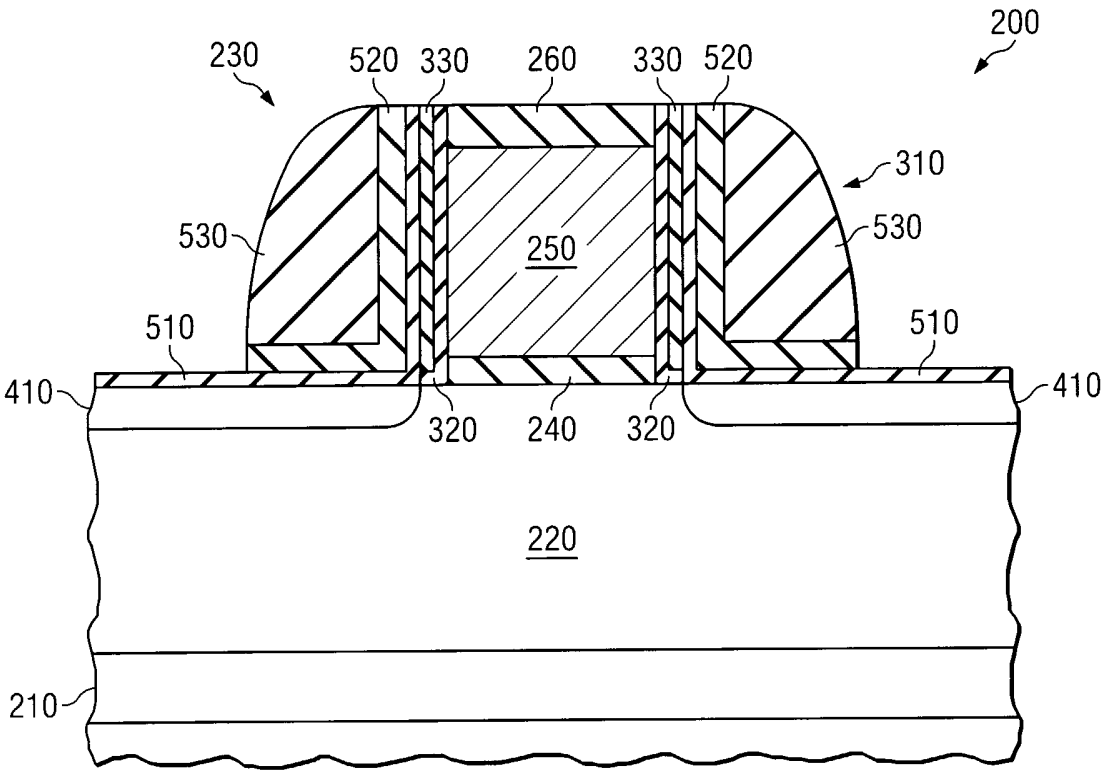

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FIG. 5

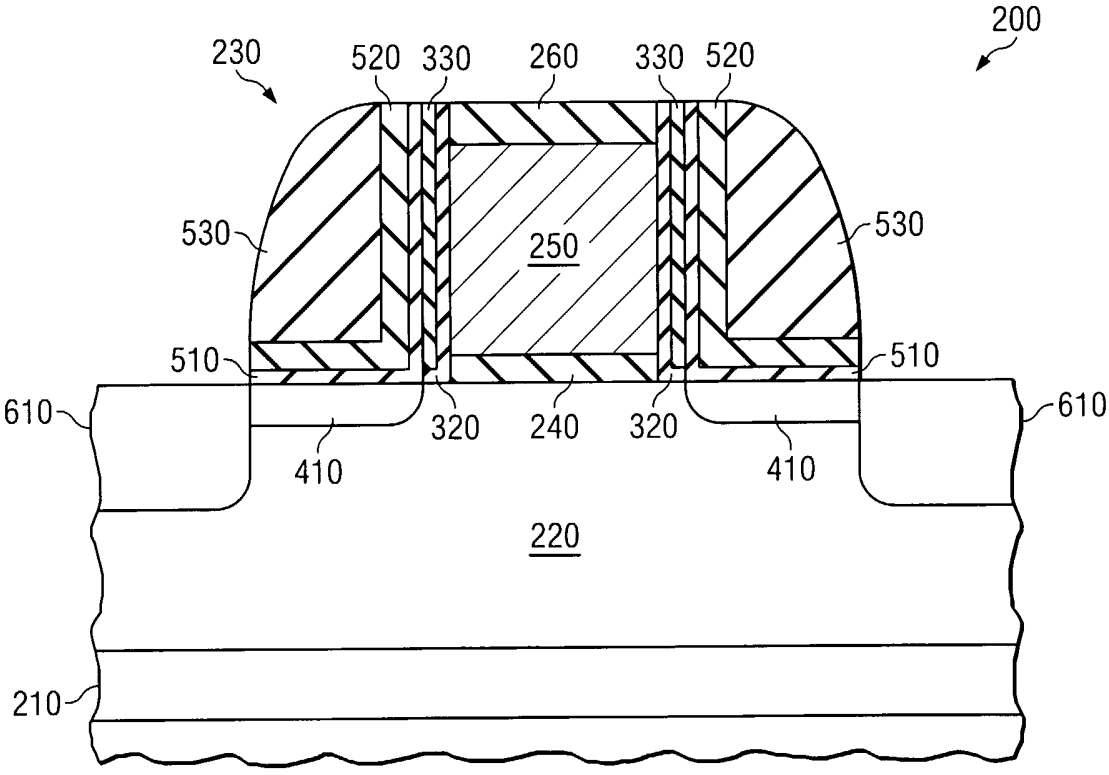

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FIG. 6

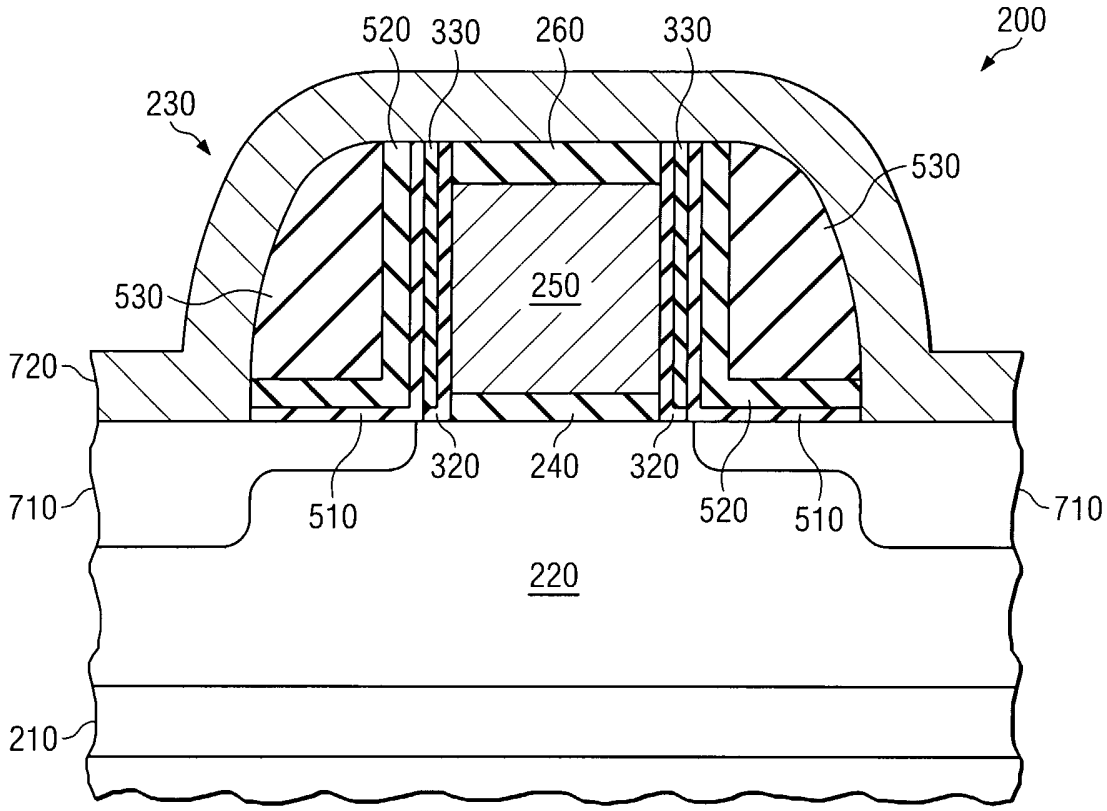

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FIG. 7

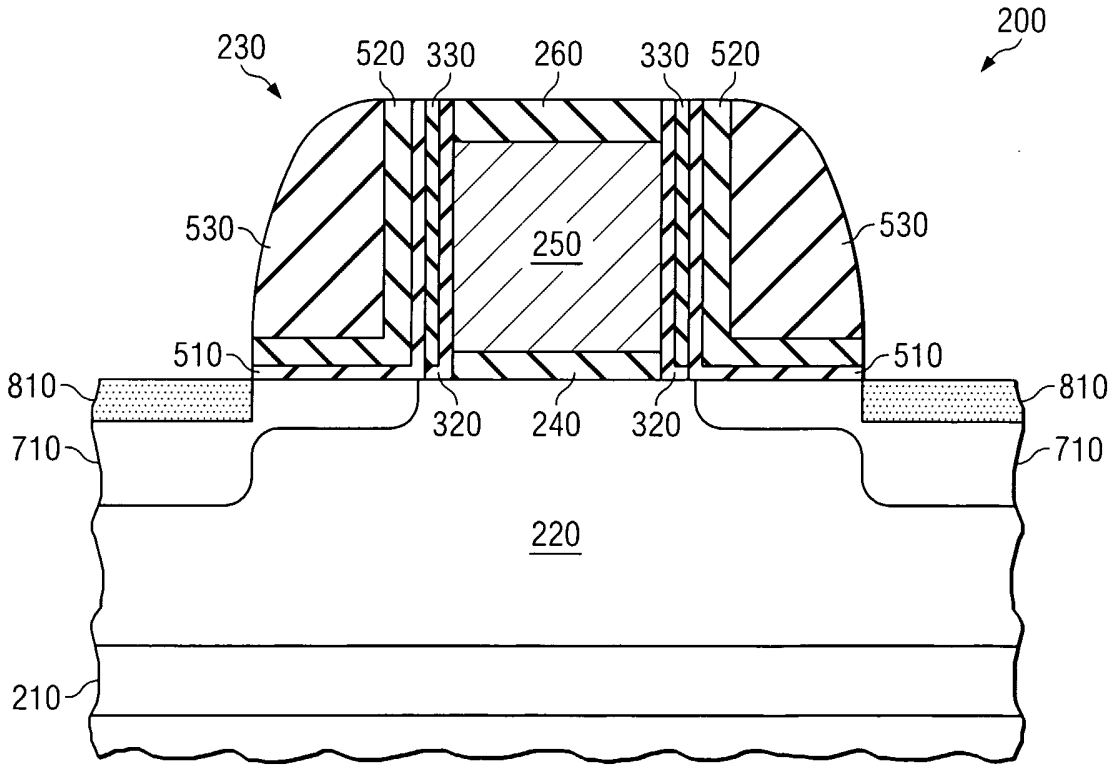

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FIG. 8

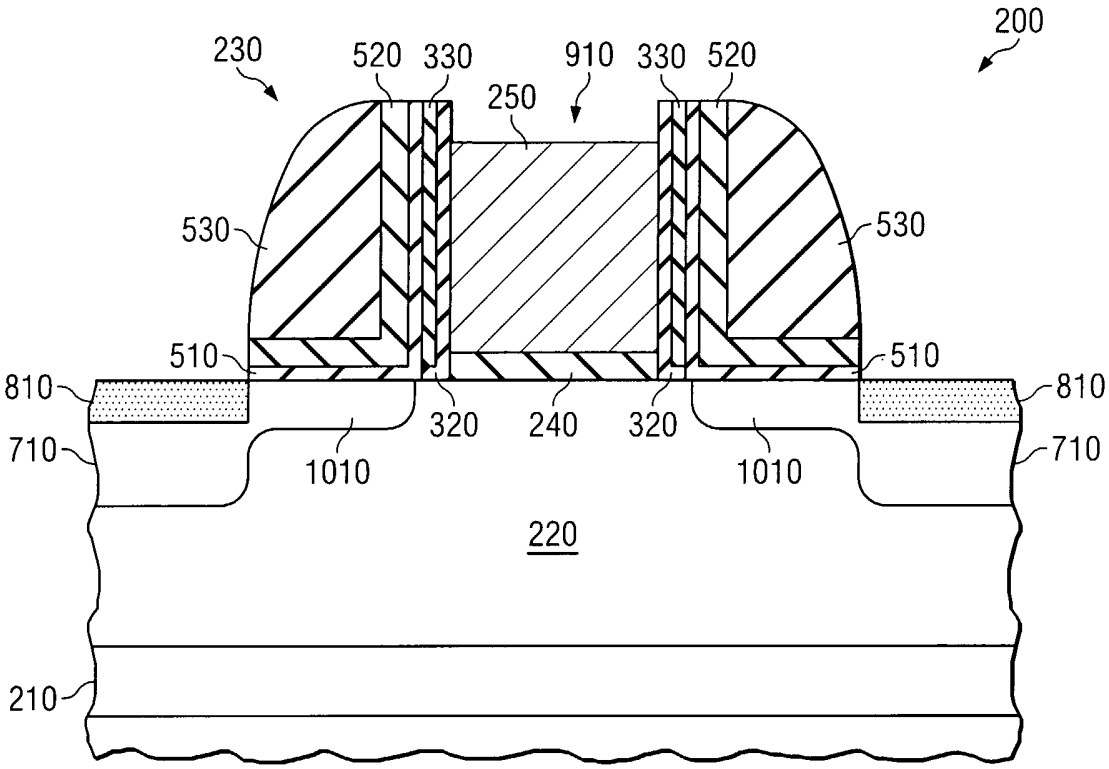

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FIG. 9

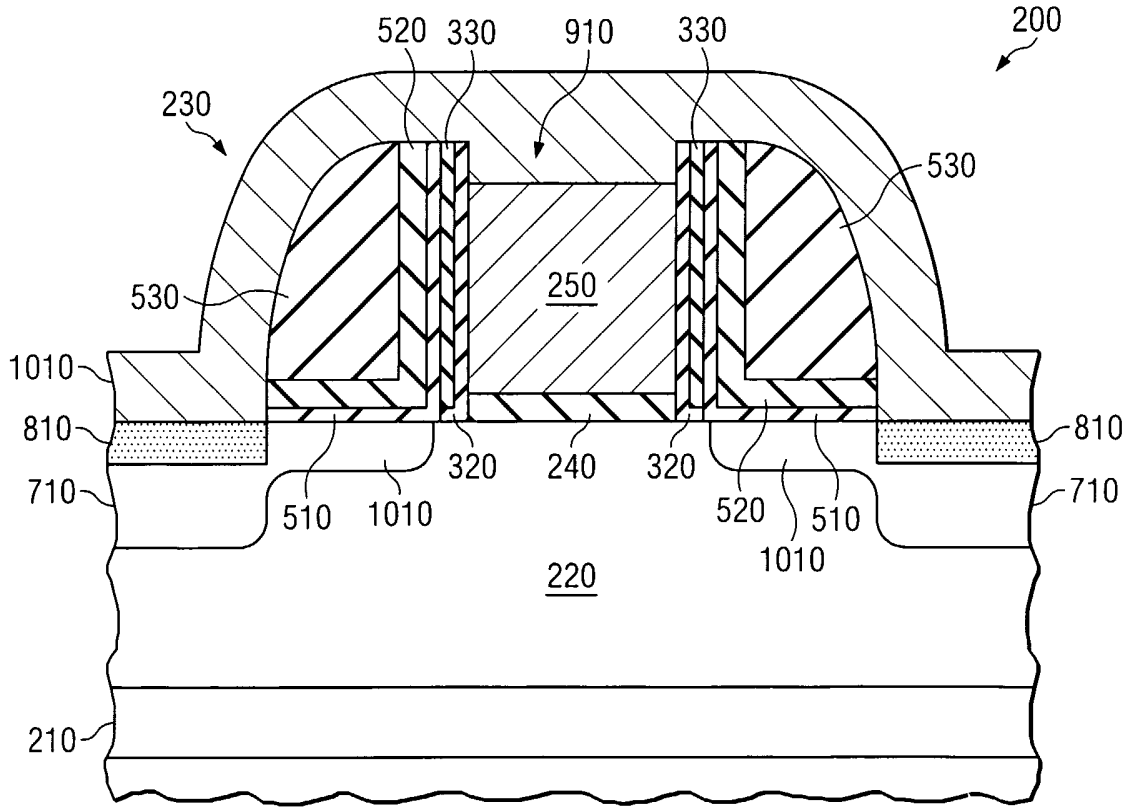

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FIG. 10

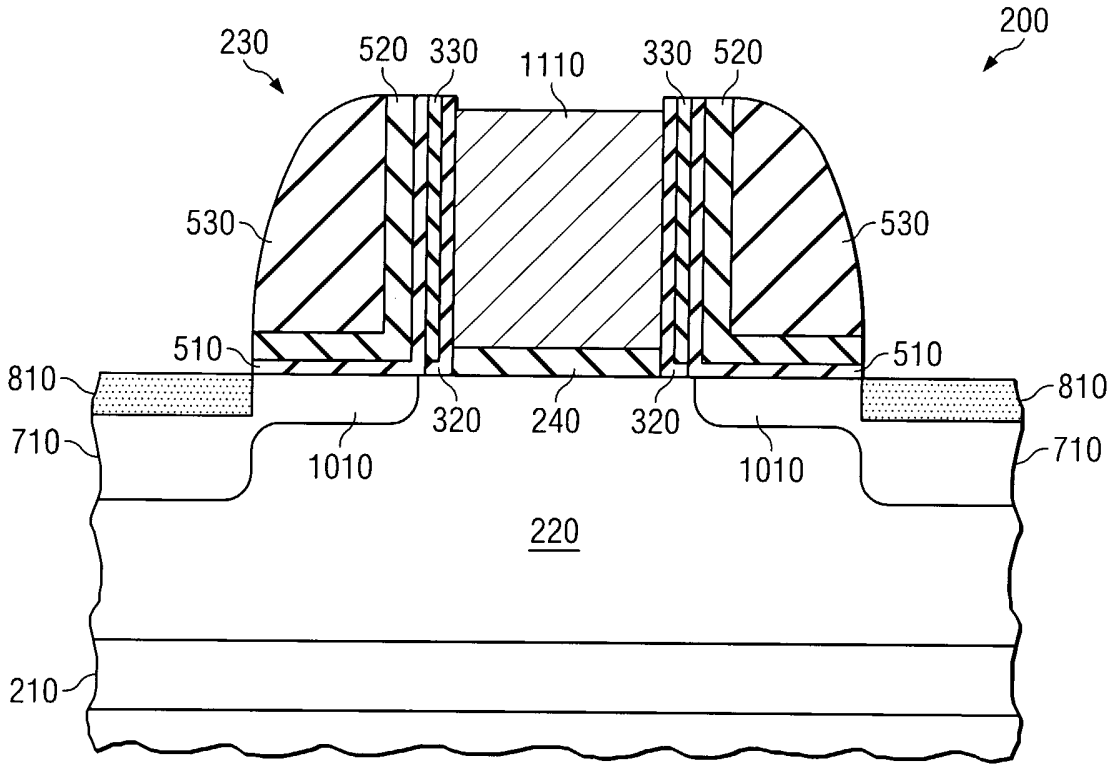

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FIG. 11

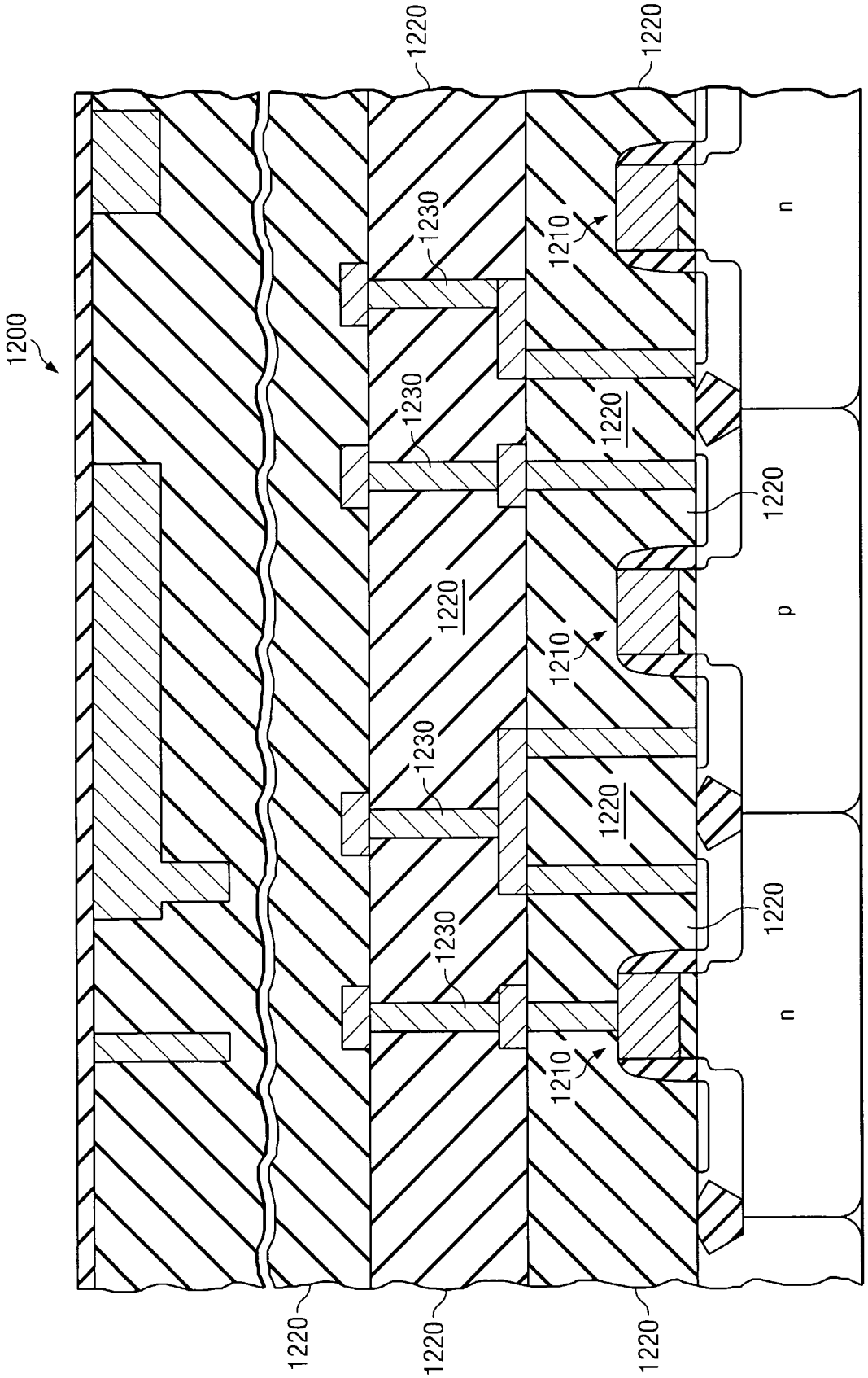

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FIG. 12

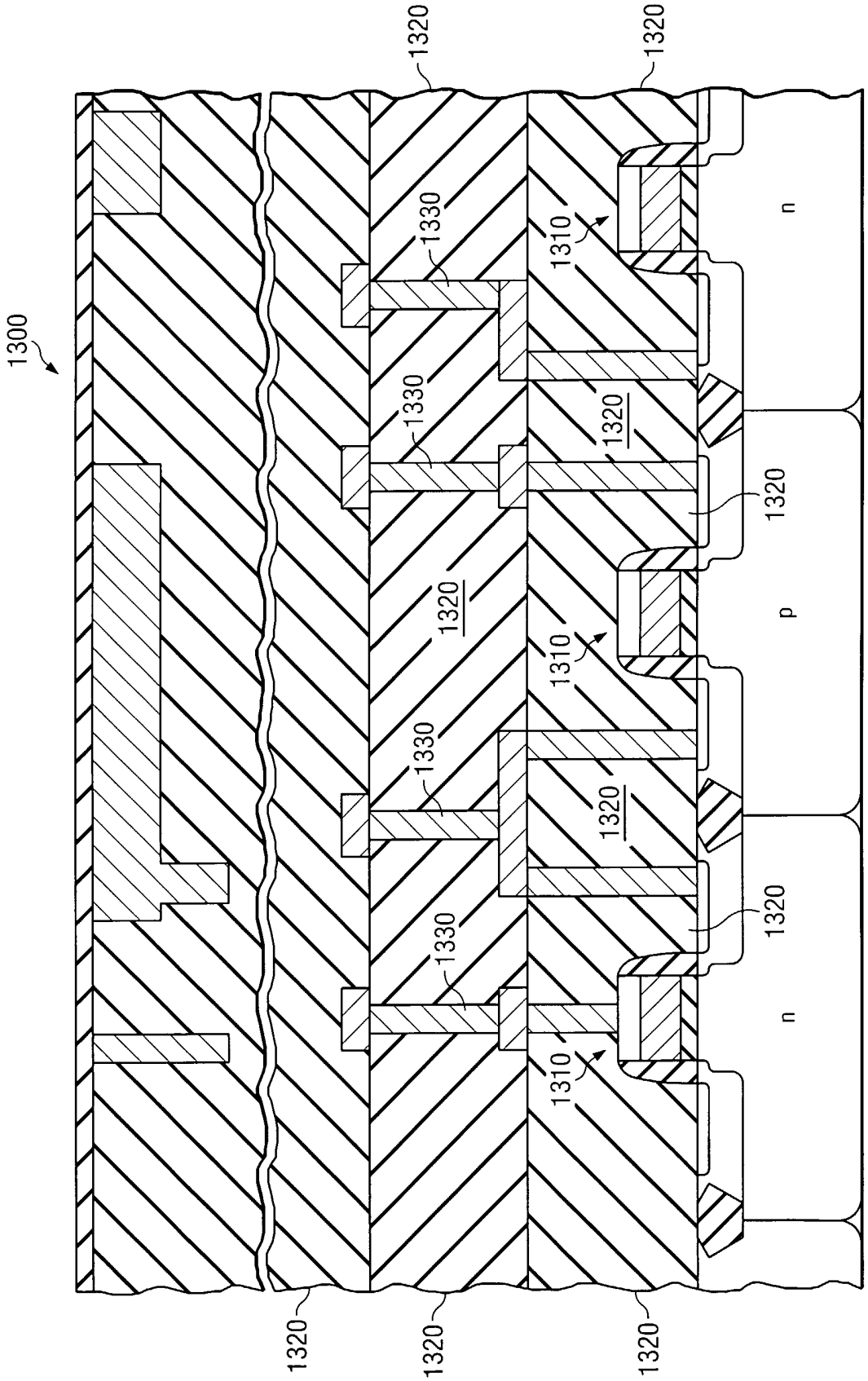

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FIG. 13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US05/10288

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : H01L 21/44
US CL : 438/583
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 438/583,592,649,651

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Continuation Sheet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,P --- Y,P	US 6,821,887 B2 (WIECZOREK et al.) 23 November 2004 (23.11.2004), see entire document.	1-3,7,9 --- 4-6,8,10-18
Y	US 6,555,453 B1 (XIANG et al.) 29 April 2003 (29.04.2003), see entire document.	4-6,8,13-15,17
Y	US 6,096,609 A (KIM et al.) 01 August 2000 (01.08.2000), see entire document.	10-18

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

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"E" earlier application or patent published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search
08 August 2005 (08.08.2005)

Date of mailing of the international search report
23 AUG 2005

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Authorized officer
JOSE DEES

Telephone No. 571-272-1569

Form PCT/ISA/210 (second sheet) (January 2004)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US05/10288

Continuation of B. FIELDS SEARCHED Item 3:
USPGPUB, USPAT, USOCR, EPO, JPO, DERWENT, IBM_TDB search terms: (((polysilicon adj gate adj electrode) and (source and drain) with (((protect$ or block$6 or mask$6) adj (layer or film)) with (silicide)) wit (silicid$5 or salcid$6)) and @ad < = "20040326", (((polysilicon adj gate adj electrode) and (source and drain)) with ((silicid$6 or salicid$6) adj gate)) and @ad < = "20040326"