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Olsen

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[54] POWER SEQUENCING CONTROL CIRCUIT

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[58] **Field of Search**.....307/235, 248, 130, 202, 239, 307/240, 241, 242, 243, 244, 246, 247, 249, 250, 251, 252, 253, 254, 255, 270, 284, 288, 290, 297; 317/31

[56] **References Cited**

UNITED STATES PATENTS

3,343,036	9/1967	Steen	317/31
3,475,061	10/1969	Steinkamp et al.	307/130
3,590,275	6/1971	Fisher	307/252 B
3,098,964	7/1963	Hetzler	307/297 X
3,227,942	1/1966	Bunch et al.	307/297 X
3,253,210	5/1966	Cummins	307/297 X
3,281,810	10/1966	Thornberg et al.	307/251 J X
3,389,325	6/1968	Gilbert	317/31 X
3,404,291	10/1968	Green et al.	307/246 X
3,412,314	11/1968	Crane	307/297 X
3,319,116	5/1967	Schick	307/235 X

OTHER PUBLICATIONS

Millman & Taub, Pulse Digital and Switching Waveforms, pgs. 297, 321–323; McGraw-Hill Inc. 1965.

Pressman, Design of Transisterized Circuits for Digital Computers; pgs. 9–221; 9–222; John F. Rider Publisher, Inc., 3/1959.

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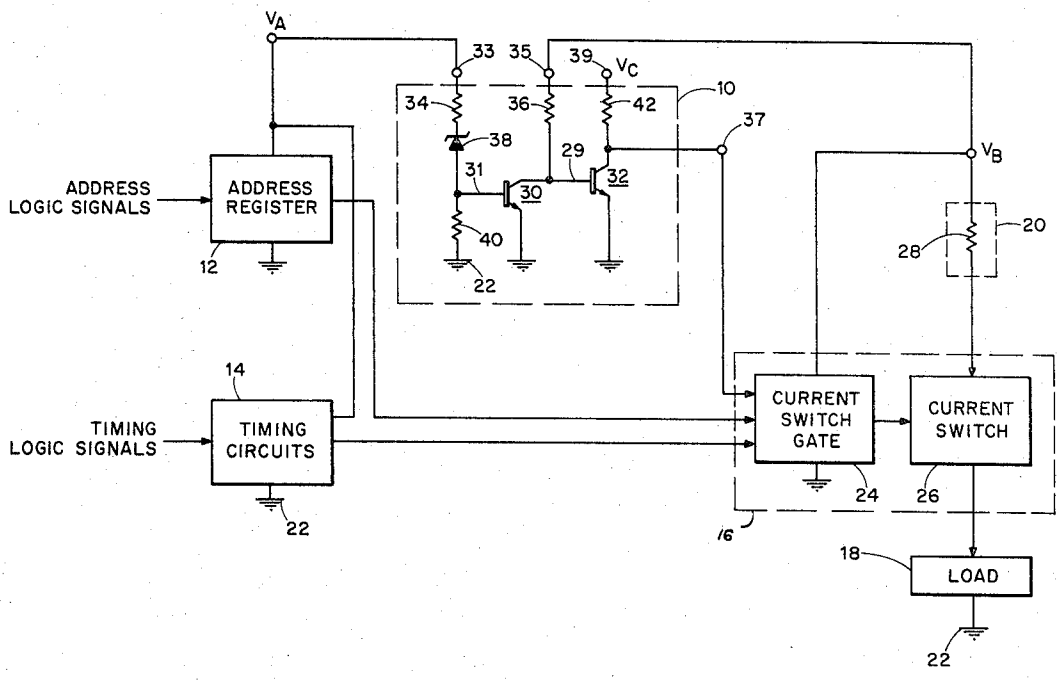
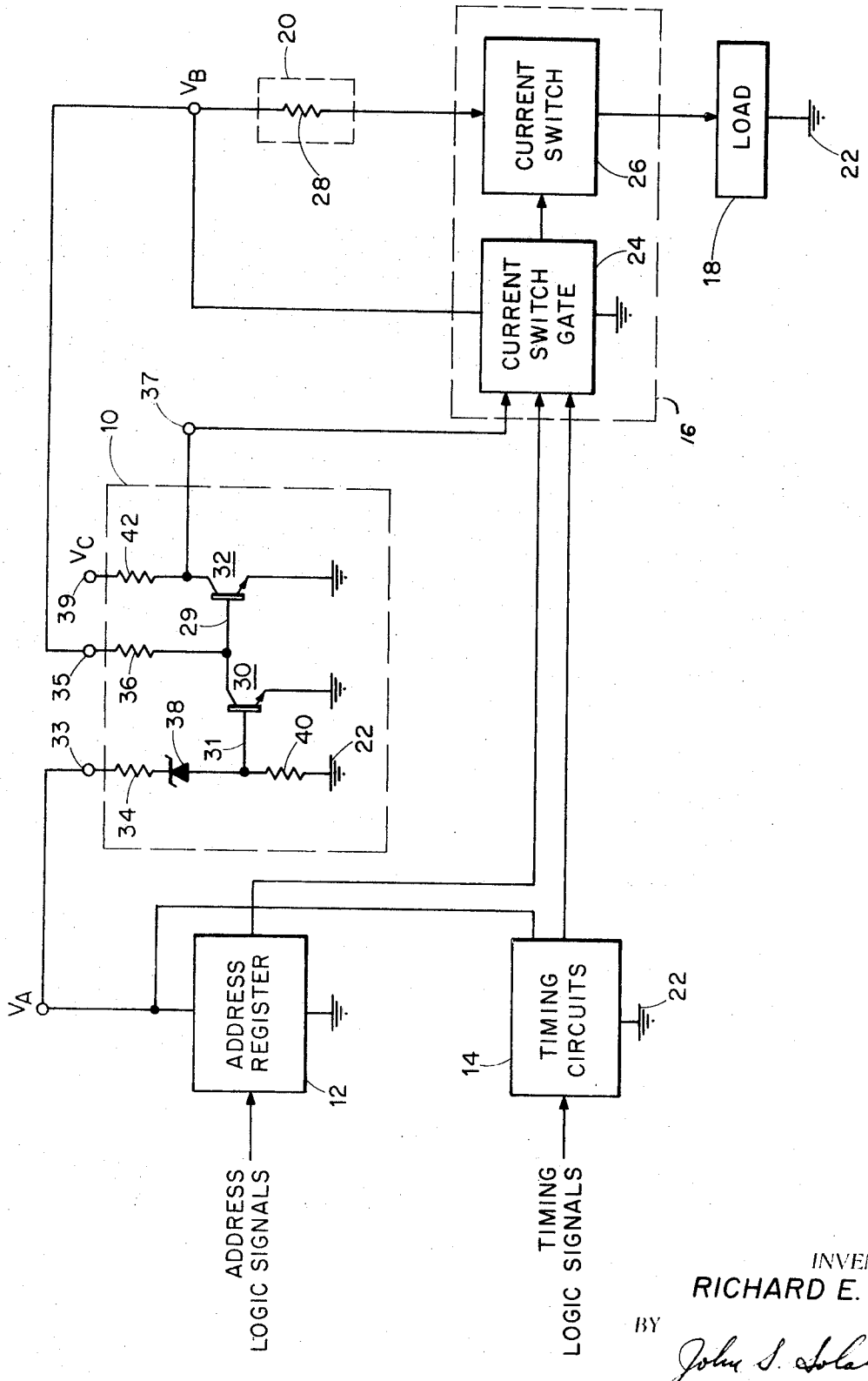
[57] **ABSTRACT**

Current applied to a load by means of a first voltage is disabled by control means in response to a change of a second voltage by a predetermined value. The control means is powered by the first voltage and includes two stages, a first for detecting a change of the second voltage and the second responsive to such change and powered by the first voltage for generating a signal for disabling the current applied to the load.

9 Claims, 1 Drawing Figure





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POWER SEQUENCING CONTROL CIRCUIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to control circuits and more particularly relates to means for terminating current supplied by a first voltage in response to a change in value of a second voltage.

2. Prior Art

In a core memory system, current through selection line circuits must not be allowed to flow unless all of the logic modules controlling these circuits are receiving enough supply voltage to function properly. One method of protecting circuitry is to utilize a fuse together with mechanical relays so that upon failure of the fuse, the mechanical relays remove all other voltages, however, when a fuse opens circuits a finite amount of time elapses before other voltages are removed due to the release time of the mechanical relays used in such protection circuits. Transistor control circuits have also been used in the prior art to remove one voltage in the event of failure of another voltage. Such a transistor circuit is shown in U.S. Pat. No. 3,122,646, patented Feb. 25, 1964. In such circuit of the prior art, a transistor, diode and resistive divider arrangement controls a first voltage in response to change of a second voltage. The apparent requirement of a third voltage for such control is a disadvantage of such prior art circuit. A circuit of the present invention detects a change in value of a first voltage and utilizes a second voltage to inhibit current produced from such second voltage.

It is therefore an object of this invention to provide an improved power control circuit requiring a minimal amount of components which utilizes the voltage of a current source to be controlled to inhibit current therefrom when a change in value of another voltage source is detected.

SUMMARY OF THE INVENTION

The purpose and objects of this invention are satisfied by providing a power sequencing control circuit which includes a first voltage for producing a current, a means for applying the current to a load, and a means for disabling the means for applying from supplying the current to the load in response to a first signal. A control means is provided which includes a first circuit stage for producing a second signal in response to a change of a second voltage below a predetermined value and the control means further includes a second circuit stage coupled to the first circuit stage and the first voltage for generating the first signal in response to the second signal.

BRIEF DESCRIPTION OF THE DRAWING

The advantage of the foregoing configuration of this invention will become more apparent upon reading the accompanying detailed description in connection with the sole FIGURE which illustrates a schematic diagram of the control circuit of the invention together with other elements with which the control circuit of the invention may be utilized.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the sole figure, a control circuit **10** is shown to receive a voltage V_A at terminal **33**, a voltage V_B at terminal **35**, and a utility voltage V_C at terminal **39**. VoltageV_C is shown as a separate voltage from voltage V_A but it should be understood that voltage V_C may be the same voltage as voltage V_A, i.e., terminal **39** may be connected to terminal **33**. Control circuit **10** includes an output control terminal **37** which in the presence of voltage V_B generates a high level signal when voltage V_A is at its normal value and which generates a low level signal when voltage V_A falls below a predetermined value. In one environment of the control circuit **10** of the invention, voltage V_A is utilized in a memory system to power an address register **12** and timing circuits **14** which receive address logic signals and timing logic signals respectively. Voltage V_B is utilized to provide current through a current source **20** shown in its simplest form as a resistor, **28** to a current switch **26**, to a load **18**, and to circuit ground **22**. Voltage V_B also powers a current switch gate **24**. Current switch gate **24** and current switch **26** are shown in combination within dotted lines **16** which combination may be that circuit produced by Texas Instruments Incorporated, having a Model No. SN75324, and further identified as a monolithic integrated circuit memory driver. Current switch gate **24** enables or disables current switch **26**. Current switch **26** is enabled when the outputs of address register **12**, timing circuits **14** and control terminal **37** are a high level. The absence of either one of the three input signals disables the memory selection lines or load **18** from receiving current from voltage V_B via current source **20**.

More particularly the control circuit **10** of the invention includes a first stage comprised basically of a resistor **34** coupled at one end to terminal **33** and coupled at the other end to the base electrode **31** of transistor **30**. Coupled to the first stage is a second circuit stage which basically includes a resistor **36** coupled at one end to terminal **35** and at the other end to base electrode **29** of transistor **32**. The collector electrode of transistor **32** is coupled to the control terminal **37**.

Basically, the operation of the control circuit **10** is as follows. When voltage V_A is at its normal voltage level, for example 5 to 6 volts, transistor **30** is turned on. Voltage V_B which for example may be approximately 14 to 15 volts, generates a current which passes through resistor **36** and which because of the turned on condition of transistor **30** allows such current to flow through the collector-emitter-path of transistor **30**. Accordingly, transistor **32** does not receive sufficient base current and remains turned off. The control terminal **37** thus provides a high signal level determined by the input characteristics of current switch gate **24** in the absence of the connection of resistor **42**. Note that as discussed herein, signal level refers to either current or voltage levels. Thus assuming the presence of the other two inputs to current switch gate **24**, the high signal level at control terminal **37** allows current switch **26** to provide current from voltage V_A to load **18**.

When voltage V_A goes below a predetermined value and the base current of transistor **30** is not sufficient for turn on, transistor **30** turns off, thereby diverting current from transistor **30** to the base-emitter-path of

transistor 32, turning transistor 32 on. The turned on condition of transistor 32 lowers the signal at control terminal 37 to essentially ground potential, thereby inhibiting current through load 18. Thus it can be seen that the voltage V_B which is utilized to provide current through load 18 is also utilized in the control circuit 10 to provide the bias current through transistor 32 to inhibit current through load 18. This is a fail safe situation since in any case, if voltage V_B fails current will not flow through load 18.

Control circuit 10 may also include a resistor 42 coupled at one end to the control terminal 37 and the collector of transistor 32 and coupled at the other end to terminal 39 which is coupled to receive a utility voltage V_C which for example may be approximately 5 to 6 volts. As stated hereinbefore voltage V_C may be directly connected to terminal 33 which is adapted to receive voltage V_A. The use of voltage V_C with resistor 42 enhances the circuit for noise immunity on the control terminal 37. Also shown is a Zener diode 38 which is coupled to one end of resistor 34 and at the other end to the base electrode 31 of transistor 30. Zener diode 38 is utilized to sharpen the voltage threshold at which the change in voltage V_A is detected. A resistor 40 is also shown connected to the base electrode 31 and to circuit ground 22. Resistor 40 is utilized to set the bias current in Zener diode 38. Thus in normal operation, with voltage V_A at its normal value, transistor 30 is turned on allowing current from terminal 35 to flow through resistor 36 and transistor 30 to circuit ground 22. With transistor 30 turned on, transistor 32 is turned off thereby raising the signal level of control terminal 37 to voltage V_C. When voltage V_A goes below the threshold value determined by resistors 34, 40 and Zener diode 38, transistor 30 turns off, turning on transistor 32 lowering the signal at control terminal 37 thereby inhibiting current through load 18.

Thus there has been shown a core memory system which utilizes a unique control circuit to inhibit current through selection line circuits (load) unless the logic modules such as the address register and timing circuits are receiving their proper supply voltage. It has also been seen that the control circuit of the invention is powered by the same voltage which supplies current to the load utilized in the system. This voltage inhibits current flow therefrom in response to another voltage which is detected for change in state by the control circuit of the invention. It has also been seen that such control has been provided with few components, basically two transistors and one resistor. It can be seen that certain changes may be made to the control circuit of the invention without departing from the scope thereof. For example, the NPN transistors which are utilized with positive voltages may have been PNP transistors utilized with negative voltages.

Having described the invention, what is claimed as new and secured by Letters Patent is:

1. A control circuit for a memory system which system includes addressing means and timing means powered by a second voltage source, current switch means powered by a first voltage source, said addressing means and said timing means coupled to enable said current switch means, and a memory selection line coupled to receive current by means of said current switch means and by means of said first voltage source, wherein said circuit is utilized for inhibiting said current in said selection line when said second voltage changes below a predetermined value, said circuit comprising:

A. a first circuit stage which produces a first signal when said second voltage source changes below said predetermined value;

B. a second circuit stage powered by said first voltage source and responsive to said first signal for producing a second signal; and

C. means coupling said second circuit stage to said current switch means so that the presence of said second signal inhibits said current.

2. A circuit as defined in claim 1 wherein:

A. said first circuit stage comprises a first transistor means which is turned on when said second voltage source is at its normal value and which is turned off producing said first signal when said second voltage source changes below a predetermined value, and wherein

B. said second circuit stage comprises a second transistor means which is turned off when said first transistor means is turned on and which is turned on by said first voltage source in response to said first signal, said first signal produced when said second transistor means is turned on.

3. A memory system comprising:

A. current switch means;

B. a first voltage source;

C. a memory selection line coupled to receive current by means of said current switch means and said first voltage source;

D. a second voltage source;

E. first circuit means comprising:

1. addressing means,

2. timing means, wherein said second voltage source provides power to said addressing means and said timing means, and

3. means for coupling said addressing means and said timing means to enable said current switch means;

F. a control circuit for inhibiting said current in said selection line when the value of said second voltage source changes by a predetermined amount, said control circuit comprising:

1. a first circuit stage which produces a first signal when said second voltage source changes by said predetermined amount;

2. a second circuit stage powered by said first voltage source and responsive to said first signal for producing a second signal; and

3. means for coupling said second circuit stage to said current switch means so that the presence of said second signal inhibits said current.

4. A circuit as defined in claim 3 wherein:

A. said first circuit stage includes a first transistor having a base, a collector and an emitter electrode;

B. said second circuit stage includes a second transistor having a base, a collector and an emitter electrode;

C. wherein said second voltage source is coupled to said base electrode of said fist transistor; and

D. wherein said first voltage source is coupled to said collector electrode of said first transistor and said base electrode of said second transistor.

5. A circuit as defined in claim 4 wherein said collector electrode of said second transistor is coupled to said current switch means.

6. A circuit as defined in claim 5 further comprising:

A. first resistive means coupled to receive said second voltage source at one end and coupled at the other end to said first transistor base electrodes;

B. second resistive means coupled to receive said first voltage source at one end and coupled at the other end to said first transistor collector electrode and said second transistor base electrode; and wherein

C. said first and second transistor emitter electrodes are coupled to a third voltage.

7. A circuit as defined in claim 6 further comprising:

A. Zener diode means coupled in the coupling between said first resistive means and said first transistor base electrode; and

B. fourth resistive means coupled between said first transistor base electrode and said third voltage.

8. A circuit as defined in claim 6 further comprising a third resistive means coupled at one end to said output terminal and at the other end to a fourth voltage.

9. A circuit as defined in claim 8 wherein said second and fourth voltages are equivalent.

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