



- (51) **International Patent Classification:**
H01L 29/78 (2006.01) *H01L 21/336* (2006.01)
- (21) **International Application Number:**
PCT/US2015/000193
- (22) **International Filing Date:**
23 December 2015 (23.12.2015)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (71) **Applicant:** INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95054 (US).
- (72) **Inventors:** LIU, En-Shao; 13340 Nw Keeton Park Lane, Portland, OR 97229 (US). PARK, Joodong; 2203 Nw Jesamine Way, Portland, OR 97229 (US). LEE, Chen-Guan; 14648 Nw Rich Court, Portland, OR 97229 (US). LIN, Jul-Yen; 3120 Nw John Olsen Avenue, Apt. 22203, Hillsboro, OR 97124 (US). JAN, Chia-Hong; 12849 Nw Lorraine Drive, Portland, OR 97229 (US).
- (74) **Agent:** BRODSKY, Stephen, I.; FINCH & MALONEY PLLC, c/o CPA Global, P.O. Box 52050, Minneapolis, MN 55402 (US).
- (81) **Designated States** (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM,

AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

- (84) **Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— of inventorship (*Rule 4.17(iv)*)

Published:

— with international search report (*Art. 21(3)*)

(54) **Title:** TRANSISTOR WITH INNER-GATE SPACER

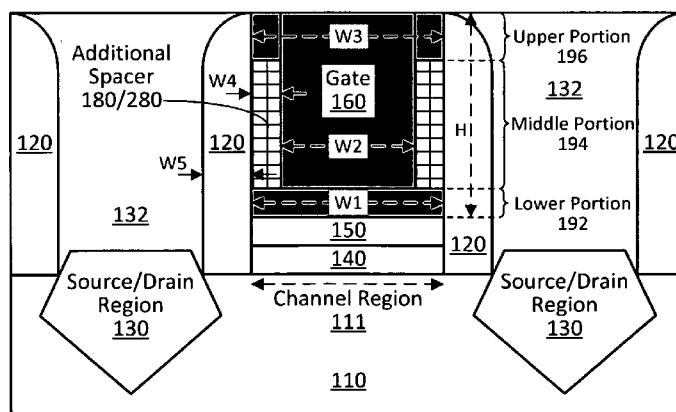


FIG. 2D

(57) **Abstract:** Techniques are disclosed for forming a transistor with one or more additional spacers, or inner-gate spacers, as referred to herein. The additional spacers may be formed between the gate and original spacers to reduce the parasitic coupling between the gate and the source/drain, for example. In some cases, the additional spacers may include air gaps and/or dielectric material (e.g., low-k dielectric material). In some cases, the gate may include a lower portion, a middle portion, and an upper portion. In some such cases, the lower and upper portions of the gate may be wider between the original spacers than the middle portion of the gate, which may be as a result of the additional spacers being located between the middle portion of the gate and the original spacers. In some such cases, the gate may approximate an I-shape, C-shape, D-shape, $\perp$ -shape, L-shape, or J-shape, for example.

TRANSISTOR WITH INNER-GATE SPACER

BACKGROUND

5 Semiconductor devices are electronic components that exploit the electronic properties of semiconductor materials, such as silicon (Si), germanium (Ge), and gallium arsenide (GaAs). A field-effect transistor (FET) is a semiconductor device that includes three terminals: a gate, a source, and a drain. A FET uses an electric field applied by the gate to control the electrical conductivity of a channel through which charge carriers (e.g., electrons or holes) flow from the
10 source to the drain. Some FETs have a fourth terminal called, the body or substrate, which can serve to bias the transistor into operation. A metal-oxide-semiconductor FET (MOSFET) uses an insulator between the gate and the body of the transistor and MOSFETs are typically used for amplifying or switching electronic signals. MOSFETs are one of the most common transistors in both digital and analog circuits. In some cases, MOSFETs include side-wall spacers, referred to
15 generally as spacers, on either side of the gate that can help determine the channel length and can help with replacement gate processes, for example.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A-F illustrate example integrated circuit structures resulting from a method configured to form a transistor including air gap inner-gate spacers, in accordance with some
20 embodiments of this disclosure.

Figures 2A-C illustrate example integrated circuit structures resulting from a method configured to form a transistor including dielectric material inner-gate spacers, in accordance with some embodiments of this disclosure.

Figure 2D illustrates the example structures of Figures 1F and 2C, with various
25 dimensions, regions, and portions indicated for ease of description, in accordance with some embodiments.

Figures 3A-F illustrate variations that may occur to the transistor gate of the example structure of Figure 2D, in accordance with some embodiments of this disclosure.

Figure 4 illustrates example non-planar transistor architectures including additional
30 spacers, in accordance with some embodiments of this disclosure.

Figure 5 illustrates a computing system implemented with integrated circuit structures or devices formed using the techniques disclosed herein, in accordance with some embodiments.

These and other features of the present embodiments will be understood better by reading the following detailed description, taken together with the figures herein described. In the drawings, each identical or nearly identical component that is illustrated in various figures may be represented by a like numeral. For purposes of clarity, not every component may be labeled in every drawing. Furthermore, as will be appreciated, the figures are not necessarily drawn to scale or intended to limit the described embodiments to the specific configurations shown. For instance, while some figures generally indicate straight lines, right angles, and smooth surfaces, an actual implementation of the disclosed techniques may have less than perfect straight lines and right angles, and some features may have surface topography or otherwise be non-smooth, given real-world limitations of fabrication processes. In short, the figures are provided merely to show example structures.

DETAILED DESCRIPTION

Techniques are disclosed for forming a transistor with one or more inner-gate spacers. These spacers are generally referred to herein as inner-gate spacers or additional spacers, because they are inside the standard (original) gate spacers normally provided on sides of the gate stack. The additional spacers may be formed between the gate and original gate spacers to reduce the parasitic coupling between the gate and the source/drain, for example. In some cases, the additional spacers may include air gaps and/or dielectric material (e.g., low-k dielectric material). In some cases, the gate may include a lower portion, a middle portion, and an upper portion, where the middle portion is between the lower and upper portions and where the lower portion is closer to the channel region than the middle portion. In some such cases, the lower portion of the gate may be wider between the original gate spacers than the middle portion of the gate, which may be as a result of the additional spacers being located between the middle portion of the gate and the original gate spacers. In such cases, the gate may approximate an upside down “T” shape (e.g., “⊥”). In still other such cases, the upper portion of the gate may also be wider between the original gate spacers than the middle portion of the gate (e.g., as a result of the deposition of additional gate material), which may form a gate that approximates an “I” shape (e.g., with the horizontal lines elongated somewhat). Numerous variations and configurations will be apparent in light of this disclosure.

General Overview

Numerous non-trivial challenges are present in fabricating semiconductor transistors particularly as the industry attempts to keep up with Moore’s law. For example, as dimensions of transistors, such as MOSFETs, keep scaling down, it becomes more and more challenging for

traditional lithography to reliably print small critical dimensions. A major factor in transistor delay is the parasitic capacitance around the gate, with a large contribution of the delay coming from the gate and source capacitance and/or the gate and drain capacitance, generally referred to herein as the gate-source/drain capacitance. Dielectric material referred to as side-wall spacers, gate spacers, or generally, spacers, can be formed on either side of the gate (between the gate and source/drain) to help lower the gate-source/drain capacitance, but such spacers have limits, particularly as dimensions of transistors keep scaling down. Some issues caused by continuous scaling of transistors has been addressed by relying on advances in lithography development. However, new lithography tools and next-generation lithography (NGL) techniques used to assist with achieving smaller critical dimensions during transistor formation, such as extreme ultraviolet lithography (EUVL), electron-beam lithography (EBL), and x-ray lithography, are costly and/or have low throughput issues.

Thus, and in accordance with one or more embodiments of this disclosure, techniques are provided for forming a transistor with one or more additional spacers, or so-called inner-gate spacers, as referred to herein. As previously described, side-wall spacers, sometimes referred to as gate spacers, or more generally, spacers, may be formed on either side of a transistor gate to help lower the gate-source/drain capacitance (or for other reasons, such as to help determine channel length and help with replacement gate processes, for example). In some embodiments, additional, inner-gate spacers can be formed inside of the original gate spacers and on either side of at least a portion of the gate to, for example, further reduce gate-source/drain parasitic capacitance. In some embodiments, the inclusion of the additional spacers may cause the gate to approximate an "I" shape, as will be apparent in light of the present disclosure. Further, in some such embodiments, the I-shaped gate may include a lower portion, a middle portion, and an upper portion, where the middle portion is narrower in width (dimension between the original gate spacers) than the lower and upper portions, as a result of the inclusion of the additional spacers, thereby forming an approximate I-shape when a cross section is taken in an orthogonal-to-gate direction. In some embodiments, the additional spacers may include air gaps and/or dielectric material (e.g., a low-k dielectric), for example. In some embodiments, the lower portion of the I-shaped gate may include a gate liner layer that is deposited prior to depositing the rest of the gate material, for example. In some such embodiments, the gate liner layer material may include different material than the rest of the gate, to enable selectively etching the gate liner layer material relative to the surrounding materials (e.g., to form trenches for the additional spacers), as will be described in more detail herein. In some embodiments, the upper

portion of the I-shaped gate may be formed using angled deposition techniques to, for example, add gate material at the gate contact location and increase contact surface area.

As previously described, in some embodiments, the term I-shaped is used to refer to gates formed using techniques described herein. However, in some such embodiments, the I-shape descriptor is not intended to limit such gates to an exact or perfect "I" shape. Instead, the I-shape descriptor is intended to be a general approximation of the shape of the gate, in some embodiments. Numerous variations on the shape of the gate will be apparent in light of this disclosure, and in some embodiments, the variations may be desired, while in other embodiments, the variations may be a result of real-world fabrication techniques. For example, in some embodiments, the additional, inner-gate spacer on one side of the gate may have a different width (dimension between the gate and original gate spacer) and/or height (dimension substantially perpendicular to the width) than the additional, inner gate spacer on the opposing side of the gate. In some such embodiments, an asymmetrical I-shaped gate may be formed. Further, in some embodiments, an additional spacer may only be formed on one side of the gate and not the other, such that the gate will only include one half of an "I" shape, and may more closely approximate a "C" shape or a backwards "C" shape, for example. In some embodiments, additional gate material may be deposited in the upper portion of the I-shaped gate to reduce contact resistance to the gate, for example. However, in still other embodiments, the upper portion of the I-shaped gate may not be formed, such that the gate may more closely approximate an upside down "T" or the perpendicular symbol (" $\perp$ "), for example. In some such embodiments, where the additional spacer is only formed on one side of the gate, the gate may more closely approximate an "L" shape, for example. Thus, numerous gate shapes can be manifested using one or more additional, inner-gate spacers as provided herein. The resulting gate shape may be symmetrical or asymmetrical, and may have one or more relatively thin gate regions above and/or below relatively wider gate region(s), depending on the forming process employed, as will be appreciated in light of this disclosure and the various example embodiments provided.

Numerous benefits will be apparent in light of this disclosure. For example, in some embodiments, the additional gate spacer reduces the undesired parasitic capacitance coupling at the gate-source/drain interface. In some embodiments, a wide range of additional spacer materials are enabled, such as various dielectric materials (e.g., low-k dielectrics or high-k dielectrics), air gaps, or any other suitable material depending on the end use or target application. In some embodiments, the area for source/drain contact materials is maximized, as the additional spacers are formed as inner spacers inside of the original gate spacers. In some

such embodiments, maximizing the area for source/drain contact materials can beneficially reduce the contact resistance to the source/drain regions. As previously described, in some embodiments, the techniques maintain the top area of the gate material, so the impact to the contact resistance between local interconnects and the gate is minimal or trivial (or there may be no impact, in some cases). In some embodiments, the techniques enable the use of photolithography techniques to address the issue of transistor delay caused by parasitic capacitance from the gate-source and/or gate-drain interface as opposed to attempting to address such issues using costly and/or low throughput next-generation lithography (NGL) techniques (e.g., EUVL, EBL, and x-ray lithography techniques).

Use of the techniques and structures provided herein may be detectable using tools such as scanning/transmission electron microscopy (SEM/TEM), composition mapping, x-ray crystallography or diffraction (XRD), secondary ion mass spectrometry (SIMS), time-of-flight SIMS (ToF-SIMS), atom probe imaging or tomography, local electrode atom probe (LEAP) techniques, 3D tomography, high resolution physical or chemical analysis, to name a few suitable example analytical tools. In particular, in some embodiments, such tools may indicate a structure or device configured with one or more additional, inner-gate spacers between the original gate spacers of a transistor and the transistor gate. In some such embodiments, the additional spacers may include air gaps and/or dielectric material (e.g., low-k dielectric material). In some embodiments, the techniques may form a gate having a lower portion (where the lower portion is closest to the transistor channel region or gate dielectric) that has a greater width between the spacers than a middle portion of the gate. In some such embodiments, the lower portion may include the gate liner layer material and the middle portion may include additional spacers on either side. As can be understood based on the present disclosure, in some such embodiments, the additional spacers occupy space that would otherwise be occupied by gate material, thereby creating the narrower middle portion of the gate. In some such embodiments, the gate may be approximately I-shaped and include a lower portion, a middle portion, and an upper portion, where the middle portion is narrower in width (dimension between the original gate spacers) than the lower and upper portions, for example. Other example gate shapes derivative of the I-shape may be manifested, in some embodiments (e.g., C-shape, J-shape, L-shape, I-shape, J-shape, [-shape, t-shape, J-shape, to provide a few examples). In some embodiments, the techniques described herein may be detected based on the materials of different transistor features observed, for example. In some embodiments, the technique can be detected by measuring the benefits achieved, such as the improvements in parasitic capacitance

coupling at the gate-source/drain interface, for example. Numerous configurations and variations will be apparent in light of this disclosure.

Architecture and Methodology

Figures 1A-F illustrate example integrated circuit structures resulting from a method configured to form a transistor including air gap inner-gate spacers, in accordance with some embodiments of this disclosure. Figures 2A-C illustrate example integrated circuit structures resulting from a method configured to form a transistor including dielectric material inner-gate spacers, in accordance with some embodiments of this disclosure. The illustrations provided in Figures 1A-F and 2A-C are along the orthogonal-to-gate direction, illustrating a cross-sectional view that may be achieved, for example, using SEM or TEM. In some embodiments, the inner-gate or additional spacers may result in an I-shaped gate, as will be described in more detail herein. Note that, in some embodiments, although the final gate structure is primarily depicted as approximately I-shaped (e.g., in Figures 1F and 2C), numerous variations on the gate shape and additional spacer configurations will be apparent in light of this disclosure (e.g., as described with reference to Figures 3A-F). Also note that although the integrated circuit structures are primarily depicted in the context of forming a transistor having a planar configuration, the present disclosure is not intended to be so limited. For example, in some embodiments, the techniques described herein may be used to form a transistor having a non-planar configuration, such as a dual-gate configuration, finned configuration (e.g., finFET or tri-gate), or gate-all-around configuration (e.g., including one or more nanowires or nanoribbons), as will be described in more detail with reference to Figure 4. Further, in some embodiments, the techniques can be used to form p-type and/or n-type transistor devices, such as p-type MOSFET (p-MOS), n-type MOSFET (n-MOS), p-type tunnel FET (p-TFET), or n-type TFET (n-TFET), to name a few examples. Further yet, in some embodiments, the techniques may be used to benefit either or both of p-type and n-type transistors included in complementary MOS (CMOS) or complementary TFET (CTFET) devices, for example. Further still, in some embodiments, the techniques may be used with devices of varying scales, such as transistor devices having critical dimensions in the micrometer range or in the nanometer range (e.g., transistors formed at the 32, 22, 14, 10, 7, or 5 nm process nodes, or beyond).

Figure 1A illustrates an example integrated circuit structure after source/drain processing has been performed and after the gate region has been opened to form the example resulting structure shown, in accordance with an embodiment. As shown, the example structure includes substrate 110, source/drain regions 130 located above and in substrate 110, source/drain contacts 132 located on the source/drain regions 130, and spacers 120 adjacent to the source/drain

contacts 132 and also adjacent to the gate trench 122. As can be understood based on Figure 1A, in some embodiments, the structure may have included a dummy gate stack prior to removal to form gate trench 122 in the structure shown. In some such embodiments, formation of the dummy gate stack may have included dummy gate oxide deposition, dummy gate electrode (e.g., poly-Si) deposition, and patterning hardmask deposition, for example. Such deposition processes may include any suitable deposition techniques, such as chemical vapor deposition (CVD), atomic layer deposition (ALD), physical vapor deposition (PVD), and/or any other suitable process, depending on the dummy gate being formed. Additional processing may include patterning the dummy gate material to form the shape of the gate trench 122 shown, for example. As can be understood based on this disclosure, the dummy gate was used as a sacrificial structure, which may have allowed for the formation of other components, such as spacers 120. As can also be understood, the dummy gate may have protected the gate region (e.g., the surface under gate trench 122) during processing, such as during the source/drain 130, 132 processing. Note that although the techniques are illustrated in this example embodiment in a gate last process flow, in some embodiments, the techniques may be performed in a gate first process flow, such that the additional spacers are formed prior to source/drain processing, for example, or at any other suitable stage of the transistor fabrication process flow.

In some embodiments, substrate 110 may include: a bulk substrate including a group IV material or compound, such as silicon (Si), germanium (Ge), silicon carbide (SiC), or SiGe and/or at least one group III-V compound and/or sapphire and/or any other suitable material(s) depending on the end use or target application; an X on insulator (XOI) structure where X is one of the aforementioned materials (e.g., group IV and/or group III-V and/or sapphire) and the insulator material is an oxide material or dielectric material or some other electrically insulating material; or some other suitable multilayer structure where the top layer includes one of the aforementioned materials (e.g., group IV and/or group III-V and/or sapphire). Note that group III-V compounds/materials include at least one group III element (e.g., aluminum, gallium, indium, boron, thallium) and at least one group V element (e.g., nitrogen, phosphorus, arsenic, antimony, bismuth), such as gallium nitride (GaN), gallium arsenide (GaAs), indium gallium nitride (InGaN), and so forth. Although substrate 110 in this example embodiment as having a thickness (the vertical dimension, as shown) similar to the other features for ease of illustration, in some instances, substrate 110 may be much thicker than the other features, such as having a thickness in the range of 50 to 950 microns, for example. In some embodiments, substrate 110 may be used for one or more other integrated circuit (IC) devices, such as various diodes (e.g., light-emitting diodes (LEDs) or laser diodes), various transistors (e.g., MOSFETs or TFETs),

various capacitors (e.g., MOSCAPs), various microelectromechanical systems (MEMS), various nanoelectromechanical systems (NEMS), various sensors, or any other suitable semiconductor or IC devices, depending on the end use or target application. Accordingly, in some embodiments, the transistor structures described herein may be included in a system-on-chip (SoC) application, as will be apparent in light of this disclosure.

In some embodiments, spacers 120 may be formed using a dummy gate stack, as previously described. The material of spacers 120, in some embodiments, may include any suitable materials, such as dielectric materials, oxides (e.g., a silicon oxide material), and/or nitrides (e.g., a silicon nitride material). In some embodiments, gate trench 122 may be formed by removing a dummy gate stack, as previously described, using, for example, wet and/or dry etch processes. Note that in some embodiments, the areas outside of gate trench 122 (e.g., the source/drain contact 132 areas) may be covered by an insulating material, such as an inter-layer dielectric (ILD) material, to allow for subsequent processing, as illustrated in Figure 4 and described below.

As can be seen in this example embodiment, source/drain regions 130 may have been formed by etching out a portion of substrate 110 and depositing (or growing or regrowing) the source/drain region 130 material, using, for example an epitaxial deposition process such as CVD, metal-organic chemical vapor deposition (MOCVD), or molecular-beam epitaxy (MBE), to name a few example processes. In some embodiments, the source/drain epitaxial regions may be grown after performing an etch-under-cut (EUC) process. In some such embodiments, the source/drain regions may extend under spacers 136 and/or under the gate stack, and such extended portions may be referred to as source/drain tips or extensions, for example. In some embodiments, the source/drain may be completely in the substrate, may be a portion of the substrate (e.g., including doping or otherwise altered), may be over the substrate, or any combination thereof. In some embodiments, source/drain regions 130 may include any suitable materials and suitable dopants, depending on the end use or target application. For example, in an embodiment where substrate 110 includes silicon and the transistor device is to be a p-type MOSFET, source/drain regions 130 may both include p-type doped silicon (e.g., where boron is the p-type dopant). In another example embodiment, where substrate 110 includes silicon and the transistor device is to be an n-type MOSFET, source/drain regions may both include n-type doped silicon (e.g., where phosphorus is the n-type dopant). In some embodiments, any suitable source/drain 130 material and optional doping schemes may be used, depending on the end use or target application. For example, in TFET configurations, the source and drain regions 130

may be oppositely type doped (e.g., source is p-type doped and drain is n-type doped), with the channel region being minimally doped or undoped (or intrinsic/i-type).

In some embodiments, the source/drain region 130 material may be native to substrate 110 and may or may not include doping (e.g., via implantation), or the source/drain region 130 material may be formed using replacement material, which may or may not include removing a portion of the substrate to form source/drain trenches for deposition/growth of the replacement source/drain regions 130. In some embodiments, source/drain regions 130 may include a multi-layer structure of two or more material layers. In some embodiments, source/drain regions 130 may include grading (e.g., increasing and/or decreasing) the content of one or more materials in at least a portion of the regions 130. For instance, in some embodiments, a passivation material may be deposited prior to the deposition of the primary source/drain material to assist with the quality of the interface between the source/drain material and the substrate material, for example, depending on the end use or target application. Further, in some embodiments, a contact-improving material may be formed on the top of the source/drain region material to assist with making contact to source/drain contacts 132, for example, depending on the end use or target application. In some embodiments, source/drain regions 130 may extend under spacers 120 and may even extend under the gate region (e.g., under gate trench 122 in Figure 1A), and such extended source/drain portions may be referred to as source/drain extensions or tips. For example, in the structure shown in the embodiment of Figure 1A, the source/drain regions partially extend under spacers 120 (e.g., they extend about halfway under the spacers 120). The techniques described herein are not intended to be limited to any specific source/drain configuration.

In some embodiments, source/drain contacts 132 may be formed using any suitable techniques, such as using any suitable deposition processes (e.g., CVD, ALD, or PVD). In some embodiments, source/drain contacts 132 may include any suitable material, such as a conductive metal or alloy (e.g., aluminum, tungsten, silver, nickel-platinum, or nickel-aluminum). In some embodiments, metallization of the source/drain contacts 132 may be carried out, for example, using a silicidation or germanidation process (e.g., generally, deposition of contact metal followed by annealing).

Figure 1B illustrates an example structure after gate dielectric layer 140 and optional work-function layer 150 have been formed in the gate trench 122 of the structure of Figure 1A, in accordance with an embodiment. In some embodiments, gate dielectric layer 140 and optional work-function layer 150 may be formed using any suitable techniques, such as using any suitable deposition processes (e.g., CVD, ALD, or PVD). In some embodiments, the material of layers

140 and/or 150 may be conformal to the inside of gate trench 122, such that some material is formed on the sides of the gate trench 122. In some such embodiments, the material on the sides of the gate trench 122 may be removed using a wet or dry etch process, for example. In other embodiments, some material or material layers (e.g., the gate dielectric layer 140) may remain on the trench sides. For example, in some such embodiments, where a portion of the gate dielectric layer 140 is on the gate trench 122 sides (e.g., based on desired processing and/or as a result of real-world fabrication), the gate dielectric layer 140 may approximate a U-shape, or if the layer 140 was on just one side, it may approximate an L-shape or a backwards L-shape, for example. As will be understood based on the present disclosure, in some such embodiments, the additional spacers may be formed on the inside of such vertical portions of the gate dielectric layer 140, for example. In some embodiments, gate dielectric 140 may include silicon dioxide and/or a high-k dielectric material, depending on the end use or target application. Examples of high-k gate dielectric materials include, for instance, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric layer 140 to improve its quality when a high-k material is used, for example. In some embodiments, gate dielectric layer 140 may include a multi-layer structure of two or more material layers. In some embodiments, gate dielectric layer 140 may include grading (e.g., increasing and/or decreasing) the content of one or more materials in at least a portion of the gate dielectric layer 140.

In some embodiments, one or more work-function layers 150 may be present to increase the interface quality between the gate dielectric 140 and subsequently deposited gate material and/or to improve the electrical properties between the gate dielectric 140 and the subsequently deposited gate material, for example. In embodiments where the one or more work-function layers 150 are present, the material of the one or more layers may include any suitable material, such as a non-metal, metal, or metal alloy material, depending on the end use or target application. However, in some embodiments, the one or more work-function layers 150 need not be present.

Figure 1C illustrates an example structure after gate liner layer 162 has been formed above the gate dielectric 140 (and above work-function layer 150, where present) of the structure of Figure 1B, in accordance with an embodiment. In some embodiments, gate liner layer 162 may be deposited or grown in a conformal manner, such that the layer is deposited as shown in Figure 1C, for example. In some embodiments, gate liner layer 162 may be deposited or grown using

any suitable processes (e.g., CVD, ALD, or PVD) in a majority of or the entirety of the space above work-function layer 150, and additional processing may then be performed to form the shape of the gate liner layer 162 shown (e.g., planarize/polish followed by a dry etch process to remove gate liner layer material).

Figure 1D illustrates an example structure after gate body 164 material has been formed on the gate liner layer 162 of the structure of Figure 1C, in accordance with an embodiment. Note that in this example embodiment, gate body 164 is referred to as such to assist with description of the various gate components, as the final gate 160 may include gate liner layer 162, gate body 164, and optionally additional gate material 166, in some embodiments, as will be described in more detail with reference to Figures 2D and 3B. In some embodiments, gate body 164 may be deposited or grown using any suitable processes (e.g., CVD, ALD, or PVD), and in some cases, such deposition/growth may be followed by a planarization or polish process to form the structure shown in Figure 1D, for example. In some embodiments, the material of gate liner 162 and gate body 164 may include any suitable material, such as polysilicon, silicon nitride, silicon carbide, or various suitable metals or metal alloys, such as aluminum (Al), tungsten (W), titanium (Ti), tantalum (Ta), copper (Cu), titanium nitride (TiN), or tantalum nitride (Ta₂N₃), for example. In some embodiments, the gate liner layer 162 material may be selected to have a higher relative etch rate for a given etchant than the etch rate of the selected gate body 164 material, such that at least a portion of the gate liner layer 162 can be selectively etched and removed (e.g., from the side-walls of gate body 164 to form, for example, the resulting structure shown in Figure 1E). In some such embodiments, the selectivity of the etch may be such that the gate liner layer 162 material may be removed at a rate of at least 1.5, 2, 3, 5, 10, 25, 50, or 100 times faster than the material surrounding features (e.g., gate body 164), or some other suitable minimum relative selective etch rate, for a given etchant. For instance, in an embodiment, gate liner layer 162 material may include aluminum and gate body 164 material may include tungsten, where a suitable etchant may include an SC-1 etchant, such as ammonium hydroxide (NH₄OH) or hydrogen peroxide (H₂O₂), to provide one specific example combination. In such an example combination, the SC-1 etchant can selectively etch out the Al gate liner layer 162 material, as will be described in more detail below.

Figure 1E illustrates an example structure after gate liner layer 162 was selectively etched from the side-walls of gate body 164 from the structure of Figure 1D to form additional spacer trenches 170, in accordance with an embodiment. As previously described, the material of gate liner layer 162 may be selected, in some embodiments, such that it can be selectively removed (e.g., via a wet etch process) relative to surrounding materials (such as the material of gate body

164). Accordingly, in some such embodiments, a suitable etchant may be used to selectively remove gate liner layer 162 material and form additional spacer trenches 170. In some embodiments, the etch depth may be controlled by total etch time and/or etch rate, or other process conditions, for example. Continuing from the structure of Figure 1E, in some
5 additional spacer trenches 170 may be kept as air space to form air gap additional spacers 180 on either side of a portion of gate body 164, as will be described with reference to the example structure of Figure 1F, while in other embodiments, the additional spacer trenches 170 may be filled with a dielectric material to form dielectric additional spacers 280, as will be described with reference to the example structures of Figures 2A-C. Numerous
10 variations on the transistor structures will be apparent in light of this disclosure, and some such variations will be described with reference to Figures 3A-F, in accordance with some embodiments.

Figure 1F illustrates an example structure after additional gate material 166 has been deposited in the upper portion of additional spacer trenches 170 of the structure of Figure 1E, in
15 accordance with an embodiment. As can also be seen, in this example embodiment, depositing additional gate material 166 forms air gap additional spacers 180 on either side of gate body 164, where the additional spacers 180 are between the gate body 164 and originally formed spacers 120. In some embodiments, additional gate material 166 may be deposited using an angled deposition or growth process (e.g., using angled CVD or PVD) to form the additional gate
20 material 166 in only an upper portion of the additional spacer trenches 170. In some such embodiments, the deposition process may be performed at an angle in the range of, for example, 5-75 degrees relative to horizontal (major access of substrate 110), where 90 degrees relative to horizontal would represent depositing the additional gate material straight down into additional spacer trenches 170. As can be understood based on this disclosure, in some embodiments, the
25 angle used for the deposition process may affect the amount of additional gate material 166 formed in the upper portion of additional spacer trenches 170 and thereby affect the size of additional spacers 180. In some embodiments, a planarization and/or polish process may be performed after the angled deposition process to form the example structure of Figure 1F.

In some embodiments, additional gate material 166 may include any suitable material, such
30 as polysilicon, silicon nitride, silicon carbide, or various suitable metals or metal alloys, such as aluminum (Al), tungsten (W), titanium (Ti), tantalum (Ta), copper (Cu), titanium nitride (TiN), or tantalum nitride (TaN), for example. In some embodiments, additional gate material 166 may include the same material as the material of gate body 164, while in some embodiments, additional gate material 166 may include different material than the material of gate body 164.

In some embodiments, additional gate material 166 may include the same material as the material of gate liner layer 162, while in some embodiments, additional gate material 166 may include different material than the material of gate liner layer 162. In some embodiments, additional gate material 166 may be formed to maintain gate contact area for local interconnects, which can help ensure that the structure does not pay a contact resistance penalty as a result of the additional spacers 180, for example. Therefore, in some such embodiments, the gate-source/drain parasitic capacitance can be reduced with minimal or no increase in contact resistance to the gate 160.

Figure 2A illustrates an example structure after dielectric material 280 (to be used as additional spacers) is deposited in the additional spacer trenches 170 of the structure of Figure 1E, in accordance with an embodiment. As previously described, in some embodiments, the fabrication process may continue from the structure of Figure 1E to form dielectric material additional spacers (as opposed to air gap additional spacers). In some embodiments, the additional spacer dielectric material 280 may be deposited using any suitable deposition or growth process (e.g., CVD, ALD, or PVD), and in some cases, such deposition/growth may be followed by a planarization or polish process to form the structure shown in Figure 2A, for example. In some embodiments, the dielectric material 280 may be any suitable dielectric, such as silicon dioxide (having a dielectric constant, k , of 3.9), a low- k dielectric (materials having a dielectric constant lower than that of silicon dioxide; $k < 3.9$), or a high- k dielectric (materials having a dielectric constant higher than that of silicon dioxide; $k > 3.9$), depending on the end use or target application. In some such embodiments where the dielectric material 280 is a low- k dielectric, the material may include carbon and/or fluorine-doped silicon dioxide, porous silicon dioxide, porous carbon and/or fluorine-doped silicon dioxide, or any other suitable low- k dielectric material. In some embodiments, additional spacer dielectric material 280 may include a multi-layer structure of two or more material layers. In some embodiments, additional spacer dielectric material 280 may include grading (e.g., increasing and/or decreasing) the content of one or more materials in at least a portion of the material 280.

In some embodiments, the additional spacer dielectric material 280 may be selected to have a higher relative etch rate for a given etchant than the etch rate of the selected original spacer 120 material, such that at least a portion of the additional spacer dielectric material 280 can be selectively etched and recessed (e.g., to form the resulting structure shown in Figure 2B). In some such embodiments, the selectivity of the etch may be such that the additional spacer dielectric material 280 may be removed at a rate of at least 1.5, 2, 3, 5, 10, 25, 50, or 100 times faster than the material of surrounding features (e.g., original spacers 120), or some other

suitable minimum relative selective etch rate, for a given etchant. For instance, in an embodiment, additional spacer dielectric material 280 may include silicon dioxide and the material of original spacers 120 may include silicon nitride, where a suitable etchant may include dilute hydrofluoric acid (DHF), to provide one specific example combination. In such an example combination, the DHF can selectively etch out the silicon dioxide additional spacer material 280, as will be described in more detail below.

Figure 2B illustrates an example structure after additional spacer dielectric material 280 has been etched to form recesses 270 in the structure of Figure 2A, in accordance with an embodiment. As previously described, the material of additional spacer dielectric material 280 may be selected, in some embodiments, such that it can be selectively removed (e.g., via a wet etch process) relative to surrounding materials (such as the material of original spacers 120). Accordingly, in some such embodiments, a suitable etchant may be used to selectively remove dielectric material 280 and form recesses 270. In some embodiments, the recess etch depth may be controlled by total etch time and/or etch rate, or other process conditions, for example.

Figure 2C illustrates an example structure after additional gate material 166 has been deposited in additional spacer material recesses 270 of the structure of Figure 2B, in accordance with an embodiment. The previous relevant disclosure with reference to additional gate material 166 is equally applicable here, such as the processes used to form additional gate material 164 and the materials that additional gate material 166 may include. However, in this example embodiment, an angled deposition process need not be used, as the deposition is performed to substantially fill the additional spacer material recesses 270 and thus the deposition or growth is performed on the top surface of additional spacer 280 (and optionally followed by a planarization and/or polish process) to form the structure of Figure 2C, for example.

Figure 2D illustrates the example structures of Figures 1F and 2C, with various dimensions, regions, and portions indicated for ease of description, in accordance with some embodiments. Note that Figure 2D applies to structures including both air gap additional spacers 180 and dielectric material additional spacers 280, and therefore the additional spacers regions 180/280 are indicated with different shading to indicate that the regions could include one or both air gap(s) and dielectric material. As can be seen in Figure 2D, the gate 160 in this example embodiment includes the material of gate liner layer 162, gate body 164, and additional gate material 166. Note that gate 160 includes grey shading in Figure 2D to assist with visually identifying the gate 160 in the figure and to assist with illustrating the gate variations in Figures 3A-F, for example. Also note that, in some embodiments, where present, work-function layer 150 may be considered a part of gate 160, depending on the material of work-function layer 150,

for example. As can also be seen in Figure 2D, the gate 160 has been indicated to have three portions: lower portion 192, middle portion 194, and upper portion 196. In this example embodiment, gate liner layer 162 completely (or at least primarily, in some cases) makes up lower portion 192 of gate 160 and has a width W1. Further, the area of gate body 164 with additional spacers 180/280 on either side completely (or at least primarily, in some cases) makes up the middle portion of gate 160 and has a width W2. Further yet, the area of gate body 164 with additional gate material 166 on either side completely (or at least primarily, in some cases) makes up the upper portion of gate 160 and has a width W3. Note that the width dimensions of gate 160 (indicated as W1, W2 and W3) are the dimensions between original spacers 120, in this example embodiment. Also note that the additional spacers 180/280 width W4 and original spacers 120 width W5 are indicated for ease of description. Only the total height H of gate 160 is indicated, but the height of various features, areas, or portions may be described herein, and such heights are the dimensions parallel to the height indicated with H. In some embodiments, the one or more additional spacers 180/280 included in the structure may not be adjacent to the gate dielectric layer 140 and/or the work-function layer 150. In other words, in some embodiments, the one or more additional spacers 180/280 included in the structure may not be between spacers 120 and gate dielectric 140 and/or the one or more additional spacers 180/280 may not be between spacers 120 and work-function layer 150. For instance, the example structure in Figure 2D illustrates that the additional spacers 180/280 are not between the spacers 120 and the gate dielectric 140, and also illustrates that the additional spacers 180/280 are not between the spacers 120 and the work-function layer 150.

In the example structure of Figure 2D, the channel region 111 of the transistor structure is indicated to show that the width of channel region 111 approximates the width W1 of the lower portion of the gate 160. As can also be understood based on the present disclosure, the channel region 111 is generally between the source/drain regions 130 and allows current or carriers to flow between the source and drain, where such flow is regulated by gate 160, in some embodiments. Note that channel region 111 may be referred to as such, in some embodiments, whether the transistor structure is fully formed and the region is actually used as a conductive channel or whether the structure is not fully formed and the region is intended to be used as a conductive channel. In this example embodiment, channel region 111 is located in substrate 110. However, in some embodiments, the channel region 111 may be located on and/or above the substrate 110, as opposed to in it, such as in the case of a nanowire configuration (described in more detail with reference to Figure 4). In some embodiments, the channel region 111 may be n-type, p-type, or be undoped (or minimally doped) and thus have doping intrinsic to the

semiconductor material in which the region resides (i-type), depending on the end use or target application. In some embodiments, gate liner layer 162 may allow for the width of channel region 111 to be approximately or completely maintained (e.g., as compared to if additional spacers 180/280 were not present) while also gaining parasitic coupling reduction benefits achieved through the inclusion of additional spacers 180/280.

In some embodiments, the width W1 of the lower portion 192 of gate 160 may be wider than the width W2 of the middle portion 194 of gate 160. In some such embodiments, the relatively narrower middle portion 194 of gate 160 may be as a result of the presence of additional spacers 180/280 between original spacers 120 and that middle portion of gate 160 (specifically, gate body 164). For instance, as can be understood in the example structure shown in Figure 2D, the width W1 of lower portion 192 of gate 160 (and the width W3 of upper portion 196) in this example embodiment is the total width between spacers 120. Therefore, the inclusion of additional spacers 180/280 on either side of gate 160 and between original spacers 120, in this example embodiment, results in a reduction of the width W2 of the middle portion 194 of gate 160, such that W2 added to two times W4 (the width of additional spacers 180/280, which is the same in this example embodiment) is the same as W1 (which is also the same as W3), as can be seen in Figure 2D. In some embodiments, the width W3 of upper portion 196 of gate 160 may be wider than the width W2 of the middle portion 194 of gate 160. In some such embodiments, the relatively narrower middle portion 194 of gate 160 may be as a result of the presence of additional spacers 180/280 between original spacers 120 and gate 160 (specifically, gate body 164). In some embodiments, the width W3 of upper portion 196 of gate 160 may be approximately the same as the width W2 of middle portion 194 of gate 160, such as in embodiments where additional gate material 166 is not deposited. In some embodiments, the width W1 of the lower portion 192 of gate 160 may be at least 5, 10, 15, 25, or 50 % wider than the width W2 of the middle portion 194, or some other suitable minimum percentage difference, for example. In some embodiments, the width W3 of the upper portion 196 of gate 160 may be at least 5, 10, 15, 25, or 50 % wider than the width W2 of the middle portion 194, or some other suitable minimum percentage difference, for example.

In some embodiments, the width W4 of additional spacers 180/280 may be relatively wider than, narrower than, or at least approximately the same as the width W5 of spacers 120. For example, in some such embodiments, the ratio of W4:W5 may be approximately 1:1, 1.5:1, 1:1.5, 2:1, 1:2, 3:1, 1:3, or any other suitable ratio of W4:W5, depending on the end use or target application. In some embodiments, the height of the upper portion 196 of gate 160 may be greater than, less than, or at least approximately the same as the height of lower portion 192 of

gate 160 (in the example structure of Figure 2D, the height of upper portion 196 is shown as greater than the height of lower portion 192). In some embodiments, the height of the middle portion 194 of gate 160 may be greater than, less than, or at least approximately the same as the height of upper portion 192 of gate 160 (in the example structure of Figure 2D, the height of middle portion 194 is shown as greater than the height of upper portion 196). In some embodiments, the height (or maximum height) of additional spacers 180/280 may be less than the height (or maximum height) of spacers 120. For instance, in some such embodiments, the height of additional spacers 180/280 may be less than 90, 75, 50, 25, or 10 % of the height of spacers 120, or some other suitable maximum percentage, for example.

In some embodiments, the widths W1, W2, and W3 of the lower portion 192, middle portion 194, and upper portion 196 of gate 160, respectively, may be in the range of 50 to 500 nm, or any other suitable width, depending on the end use or target application. In some embodiments, the width W1 of the lower portion 192 of gate 160 may be at least 2, 5, 10, 15, 20, 25, or 50 nm wider than the width W2 of the middle portion 194 of gate 160, or some other suitable minimum difference, for example. In some embodiments, the widths W4 and W5 of additional spacers 180/280 and original spacers 120, respectively, may be in the range of 2 to 100 nm (e.g., 5-15 nm), or any other suitable width, depending on the end use or target application. In some embodiments, the difference in width between additional spacers 180/280 (having width W4) and original spacers 129 (having width W5) may be approximately 0, 1, 2, 3, 5, 10, 15, or 20 nm, or some other suitable difference, regardless of which features are wider, for example. In some embodiments, the total height H of gate 160 may be in the range of 50 to 500 nm, or any other suitable height, depending on the end use or target application. In some embodiments, the height of original spacers 120 may be at least 5, 10, 25, 50, 100, 150, 200, or 250 nm greater than the height of additional spacers 180/280, or some other suitable minimum difference, for example. Note that, in some example cases, the dimensions (e.g., widths or heights) described herein may be the maximum dimensions of a given feature. For instance, in some embodiments, the width of additional spacers 180/280 may vary going down the feature, such that the width W4 described herein refers to the maximum width of additional spacers 180/280 between spacers 120 and gate 160, to provide an example.

In some embodiments, the gate approximates an "I" shape, such as the approximate I-shaped gate 160 shown in the example structure of Figure 2D. As can be understood based on this disclosure, the I-shape can be achieved through the formation of additional spacers 180/280 on either side of gate body 164 and between original spacers 120. However, in some such embodiments, the I-shape descriptor is not intended to limit such gates to an exact or perfect "I"

shape. Instead, the I-shape descriptor is intended to be a general approximation of the shape of the gate, in some embodiments. For example, in some such embodiments, the lower portion of the I-shaped gate may have a different width and/or height than the upper portion of the I-gate shaped. Further, in some such embodiments, the left side of the I-shaped gate may not be symmetrical with the right side, for example. Other example gate shapes derivative of the I-shape may be manifested, in some embodiments (e.g., C-shape, J-shape, L-shape, J-shape, J-shape, [-shape, l-shape, l-shape, to provide a few examples). Note that although the original spacers 120, additional spacers 180/280, and gate 160 are illustrated in Figure 2D as having a number of symmetries in this example embodiment (e.g., spacers 120 mirror each other, additional spacers 180/280 mirror each other, gate 160 is symmetrical about its vertical central axis, and so forth), in some embodiments, structural variations may occur as a result of desired processing and/or as a result of real-world fabrication processes. Some examples of variations that may occur will be described with reference to Figures 3A-F below, in accordance with some embodiments.

Figures 3A-F illustrate variations that may occur to the transistor gate of the example structure of Figure 2D, in accordance with some embodiments. Note that only a portion of the structure of Figure 2D including spacers 120, gate 160, and additional spacers 180 and/or 280 is shown in Figures 3A-F to assist with illustrating variations that may occur to the transistor gate and other features. The previous relevant disclosure with reference to spacers 120, gate 160, air gap additional spacers 180, and dielectric additional spacers 280 is equally applicable here. However, the gates in Figures 3A-F are indicated with their corresponding figure letter, with the gate of Figure 3A indicated as 160A, the gate of Figure 3B indicated as 160B, and so forth, for ease of reference. Also note that 180/280 indicates that the additional spacer may include an air gap(s) and/or dielectric material, as was the case with the structure of Figure 2D. Figure 3A is provided to illustrate that an additional spacer 180/280 may be formed on only one side of gate 160A, in some embodiments. In some such embodiments, gate 160A may approximate a “C” shape or a backwards “C” shape, for example. Figure 3B is provided to illustrate that additional gate material 166 may not be deposited, in some embodiments. For example, in some such embodiments, additional spacer dielectric material 280 may be deposited in additional spacer trenches 170, but not recessed, to form the final gate structure 160B shown in Figure 3B. In some such embodiments, the upper portion of an I-shaped gate may not be formed, such that the gate may more closely approximate a perpendicular symbol (“⊥”), for example. As can be understood based on this disclosure, variations can be combined in any suitable manner, such as only forming an additional spacer on one side of the gate (e.g., as shown in Figure 3A) and not

depositing additional gate material (e.g., as shown in Figure 3B), thereby forming a gate that may closely approximate an “L” shape, in an example embodiment. Figure 3C is provided to illustrate that the gate liner layer 162 may not be evenly etched, whether desired or as a result of real-world fabrication processes, resulting in additional spacers 180/280 of differing height, for example. In some such embodiments, the lower portion of the gate formed 160C may be asymmetrical, as shown in Figure 3C, for example.

Figure 3D is provided to illustrate that the additional spacer on one side of the gate may be an air gap additional spacer 180, while the additional spacer on the other side of the gate may be a dielectric material additional spacer 280. In addition, Figure 3D is provided to illustrate that the additional gate material 166 may not be formed in a symmetrical manner, in some embodiments, whether desired or as a result of real-world fabrication processes, resulting in the gate 160D shown. In the example embodiment shown in Figure 3D, the additional gate material 166 extends to a lower point above the air gap additional spacer 180 than above the dielectric material additional spacer 280, which may be a result of the depth of the dielectric additional spacer recess 270 formed (e.g., as described with reference to Figure 2B) and/or the specific angle used for depositing additional gate material 166, for example. Figure 3E is provided to illustrate that the additional spacers 180/280 on either side of the gate 160E may have different widths, in some embodiments, such that one of the additional spacers is wider than the other one (the left additional spacer is wider, in this example case). Figure 3E is also provided to illustrate that the original spacers 120 on either side of the gate 160E may have different widths, in some embodiments, such that one of the original spacers is wider than the other one (the right spacer is wider, in this example case). Figure 3F is provided to illustrate that multi-layer additional spacers may be formed, in some embodiments, whether desired or as a result of real-world fabrication processes. For example, as shown in Figure 3F, dielectric material 280 is formed in a lower portion of the total additional spacer area on either side of gate 160F and air gaps 180 are formed above the dielectric material 280, resulting in additional spacers including both dielectric material 280 and air gaps 180, in this example embodiment. As previously described, the additional spacer area may include more than one material, such as two or more different dielectric materials, in some embodiments. As can also be seen in Figures 3A-F, the example structures include topography variations that may occur as a result of the scale of the structures (e.g., structures including nanometer critical dimensions), the fabrication processes used, and/or the desired structure being formed, for example.

Figure 4 illustrates example non-planar transistor architectures including additional spacers, in accordance with some embodiments of this disclosure. The previous relevant

disclosure with reference to features already described (e.g., substrate 110, gate dielectric 140, optional work-function layer 150, additional spacers 180/280, and so forth) is equally applicable here. However, as can be seen in the example embodiment of Figure 4, the transistor structure includes a finned channel region 402 and a nanowire channel region 404 to illustrate two example non-planar transistor configurations that the techniques described herein can be used with. Note that the structure in this example embodiment also includes finned source/drain regions 130 and 131, where source/drain regions 130 are replacement source/drain regions and source/drain regions 131 are native to substrate 110 and include the same or similar material as substrate 110. Also note that shallow trench isolation (STI) regions 112 are shown between the set of fins in this example embodiment and may be present to assist with electrical isolation of the fins. Further note that inter-layer dielectric (ILD) material 114 is shown formed over portions of the structure, in this example embodiment, which may be used to protect the source/drain regions during gate processing, for example. In some embodiments, the STI and ILD materials may be formed using any suitable techniques and may include any suitable materials, depending on the end use or target application. As shown, the example structure includes two fins, which may have been formed using any suitable techniques, such as patterning and etching substrate 110 to form the desired number of fins, and optionally etching and removing the fins to replace them with fins of different material (e.g., to form the fins used for source/drain regions 130).

As can be understood based on this disclosure, the gate (e.g., gate liner layer 162, gate body 164, and additional gate material 166) is formed on three portions of the finned channel region 402 to create a finned transistor configuration. Such a finned configuration is sometimes referred to as a tri-gate, three-dimensional (3D), or finFET configuration, as the conductive channel of such finned configurations essentially resides along three different outer substantially planar regions of the fin (and thus there are three effective gates). In some embodiments, other types of non-planar transistor configurations can be achieved using the techniques described herein, such as dual-gate configurations, in which the conductive channel, for example, principally resides only along two side-walls of the fin (and not along the top of the fin). Another non-planar transistor configuration is a nanowire (also referred to as a nanoribbon or gate-all-around) configuration, which is configured similarly to a fin-based configuration, but instead of a finned channel region where the gate is on three portions, one or more nanowires are used and the gate material generally surrounds each nanowire, such as the two nanowires 404 illustrated in Figure 4. Such nanowire configurations may be achieved, in some embodiments, by including sacrificial material in the channel region of the fin and etching out the sacrificial

material prior to forming the gate stack when the channel region is exposed (e.g., prior to forming gate dielectric layer 140). In some embodiments, non-planar configurations may be used to provide benefits, such as increasing carrier mobility or increasing the effective control of the charge in the channel regions, for example.

As can be seen in the example embodiment of Figure 4, the width F_w and height F_h of the two fins are shown as the same for ease of illustration. In some embodiments, the fins may be formed to have widths F_w in the range of 3 to 100 nm, for example, or any other suitable width depending on the end use or target application. In some embodiments, the fins may be formed to have heights F_h in the range of 5 to 100 nm, or any other suitable height depending on the end use or target application. In some embodiments, the fins may be formed with a desired approximate height F_h to width F_w ratio ($F_h:F_w$), such as approximately 1.5:1, 2:1, 3:1, 4:1, 5:1, or any other suitable $F_h:F_w$ ratio, depending on the end use or target application. Note that although two fins in the example structure of Figure 4 are illustrated as having the same widths F_w and heights F_h , the present disclosure is not intended to be so limited. For example, in some embodiments, fins formed on the same substrate or die may be formed to have varying widths and/or heights, depending on the end use or target application. Also note that although two fins are illustrated in the example structure of Figure 4, any number of fins may be formed during the integrated circuit fabrication process, such as 1, 3, 5, 10, 100, thousands, millions, or more, depending on the end use or target application. Numerous variations and configurations will be apparent in light of this disclosure.

Example System

Figure 5 illustrates a computing system 1000 implemented with integrated circuit structures or devices formed using the techniques disclosed herein, in accordance with some embodiments. As can be seen, the computing system 1000 houses a motherboard 1002. The motherboard 1002 may include a number of components, including, but not limited to, a processor 1004 and at least one communication chip 1006, each of which can be physically and electrically coupled to the motherboard 1002, or otherwise integrated therein. As will be appreciated, the motherboard 1002 may be, for example, any printed circuit board, whether a main board, a daughterboard mounted on a main board, or the only board of system 1000, etc.

Depending on its applications, computing system 1000 may include one or more other components that may or may not be physically and electrically coupled to the motherboard 1002. These other components may include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a

battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth). Any of the components included in computing system 1000 may include one or more integrated circuit structures or devices formed using the disclosed techniques in accordance with an example embodiment. In some embodiments, multiple functions can be integrated into one or more chips (e.g., for instance, note that the communication chip 1006 can be part of or otherwise integrated into the processor 1004).

The communication chip 1006 enables wireless communications for the transfer of data to and from the computing system 1000. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 1006 may implement any of a number of wireless standards or protocols, including, but not limited to, Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing system 1000 may include a plurality of communication chips 1006. For instance, a first communication chip 1006 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1006 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 1004 of the computing system 1000 includes an integrated circuit die packaged within the processor 1004. In some embodiments, the integrated circuit die of the processor includes onboard circuitry that is implemented with one or more integrated circuit structures or devices formed using the disclosed techniques, as variously described herein. The term “processor” may refer to any device or portion of a device that processes, for instance, electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 1006 also may include an integrated circuit die packaged within the communication chip 1006. In accordance with some such example embodiments, the integrated circuit die of the communication chip includes one or more integrated circuit structures or devices formed using the disclosed techniques as variously described herein. As

will be appreciated in light of this disclosure, note that multi-standard wireless capability may be integrated directly into the processor 1004 (e.g., where functionality of any chips 1006 is integrated into processor 1004, rather than having separate communication chips). Further note that processor 1004 may be a chip set having such wireless capability. In short, any number of processor 1004 and/or communication chips 1006 can be used. Likewise, any one chip or chip set can have multiple functions integrated therein.

In various implementations, the computing device 1000 may be a laptop, a netbook, a notebook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra-mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, a digital video recorder, or any other electronic device that processes data or employs one or more integrated circuit structures or devices formed using the disclosed techniques, as variously described herein.

Further Example Embodiments

The following examples pertain to further embodiments, from which numerous permutations and configurations will be apparent.

Example 1 is a transistor including: a channel region; a gate above the channel region, the gate including an upper portion, a middle portion, and a lower portion, wherein the middle portion is between the lower and upper portions and wherein the lower portion is closer to the channel region than the middle portion; and spacers on either side of the gate; wherein the lower portion of the gate is wider between the spacers than the middle portion of the gate.

Example 2 includes the subject matter of Example 1, wherein the upper portion of the gate is wider between the spacers than the middle portion of the gate.

Example 3 includes the subject matter of any of Examples 1-2, wherein the gate is approximately I-shaped.

Example 4 includes the subject matter of any of Examples 1-3, further including at least one additional spacer between the middle portion of the gate and one of the spacers.

Example 5 includes the subject matter of any of Examples 1-4, further including additional spacers on either side of the gate between the middle portion of the gate and the spacers.

Example 6 includes the subject matter of any of Examples 4-5, wherein the at least one additional spacer includes an air gap.

Example 7 includes the subject matter of any of Examples 4-6, wherein the at least one additional spacer includes dielectric material.

Example 8 includes the subject matter of Example 7, wherein the dielectric material is a low-k dielectric material.

Example 9 includes the subject matter of any of Examples 7-8, wherein the additional spacer material is different than material of the spacers.

5 Example 10 includes the subject matter of any of Examples 1-9, further including a gate dielectric between the channel region and the gate.

Example 11 includes the subject matter of any of Examples 1-10, further including a work-function layer between the channel region and the gate.

10 Example 12 includes the subject matter of any of Examples 1-11, wherein the lower portion of the gate includes different material than the middle portion of the gate.

Example 13 includes the subject matter of any of Examples 1-12, wherein the lower portion of the gate has a maximum width between the spacers that is at least 5% wider than a maximum width between the spacers of the middle portion of the gate.

15 Example 14 includes the subject matter of any of Examples 1-13, wherein the lower portion of the gate has a maximum width between the spacers that is at least 5 nm wider than a maximum width between the spacers of the middle portion of the gate.

Example 15 includes the subject matter of any of Examples 1-14, wherein the lower portion of the gate is wider between the spacers than the upper portion of the gate.

20 Example 16 includes the subject matter of any of Examples 1-15, wherein the transistor is one of a p-type and n-type transistor.

Example 17 includes the subject matter of any of Examples 1-16, wherein the transistor includes at least one of the following configurations: planar, non-planar, dual-gate, finned, tri-gate, finned field-effect transistor (finFET), nanowire, nanoribbon, gate-all-around, metal-oxide-semiconductor FET (MOSFET), and tunnel FET (TFET).

25 Example 18 is a computing system including the subject matter of any of Examples 1-17.

30 Example 19 is a transistor including: a channel region; a gate above the channel region, the gate including an upper portion, a middle portion, and a lower portion, wherein the middle portion is between the lower and upper portions and wherein the lower portion is closer to the channel region than the middle portion; and spacers on either side of the gate; additional spacers, each additional spacer between the middle portion of the gate and one of the spacers; wherein the lower and upper portions of the gate are wider between the spacers than the middle portion of the gate.

Example 20 includes the subject matter of Example 19, wherein the gate is approximately I-shaped.

Example 21 includes the subject matter of any of Examples 19-20, wherein the additional spacers include air gaps.

5 Example 22 includes the subject matter of any of Examples 19-21, wherein the additional spacers include dielectric material.

Example 23 includes the subject matter of Example 22, wherein the dielectric material is a low-k dielectric material.

10 Example 24 includes the subject matter of any of Examples 19-23, wherein the additional spacer material is different than material of the spacers.

Example 25 includes the subject matter of any of Examples 19-24, further including a gate dielectric between the channel region and the gate.

Example 26 includes the subject matter of any of Examples 19-25, further including a work-function layer between the channel region and the gate.

15 Example 27 includes the subject matter of any of Examples 19-26, wherein the lower portion of the gate includes different material than the middle portion of the gate.

Example 28 includes the subject matter of any of Examples 19-27, wherein the lower portion of the gate has a maximum width between the spacers that is at least 5% wider than a maximum width between the spacers of the middle portion of the gate.

20 Example 29 includes the subject matter of any of Examples 19-28, wherein the lower portion of the gate has a maximum width between the spacers that is at least 5 nm wider than a maximum width between the spacers of the middle portion of the gate.

Example 30 includes the subject matter of any of Examples 19-29, wherein the upper portion of the gate has a maximum width between the spacers that is at least 5 nm wider than a maximum width between the spacers of the middle portion of the gate.

Example 31 includes the subject matter of any of Examples 19-30, wherein the transistor is one of a p-type and n-type transistor.

Example 32 includes the subject matter of any of Examples 19-31, wherein the transistor includes at least one of the following configurations: planar, non-planar, dual-gate, finned, tri-gate, finned field-effect transistor (finFET), nanowire, nanoribbon, gate-all-around, metal-oxide-semiconductor FET (MOSFET), and tunnel FET (TFET).

Example 33 is a computing system including the subject matter of any of Examples 19-32.

Example 34 is a method of forming a transistor, the method including: depositing gate liner material above a channel region and between spacers; depositing gate material on the gate liner material; performing a wet etch to selectively remove the gate liner material from at least a portion of either side of the gate material to form trenches; and performing at least one of:
5 depositing dielectric material in the trenches; and depositing additional gate material in an upper portion of the trenches.

Example 35 includes the subject matter of Example 34, further including etching the gate liner material prior to depositing the gate material.

10 Example 36 includes the subject matter of any of Examples 34-35, wherein depositing the additional gate material in an upper portion of the trenches includes an angled deposition process.

Example 37 includes the subject matter of any of Examples 34-36, wherein depositing the additional gate material in an upper portion of the trenches forms air gaps between the gate material and the spacers.

15 Example 38 includes the subject matter of any of Examples 34-36, wherein depositing dielectric material in the trenches is performed and further including recessing the dielectric material using a wet etch process to form recesses and depositing the additional gate material in the recesses.

20 Example 39 includes the subject matter of any of Examples 34-38, wherein depositing dielectric material in the trenches is performed and wherein the dielectric material includes low-k dielectric material.

25 Example 40 includes the subject matter of any of Examples 34-39, wherein the wet etch to selectively remove the gate liner material from at least a portion of either side of the gate material includes using an etchant that removes the gate liner material at a rate of at least three times faster than removal of the gate material.

Example 41 includes the subject matter of any of Examples 34-40, further including forming a gate dielectric above the channel region and between the spacers prior to depositing the gate liner material.

30 Example 42 includes the subject matter of any of Examples 34-41, further including forming a work-function layer above the channel region and between the spacers prior to depositing the gate liner material.

Example 43 includes the subject matter of any of Examples 34-42, wherein the transistor is one of a p-type and n-type transistor.

Example 44 includes the subject matter of any of Examples 34-43, wherein the transistor includes at least one of the following configurations: planar, non-planar, dual-gate, finned, tri-
5 gate, finned field-effect transistor (finFET), nanowire, nanoribbon, gate-all-around, metal-oxide-semiconductor FET (MOSFET), and tunnel FET (TFET).

Example 45 is a transistor including: a channel region; a gate above the channel region; spacers on either side of the gate; and additional spacers, each additional spacer between at least a portion of the gate and one of the spacers.

10 Example 46 includes the subject matter of Example 45, wherein the additional spacers include at least one of air gaps and dielectric material.

Example 47 includes the subject matter of any of Examples 45-46, wherein the additional spacers include material different than material of the spacers.

15 Example 48 includes the subject matter of any of Examples 45-47, wherein each additional spacer is between only a portion of the gate and the spacers, such that the additional spacers are not between all of the gate material and the spacers.

20 The foregoing description of example embodiments has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit this disclosure to the precise forms disclosed. Many modifications and variations are possible in light of this disclosure. It is intended that the scope of this disclosure be limited not by this detailed description, but rather by the claims appended hereto. Future filed applications claiming priority to this application may claim the disclosed subject matter in a different manner, and may generally include any set of one or more limitations as variously disclosed or otherwise demonstrated herein.

CLAIMS

What is claimed is:

1. A transistor comprising:
a channel region;
5 a gate above the channel region, the gate including an upper portion, a middle portion, and a lower portion, wherein the middle portion is between the lower and upper portions and wherein the lower portion is closer to the channel region than the middle portion; and
spacers on either side of the gate;
10 wherein the lower portion of the gate is wider between the spacers than the middle portion of the gate.
2. The transistor of claim 1, wherein the upper portion of the gate is wider between the spacers than the middle portion of the gate.
3. The transistor of claim 1, wherein the gate is approximately I-shaped.
- 15 4. The transistor of claim 1, further comprising at least one additional spacer between the middle portion of the gate and one of the spacers.
5. The transistor of claim 1, further comprising additional spacers on either side of the gate between the middle portion of the gate and the spacers.
6. The transistor of claim 4, wherein the at least one additional spacer includes an air
20 gap.
7. The transistor of claim 4, wherein the at least one additional spacer includes dielectric material.
8. The transistor of claim 7, wherein the dielectric material is a low-k dielectric material.
- 25 9. The transistor of claim 7, wherein the additional spacer material is different than material of the spacers.

10. The transistor of claim 1, further comprising a gate dielectric between the channel region and the gate.

11. The transistor of claim 1, further comprising a work-function layer between the channel region and the gate.

5 12. The transistor of claim 1, wherein the lower portion of the gate includes different material than the middle portion of the gate.

13. The transistor of claim 1, wherein the lower portion of the gate has a maximum width between the spacers that is at least 5% wider than a maximum width between the spacers of the middle portion of the gate.

10 14. The transistor of claim 1, wherein the lower portion of the gate has a maximum width between the spacers that is at least 5 nm wider than a maximum width between the spacers of the middle portion of the gate.

15. The transistor of claim 1, wherein the lower portion of the gate is wider between the spacers than the upper portion of the gate.

15 16. The transistor of claim 1, wherein the transistor is one of a p-type and n-type transistor.

17. The transistor of claim 1, wherein the transistor includes at least one of the following configurations: planar, non-planar, dual-gate, finned, tri-gate, finned field-effect transistor (finFET), nanowire, nanoribbon, gate-all-around, metal-oxide-semiconductor FET (MOSFET), and tunnel FET (TFET).
20

18. A computing system comprising the transistor of any of claims 1-17.

19. A transistor comprising:

a channel region;

a gate above the channel region;

25 a gate dielectric between the channel region and the gate;

spacers on either side of the gate; and

additional spacers, wherein each additional spacer is between at least a portion of the gate and one of the spacers and wherein the additional spacers are not between the gate dielectric and the spacers.

20. The transistor of claim 19, wherein the additional spacers include at least one of
5 air gaps and dielectric material.

21. The transistor of claim 19, wherein the additional spacers include material different than material of the spacers.

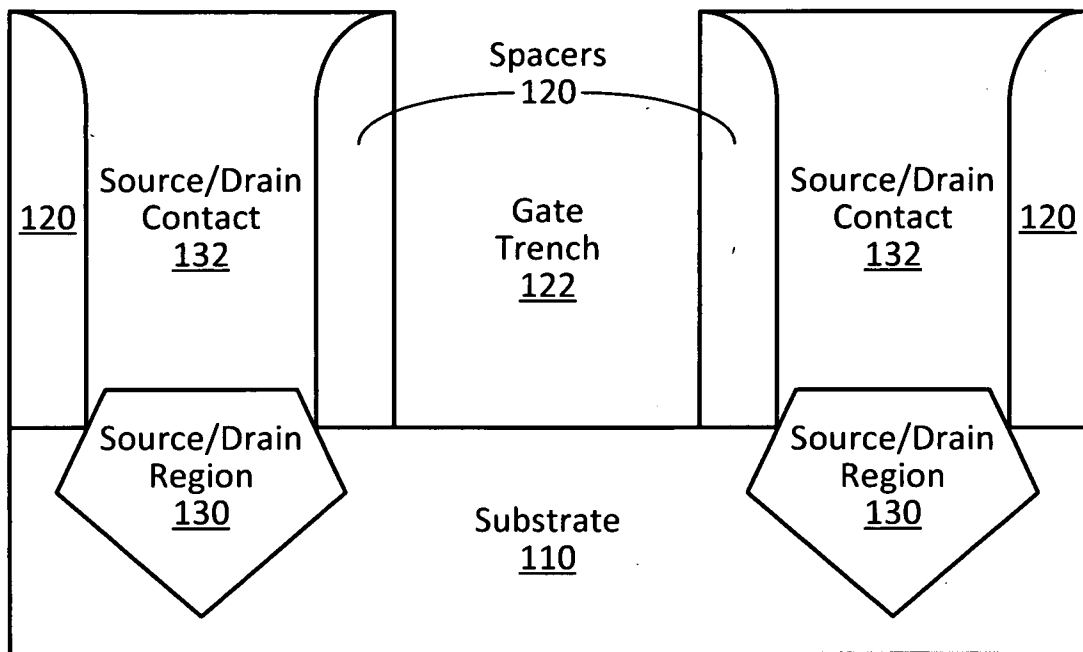
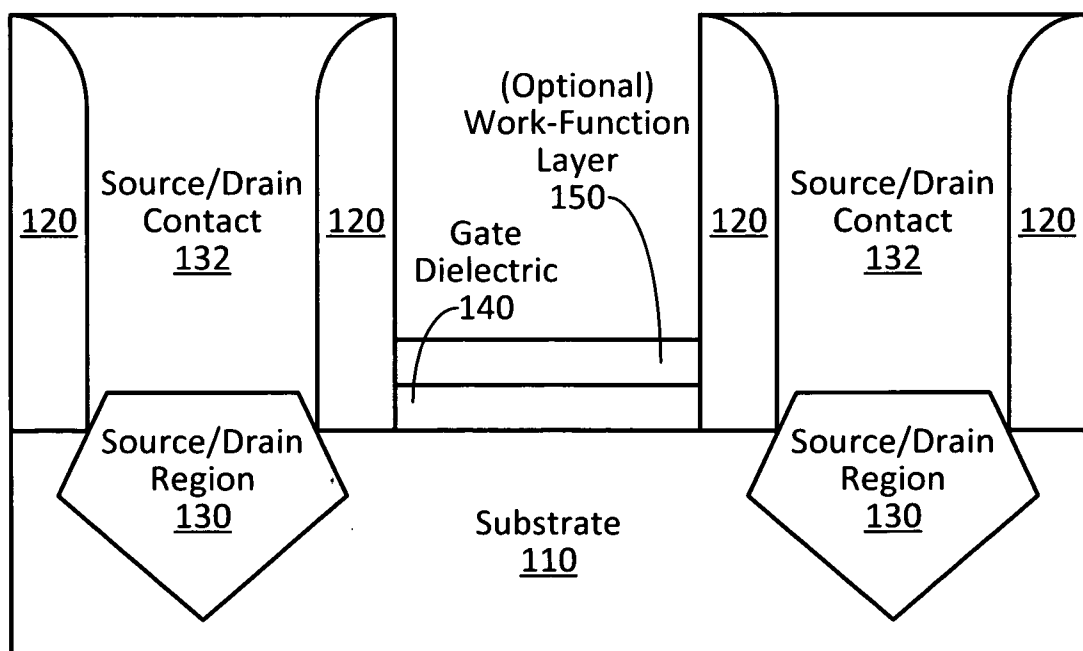
22. The transistor of any of claims 19-21, wherein each additional spacer is between
10 only a portion of the gate and the spacers, such that the additional spacers are not between all of the gate material and the spacers.

23. A method of forming a transistor, the method comprising:
depositing gate liner material above a channel region and between spacers;
depositing gate material on the gate liner material;
performing a wet etch to selectively remove the gate liner material from at least a portion
15 of either side of the gate material to form trenches; and
performing at least one of:
depositing dielectric material in the trenches; and
depositing additional gate material in an upper portion of the trenches.

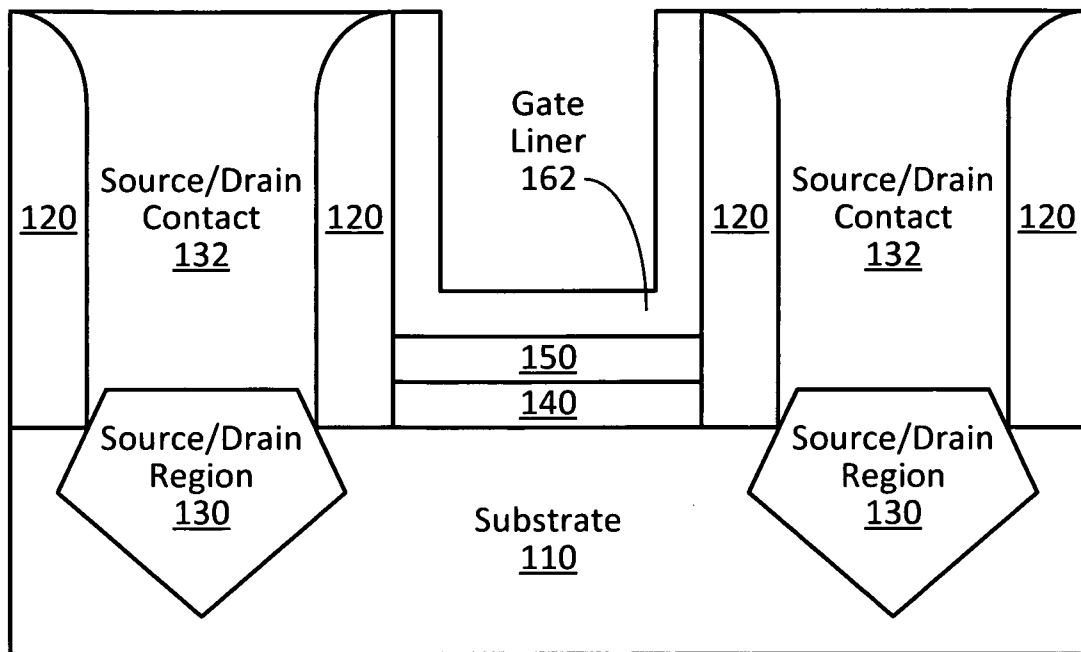
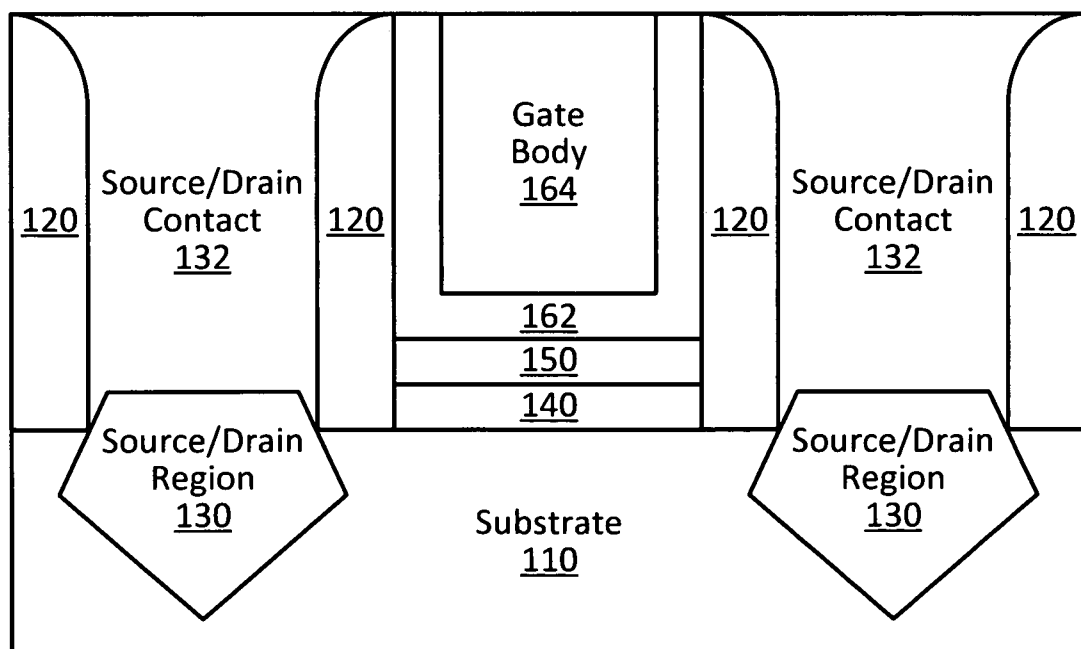
24. The method of claim 23, wherein depositing the additional gate material in an
20 upper portion of the trenches includes an angled deposition process.

25. The method of any of claims 23-24, wherein depositing the additional gate material in an upper portion of the trenches forms air gaps between the gate material and the spacers.

1/8

**FIG. 1A****FIG. 1B**

2/8

**FIG. 1C****FIG. 1D**

3/8

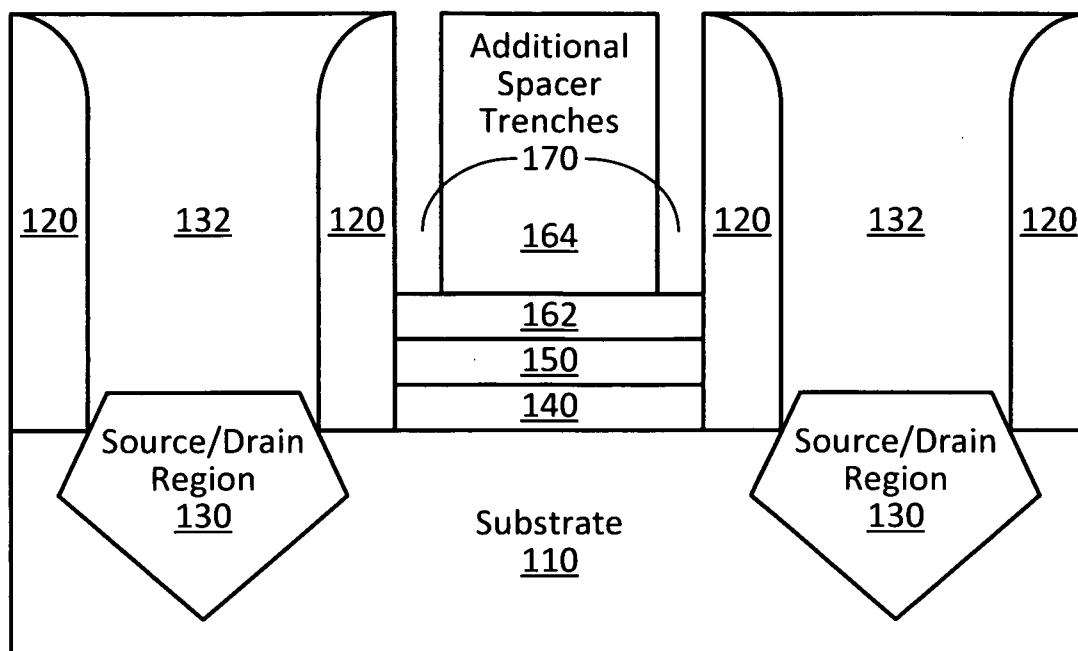


FIG. 1E

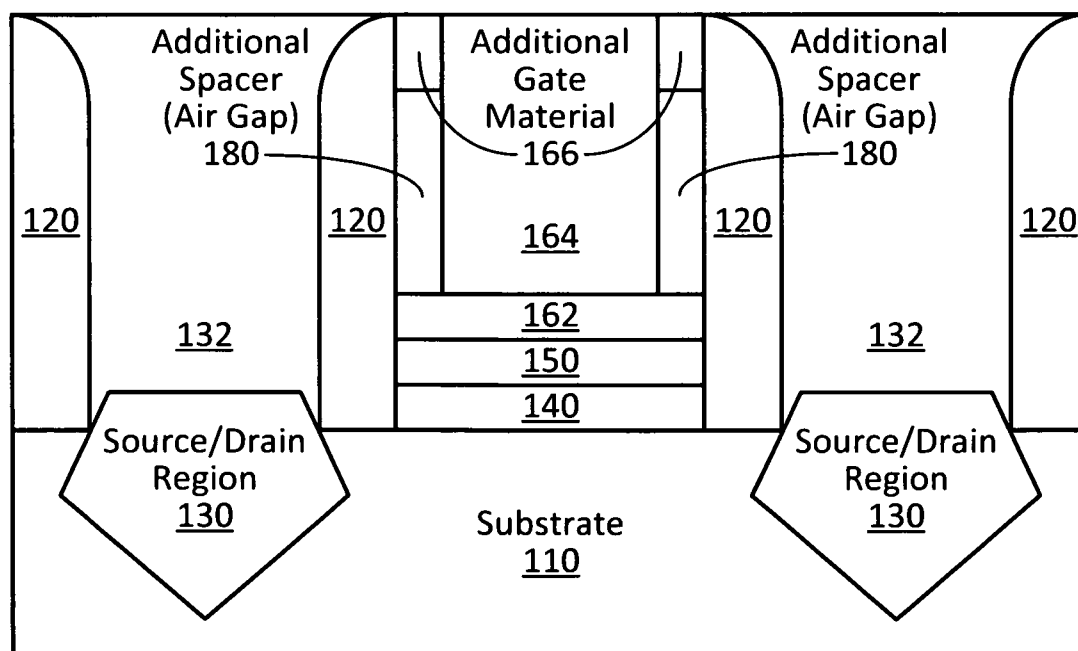


FIG. 1F

4/8

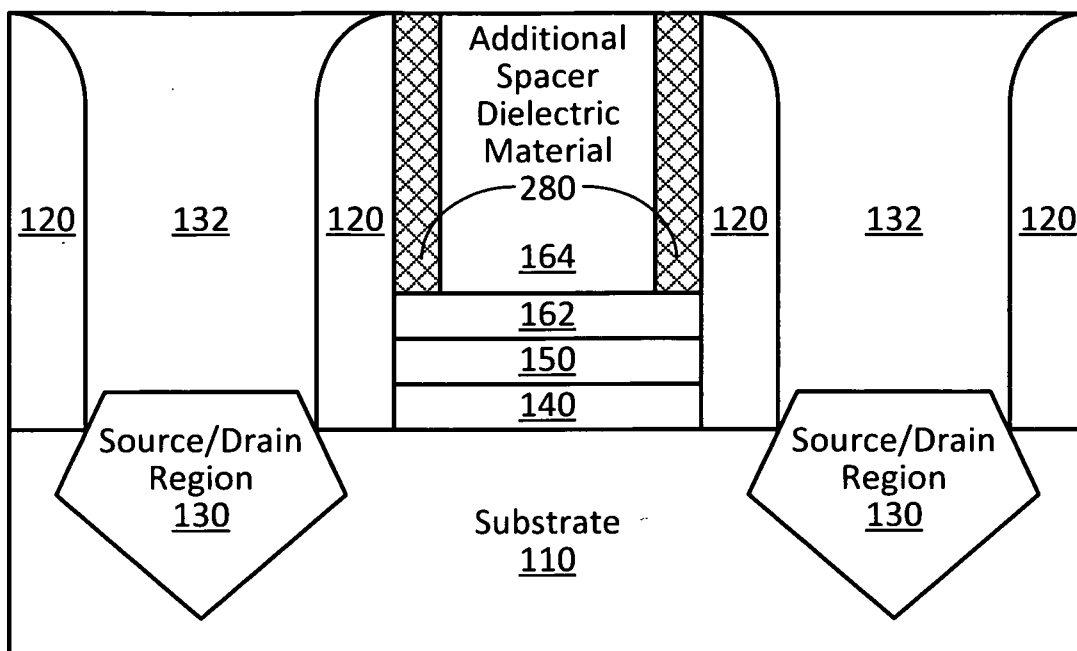


FIG. 2A

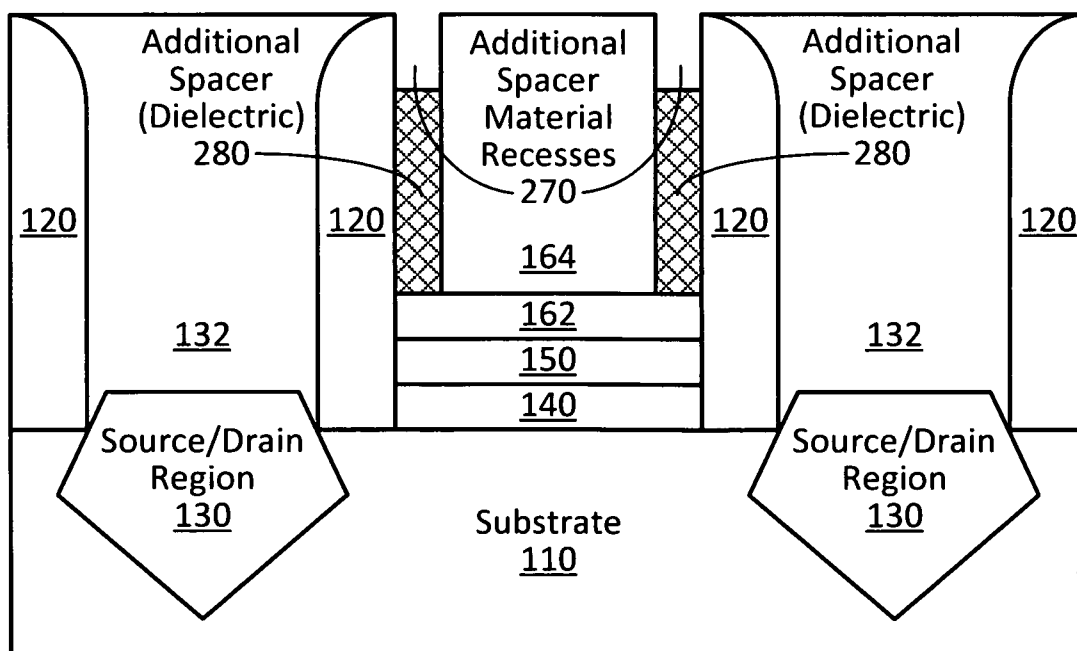


FIG. 2B

5/8

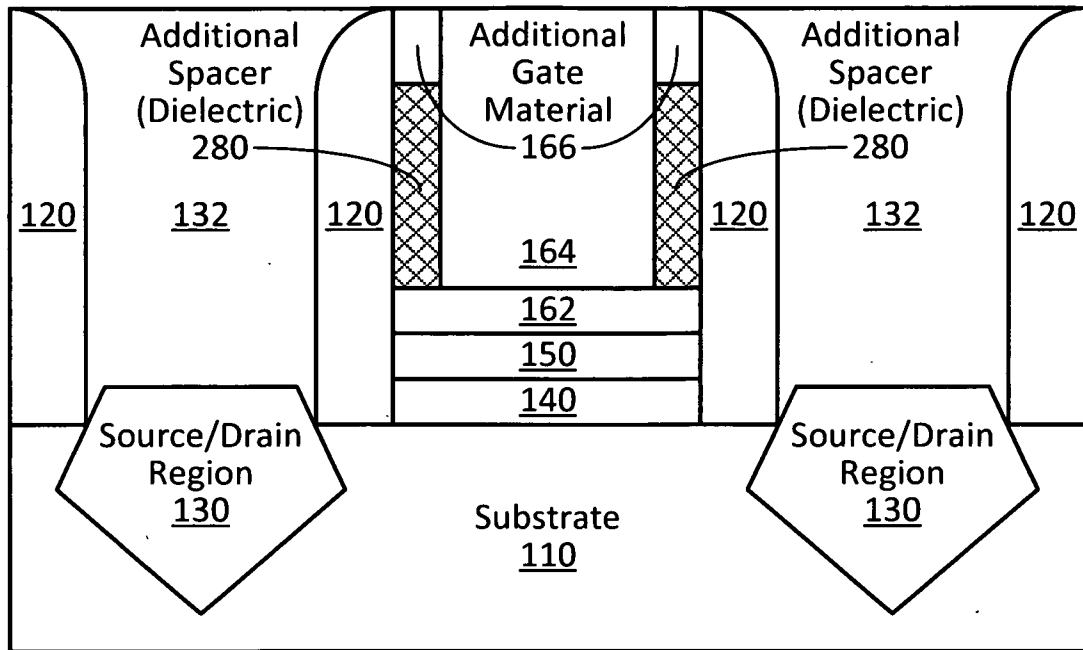


FIG. 2C

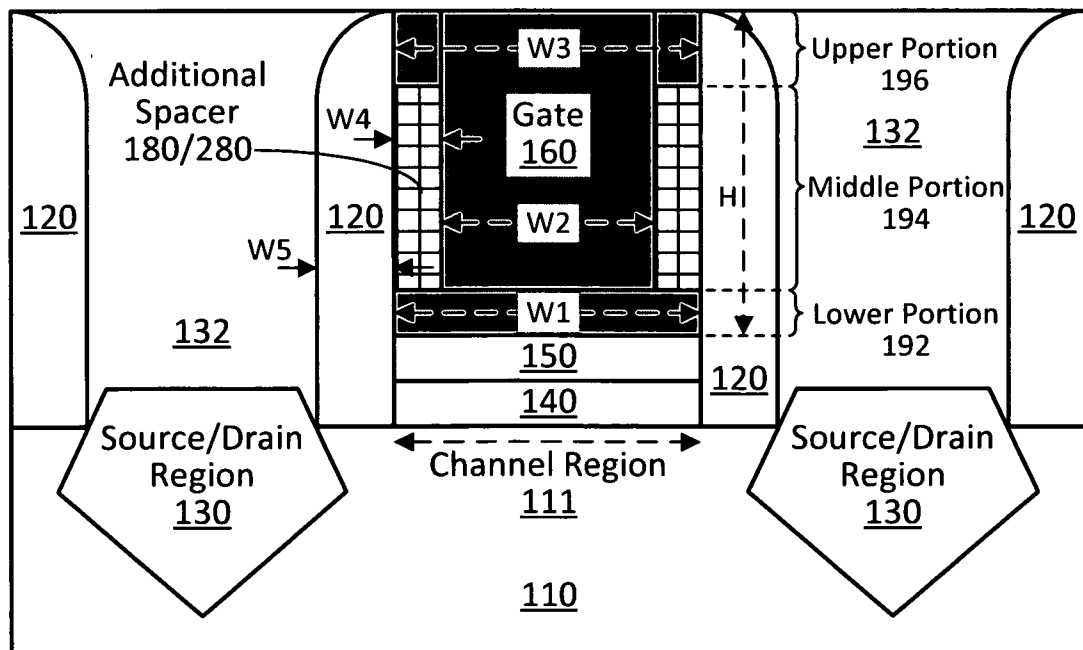


FIG. 2D

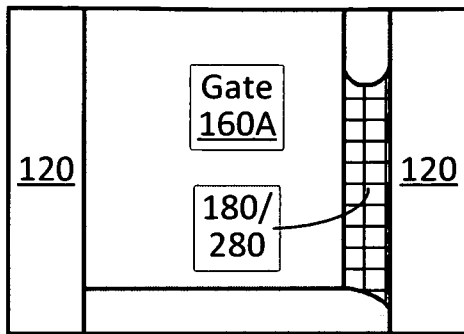


FIG. 3A

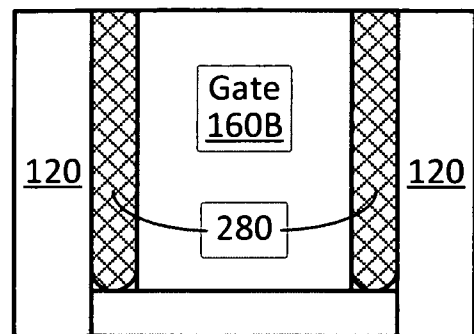


FIG. 3B

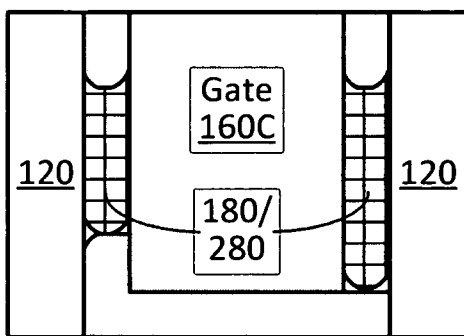


FIG. 3C

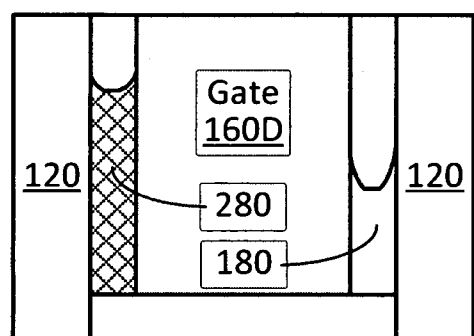


FIG. 3D

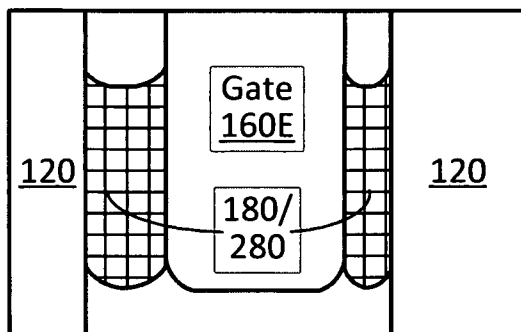


FIG. 3E

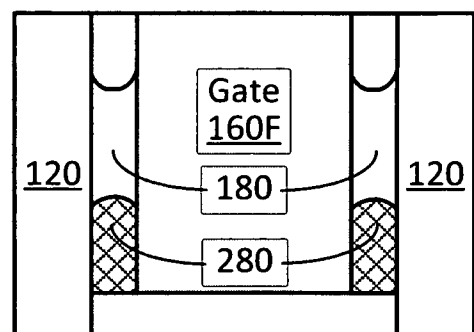


FIG. 3F

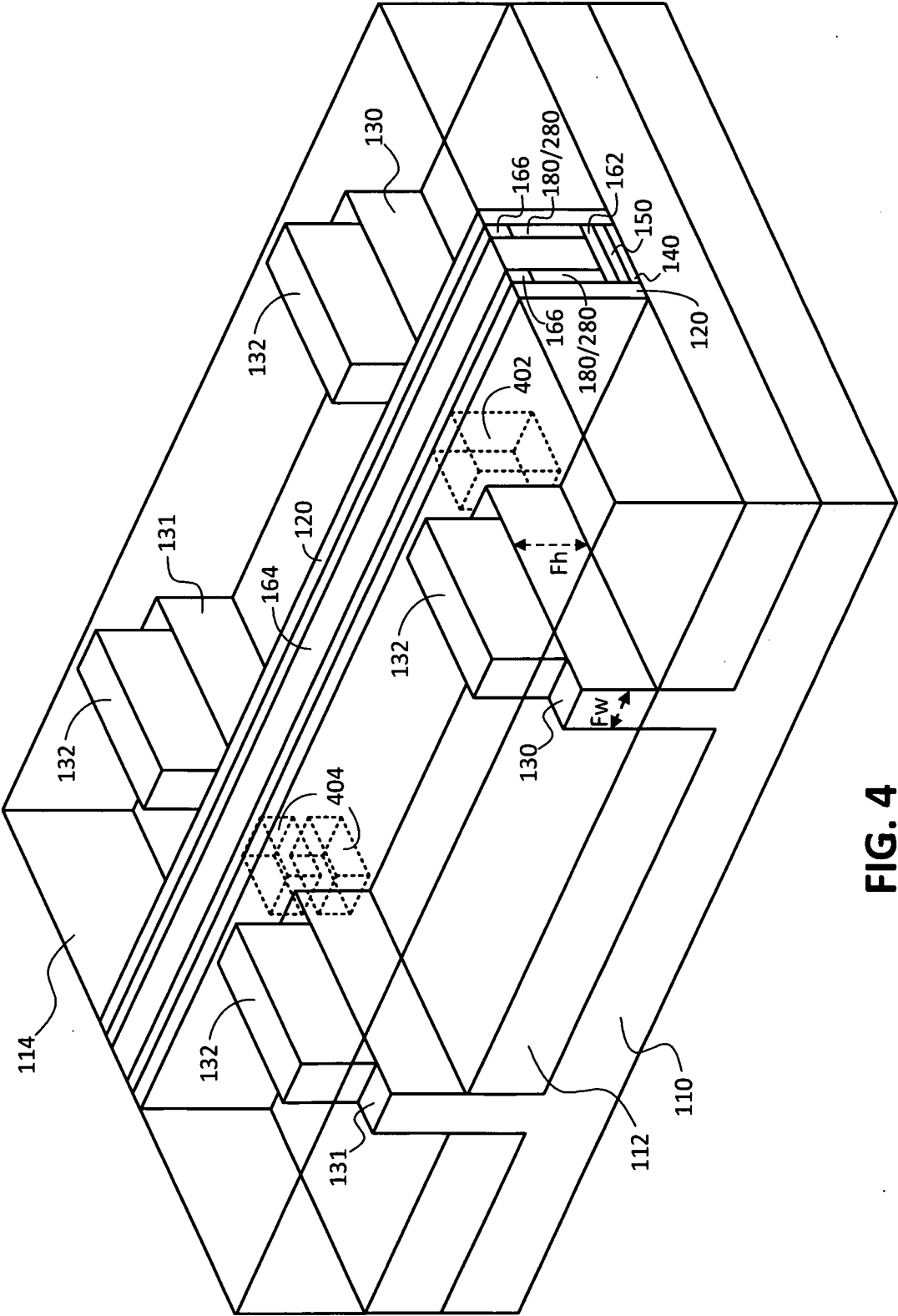


FIG. 4

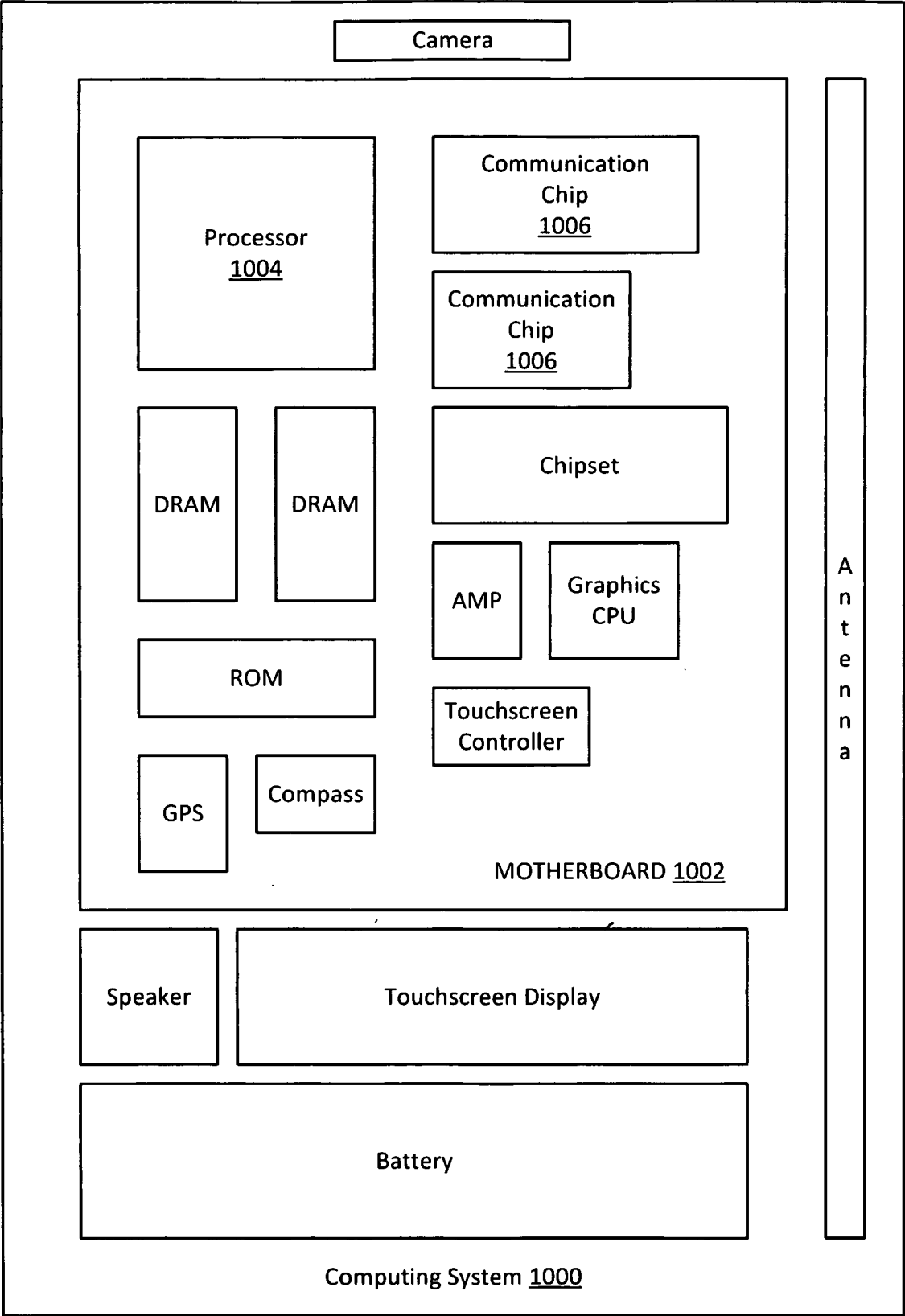


FIG. 5

A. CLASSIFICATION OF SUBJECT MATTER**H01L 29/78(2006.01)i, H01L 21/336(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/78; H01L 29/49; H01L 27/088; H01L 21/28; H01L 21/336; H01L 29/41; H01L 29/772; H01L 29/66; G06F 9/45; H01L 21/265

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: MOSFET, transistor, air spacer, air gap, inner spacer, gate, channel, I-shaped, T-shaped, dielectric layer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014-0217520 A1 (STMICROELECTRONICS S.A. et al.) 07 August 2014 See abstract; paragraphs [0037]-[0063]; claims 1-11; and figures 2-4D.	1-25
A	US 2013-0187229 A1 (CHENG, KANGGUO et al.) 25 July 2013 See abstract; paragraphs [0003]-[0022]; and figures 1-11.	1-25
A	US 8815669 B2 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 26 August 2014 See abstract; columns 5-7; and figures 5-22.	1-25
A	US 5716861 A (MOSLEHI, MEHRDAD M.) 10 February 1998 See abstract; columns 2-7; and figures 1-12.	1-25
A	US 2015-0014788 A1 (PARK, MIN-YEOP et al.) 15 January 2015 See abstract; paragraphs [0063]-[0099]; and figures 1-7.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

21 September 2016 (21.09.2016)

Date of mailing of the international search report

22 September 2016 (22.09.2016)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

CHOI, Sang Won

Telephone No. +82-42-481-8291



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/000193

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2014-0217520 A1	07/08/2014	EP 2763177 A1 US 9117805 B2	06/08/2014 25/08/2015
US 2013-0187229 A1	25/07/2013	CN 104081506 A US 2015-0137240 A1 US 9034701 B2 WO 2013-109481 A1	01/10/2014 21/05/2015 19/05/2015 25/07/2013
US 8815669 B2	26/08/2014	US 2014-0138751 A1 US 8685817 B1	22/05/2014 01/04/2014
US 5716861 A	10/02/1998	JP 06-163571 A KR 10-0274555 B1 US 5949105 A	10/06/1994 15/12/2000 07/09/1999
US 2015-0014788 A1	15/01/2015	CN 104282756 A KR 10-2015-0008304 A	14/01/2015 22/01/2015