



- (51) International Patent Classification:
H01L 21/02 (2006.01)
- (21) International Application Number:
PCT/US2014/035702
- (22) International Filing Date:
28 April 2014 (28.04.2014)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
13/871,713 26 April 2013 (26.04.2013) US
- (63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:
US 13/871,713 (CON)
Filed on 26 April 2013 (26.04.2013)
- (71) Applicant: **TEXAS INSTRUMENTS INCORPORATED** [US/US]; P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).
- (71) Applicant (for JP only): **TEXAS INSTRUMENTS JAPAN LIMITED** [JP/JP]; 24-1, Nishi-shinjuku 6-chome, Shinjuku-ku, 160-8366 (JP).
- (72) Inventors: **TOMOMATSU, Hiroyuki**; 3-2-20-705 Ishigaki-Higashi, Beppu-City, Oita-pref, 874-0919 (JP). **KUSAMAKI, Motoaki**; 2-1-48-303 Ishigaki-Nishi, Beppu-City, Oita-Pref, 874-0910 (JP). **KUBOTA, Kohichi**; 2-4-19-202 Ishigaki-higashi, Beppu-city, Oita-Pref, 874-0919 (JP). **MASUDA, Yuta**; 3824-5-b201 Hiji-Machi, Hayami-gun, Oita-pref, 879-1506 (JP). **SUGIHARA, Akihiro**; 7-2-b101 Midorigaoka-machi, Beppu-City, Oita-Pref, 874-0911 (JP). **KITADA, Hiroshi, Sera**; 1-17-9-305 Honkomagome Bunkyo-Ku, Tokyo, 113-0021 (JP). **KONNO, Takeshi**; 3-13-3-305 Minami, Ushiku-City, Ibaraki-Pref, 300-1222 (JP).
- (74) Agents: **FRANZ, Warren, L.** et al.; Texas Instruments Incorporated, Deputy General Patent Counsel, P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).
- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM,

[Continued on next page]

(54) Title: PHOTODETECTOR ARRAY HAVING DIFFERENT PHOTODIODE STRUCTURES

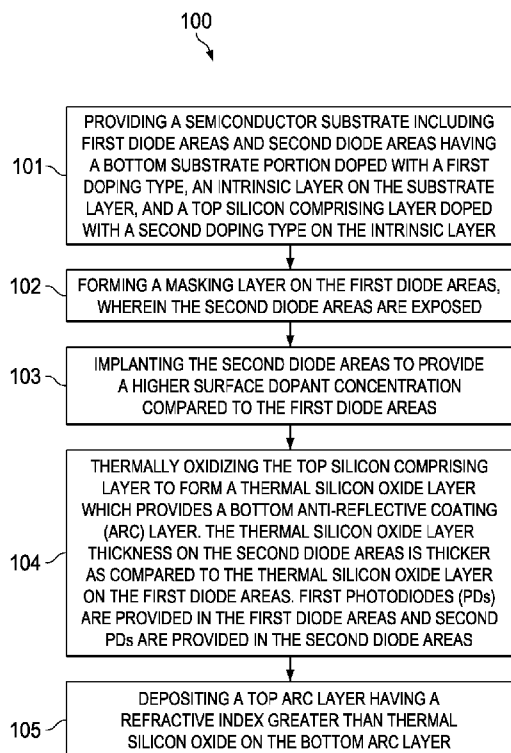


FIG. 1

(57) Abstract: A method (100) of fabricating a photodiode array having different photodiode structures includes providing (101) a semiconductor or substrate having first and second diode areas including a bottom substrate portion doped with a first doping type, an intrinsic layer, and a top silicon layer doped with a second doping type. The second diode areas are implanted (103) with the second doping type. A dopant concentration in the surface of the second diode areas is at least three times higher than in the first diode areas. The top silicon layer is thermally oxidized (104) to form a thermal silicon oxide layer to provide a bottom Anti-Reflective Coating (ARC) layer. The second diode areas grow thermal silicon oxide thicker as compared to the first diode areas. A top ARC layer is deposited (105) on the bottom ARC layer. First PDs are provided in the first diode areas and second PDs provided in the second diode areas.



AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU,

LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

Published:

- with international search report (Art. 21(3))
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))

PHOTODETECTOR ARRAY HAVING DIFFERENT PHOTODIODE STRUCTURES

[0001] Disclosed embodiments relate to photodetector arrays and photodetector integrated circuits (ICs) including photodiode arrays, and methods of making the same.

BACKGROUND

[0002] A photodetector IC (PDIC) includes an array of discrete photodiodes (photodiode array = PDA) on a common substrate material, typically a silicon chip, amplifiers, and readout circuitry. Electromagnetic radiation received by the photodiodes generates electron-hole pairs, and the electrons migrate to the nearest junction, typically a PIN junction or a NIP junction. A PIN or NIP junction is a diode with a wide, lightly doped near-intrinsic semiconductor region (I) between a p-type semiconductor and an n-type semiconductor region which are both typically heavily doped as they are used for ohmic contacts. The light doping level in the intrinsic region results in low junction capacitance for both junctions. After a fixed integration time the charge accumulated at each photodiode (PD) element is sequentially read with readout circuitry to generate the electrical response of the PDIC.

[0003] Some PDICs are used for processing CD, DVD and Blu-ray formats as part of an optical pick-up apparatus, where CD, DVD and Blu-ray each operate at different wavelengths (bands). A typical optical pick-up apparatus enables information to be recorded, reproduced and erased with respect to a CD group disc (e.g. CD, CD-ROM, CD-R and CD-RW), a DVD group disc (e.g. DVD, DVD-ROM, DVD-RAM, DVD-R and DVD-RW, DVD+R, DVD+RW), and Blu-ray format discs, with single or multiple layer formats. The typical optical pick-up apparatus has an infrared semiconductor laser device for the CD (at about 780 nm), a red semiconductor laser device for the DVD (at about 650 nm) and a blue laser device for the Blu-ray (at about 405 nm). During operation of the optical pick-up apparatus a portion of the light from the respective lasers and a portion of the light from the respective group discs is directed by a beam splitter to the PDs of the PDA.

[0004] Generally, the process used to form PDAs forms a single anti-reflective coating (ARC) having a particular ARC film structure (materials and/or thicknesses) designed so that one of the bands (CD, DVD or Blu-ray) is processed at a high sensitivity. Sensitivity for a

photodiode is generally defined as the ratio of its output current to incident light power (e.g., in amps/watt (A/W)). For example, the ARC stack for the photodiodes may be designed so that the Blu-ray band (405 nm radiation) may have nearly its highest possible sensitivity.

SUMMARY

[0005] Disclosed embodiments recognize the conventional Anti-Reflective Coating (ARC) stack design choice for all the photodiodes (PDs) in the photodiode array (PDA) which involves a design so that one band (e.g., the Blu-ray band (for 405 nm radiation)) has nearly its highest possible sensitivity, results in the sensitivity of the PDs processing the other bands (e.g., DVD and CD bands (650 nm and 780 nm radiation, respectively)) being generally significantly lower as compared to their highest possible sensitivity. Disclosed embodiments describe processing steps and resulting PDA structures having first PDs in first diode areas having a first anti-reflective coating (ARC) stack and second PDs in second diode areas having a second ARC film stack which is different from the first ARC film stack. For CD, DVD and Blu-ray applications, disclosed PDA designs make possible independently designing the Blu-ray PDs, and DVD and CD's PDs to eliminate the conventional requirement to sacrifice the sensitivity for one or more bands (e.g., DVD and CD) to obtain nearly the highest possible sensitivity in a selected band (e.g., Blu-ray).

[0006] Disclosed PDAs provide PDs having at least two different photodiode structures, and have a multi-layer (e.g., a double-layer, or optionally a triple layer) ARC film structure including a top ARC layer and a bottom ARC layer, with the lower ARC layer being thermal silicon oxide that includes thicker regions and thinner regions across the top silicon comprising surface layer. Disclosed methods benefit from differential doping of the top silicon comprising surface of at least three times (e.g., $\geq$ an order of magnitude (10x) difference) in surface doping concentration in the final device, which enables the thermal oxidation rate over the PDs and thus the ARC film stack in the first diode areas (with PDs referred to therein as first PDs) to be different (e.g., lower) as compared to the thermal oxidation rate over the PDs and thus the ARC film stack in the second diode areas (with the other PDs referred to therein as second PDs). Applied to PDICs for processing Blu-ray, DVD and CD, each DVD and CD PDs can have a lower surface doping concentration (and thus thinner thermal silicon oxide in their ARC stacks) as compared to the doping concentration for the Blu-ray PDs (and thus thicker thermal silicon oxide in their ARC stacks).

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIG. 1 is a flow chart of steps in an example method for fabricating a photodiode array (PDA).

[0008] FIGS. 2A-D are cross-sectional views showing steps in an example method for fabricating a PDA such as shown in FIG. 1.

[0010] FIG. 3 is a cross-sectional view of an example PDA.

[0011] FIG. 4 illustrates experimental and simulated photodiode (PD) sensitivity results as a function of thermal oxide thickness in graphical form for an example PDA based on the PDs of a type described in reference to FIG. 3.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0012] FIG. 1 shows steps in an example method 100 for fabricating a photodiode array (PDA) having first photodiodes (PDs) in first diode areas having a first anti-reflective coating (ARC) stack and second PDs in second diode areas having a second ARC film stack which is different from the first ARC film stack, according to an example embodiment. Step 101 comprises providing a semiconductor substrate (e.g., a semiconductor wafer) including first diode areas and second diode areas having a bottom substrate portion doped with a first doping type, an intrinsic layer on the substrate layer, and a top silicon comprising layer doped with a second doping type on the intrinsic layer. The bottom substrate portion provides a bottom diode layer and the top silicon comprising layer provides a top diode layer. As used herein, an "intrinsic layer" is defined as a silicon comprising layer having a doping level $\leq 1 \times 10^{16} \text{ cm}^{-3}$, typically being around 10^{13} cm^{-3} (10^{13} cm^{-3} = about 450 ohm-cm for n-type doping and about 1,320 ohm-cm for Boron doping (at 300 K). The semiconductor substrate may be an epitaxial article.

[0013] The semiconductor substrate which provides the bottom substrate portion can be doped p-type or n-type, such as a p+ (doping $\geq 5 \times 10^{19} \text{ cm}^{-3}$) or an n+ substrate (doping $\geq 5 \times 10^{19} \text{ cm}^{-3}$). The substrate can comprise silicon, silicon-germanium, or other silicon comprising substrate material. As noted above, the intrinsic layer can be an epitaxial layer, and the top silicon comprising layer can also be an epitaxial layer.

[0014] FIG. 2A shows a semiconductor substrate 200 (e.g., a semiconductor wafer) having bottom substrate portion 201 doped with the first doping type, an intrinsic layer 202

thereon, and a top silicon comprising layer 203 doped with the second doping type (n-type in this example). The first doping type can be p-type and the second doping type can be n-type, or the first doping type can be n-type and the second doping type can be p-type.

[0015] Electrical isolation between the first diode area 220 and second diode area 230 is provided as shown by LOCOS region 211 (LOCAl Oxidation of Silicon, is a microfabrication process where silicon dioxide is formed in selected areas on a silicon wafer having the Si-SiO₂ interface at a lower point than the rest of the silicon surface), on a junction isolation region 206 between the first and second diode areas. When using junction isolation region 206 as shown in FIGS. 2A-2D, 3A, 3B and 4, the intrinsic layer 202 will be of a dopant type that is opposite to that of the top silicon comprising layer 203 (and the same dopant type as the bottom substrate portion 201). For example, for the top silicon comprising layer 203 being n-type, the junction isolation region 206 will be p-type.

[0016] Although not shown, trench isolation may also be used to replace LOCOS region 211 and junction isolation region 206. In this case, the intrinsic layer 202 can be either dopant type.

[0017] Step 102 comprises forming a masking layer on the first diode areas. The masking layer can be a photoresist layer, or other layer such as a dielectric layer that can be easily selectively removed. The second diode areas are exposed by the pattern of the masking layer.

[0018] Step 103 comprises implanting a surface of the second diode areas 230 with the second doping type while the masking layer protects the first diode areas 220 from the implant to provide in the final PDA a dopant concentration at a surface of the top diode layer in the second diode areas that is at least three (3) times higher than the first surface doping concentration at a surface of the top diode layer in the first diode areas. The surface doping difference can be at least an order of magnitude higher in another embodiment.

[0019] The surface of the top diode layer in the first diode areas 220 may optionally include an implant to adjust (typically increase) the resulting thermal oxide thickness as compared the resulting thermal oxide thickness when the top diode layer in the first diode areas is not implanted. It is also possible to implant both the top diode layer in the first diode areas 220 and in the second diode areas 230 with a first implant, and use a selective second implant that implants the top diode layer in the second diode areas 230 but does not implant the top diode layer in the first diode areas 220.

[0020] FIG. 2B shows the semiconductor substrate 200' (e.g., a wafer) during step 103 implantation and the resulting implanted top silicon comprising layer 204 in the second diode areas 230 having a higher surface dopant concentration compared to the surface dopant concentration in the top silicon comprising layer 203 for the first diode areas 220, where the masking layer (e.g., resist pattern) 214 is over the first diode areas 220. Method 100 uses a higher doping concentration at a surface of the top silicon comprising layer 204 in the second diode areas 230 as compared to the doping concentration at a surface of the top silicon comprising layer 203 in the first diode areas 220 to form different thermal oxide layer thicknesses as described below.

[0021] The kinetics of thermal oxidation of silicon are understood in the art. The Deal-Grove (linear-parabolic) model describes physical and chemical processes occurring during the thermal oxidation of silicon, where the silicon oxide growth rate in the linear regime is limited by the speed of the interface reaction in the thin film regime when the silicon oxide film is generally less than about 500 angstroms. As a result, the oxidation rate in the linear regime is significantly affected by surface doping level and type since the dopant alters the free energy of the silicon interface, changing the rate of interfacial chemical reactions. Dopant type (n or p) affects the free energy in different ways, and both n-type and p-type doping can be used to increase the silicon oxide growth rate in the linear regime, which is sometimes referred to in the art as "the dopant effect.". The dependence of the silicon oxide growth rate on doping level and type. For phosphorous, as the concentration of phosphorus increases from $1 \times 10^{19} \text{ cm}^{-3}$ to $1 \times 10^{21} \text{ cm}^{-3}$, the silicon oxide growth rate in the linear regime can increase in excess of 1,000 percent.

[0022] Step 104 comprises thermally oxidizing the top silicon comprising layer to form a thermal silicon oxide layer which provides a bottom ARC layer, wherein the second diode areas 230 grow the thermal silicon oxide layer thicker as compared to the thermal silicon oxide layer in the first diode areas 220. The thermal silicon oxide layer disposed between the top ARC layer described below and the silicon comprising surface of the PDs can reduce the tension/stress between the Si comprising surface and the Si and top ARC layer (e.g., silicon nitride).

[0023] FIG. 2C illustrates the semiconductor substrate 200" (e.g., a wafer) with the thermal silicon oxide layer 207 that results after the step 104 thermally oxidizing where the thermal silicon oxide layer 207 thicker over the second diode areas 230 results (which have a

having a higher surface dopant concentration) as compared to the thickness of the thermal silicon oxide thickness layer 207 over the first diode areas 220.

[0024] Step 105 comprises depositing a top ARC layer having a refractive index (n_f) greater than thermal silicon oxide (n_f about 1.46) on the bottom ARC layer. The second ARC layer can comprise silicon nitride (n_f about 2.01), silicon oxynitride, or aluminum oxide (n_f about 1.77). It is also possible to add additional ARC layer(s), such as a third ARC layer. After step 105, first PDs are provided in the first diode areas 220 and second PDs are provided in the second diode areas 230.

[0025] FIG. 2D illustrates the semiconductor substrate 200''' after step 105. The top ARC layer 242 is then patterned, pre-metal dielectric deposited, followed by contact processing, metallization and a passivation overcoat to form the completed PDIC die 300 shown in FIG. 3, where first PDs 320 are provided in the first diode areas 220 shown in FIGS. 2A-D and second PDs 330 are provided in the second diode areas 230 shown in FIGS. 2A-D, where the first PDs and the second PDs have different photodiode structures.

[0026] FIG. 3 depicts a disclosed PDA 300 showing a portion thereof. PDA 300 can be embodied as a PIN PDA or a NIP PDA, respectively. Generally, PDA 300 will be in a two dimensional array of PDs in a plurality of rows and columns, and each PD when embodied as a PD integrated circuit (PDIC) will be coupled to an amplifier on the chip, and the PDIC will generally also include readout circuitry. PDA 300 includes a semiconductor substrate having a bottom substrate portion 201 doped with a first doping type, an intrinsic layer 202 on the bottom substrate portion, and a top silicon comprising layer 203 doped with a second doping type on the intrinsic layer 202. As noted above, there is a first PDA 320 corresponding to the first diode areas 220 shown in FIGS. 2A-2D, and a second PDA 330 corresponding to the second diode areas 230 shown in FIGS. 2A-2D, with the bottom substrate portion 201 providing a bottom diode layer and the top silicon comprising layer 203 providing a top diode layer.

[0027] The doping at the semiconductor surface of the first PDA 320 is shown as region 209 which includes an optional implant to provide doping beyond that of top silicon comprising layer 203 in the first diode areas. The doping at the semiconductor surface of the second PDAs 330 is shown as top silicon comprising layer 204 which includes an implant described above, designed to provide a higher doping concentration at the top silicon comprising surface as

compared to the doping concentration at the top silicon comprising surface of the first PDA 320, which is at least three times higher (e.g., an order of magnitude higher).

[0028] The thermal silicon oxide layer 207 is on a surface of the top silicon comprising layers 204 for PDA 330 and for top silicon comprising layers 209 for PDA 320. Thermal silicon oxide layer 207 provides a bottom ARC layer for PDA 320 and second PDA 330, respectively. The thermal silicon oxide layer 207 is thicker for the second PDA 330 as compared to the thermal silicon oxide layer 207 for the first PDA 320. In one embodiment, the thermal silicon oxide layer 207 in the second PDA 330 is 100 to 240 Å thick and the thermal silicon oxide layer 207 in the first PDA 320 is 20 to 95 Å thick.

[0029] Thermal silicon oxide is known in the art to be physically distinct from other silicon oxides formed by other methods, such as chemical vapor deposition (CVD) and its variants. These distinctions include thermal silicon oxide having (1) a nearly electrically perfect interface between silicon and silicon oxide; (2) higher dielectric strength of the thermal silicon oxide; and (3) excellent control of the thickness uniformity of the silicon oxide film. For example, regarding dielectric strength, thermal silicon oxides can provide dielectric strength of $>1 \times 10^7$ V/cm; while CVD silicon oxides have a lower dielectric strength typically being 1×10^6 V/cm to 3×10^6 V/cm.

[0030] The top ARC layer 242 has a refractive index greater than thermal silicon oxide and is on the thermal silicon oxide layer 207/bottom ARC layer. PDA 300 is shown including a sinker diffusion 226 for providing a low resistance connection from the top side of the PDA 300 to the bottom substrate portion 201, and contact regions 228 allowing low resistance contacts to regions 209 and 204 which provides the top diode layer for first PDA 320 and second PDA 330, respectively. PDA 300 includes a pre-metal dielectric layer 310, filled contacts 312 through the pre-metal dielectric (PMD) layer 310, a multilayer metal stack 315 on the PMD layer 310, and a passivation overcoat layer 340 on the multilayer metal stack 315. There are apertures in the multilayer metal stack 315 and passivation overcoat layer 340 to provide exposed ARC surfaces to the ambient (except at their periphery) for receiving incident radiation (light) at the respective PDAs 320 and 330.

[0031] FIG. 4 provides experimental and simulated PD sensitivity results as a function of thermal oxide thickness in graphical form from an example PDA based on the PDs described relative to FIG. 3. The top ARC layer was silicon nitride about 520 Å thick for all PDs. All PDs

were PIN PDs. Both the first PDs in the first diode areas and second PDs in the second diode areas both received n-type ion implants, with their n-type implants being different. First PDs 320 received phosphorous at 70 keV at a dose of $5.0 \times 10^{13} \text{ cm}^{-2}$ with the resulting thermal oxide thickness 207 being about 80A, and the second PDs received arsenic at 80 keV at a dose of $5.0 \times 10^{14} \text{ cm}^{-2}$ with the resulting thickness of the thermal silicon oxide layer 207 being about 150A.

[0032] From the data provided, it can be seen using a conventional single thermal oxide thickness, such as at the 80 A and 150 A values shown on the experimental data, PD sensitivity is traded off between the Blu-ray PDs and CD and DVD PDs. At 80 A, the PD sensitivity for Blu-ray is 0.314 A/W, for DVD 0.448 A/W CD 0.471 A/W. At 150 A, the PD sensitivity for Blu-ray is 0.272 A/W (reduced relative to 80 A), for DVD 0.471 A/W (increased relative to 80 A), and for CD 0.492 A/W (increased relative to 80 A). As disclosed above, by selective implantation, disclosed PDAs can provide thinner thermal oxide (e.g., 80 A) for some PDs, such as Blu-ray PDs, and a thicker thermal oxide (e.g., 150 A) for other PDs (for DVD and CD). As a result, in one example disclosed PDs can provide relatively high sensitivity for Blu-ray, DVD and CD PDs by providing 80 A thermal oxide for Blu-ray PDs to provide a PD sensitivity for Blu-ray of 0.314 A/W, while providing 150 A thermal oxide for DVD and CD PDs to provide a PD sensitivity of 0.471 A/W and 0.492 A/W respectively.

[0033] Disclosed embodiments can be used to form semiconductor die that may be integrated into a variety of assembly flows to form a variety of different devices and related products. The semiconductor die may include various elements therein and/or layers thereon, including barrier layers, dielectric layers, device structures, active elements and passive elements including source regions, drain regions, bit lines, bases, emitters, collectors, conductive lines, conductive vias, etc. Moreover, the semiconductor die can be formed from a variety of processes including bipolar, CMOS, BiCMOS and MEMS.

[0034] Those skilled in the art to which this disclosure relates will appreciate that many other embodiments and variations of embodiments are possible within the scope of the claimed invention, and further additions, deletions, substitutions and modifications may be made to the described embodiments without departing from the scope of this disclosure.

CLAIMS

What is claimed is:

1. A method of fabricating a photodiode array, comprising:
 - providing a semiconductor substrate including first diode areas and second diode areas having a bottom substrate portion doped with a first doping type, an intrinsic layer on the substrate portion, and a top silicon comprising layer doped with a second doping type on the intrinsic layer, the bottom substrate portion providing a bottom diode layer and the top silicon comprising layer providing a top diode layer,
 - forming a masking layer on the first diode areas;
 - implanting the second diode areas with the second doping type while the masking layer protects the first diode areas to provide a second surface dopant concentration in a surface of the second diode areas that is at least three times higher than a first surface dopant concentration in a surface of the first diode areas;
 - thermally oxidizing the top silicon comprising layer to form a thermal silicon oxide layer to provide a bottom anti-reflective coating (ARC) layer, wherein the second diode areas grow the thermal silicon oxide layer thicker as compared to the thermal silicon oxide layer on the first diode areas, and
 - depositing a top ARC layer having a refractive index greater than thermal silicon oxide on the bottom ARC layer,
 - wherein first photodiodes (PDs) are provided in the first diode areas and second PDs are provided in the second diode areas.
2. The method of claim 1, wherein the top ARC layer comprises silicon nitride.
3. The method of claim 1, wherein the second surface dopant concentration is at least an order of magnitude higher than the first surface dopant concentration.
4. The method of claim 1, wherein the first doping type is n-type and the second doping type is p-type.

5. The method of claim 1, wherein the first doping type is p-type and the second doping type is n-type.
6. The method of claim 1, wherein the thermal silicon oxide layer in the second diode areas is 100 to 240 Å thick and the thermal silicon oxide layer in the second diode areas is 20 to 95 Å thick.
7. The method of claim 1, wherein the thermally oxidizing comprises a steam oxidation.
8. The method of claim 1, further comprising implanting the surface of the second diode areas with the second doping type.
9. A photodetector array, comprising:
 - a semiconductor substrate including first diode areas and second diode areas having a bottom substrate portion doped with a first doping type, an intrinsic layer on the bottom substrate portion, and a top silicon comprising layer doped with a second doping type on the intrinsic layer, the bottom substrate portion providing a bottom diode layer and the top silicon comprising layer providing a top diode layer,
 - wherein a second surface dopant concentration in a surface of the second diode areas that is at least three times higher than a first surface dopant concentration in a surface of the first diode areas;
 - a thermal silicon oxide layer on the top silicon comprising layer which provides a bottom anti-reflective coating (ARC) layer for the first and second diode areas, wherein the second diode areas have the thermal silicon oxide layer thicker as compared to the thermal silicon oxide layer on the first diode areas, and
 - a top ARC layer having a refractive index greater than the thermal silicon oxide layer on the bottom ARC layer,
 - wherein first PDs are provided in the first diode areas and second PDs are provided in the second diode areas.

10. The PDA of claim 9, wherein the top ARC layer comprises silicon nitride.
11. The PDA of claim 9, wherein the second surface dopant concentration is at least an order of magnitude higher than the first surface dopant concentration.
12. The PDA of claim 9, wherein the first doping type is n-type and the second doping type is p-type.
13. The PDA of claim 9, wherein the first doping type is p-type and the second doping type is n-type.
14. The PDA of claim 9, wherein the thermal silicon oxide layer in the second diode areas is 100 to 240 Å thick and the thermal silicon oxide layer in the second diode areas is 20 to 95 Å thick.
15. The PDA of claim 9, wherein the surface of the second diode areas included an implanted surface region of the second doping type.
16. The PDA of claim 10, wherein the semiconductor substrate comprises silicon or silicon germanium.

1/5

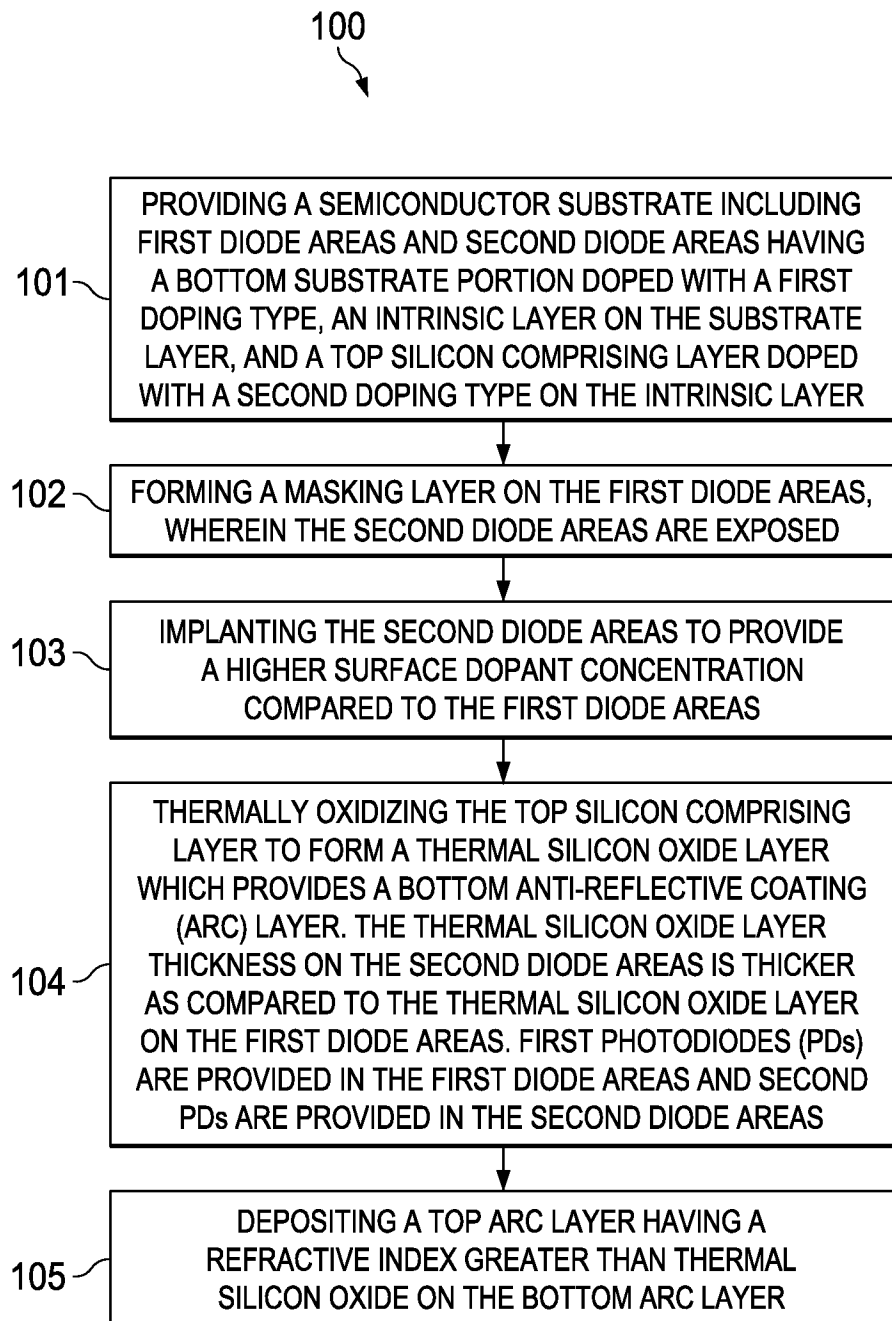


FIG. 1

2/5

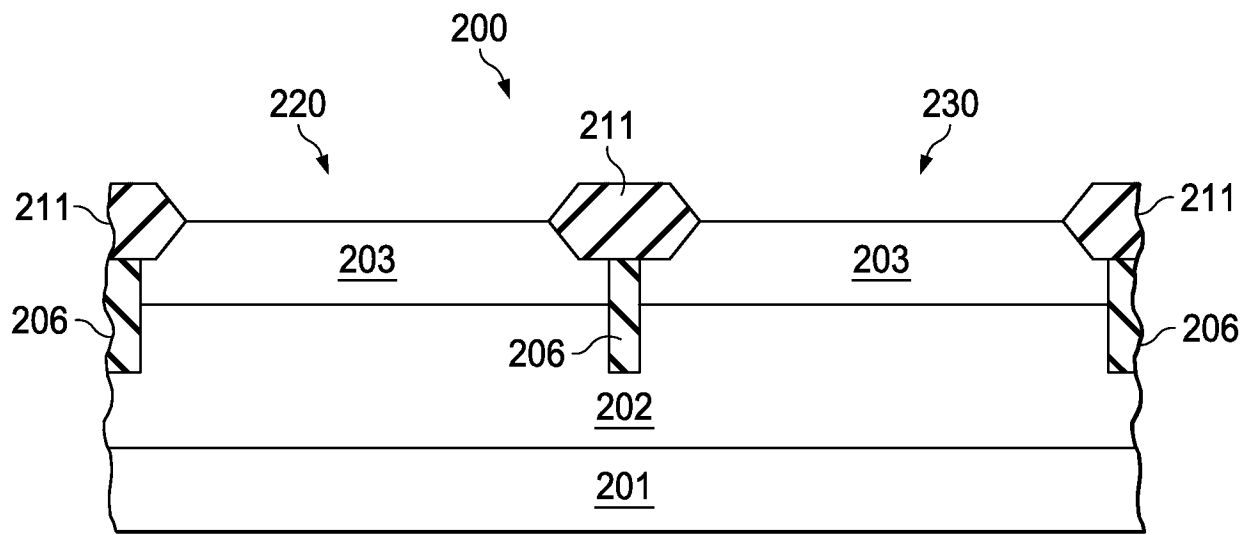


FIG. 2A

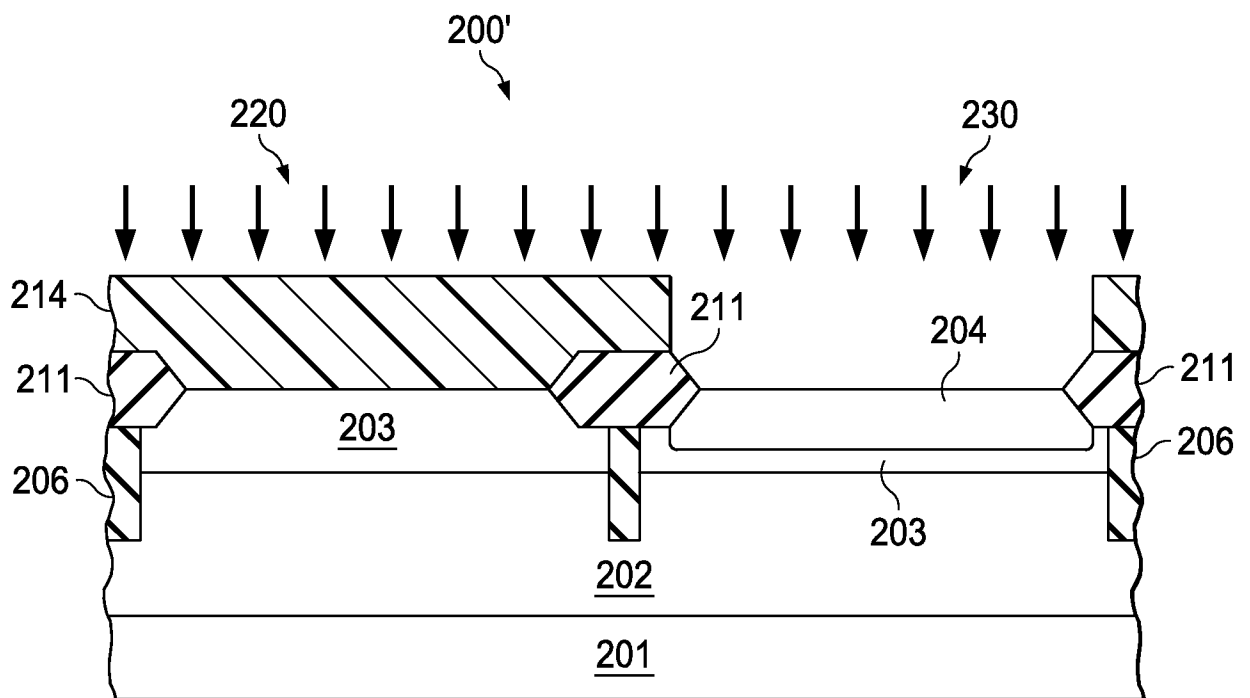


FIG. 2B

3/5

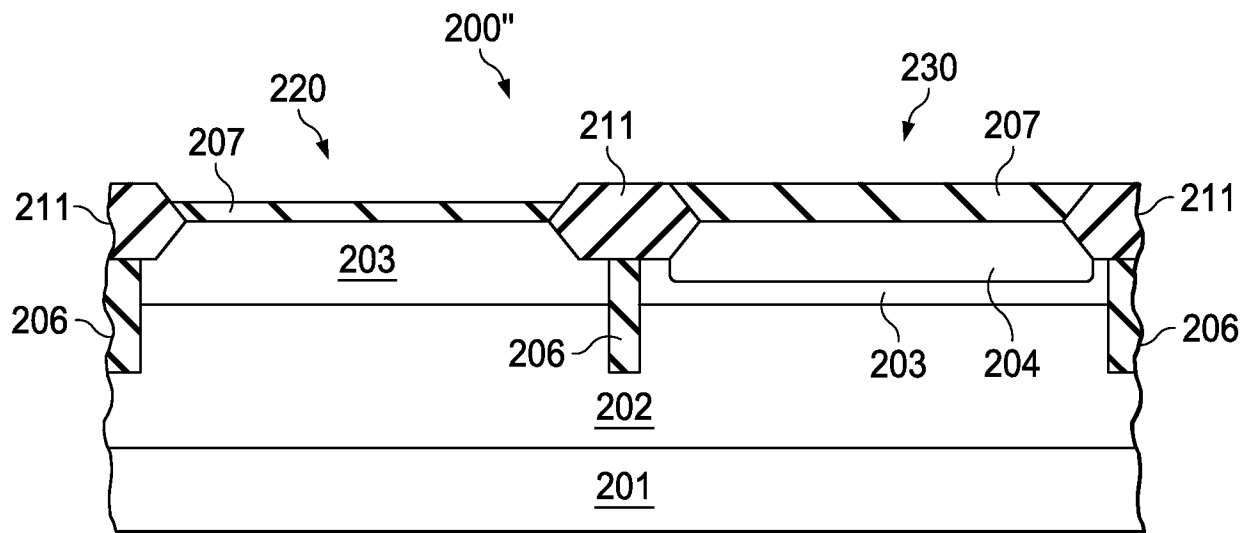


FIG. 2C

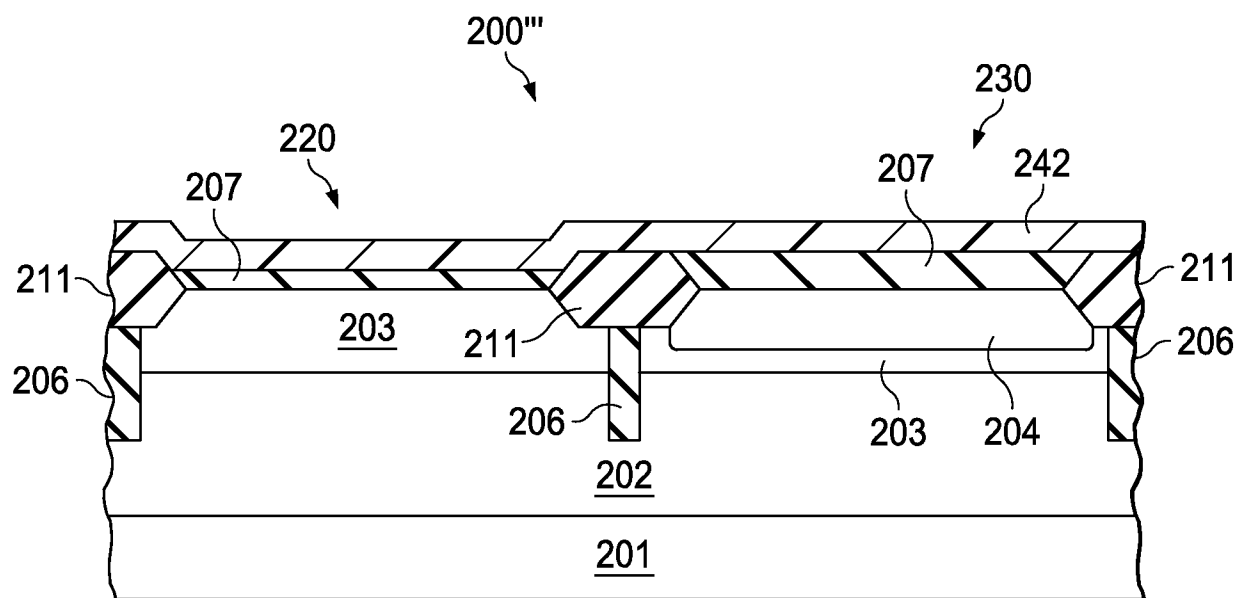


FIG. 2D

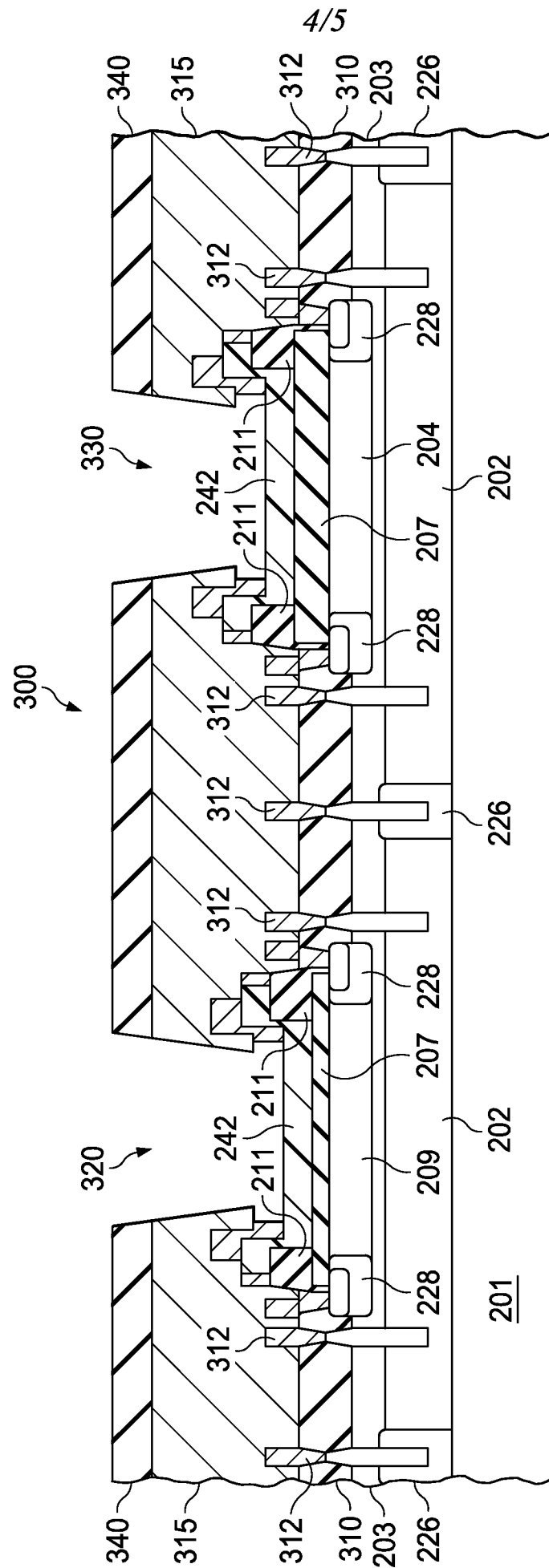
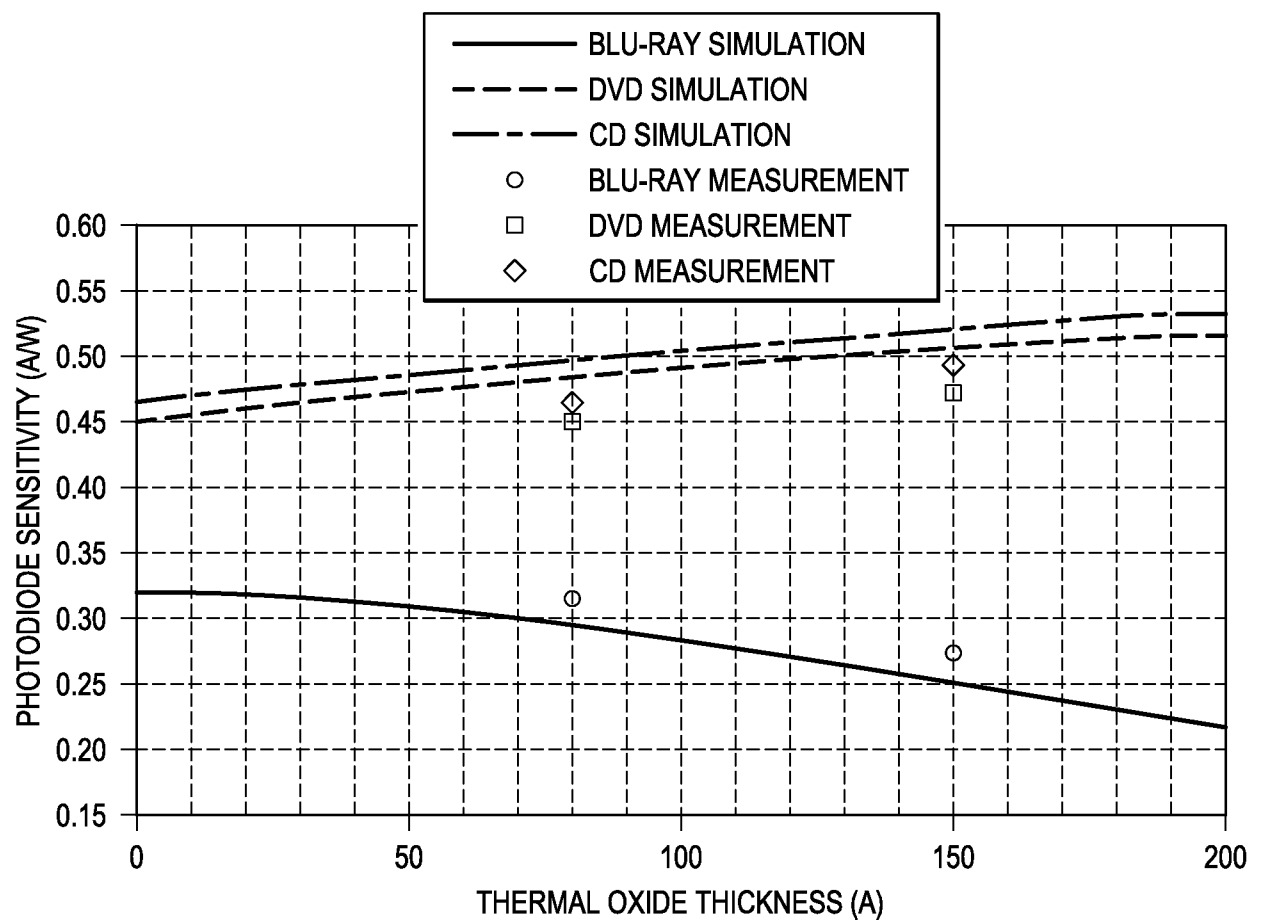


FIG. 3

5/5

FIG. 4



INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2014/035702

A. CLASSIFICATION OF SUBJECT MATTER <i>H01L 21/0288 (2006.01)</i> According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H01L 21/00, 31/00, 31/02, 31/0216, 31/0224, 31/06, 31/072, 31/10, 31/101, 31/102, 31/103, 31/108, 31/14, 31/18 Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2008/129433 A2 (KONINKLIJKE PHILIPS ELECTRONICS N.V. et al.) 30.10.2008	1-16
A	US 2007/0012948 A1 (J. CHRISTOPHER DRIES et al.) 18.01.2007	1-16
A	EP 1737047 A1 (NEC CORPORATION) 27.12.2006	1-16
A	US 2010/0163759 A1 (STMICROELECTRONICS S.R.L.) 01.07.2010	1-16
A	EP 1995793 A1 (NEC CORPORATION) 26.11.2008	1-16
A	RU 75505 U1 (INSTITUT FIZIKI POLUPROVODNIKOV SIBIRSKOGO OTDELENIYA ROSSYSKOI AKADEMII NAUK) 10.08.2008	1-16
☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.		
* Special categories of cited documents: “A” document defining the general state of the art which is not considered to be of particular relevance “E” earlier document but published on or after the international filing date “L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) “O” document referring to an oral disclosure, use, exhibition or other means “P” document published prior to the international filing date but later than the priority date claimed “T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention “X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone “Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art “&” document member of the same patent family		
Date of the actual completion of the international search 15 August 2014 (15.08.2014)		Date of mailing of the international search report 28 August 2014 (28.08.2014)
Name and mailing address of the ISA/RU: FIPS, Russia, 123995, Moscow, G-59, GSP-5, Berezhkovskaya nab., 30-1 Facsimile No. +7 (499) 243-33-37		Authorized officer M. Bryleva Telephone No. 499-240-25-91