

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
30 November 2006 (30.11.2006)

PCT

(10) International Publication Number
WO 2006/127927 A1

(51) International Patent Classification:
H03C 3/09 (2006.01) **H04L 27/20** (2006.01)

(21) International Application Number:
PCT/US2006/020297

(22) International Filing Date: 24 May 2006 (24.05.2006)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/684,016 24 May 2005 (24.05.2005) US

(71) Applicant (for all designated States except US): **AXIOM MICRODEVICES, INC.** [US/US]; 21 Technology Drive, Suite 102, Irvine, CA 92618 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **ZACHAN, Jeff** [US/US]; 40 Vista Del Cerro, Aliso Viejo, CA 92656 (US). **HARTMAN, David** [US/US]; 26861 Anadale Drive, Laguna Hills, CA 92653 (US). **LIN, Ming** [—/US]; 37 Copper Leaf, Irvine, CA 92602 (US). **DAMGAARD, Morten** [DK/US]; 24911 Sausalito Street, Laguna Hills, CA 92653 (US). **KEE, Scott** [US/US]; 2480 Irvine Blvd., #301, Tustin, CA 92782 (US).

(74) Agents: **ROURK, Christopher, J.** et al.; Jackson Walker L.L.P., 901 Main Street, Suite 6000, Dallas, TX 75202 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

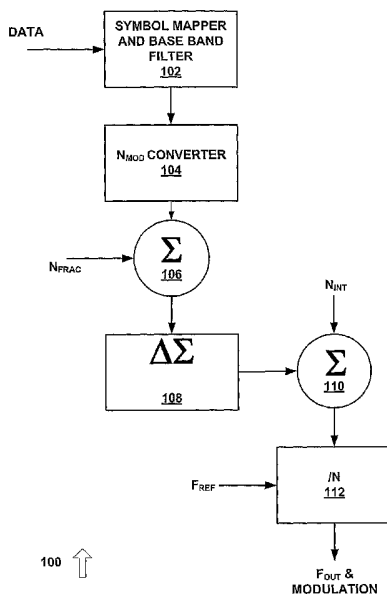
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

[Continued on next page]

(54) Title: A METHOD FOR MODULATING PHASE OR FREQUENCY IN A COMMUNICATION SYSTEM USING CLOCK DIVISION



(57) Abstract: A direct division modulator is provided. The direct division modulator includes a symbol mapper converting the input data from a binary bitstream to a desired frequency deviation, such as where the frequency deviation data encodes the information from the bitstream. A converter generates a divide value using the desired frequency deviation information, and a summer adds an average value to the divide value. A converter quantizes the divide value and shapes quantization noise associated with the quantized divide value. A divider modulates a reference signal with the quantized divide value and generates an output signal.

WO 2006/127927 A1



For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

5

TITLE: A Method For Modulating Phase Or
10 Frequency In A Communication System Using Clock Division.

RELATED APPLICATIONS

This application claims priority to U.S. Provisional
15 Application 60/684,016, filed May 24, 2005, entitled "A
METHOD FOR MODULATING PHASE OR FREQUENCY IN A COMMUNICATION
SYSTEM USING CLOCK DIVISION," which is hereby incorporated
by reference for all purposes.

20

FIELD OF THE INVENTION

[0001] The present invention relates generally to
communication techniques using phase or frequency
modulation, such as in conjunction with a power amplifier.

BACKGROUND OF THE INVENTION

[0002] There are a number of approaches to solving the problem of modulating radio frequency (RF) carrier phase and frequency. The translational loop (TL), or offset phase-locked loop (PLL) uses a mixer in the feedback path of a transmit PLL to offset the output carrier frequency and an analog baseband I/Q data modulator in either the reference or feedback path of the transmit PLL to apply modulation. The primary drawback to the TL is that it requires well matched IF circuits that can occupy much more area than a design comprised primarily of digital blocks.

[0003] Another approach to modulating the output RF carrier is to apply the modulation via the feedback divider in a fractional-N PLL synthesizer. In this case a sigma-delta programmed multi-modulus divider is typically used to vary the loop output frequency and/or phase. The primary drawback to this architecture is that it requires careful calibration of the loop components and pre-emphasis filtering of the digital data in order to mitigate the distortion caused by the filtering in the PLL when the data bandwidth is greater than or comparable to the loop bandwidth. In some cases, this calibration can be more difficult by the fact that the fractional-N PLL bandwidth must be made narrower than the signal bandwidth in order to reject the shaped sigma-delta quantization noise and reference source noise.

[0004] In an integrated circuit with an integrated power amplifier (PA) in the modulation path, which causes temperature drift of loop components during a burst, the design requires either an adaptive pre-emphasis filter or a

[0005] technique for adaptively adjusting the loop gain,
both of which are non-optimal.

SUMMARY OF THE INVENTION

[0006] Therefore, a modulation technique is provided where the data requires no or minimal pre-emphasis, so the loop bandwidth of the transmit loop can be kept wide with respect to the data bandwidth.

[0007] In particular, a direct division modulation technique is provided that allows a wide loop bandwidth to be provided relative to the data bandwidth.

[0008] In accordance with an exemplary embodiment of the present invention, a direct division modulator is provided. The direct division modulator includes a symbol mapper converting the input data from a binary bitstream to a desired frequency deviation, such as where the frequency deviation data encodes the information from the bitstream.

A converter generates a divide value using the desired frequency deviation information, and a summer adds an average value to the divide value. A converter quantizes the divide value and shapes quantization noise associated with the quantized divide value. A divider modulates a reference signal with the quantized divide value and generates an output signal.

[0009] The present invention provides many important technical advantages. One important technical advantage of the present invention is a modulation architecture where the transmit loop is a translational loop with an integrated power amplifier which can mitigate AM/PM distortion created by the power amplifier if the power amplifier is within the loop.

[0010] Those skilled in the art will further appreciate the advantages and superior features of the invention together with other important aspects thereof on reading the

[0011] detailed description that follows in conjunction with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIGURE 1 is a diagram of a process for direct divided modulation (DDM) as a phase/frequency modulation technique, in accordance with an exemplary embodiment of the present invention;

[0013] FIGURES 2A and 2B are diagrams of systems showing exemplary implementations the of the DDM modulator with an associated transmitter in accordance with an exemplary embodiment of the present invention; and

[0014] FIGURE 3 is a diagram of a system showing an implementation the of the DDM modulator digital processing as it would be used in a GSM/EDGE system in accordance with an exemplary embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0015] In the description which follows, like parts are marked throughout the specification and drawing with the same reference numerals, respectively. The drawing figures
5 may not be to scale and certain components may be shown in generalized or schematic form and identified by commercial designations in the interest of clarity and conciseness.

[0016] **FIGURE 1** is a diagram 100 of a process for direct divided modulation (DDM) as a phase/frequency modulation
10 technique, in accordance with an exemplary embodiment of the present invention. This technique can be used with GSM signals, EDGE signals, or other suitable applications, such as where the carrier phase or frequency is modulated. A programmable divider is used to apply phase or frequency
15 modulation to a periodic source signal.

[0017] In one exemplary implementation, the DDM adds phase and/or frequency modulation via the divider /N 112 to the input clock signal F_{ref} . F_{ref} is a signal applied to the DDM that can come from a source that operates at a suitable
20 clock frequency, including an integer-N frequency synthesizer, fractional-N synthesizer, crystal oscillator, or other suitable sources.

[0018] Data in a digital format is input to symbol mapper and baseband filter 102, which converts the input data from
25 a binary bitstream to a digitized instantaneous frequency output. This output defines the desired frequency deviation at F_{out} . Once the data has been mapped, filtered and converted to a frequency value, it is provided to N_{mod} converter 104, which manipulates the output from symbol
30 mapper and baseband filter 102 into a frequency divide word that can be added to a channel select divide value N_{frac} in

summer 106. In this manner, the frequency deviation information is converted into a divide value for modulating the frequency, such that the divide value is inversely proportional to the frequency deviation information. N_{frac} is added to give an average divide value, to allow a particular output frequency at F_{out} to be selected to modulate around.

[0019] In one exemplary embodiment, N_{frac} is related to F_{ref} and F_{out} (e.g., $N_{\text{int}} + N_{\text{frac}}$ would be 5.25 if F_{ref} is 5.25 gigahertz and F_{out} is one gigahertz). Sigma-delta ($\Delta\Sigma$) converter 108 quantizes the divide value to a smaller number of bits and shapes the error caused by quantization in such a way that the error is small near the desired frequency but larger at frequencies that are farther away from the desired frequency. In one exemplary embodiment, the shaping algorithm essentially takes the three most significant bits of a 26 bit divide value, where the error signal is further used to shape the signal. The output of sigma-delta converter 108 is summed through summer 110 with a suitable integer divide value N_{int} to provide further channel selection programmability. Adding a constant value biases the output divide value, essentially allowing selection of the average divide value. It is further noted that N_{int} can pass through the sigma-delta converter 108 if added to the input stream to sigma-delta converter 108, it can be provided to the signal stream either before after sigma-delta converter 108.

[0020] The output of summer 110 is presented to the divider /N 112, where its output, F_{out} , represents a divided value of F_{ref} with data and modulation. Divider /N 112 can

be a programmable counter or other suitable frequency dividing circuit.

[0021] F_{out} can be transmitted unaltered or can be further processed, filtered, up-converted, or down-converted.

5 Likewise, a suitable form of digital and/or analog filtering can be applied to F_{out} , direct up conversion via mixing of F_{out} can be applied, up conversion of F_{out} via an offset PLL or translation loop can be applied, or other suitable signal processing techniques can be applied.

10 [0022] FIGURES 2A and 2B are diagrams of systems 200A and 200B showing an implementation the of the DDM modulator with an associated transmitter in accordance with an exemplary embodiment of the present invention. System 200A allows modulation to be applied directly to transmit translation
15 loop.

[0023] System 200A can be implemented in a compact and mostly digital implementation, in one exemplary embodiment. Transmit loop 204 is a translational loop (TL) with a power amplifier 210 that mitigates amplitude modulation and phase
20 modulation distortion when the power amplifier is within the loop and allows for a wide closed loop bandwidth. Direct divided modulator (DDM) 212 allows the transmit loop bandwidth to be kept wide, such as to allow error correction of errors introduced in the output by the power amplifier,
25 but can also be implemented without a power amplifier.

[0024] System 200A converts the input signal to a suitable output frequency through the action of mixer 224 and attenuates the phase noise introduced by DDM 212. The input data requires little or no pre-emphasis as the loop
30 bandwidth of transmit loop 204 can be kept wide with respect to the data bandwidth. The frequency plan is highly

flexible since DDM 212 can divide by any suitable number, which can also help to avoid unwanted spurs by providing multiple options to generate a given frequency. If reference clock feed-through is an issue in transmit loop 5 204, F_{out} can be adjusted to a higher frequency to allow for more attenuation via transmit loop low-pass filter 214.

[0025] In one exemplary embodiment, system 200A operates using reference frequency source 220 to produce the input clock F_{ref} to DDM 212. Input data and N_{frac} are also provided 10 to DDM 212 as described in FIGURE 1.

[0026] Clock signal F_{ref} is applied to DDM 212 to produce the modulated reference F_{out} , and is also provided to $/M$ divider 222, having a division factor of M , which in one exemplary embodiment is programmable. The output of $/M$ 15 divider 222 is clock signal F_b , which is applied to mixer 224 in the feedback path of transmit loop 204, which mixes the output of transmit loop 204 down to the same frequency as modulated reference F_{out} .

[0027] Both the output of the DDM 212 and the output of 20 mixer 224 are applied to phase-frequency detector 226. Down conversion is accomplished by mixing the output of $/M$ divider 222 and power amplifier 210. The output of phase-frequency detector 226 is applied to charge pump (CP) 228, the output of which is then applied to low-pass filter 214 25 to pass a modulation signal that is applied to voltage-controlled oscillator 229, which produces the modulated output signal at the output radio frequency or at a multiple of the output radio frequency.

[0028] The modulated output signal is then divided, where 30 suitable, such as by divider 230, and the signal is then applied to power amplifier 210, which amplifies the signal

to a suitable transmit level. The output of power amplifier 210 is sensed (as shown by the dotted line) and applied to the feedback loop.

[0029] In one exemplary embodiment, transmit loop 204 can be a 4th order Type II (charge pump phase-frequency detector) loop with mixer 224 in the feedback path. Power amplifier 210 can be integrated in the loop in order to track amplitude modulation to phase modulation (AM to PM) distortion in an EDGE transmission mode or other suitable data. The loop bandwidth can be kept wide in order to avoid distorting the transmitted signal and to minimize synchronization problems with the amplitude modulation loop.

[0030] System 200B utilizes an architecture similar to that of system 200A, except that the output from voltage-controlled oscillator 229 is provided to both divider 230 and mixer 224, so as to eliminate the need to provide feedback to mixer 224 from power amplifier 210. Furthermore, the voltage-controlled oscillator 229 can also be provided to only the divider 230, in which case, the mixer receives the output of the divider 230 as shown by the dotted line. Lastly, voltage controlled oscillator 229 can be used to drive both power amplifier 210 and mixer 224, eliminating divider 230. System 200B further utilizes two exemplary reference frequency sources 220A and 220B, each generating a reference frequency of F_{ref} . Reference frequency sources 220A and 220B can likewise be used in conjunction with system 200A.

[0031] FIGURE 3 is a diagram of a system 300 showing an implementation of the DDM modulator in conjunction with digital processing as it would be used in a GSM/EDGE system in accordance with an exemplary embodiment of the present

invention. System 300 provides an exemplary embodiment of symbol mapper and base band filter 102 and N_{mod} calculation and interpolation.

[0032] System 300 includes registers for the static
5 fractional (N_{frac}) and integer (N_{int}) divide values and the two coefficients associated with calculating N_{mod} . System 300 receives input bits from the serial data interface and can perform suitable processes for GMSK modulation. In one
10 exemplary embodiment, differential encoder 302 receives the input bit stream, and non-return to zero encoder 304 (NRZ) maps [0,1] bit sequences to [1,-1]. Up-sampler 306 increases the sample rate to a suitable number, such as 12 samples per symbol. Gaussian filter 308 is then applied to reduce the signal bandwidth according to the GSM
15 specification.

[0033] For the exemplary EDGE 8 phase-shift keyed bits of data, the following operations can be used. The 8 phase-shift keyed bits of data are mapped by 8-PSK mapper 310 to extract the in-phase and quadrature phase data. Up-sampler
20 312 increases the sample rate to a suitable number, such as 12 samples per symbol. FIR filter 314 is then applied to the signal to reduce the signal bandwidth according to the GSM specification. In-phase/quadrature-phase to R/Theta conversion is then performed, such as by CORDIC converter
25 315 or other suitable converters. The magnitude $R(\text{mag})$ is passed to the AM loop through cascaded integrator-comb (CIC) interpolation filter 316 and delay alignment 318.

[0034] The phase to frequency conversion signal path can be common from CORDIC converter 215, which can provide the
30 phase data to a phase differentiator 320. Output from Gaussian filter 308 or phase differentiator 320, labeled as

F_{mod} , is provided to N_{mod} calculator 322 through switch 321A or 321B, depending upon the mode of operation (GSM or EDGE). The N_{mod} output is then added to a suitable fixed fractional offset N_{frac} via summer 324. The signal can then be up-
5 sampled to a suitable sample frequency, such as 26 MHz, and filtered by interpolator 326. One suitable method of accomplishing upsampling and filtering is through the use of a CIC filter. The division word is then applied to sigma-delta modulator 328, which is clocked by the output
10 modulated signal. A suitable division value is applied to $/N$ divider 332, which also receives reference frequency F_{ref} .
[0035] Differential encoder 302 can be started as if it had received a sequence of 1's. This means that the $d[i-1]$ value (in the register) at start-up can be a 1. Each
15 successive bit can be calculated as shown:

$$\begin{aligned}y[i] &= d[i] \oplus d[i-1] \\d[-1] &= 1\end{aligned}$$

[0036] Likewise, GMSK non-return to zero encoder 304 mapping can be used to convert the differentially encoded
20 data to a binary non-return to zero format, such as where the circuit maps [0 1] to [1 -1]:

$$a[i] = 1 - 2y[i]$$

[0037] In one exemplary embodiment, the GMSK Gaussian
25 filter 308 can use a symmetric 60-tap FIR filter with 12 samples per symbol. The input data can be up-sampled prior to applying the Gaussian filter.

[0038] In another exemplary embodiment, 8-PSK mapper 310
30 can map the input 3 bit symbol to an in-phase and quadrature phase constellation point, and can also perform $3\pi/8$ rotation or other suitable rotation that may be required

after each symbol, such as by 3GPP TS 45.004, Technical Specification Group GSM/EDGE Radio Access Network; Modulation, which is hereby incorporated by reference for all purposes.

5 [0039] FIR filter 314 can be an 8-PSK transmit filter, such as a 60-tap FIR filter or other suitable filters. The tap values and number of symbols over which to filter can be selected as suitable, such as to comply with 3GPP TS 45.004, Technical Specification Group GSM/EDGE Radio Access Network; 10 Modulation. The input data can up-sampled by up-sampler 312, such as to 12 samples per symbol or other suitable samples, prior to filtering.

15 [0040] CORDIC converter 315 is used to generate amplitude and phase (R/Theta) values from the in-phase/quadrature-phase base-band output of the FIR filter 314, such as by use of a CORDIC algorithm or other suitable algorithms. In one exemplary embodiment, an iterative algorithm, such as one that uses a look-up table for angle calculation, can be used. The size of the table can be the same as the number 20 of iterations, or other suitable sizes. The word-width can be set to maintain the RMS phase error below a predetermined level, such as 1°. A fixed magnitude correction can be applied after the R/Theta calculation, such as that described in Hu, YH, "CORDIC-Based VLSI Architectures for 25 Digital Signal Processing," IEEE Signal Processing Magazine, July 1992, which is hereby incorporated by reference for all purposes.

30 [0041] The phase to frequency conversion can be performed using a simple differentiator with its output value scaled by the sample frequency. The sample frequency word can be

stored in a register and used to multiply the delta between successive phase samples.

[0042] In one exemplary embodiment, frequency to N_{mod} conversion can be performed using a second order Taylor series that avoids the necessity for a division (or inversion) of the modulation frequency, such as where the division may be necessitated by the action of the DDM modulation. One exemplary formula is:

$$N_{\text{mod}} = a_1 F_{\text{mod}} + a_2 F_{\text{mod}}^2$$

$$a_1 = -\frac{(N_{\text{int}} + N_{\text{frac}})^2}{F_{\text{ref}}}$$

$$a_2 = \frac{(N_{\text{int}} + N_{\text{frac}})^3}{F_{\text{ref}}^2}$$

where:

F_{ref} = frequency of a reference frequency source

N_{int} = fixed integer value

N_{frac} = fractional divide value

a_1, a_2 = coefficients calculated in advance of the burst.

[0043] The interpolator 326 can be used to upsample and filter the frequency data to a rate suitable for application to sigma-delta modulator 328 which is operated at the IF frequency. If this were done without any intervening interpolation filtering the resulting sample images would lie at multiples of 3.25 MHz, which would make the rejection requirement in the transmit loop difficult to meet. In order to avoid this problem the data can be up sampled to 26 MHz using interpolator 326. One suitable method of accomplishing this upsampling and filtering is through the use of a CIC filter.

[0044] In view of the above detailed description of the present invention and associated drawings, other modifications and variations are apparent to those skilled in the art. It is also apparent that such other
5 modifications and variations may be effected without departing from the spirit and scope of the present invention.

WHAT IS CLAIMED IS:

1. A direct division modulator comprising:

a symbol mapper converting the input data from a binary
5 bitstream to a desired frequency deviation;

a converter generating a divide value using the desired
frequency deviation information;

a summer adding an average value to the divide value;

a converter quantizing the divide value and shaping
10 quantization noise associated with the quantized divide
value; and

a divider modulating a reference signal with the
quantized divide value and generating an output signal.

15 2. The direct division modulator of claim 1 wherein
the divide value is derived from modulation frequency
deviation information and the quantized divide value is
inversely proportional to the instantaneous output
frequency.

20 3. The direct division modulator of claim 1 further
comprising a frequency source providing the reference
signal.

25 4. The direct division modulator of claim 1 further
comprising a transmit loop receiving the output signal and
rejecting the quantization noise.

5 5. The direct division modulator of claim 3 further comprising a transmit loop receiving the output signal and the reference signal and modulating the output signal with the reference signal to aid in rejecting the quantization noise.

10 6. The direct division modulator of claim 1 wherein the average value comprises an integer portion and a fractional portion.

15 7. The direct division modulator of claim 1 wherein the average value comprises a fractional portion that is added to the divide value prior to the converter and an integer portion that is added to the quantized divide value prior to modulation of the divide value with the divider.

 8. The direct division modulator of claim 1 wherein the converter is a sigma-delta converter.

9. A system for transmitting a signal comprising:
a frequency source generating a reference frequency;
a direct division modulator receiving a binary
bitstream of input data, modulating a desired frequency
5 deviation onto the reference frequency, and dividing the
reference frequency by an predetermined number; and
a transmit loop receiving the modulated and divided
reference signal and the reference signal and generating a
modulated transmission signal.

10

10. The system for transmitting a signal of claim 9
wherein the transmit loop further comprises:

a divider receiving the reference signal and reducing
the reference signal to a clock signal; and

15

a phase-frequency detector receiving a signal derived
from the clock signal and the modulated and divided
reference signal and outputting a noise-reduced modulated
and divided reference signal.

11. The system of claim 9 wherein the direct division
20 modulator further comprises a selector allowing controllable
processing of an 8-PSK signal or a GMSK signal.

12. The system of claim 11 wherein the direct division
modulator further comprises a FIR filter in a signal
25 processing path for the 8-PSK.

13. The system of claim 11 wherein the direct division
modulator further comprises a Gaussian filter in a signal
processing path for the GMSK signal.

30

14. The system of claim 9 wherein the divide value is derived from modulation frequency deviation information and the divide value is inversely proportional to the frequency deviation information.

5

15. The system of claim 9 wherein the predetermined number is one of an integer or a fraction.

16. A method for direct division modulator comprising:
converting the input data from a binary bitstream to a
desired frequency deviation;
generating a divide value using the desired frequency
5 deviation information;
adding an average value to the divide value;
quantizing the divide value and shaping quantization
noise associated with the quantized divide value; and
modulating a reference signal with the quantized divide
10 value and generating an output signal.

17. The method of claim 16 wherein the divide value is
derived from modulation frequency deviation information and
the quantized divide value inversely proportional to the
15 instantaneous output frequency.

18. The method of claim 16 further comprising
receiving the output signal and rejecting the quantization
noise.

20 19. The method of claim 18 further comprising
receiving the output signal and the reference signal and
modulating the output signal with the reference signal to
aid in rejecting the quantization noise.

25 20. The method of claim 16 wherein the average value
comprises a fractional portion that is added to the divide
value prior to the quantizing step an integer portion that
is added to the quantized divide value prior to the
30 modulating step of the divide value with the divider.

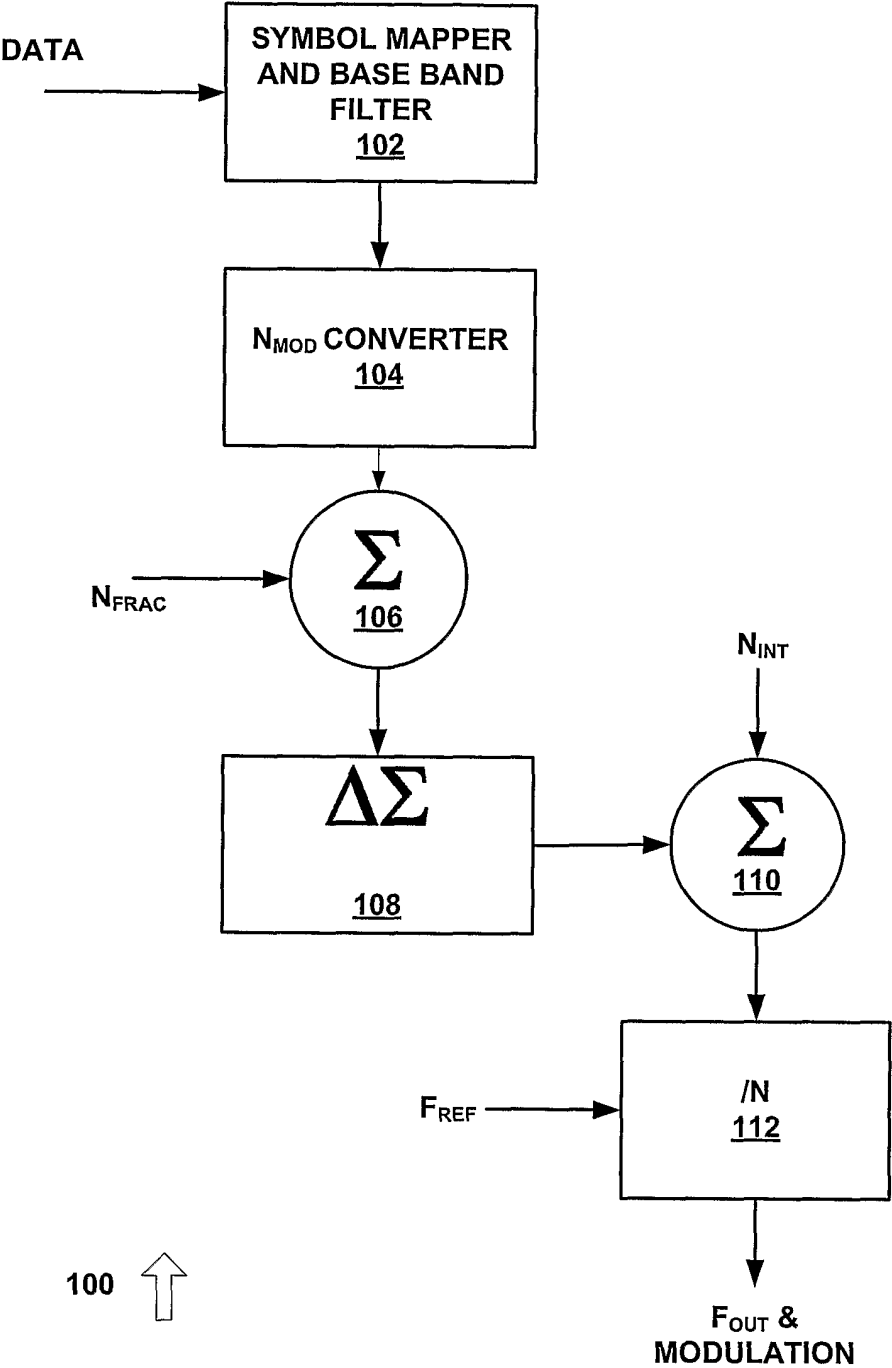


FIGURE 1

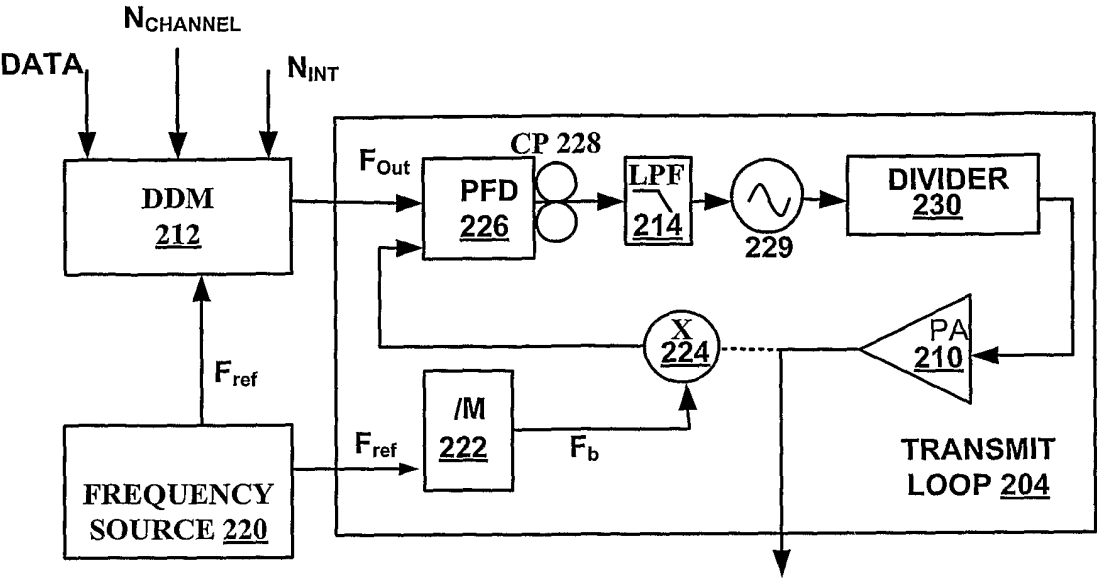


FIGURE 2A

200A ↑

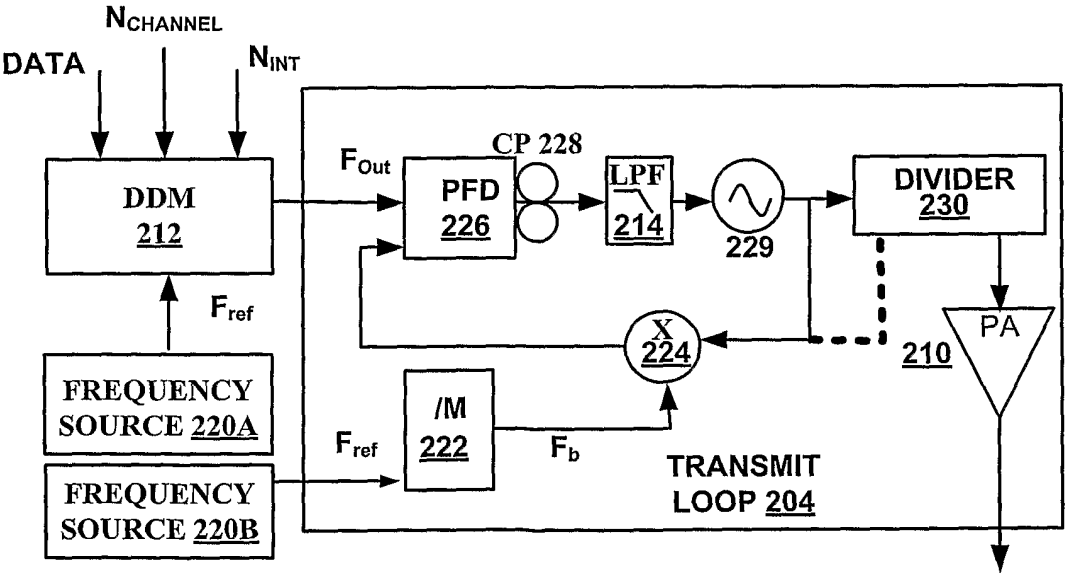


FIGURE 2B

200B ↑

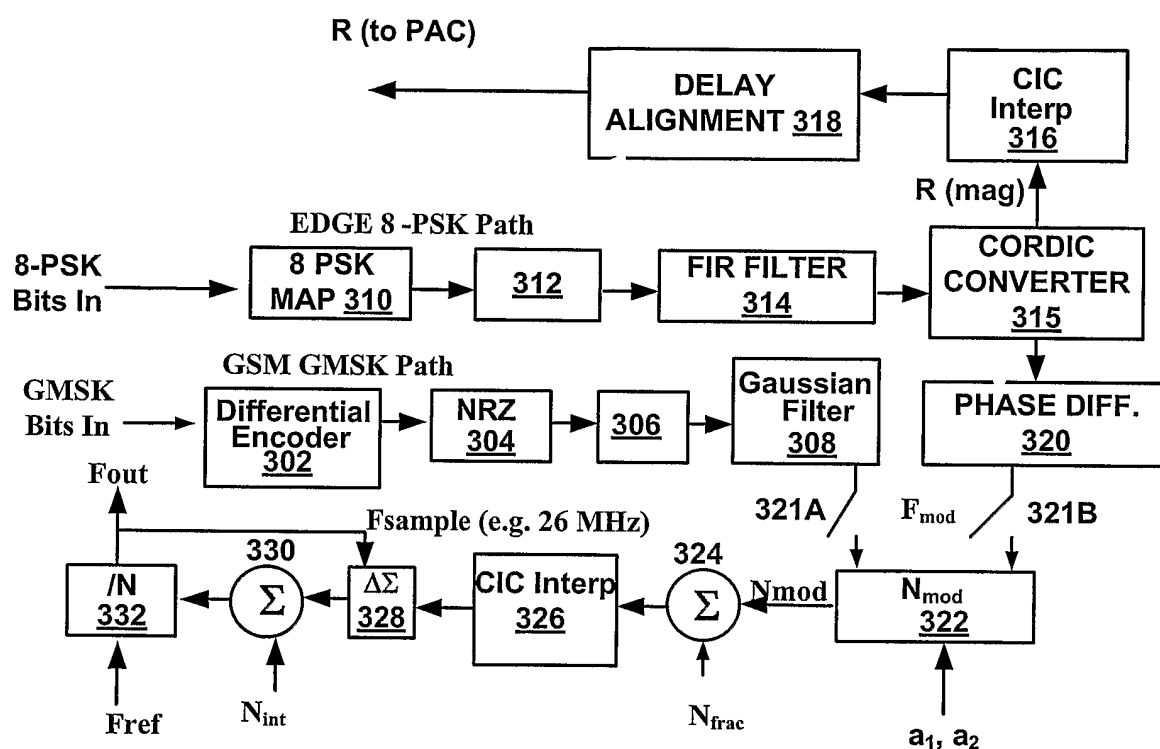


FIGURE 3

300 ↑

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/020297

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03C3/09 H04L27/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03C H04L H03L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EP0-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1 345 375 A (MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD) 17 September 2003 (2003-09-17) abstract figures 1-14 paragraphs [0002] - [0005], [0009], [0018], [0038] - [0040], [0042], [0043], [0059] - [0061], [0063], [0064], [0066]	1-20
X	EP 0 961 412 A (MOTOROLA SEMICONDUCTEURS S.A) 1 December 1999 (1999-12-01) abstract; figure 1 paragraphs [0012] - [0026]	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
"&" document member of the same patent family

Date of the actual completion of the international search

4 October 2006

Date of mailing of the international search report

11/10/2006

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

GONZALEZ GUTIERREZ

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2006/020297

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
EP 1345375	A	17-09-2003	CN 1444338 A	24-09-2003
			JP 2003273651 A	26-09-2003
			US 2005213697 A1	29-09-2005
			US 2003174026 A1	18-09-2003
EP 0961412	A	01-12-1999	DE 69826835 D1	11-11-2004
			DE 69826835 T2	23-02-2006
			US 6211747 B1	03-04-2001